CSEE W4823 Advanced Logic Design

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Lab 7 Report

Due to the design of our FIR filter, we only needed to write a memory block for the CMEM as it made more sense for IMEM to be integrated within our ALU. For CMEM, we used the memory compiler to generate SRAM arrays which gave us the cmem.v file. We then created cmem_large.v to instantiate the generated memory block as a module.

Performance Analysis Report

```
List of nonannotated nets :
1
****************************************
Report : Time Based Power
Design : cmem_large
Version: U-2022.12-SP5
Date   : Sat Nov 23 17:02:01 2024
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network              0.0000    0.0000    0.0000    0.0000 ( 0.00%)  i
register                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
combinational           2.098e-08    0.0000 5.680e-11 2.104e-08 (57.69%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000 1.543e-08    0.0000 1.543e-08 (42.31%)

  Net Switching Power  = 1.543e-08   (42.31%)
  Cell Internal Power  = 2.098e-08   (57.53%)
  Cell Leakage Power   = 5.680e-11   ( 0.16%)
                         ---------
Total Power            = 3.647e-08  (100.00%)

X Transition Power     =    0.0000
Glitching Power        =    0.0000

Peak Power             = 7.200e-04
Peak Time              =  5801.531

1
****************************************
Report : Time Based Power
        -hierarchy
Design : cmem_large
Version: U-2022.12-SP5
Date   : Sat Nov 23 17:02:01 2024
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                                    Int      Switch   Leak     Total
Hierarchy                           Power    Power    Power    Power    %
--------------------------------------------------------------------------------
cmem_large                          2.10e-08 1.54e-08 5.68e-11 3.65e-08 100.0


                                    Peak     Peak            Glitch   X-tran
Hierarchy                           Power    Time            Power    Power
--------------------------------------------------------------------------------
cmem_large                          7.20e-04 5801.531-5801.532
                                                                0.000    0.000
1
```

The Result of CMEM testbench

```
Transcript
# Loading work.cmem
# Loading work.CLKBUFX2TS
# Loading instances from ../../dc/fir/cmem_large.syn.sdf
# Loading timing data from ../../dc/fir/cmem_large.syn.sdf
# ** Note: (vsim-3587) SDF Backannotation Successfully Completed.
#    Time: 0 ps  Iteration: 0  Instance: /testbench File: test_cmem.v
# ** UI-Msg (Warning): (vish-4014) No objects found matching '/testbench/q'.
# Executing ONERROR command at macro ./waveformat.do line 8
# Starting cmem testbench
# dataIn = 0, Address = 0
# Expected: 0, Got: 0
# dataIn = 1, Address = 1
# Expected: 1, Got: 1
# dataIn = 2, Address = 2
# Expected: 2, Got: 2
# dataIn = 3, Address = 3
# Expected: 3, Got: 3
# dataIn = 4, Address = 4
# Expected: 4, Got: 4
# dataIn = 5, Address = 5
# Expected: 5, Got: 5
# dataIn = 6, Address = 6
# Expected: 6, Got: 6
# dataIn = 7, Address = 7
# Expected: 7, Got: 7
# dataIn = 8, Address = 8
# Expected: 8, Got: 8
# dataIn = 9, Address = 9
# Expected: 9, Got: 9
# ** Note: $finish    : test_cmem.v(58)
#    Time: 9200 ns  Iteration: 1  Instance: /testbench
# 1
# Break in Module testbench at test_cmem.v line 58
add wave -position insertpoint  \
```

Waveform Result of Functional CMEM