CPE301 – SPRING 2019

Design Assignment 2B

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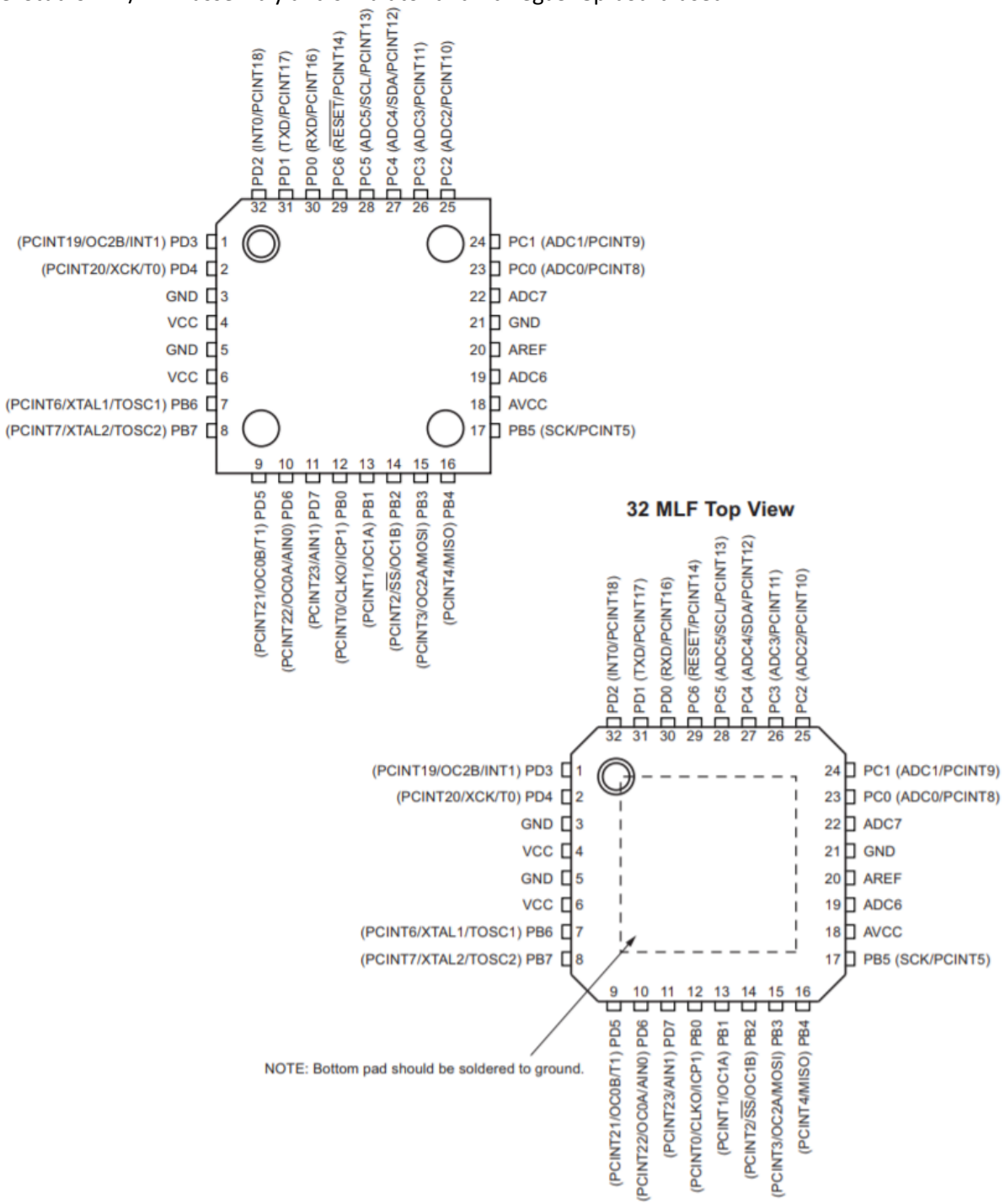
Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS

Atmel Studio 7 w/ AVR assembly and simulator and Atmega328p board used.



PortB2 is connected to LED3 and PortC2 is connected to SW1.

2. INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A

Task 1 Assembly Code:

```
.org 0                                  ;location for reset
       jmp start
.org 0x02                               ;location for ext_int0
       jmp ex0_isr

start:
       ldi r20, high(RAMEND)
       out sph, r20
       ldi r20, low(RAMEND)
       out spl, r20                ;initialize stack

       ldi r16, 0x00               ;initialize output
       ldi r20, 0x2
       sts eicra, r20                  ;make INT0 falling edge triggered
       sbi ddrb, 2                     ;set portb2 as output (led)
       sbi portd, 2                ;set pull up
       ldi r20, 1<<int0            ;enable INT0
       out eimsk, r20
       sei                                     ;enable interrupt
off:
       out portb, r16
       rjmp off                        ;turn led off until interrupt


delayon:                                ;delay for 1.25 seconds
       ldi r20, 100
delayon1:
       ldi r21, 100
delayon2:
       ldi r22, 200
delayon3:
       nop
       nop
       dec r22
       brne delayon3
       dec r21
       brne delayon2
       dec r20
       brne delayon1
       ret


ex0_isr:
       in r21, portb
       ldi r22, (1<<2)                 ;toggles pb5
       eor r21, r22                ;toggles led pb2
       out portb, r21                  ;turn led pb2 on
       rcall delayon               ;call delay
       reti                            ;return here until interrupt
```

Task 1 C Code:

```
#define F_CPU 8000000UL                         //set cpu mhz for delay
#include <avr/io.h>
#include <avr/interrupt.h>
#include <util/delay.h>


int main(void)
{
              DDRB |= (1<<2);                           //set pb2 as output
              PORTB &= (1<<2);                  //clear pb2
              PORTD = 1<<2;                     //enable pd2

              EICRA = 0x02;
              EIMSK = 1<<INT0;                  //enable pc set 0 interrupt
              sei();                                    //enable global interrupt

              while (1);
}


ISR(INT0_vect)
{
       PORTB ^= (1<<2);                         //toggle pb2 during interrupt
       _delay_ms(1250);                         //delay for 1.25 seconds
       PORTB ^= (1<<2);                         //toggle pb2 during interrupt
}
```

3. DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A

N/A

4. SCHEMATICS

N/A

5. SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)

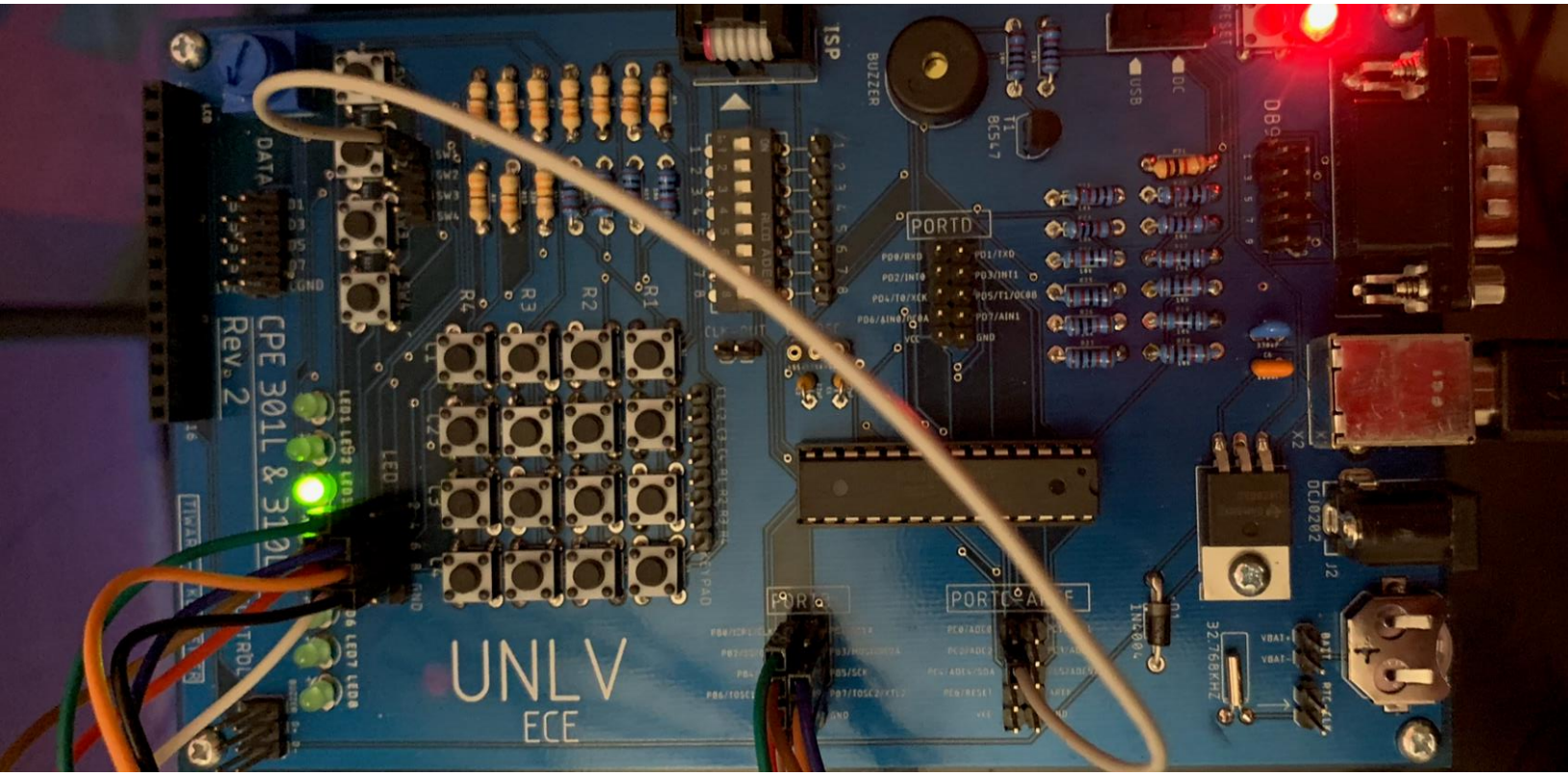
Task 1:
Assembly:
Full period is 1.25 s, the following screenshot was taken at the end of one loop.

Cycle Counter	1250346
Frequency	1.000 MHz
Stop Watch	1,250.35 ms

C:
Full period is 1.25 s, the following screenshot was taken at the end of one loop.

Cycle Counter	1250346
Frequency	1.000 MHz
Stop Watch	1,250.35 ms

6. SCREENSHOT OF EACH DEMO (BOARD SETUP)



7. VIDEO LINKS OF EACH DEMO

https://youtu.be/uixC4MPNSFE

8. GITHUB LINK OF THIS DA

https://github.com/tylergardenhire/submission_projects.git

Student Academic Misconduct Policy
http://studentconduct.unlv.edu/misconduct/policy.html

"*This assignment submission is my own, original work*".
TYLER GARDENHIRE