CPE301 – SPRING 2019

Design Assignment 2C

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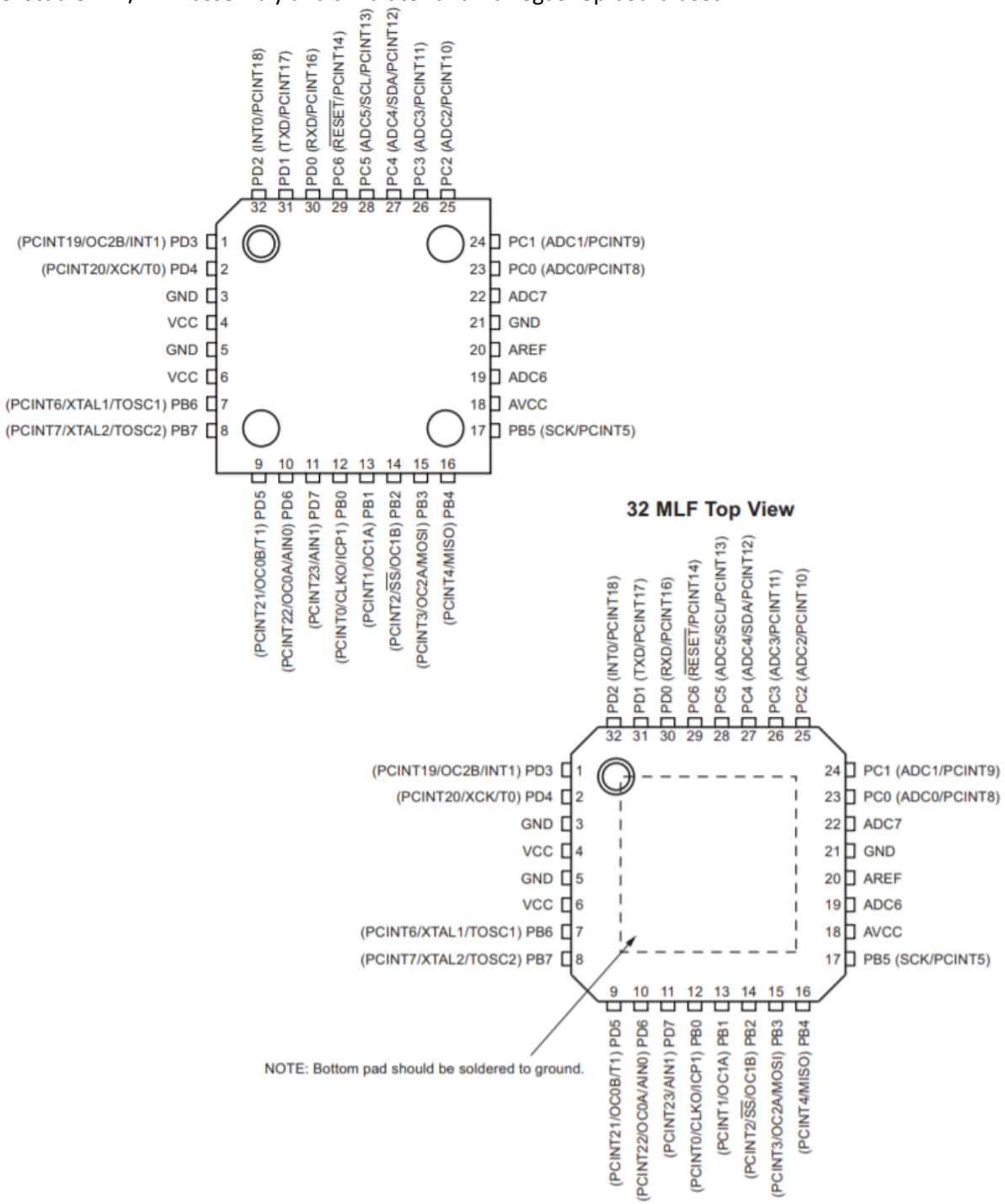
Directory: https://github.com/tylergardenhire/submission_projects.git

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS

Atmel Studio 7 w/ AVR assembly and simulator and Atmega328p board used.



PortB2 is connected to LED3 and PortC2 is connected to SW1.

2. INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A

Task 1 C code:

```
#define F_CPU 8000000UL

#include <avr/io.h>
#include <util/delay.h>

int main(void)
{
       DDRB |= (1 << DDB2);                        //pb2 as output
       TCCR0A = 0;                                          //normal operation
       TCNT0 = 0x00;                                 //start the timer
       TCCR0B |= (1<<CS01) | (1<<CS00);   //set prescaler to 64 and start the timer
    while (1)
    {
              while ((TIFR0 & 0x01)==0);
              PORTB ^= (1<<DDB1);
              TCNT0 = 0x00;
              TIFR0 = 0x01;                              //reset the overflow flag
    }
}
```

Task 2 C code:

```
# define F_CPU 8000000UL

#include <avr/io.h>
#include <util/delay.h>
#include <avr/interrupt.h>

int main(void)
{
    DDRB |= (1 << DDB2);                              //pb2 as output
       TIMSK0 |= (1 << TOIE0);
       TCNT0 = 56;                                                  //initial value
       sei();                                                       //enable interrupts
       TCCR0B |= (1 << CS01) | (1 << CS00);      //set prescaler to 64 and start the timer

    while (1)
    {
              //main loop
    }
}

ISR (TIMER0_OVF_vect)                                       //timer0 overflow interrupt
{
       TCNT0 = 56;
       PORTB ^= (1 << DDB1);
}
```

Task 3 C code:

```
#include <avr/io.h>
#include <avr/interrupt.h>

int main(void)
{
    DDRB |= (1 << DDB2);                                    //pb2 as output
       OCR0A = 40;
       TCCR0B |= (1 << CS01 | 1 << CS00);       //internal clock
       TCCR0A |= (1 << WGM01);                                  //internal clock, ctc mode,
no prescaler
       sei();
    while (1)
    {
              //wait here
    }
}

ISR (TIMER0_COMPA_vect)
{
       PORTB ^= 0x02;                                                  //toggle PORTB.2
       TIFR0 |= (1 << OCF0A);                                 //clear the compare A match
flag
}
```

3. DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A

N/A

4. SCHEMATICS

N/A

5. SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)

Task 1:
Full period is 725 ms, the following screenshot was taken at the end of one loop.

Cycle Counter	725018
Frequency	1.000 MHz
Stop Watch	725.02 ms

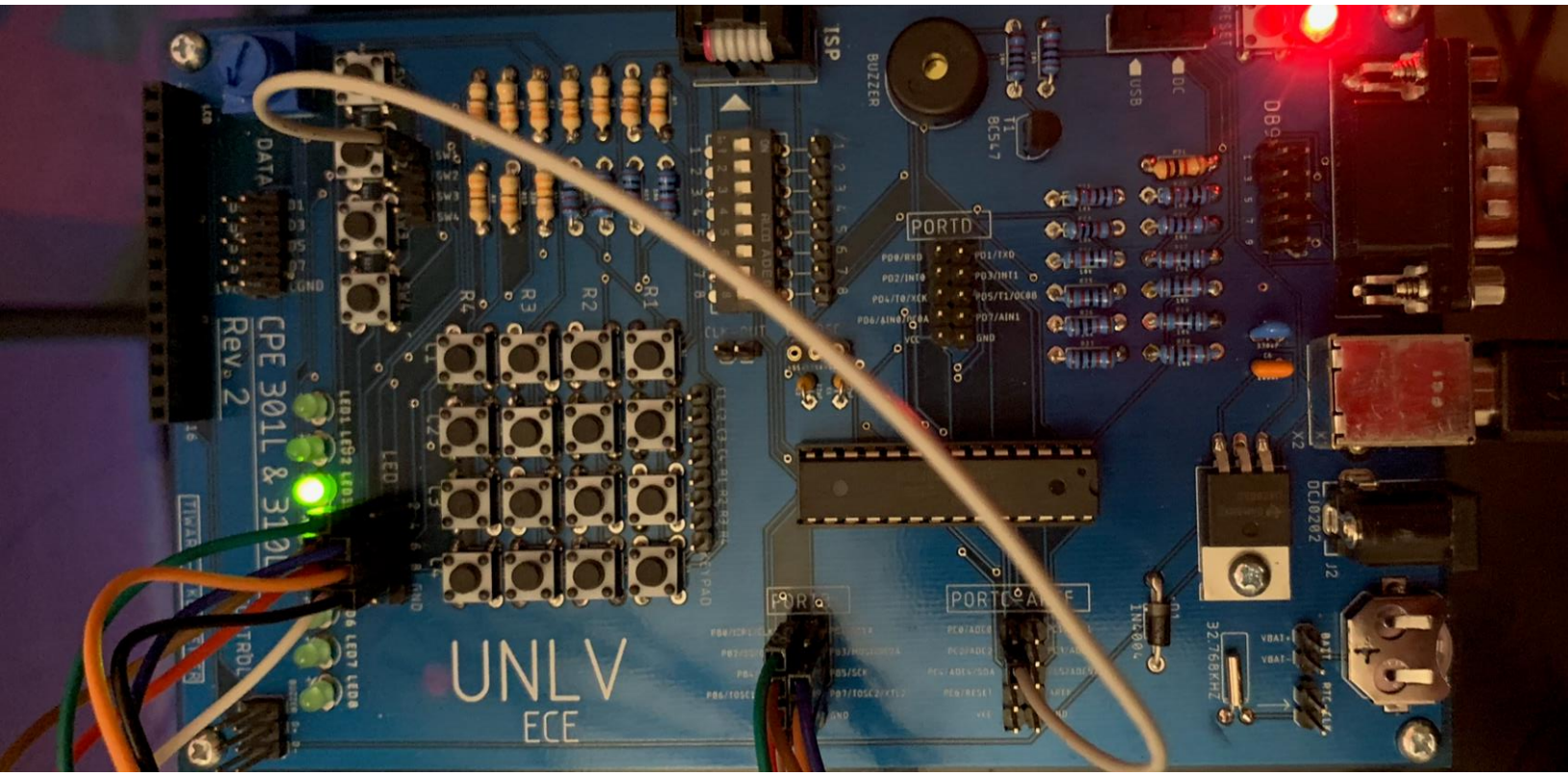
Task 2:
Full period is 725 ms, the following screenshot was taken at the end of one loop.

Cycle Counter	725018
Frequency	1.000 MHz
Stop Watch	725.02 ms

Task 3:
Full period is 725 ms, the following screenshot was taken at the end of one loop.

Cycle Counter	725018
Frequency	1.000 MHz
Stop Watch	725.02 ms

6. SCREENSHOT OF EACH DEMO (BOARD SETUP)



7. VIDEO LINKS OF EACH DEMO

https://youtu.be/ccK8sL_Mcg4

8. GITHUB LINK OF THIS DA

https://github.com/tylergardenhire/submission_projects.git

Student Academic Misconduct Policy
http://studentconduct.unlv.edu/misconduct/policy.html

"*This assignment submission is my own, original work*".
TYLER GARDENHIRE