ECE 5470/6470: VLSI Design

Class Project

The aim of the course project is to give you an experience of medium scale VLSI design using CAD tools and the standard cell library flow. This project needs to be completed in a team of 2 students or individuals. You are required to develop a medium sized digital system in Verilog. You can use the Modelsim tool for developing and testing your logic design. You will be subsequently doing synthesis, placement and routing of your design using the flows learned in class (Synopsys Design Compiler and Cadence Encounter).

Golden model

The first step in the design is to create a reference standard that you will use to validate the correctness of your designs. The reference standard should be in the form of a computer program (preferably in C/C++) that implements the specification and simulates the behavior of the chip component. As an example, to verify an 8-bit adder, your program should randomly generate two 8-bit inputs and then calculate the result and output it. You need to propose a way that you will verify your project matches this ideal behavior. It could be: matching cycle-by-cycle output from a simulator with "diff", comparing an image or audio file output, comparing standard output from a C-program, etc. You must also have a plan to come up with a minimal amount of tests.

Project ideas

Some ideas for possible projects are given here. You are welcome to choose your own ideas. Relevant projects that overlap with your other classes or research area are also acceptable.

- A floating point unit design using IEEE Standard 754.
- A standard cell biometric pattern recognition chip
- A simple MIPS type of processor
- MPEG compression/decompression
- You can download other Verilog projects from http://www.opencores.org and put them together. This project will involve lower effort in Verilog and more effort in floorplanning, placing and routing the chip.
- You can download the OpenSparc T1 processor from http://www.opensparc.net/ and place and route and verify the design. Again this involves a fairly complex effort in CAD tool flows and very little effort in Verilog.

Resources

Please access the CAD tool manuals from the wiki. You may need to alter the scripts for running synthesis, place and route. These scripts are written using the tcl scripting language. A tutorial for tcl can be found at http://www.tcl.tk/man/tcl/tutorial/tcltutorial.html . Remember, that your team is fully responsible for debugging your design and handling other issues in the project. For specific issues with CAD tools, please seek help from our TA in the course.

Deliverables:

You need to deliver a project proposal, a midterm progress report, a presentation, a final report and turn in your designs. **Please note that the dates are inflexible. If you fail to submit a deliverable by the due date, you score a zero for the part of the project grade.**

- [10 points] The project **proposal** is due in class on 03/17. Each team is required to meet with me to discuss their idea for a proposal before preparing the final version. You can meet me during my office hours on Wednesday 03/02. Please decide on your idea and possible implementation strategy before the meeting. I will give you specific feedback to finalize your outline during the meeting. The project proposal should be 1 to 2 pages, and must include:
    - Topic and specification of what you are going to design
    - Team members
    - Estimated tasks, your projected timeline and breakdown of duties of each person.
- [30 points] A **midterm progress report** is due on 03/31 in class. This report should contain description of golden model, block level design, description of project and some Verilog simulation results.
- [20 points] The **presentations** are on 04/26.
- [40 points] Each group should also submit a **final report** due at 11.59pm on 04/26. The project should be at least 8-pages (single space, font size 12). The report should include introduction and motivation, specification of your design, block diagram, simulation results, synthesis results, verification results, place and route results with area, power, performance and analysis of the results.