EE2011 Computer Organization 二甲

Final Exam

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※ 若試卷答題空間不足，請另用紙張作答。作答完畢後，掃描或拍照上傳！

Suppose there is a system with the following memory organizations: a 32-word 2-way set associative cache with block size of 4 words. The **cache** is using **physical address** and the address space for **physical memory** is **12-bit** and for **virtual memory** is **16-bit**, both of them are in byte addressing mode. The page size of the virtual memory is 256 bytes and the translation lookaside buffer (TLB) has the size of 8 entries using direct-mapping scheme. LRU scheme is used if a block in either cache or TLB has to be replaced. **When there are multiple blocks/pages available for placement in cache/physical memory, select the one with the smallest block/page number.**

(a) (15%) How many entries are required in the page table and how much memory space required for each entry in the page table for the information of where a page from virtual memory resides in the physical memory if it already exists in physical memory is required to store in the page table.
[Solution:]

(b) (15%) Please draw a diagram showing how the virtual address can be translated into physical address , data accessing and also use the physical address to check the cache if it hits. Hint: the diagram would be a combination of Fig. 5.29 of the textbook but the page table has to be shown, or the figures in p.16 of the class handout L13 added with page table. (For page table, you can refer to figure in p.14)
[Solution:]

(c) (30%) The processor executes the program using virtual address. The program has a sequence of instructions which access the data in the sequence of following addresses, 0x0054, 0x0058, 0x005C, 0x0060, 0x0064, 0x0110, 0x0114, 0x0114, 0x0118, 0x011C, 0x03D0, 0x03D4, 0x03D8, 0x03DC, 0x03E0, 0x03E4, 0x0110, 0x0114, 0x0118, 0x011C, 0x0050, 0x0054, 0x0058, 0x005C, 0x0060, 0x0064, and 0x0068 (total of 27 memory accesses). Notes that, these are virtual addresses of the data items in byte addressing. What is the **miss rate** and **page fault rate** of the memory performance? Assume that the cache and physical memory are blank initially.

[Solution:]

(d) (40%) The system has separated instruction cache and data cache. Assume the system has an ideal instruction cache which never misses. The hit time for address translation information available in TLB and data hit in data cache is negligible. The system has a base CPI of 1 and with the clock rate of 4GHz. Assuming there are 100 instructions in this program sequence and only consists of the memory access instructions mentioned in (c) and the rest of instructions are all ALU instructions and assume there is no data hazards which will cause the processor stall. The access time to physical memory is 100ns (access to page table also takes 100ns) and the access time to disk is 10ms in the case of a page fault in virtual memory access. What will be the effective CPI of this code sequence and how long will the processor take to execute these instruction sequences?

[Solution:]