ModelSim Tutorial

For the majority of this semester, each weekly homework assignment will also include a laboratory component that asks you to model a digital circuit using a hardware description language known as Verilog. Since we won't be starting to teach you the Verilog language until the recitations start, there is no official lab component this week. Instead, you should download the software we will be using to run the Verilog program we will write and complete the included tutorial to get familiar with the program.

Step 1: Download ModelSim Student Edition

Laboratory assignments will be given as your weekly homework and will emphasize the use of computer simulation tools. For logic design and simulation, ModelSim (release 20.1.1) will be used. You will need to download a free version of ModelSim at: **ModelSim download link**

When you connect to the download link given above, it will take you to Quartus Prime Lite Edition page On this page, please make sure that the edition and release appear as given below:

Select edition: Lite

Select release: 20.1.1

You will then need to scroll down the page up to the link for downloading ModelSim-Intel FPGA Edition (includes Starter Edition). You will be asked to create an account before you can download ModelSim.

ModelSim is not available for Mac users. In that case, please access the software through myapps.case.edu remotely.

Please make sure to save your work on H drive when using myapps.case.edu.

Step 2: Complete the ModelSim Tutorial

Download the ModelSim user's guide from the course Canvas website, or by going to Help>PDF Documentation>Tutorial in the ModelSim program. Once you have the pdf, complete the basic simulation tutorial in Chapter 3 and the Waveform Viewer tutorial in Chapter 6 (you do not need any prior knowledge of Verilog to complete these tutorials).

Step 3: Deliverables

When you complete your simulation, enter your name at the ModelSim >prompt as if it is a command (do not press enter), and take a screenshot. Submit your screenshot as your deliverable. A single screenshot showing the waveform and transcript windows after the simulation has been completed is sufficient as the deliverable.