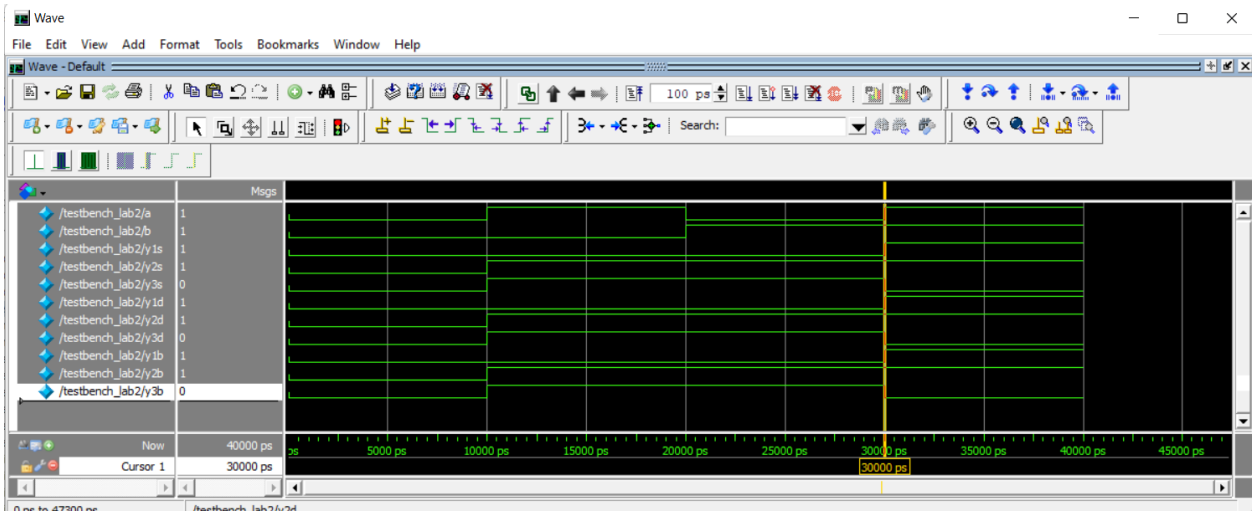
```
//edit of module_b.sv
module module_b(input logic a,b, output logic y1,y2,y3);

always_comb
begin
y1 = a & b;
y2 = a | b;
y3 = a ^ b;
end

// Complete for OR and XOR gates

endmodule


//edit of module_s.sv
module module_s(input logic a,b, output logic y1,y2,y3);

and U1 (y1,a,b);
or U2 (y2,a,b);
xor U3 (y3,a,b);

// Complete for OR and XOR gates

endmodule


//edit of module_d.sv
module module_d(input logic a,b, output logic y1,y2,y3);

assign y1 = a & b;
assign y2 = a | b;
assign y3 = a ^ b;

// Complete for OR and XOR gates

endmodule

`timescale 1ns/100ps  //testbench_lab2.sv
module testbench_lab2 (); //same no edits

   logic a, b;
   logic y1s, y2s, y3s;
   logic y1d, y2d, y3d;
```

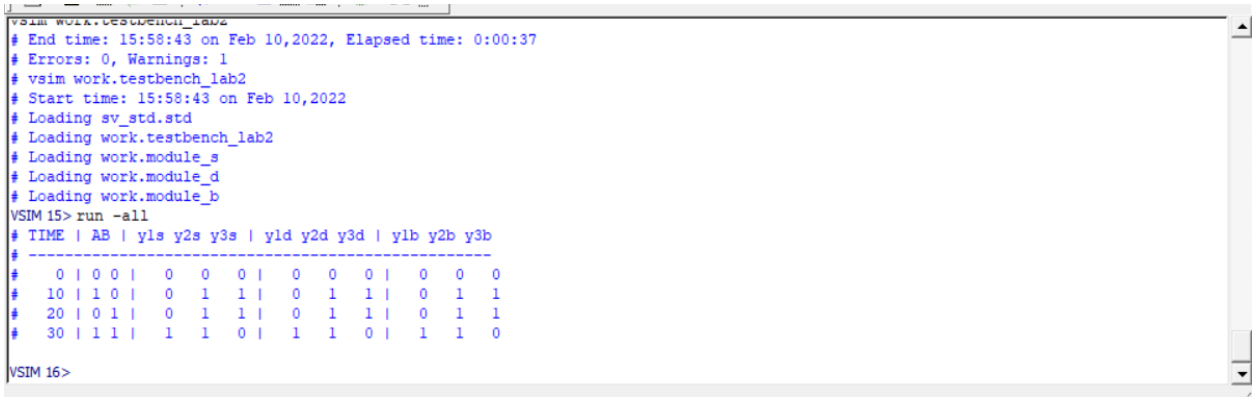
```
logic y1b, y2b, y3b;

module_s UUT1 (
    .a (a),
    .b (b),
    .y1(y1s),
    .y2(y2s),
    .y3(y3s)
);

module_d UUT2 (
    .a (a),
    .b (b),
    .y1(y1d),
    .y2(y2d),
    .y3(y3d)
);

module_b UUT3 (
    .a (a),
    .b (b),
    .y1(y1b),
    .y2(y2b),
    .y3(y3b)
);


initial begin
    a = 0;
    b = 0;
    #10;
    a = 1;
    #10;
    a = 0;
    b = 1;
    #10;
    a = 1;
    #10;
 //   $finish();
end

initial begin
    $display("TIME | AB | y1s y2s y3s | y1d y2d y3d | y1b y2b y3b");
    $display("-----------------------------------------------");
```

```
        $monitor("  %2d | %b %b |   %b    %b    %b |   %b    %b    %b |   %b    %b    %b",
            $time, a, b, y1s, y2s, y3s, y1d, y2d, y3d, y1b, y2b, y3b);

        $dumpfile("lab2.vcd");
        $dumpvars(1, a, b, y1s, y2s, y3s, y1d, y2d, y3d, y1b, y2b, y3b);
        $dumpflush;
    end

endmodule
```

// screenshot of waveform with gates



// screenshot of truth table



```
# End time: 15:58:43 on Feb 10,2022, Elapsed time: 0:00:37
# Errors: 0, Warnings: 1
# vsim work.testbench_lab2
# Start time: 15:58:43 on Feb 10,2022
# Loading sv_std.std
# Loading work.testbench_lab2
# Loading work.module_s
# Loading work.module_d
# Loading work.module_b
VSIM 15> run -all
# TIME  | AB  | y1s y2s y3s | y1d y2d y3d | y1b y2b y3b
# ------------------------------------------------------
#     0 | 0 0 |   0   0   0 |   0   0   0 |   0   0   0
#    10 | 1 0 |   0   1   1 |   0   1   1 |   0   1   1
#    20 | 0 1 |   0   1   1 |   0   1   1 |   0   1   1
#    30 | 1 1 |   1   1   0 |   1   1   0 |   1   1   0

VSIM 16>
```