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ECEN 220
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Lab #5 - Arithmetic Logic Unit

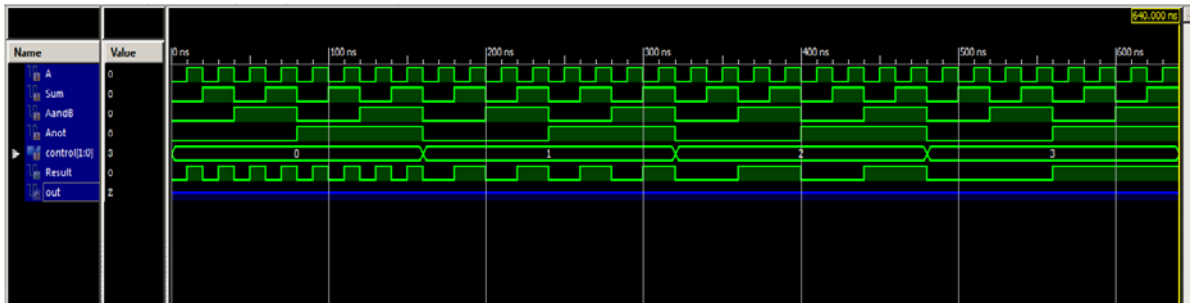
MUX 4:1:

VERILOG:

```
module MUX41(
   input A,
   input Sum,
   input AandB,
   input Anot,
   input [1:0] control,
   output Result
   );
         wire out;
         assign Result= control == 2'b00 ? A :
         control == 2'b01 ? Sum :
         control == 2'b10 ? AandB :
         Anot;

Endmodule
```

TCL:

```
wave add / -radix hex
isim force add A 0 -time 0 -value 1 -time 10ns -repeat 20ns
isim force add Sum 0 -time 0 -value 1 -time 20ns -repeat 40ns
isim force add AandB 0 -time 0 -value 1 -time 40ns -repeat 80ns
isim force add Anot 0 -time 0 -value 1 -time 80ns -repeat 160ns
isim force add control 00 -time 0 -value 01 -time 160ns -value 10 -time 320ns -value 11 -time 480ns
```

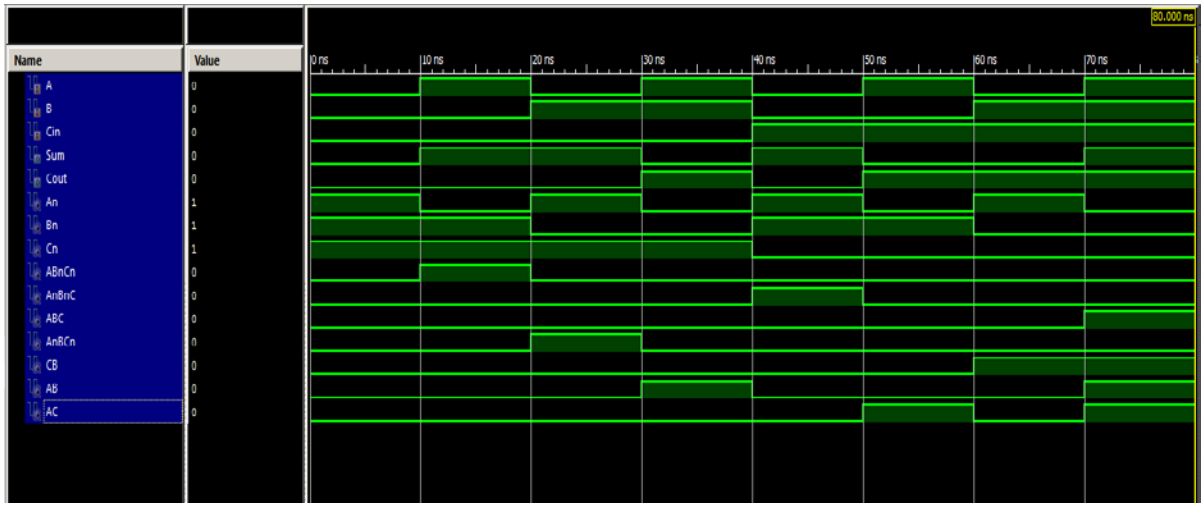


Full Adder:
VERILOG:

```
module FullAdder(
   input A,
   input B,
   input Cin,
   output Sum,
   output Cout
   );
         wire An,Bn,Cn,ABnCn,AnBnC,ABC,AnBCn,CB,AB,AC;

         not(An,A);
         not(Bn,B);
         not(Cn,Cin);
         and(ABnCn,A,Bn,Cn);
         and(AnBnC,An,Bn,Cin);
         and(ABC,A,B,Cin);
         and(AnBCn,An,B,Cn);
         or(Sum,ABnCn,AnBnC,ABC,AnBCn);

         and(AB,A,B);
         and(AC,A,Cin);
         and(CB,Cin,B);
         or(Cout,AB,AC,CB);

endmodule
```

TCL:

```
wave add / -radix hex
isim force add A 0 -time 0 -value 1 -time 10ns -repeat 20ns
isim force add B 0 -time 0 -value 1 -time 20ns -repeat 40ns
isim force add Cin 0 -time 0 -value 1 -time 40ns -repeat 80ns
```

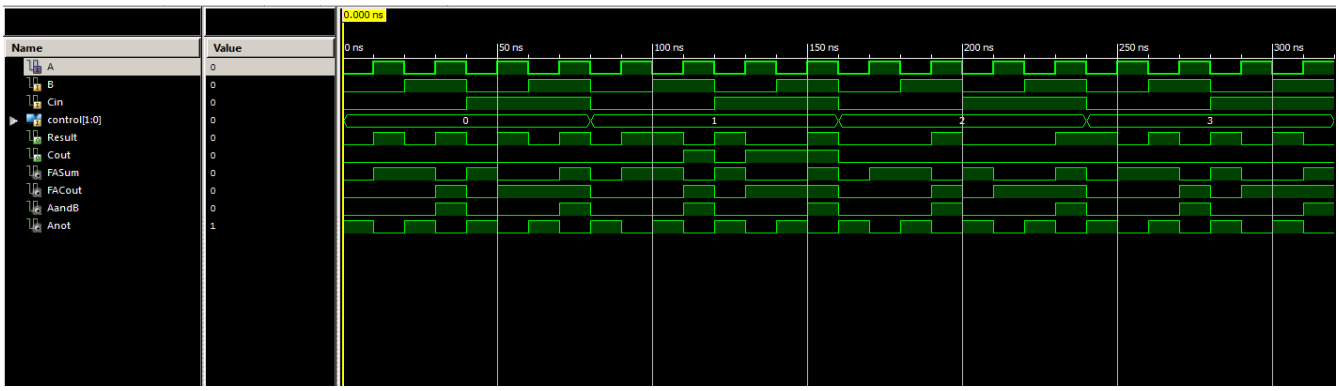


1 Bit ALU:
VERILOG:

```
module OneBitALU(
   input A,
   input B,
   input Cin,
   input [1:0] control,
   output Result,
   output Cout
   );
         wire FASum, FACout,AandB,Anot;
         and(AandB,A,B);
         not(Anot,A);
         FullAdder FullAdd(A,B,Cin,FASum,FACout);
         assign Cout = control == 2'b01 ? FACout : 0;
         MUX41 Multiplexor(A,FASum,AandB,Anot,control,Result);

Endmodule
```

TCL:

```
wave add / -radix hex
isim force add A 0 -time 0 -value 1 -time 10ns -repeat 20ns
isim force add B 0 -time 0 -value 1 -time 20ns -repeat 40ns
isim force add Cin 0 -time 0 -value 1 -time 40ns -repeat 80ns
isim force add control 00 -time 0 -value 01 -time 80ns -value 10 -time 160ns -value 11 -time 240ns -
repeat 320ns
```

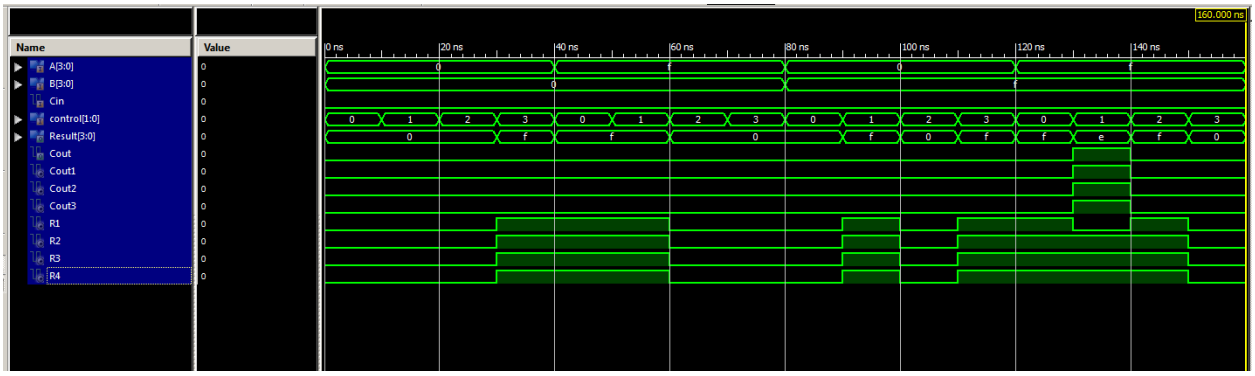


4 Bit ALU:
VERILOG:

```
module FourBitALU(
   input [3:0] A,
   input [3:0] B,
   input Cin,
         input [1:0] control,
   output [3:0] Result,
   output Cout
   );
         wire Cout1,Cout2,Cout3,R1,R2,R3,R4;
         OneBitALU A0(A[0],B[0],1'b0,control,R1,Cout1);
         OneBitALU A1(A[1],B[1],Cout1,control,R2,Cout2);
         OneBitALU A2(A[2],B[2],Cout2,control,R3,Cout3);
         OneBitALU A3(A[3],B[3],Cout3,control,R4,Cout);
         assign Result[0] = R1;
         assign Result[1] = R2;
         assign Result[2] = R3;
         assign Result[3] = R4;

endmodule
```

TCL:

```
wave add / -radix hex
isim force add Cin 0
isim force add control 00 -time 0 -value 01 -time 10ns -value 10 -time 20ns -value 11 -time 30ns -repeat 40ns
isim force add A 0000 -time 0 -value 1111 -time 40ns -repeat 80ns
isim force add B 0000 -time 0 -value 1111 -time 80ns -repeat 160ns
```



UCF:

```
## Leds
NET Result<0>  LOC = "J14"; # Bank = 1, Pin name = IO_L14N_1/A3/RHCLK7, Type = RHCLK/DUAL, Sch name = JD10/LD0
NET Result<1>  LOC = "J15"; # Bank = 1, Pin name = IO_L14P_1/A4/RHCLK6, Type = RHCLK/DUAL, Sch name = JD9/LD1
NET Result<2>  LOC = "K15"; # Bank = 1, Pin name = IO_L12P_1/A8/RHCLK2, Type = RHCLK/DUAL, Sch name = JD8/LD2
NET Result<3>  LOC = "K14"; # Bank = 1, Pin name = IO_L12N_1/A7/RHCLK3/TRDY1, Type = RHCLK/DUAL, Sch name = JD7/LD3
#NET "Led<4>"  LOC = "E17"; # Bank = 1, Pin name = IO, Type = I/O, Sch name = LD4
#NET "Led<5>"  LOC = "P15"; # Bank = 1, Pin name = IO, Type = I/O, Sch name = LD5
#NET "Led<6>"  LOC = "F4";  # Bank = 3, Pin name = IO, Type = I/O, Sch name = LD6
NET Cout  LOC = "R4";  # Bank = 3, Pin name = IO/VREF_3, Type = VREF, Sch name = LD7

## Switches
NET B<0> LOC = "G18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW0
NET B<1> LOC = "H18"; # Bank = 1, Pin name = IP/VREF_1, Type = VREF, Sch name = SW1
NET B<2> LOC = "K18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW2
NET B<3> LOC = "K17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW3
NET A<0> LOC = "L14"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW4
NET A<1> LOC = "L13"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW5
NET A<2> LOC = "N17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW6
NET A<3> LOC = "R17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW7

## Buttons
#NET "btn<0>" LOC = "B18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN0
#NET "btn<1>" LOC = "D18"; # Bank = 1, Pin name = IP/VREF_1, Type = VREF, Sch name = BTN1
NET control<0> LOC = "E18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN2
NET control<1> LOC = "H13"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN3
```

ANOMALIES:
None found