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EcEn 220
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Lab 11: Controlling the LC3 Datapath

Datapath Verilog Module

```
module Datapath(
   input clk,
   input reset,
   input [1:0] aluControl,
   input enaALU,
   input [2:0] SR1,
   input [2:0] SR2,
   input [2:0] DR,
   input regWE,
   input [1:0] selPC,
   input enaMARM,
   input selMAR,
   input selEAB1,
   input [1:0] selEAB2,
   input enaPC,
   input ldPC,
   input ldIR,
   input ldMAR,
   input ldMDR,
   input selMDR,
   input memWE,
   input flagWE,
   input enaMDR,
   output N,
   output Z,
   output P,
   output [15:0] IR
   );

        wire [15:0] Buss, aluOut, pc, MARMuxOut, eabOut, Ra, Rb, mdrOut;

        PC pcModule(ldPC,clk,reset, selPC, Buss, eabOut, pc);
        ts_driver PCdriver(pc, Buss, enaPC);

        EAB EABModule(IR[10:0], Ra, pc, selEAB1, selEAB2, eabOut);

        IR IRmodule(ldIR, clk, reset, Buss, IR);

        MARMux marmodule(IR[7:0],selMAR,eabOut,MARMuxOut);
        ts_driver enaMARMdriver (MARMuxOut, Buss, enaMARM);
```

```
        ALU alumodule(Ra, Rb, IR[5:0], aluControl, aluOut);
        ts_driver aluDriver(aluOut, Buss, enaALU);

        RegFile REG(DR,SR1,SR2,regWE,clk,reset,Buss,Ra,Rb);

        NZP nzp(Buss,reset,clk,flagWE,N,Z,P);

        Memory mem(mdrOut, Buss, clk, reset, ldMAR, ldMDR, selMDR, memWE);
        ts_driver memdriver(mdrOut, Buss, enaMDR);

endmodule
```

MASTER TCL FILE

```
source wave.tcl

isim force add clk 0 -time 0 -value 1 -time 5ns -repeat 10ns
isim force add reset 1 -time 0 -value 0 -time 12ns

run 12ns

source fetch.tcl
source and1.tcl
source fetch.tcl
source add1.tcl
source fetch.tcl
source not1.tcl
source fetch.tcl
source branch1.tcl
source fetch.tcl
source jsr1.tcl
source fetch.tcl
source load1.tcl
source fetch.tcl
source load2.tcl
source fetch.tcl
source add2.tcl
source fetch.tcl
source store.tcl
source fetch.tcl
source jump1.tcl
source fetch.tcl
source branch2.tcl
source fetch.tcl
```

WAVE TCL FILE

```
#add signals to view the IR and IR control
wave add ldIR
wave add IR -radix hex

#add signals to view the EAB control
wave add selEAB1
wave add selEAB2
wave add eabOut -radix hex

#add signals to view the MARMux control
wave add selMAR
wave add enaMARM
wave add MARMuxOut -radix hex

#add signals to view Register File control
wave add DR
wave add SR1
wave add SR2
wave add regWE

#add signals to view the Registers in the Register File
wave add /REG/R0 -radix hex
wave add /REG/R1 -radix hex
wave add /REG/R2 -radix hex
wave add /REG/R3 -radix hex
wave add /REG/R4 -radix hex
wave add /REG/R5 -radix hex
wave add /REG/R6 -radix hex
wave add /REG/R7 -radix hex
wave add Ra -radix hex
wave add Rb -radix hex

#add signals to view the ALU control
wave add aluControl
wave add enaALU
wave add aluOut -radix hex

#view the condition flags
wave add N
wave add Z
wave add P
wave add flagWE
```

#add signals to view the Memory Registers and the Memory control
wave add ldMAR
wave add /mem/MARReg -radix hex
wave add ldMDR
wave add enaMDR
wave add selMDR
wave add mdrOut -radix hex
wave add /mem/memOut -radix hex
wave add memWE

INACTIVE TCL FILE

isim force add enaALU 0
isim force add enaMARM 0
isim force add enaPC 0
isim force add enaMDR 0
isim force add ldIR 0
isim force add ldPC 0
isim force add ldMAR 0
isim force add ldMDR 0
isim force add regWE 0
isim force add memWE 0
isim force add flagWE 0

FETCH TCL FILE

source inactive.tcl

isim force add enaPC 1
isim force add ldMAR 1
run 10ns

source inactive.tcl
isim force add selPC 00
isim force add ldPC 1
isim force add ldMDR 1
isim force add selMDR 1
run 10ns

source inactive.tcl

isim force add ldIR 1
isim force add enaMDR 1
run 10ns

source inactive.tcl

AND1 TCL FILE
```
isim force add aluControl 10
isim force add SR1 000
isim force add DR 000
isim force add enaALU 1
isim force add regWE 1
run 10ns
```

ADD1 TCL FILE
```
isim force add aluControl 01
isim force add SR1 000
isim force add DR 001
isim force add enaALU 1
isim force add regWE 1
run 10ns
```

NOT1 TCL FILE
```
isim force add aluControl 11
isim force add SR1 010
isim force add DR 011
isim force add enaALU 1
isim force add regWE 1
run 10ns
```

BRANCH1 TCL FILE
```
isim force add selPC 01
isim force add selEAB1 0
isim force add selEAB2 10
isim force add ldPC 1
run 10ns
```

JSR TCL FILE
```
isim force add DR 111
isim force add regWE 1
isim force add enaPC 1
run 10ns
source inactive.tcl
isim force add selPC 01
isim force add selEAB1 0
isim force add selEAB2 11
isim force add ldPC 1
run 10ns
```

LOAD1 TCL FILE

```
isim force add selEAB1 0
isim force add selEAB2 10
isim force add enaMARM 1
isim force add ldMAR 1
isim force add selMAR 0
run 10ns
source inactive.tcl
isim force add ldMDR 1
isim force add selMDR 1
run 10ns
source inactive.tcl
isim force add DR 010
isim force add regWE 1
isim force add enaMDR 1
run 10ns
```

LEAD2 TCL FILE

```
isim force add selEAB1 0
isim force add selEAB2 10
isim force add enaMARM 1
isim force add ldMAR 1
isim force add selMAR 0
run 10ns
source inactive.tcl
isim force add ldMDR 1
isim force add selMDR 1
run 10ns
source inactive.tcl
isim force add DR 001
isim force add regWE 1
isim force add enaMDR 1
run 10ns
```

ADD2 TCL FILE

```
isim force add aluControl 01
isim force add SR1 010
isim force add SR2 001
isim force add DR 110
isim force add enaALU 1
isim force add regWE 1
run 10ns
```

STORE TCL FILE

```
isim force add selEAB1 0
isim force add selEAB2 10
isim force add enaMARM 1
isim force add ldMAR 1
isim force add selMAR 0
run 10ns
source inactive.tcl
isim force add aluControl 00
isim force add SR1 110
isim force add enaALU 1
isim force add ldMDR 1
isim force add selMDR 0
run 10ns
source inactive.tcl
isim force add memWE 1
run 10ns
```

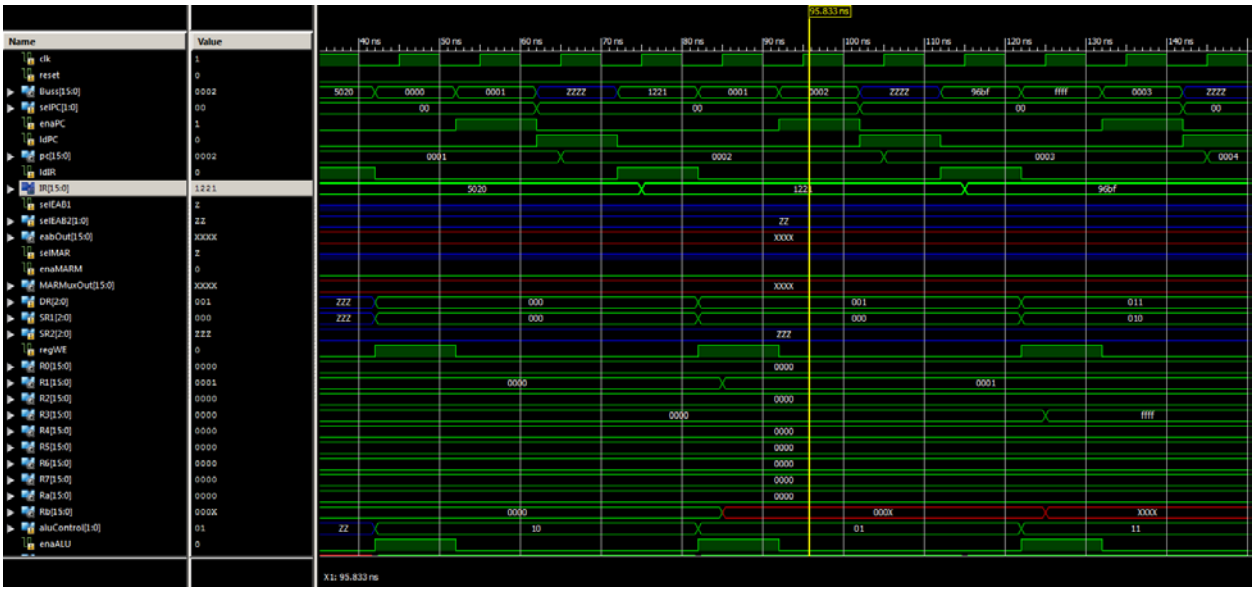
JUMP1 TCL FILE

```
isim force add SR1 111
isim force add selPC 01
isim force add selEAB1 1
isim force add selEAB2 00
isim force add ldPC 1
run 10ns
```

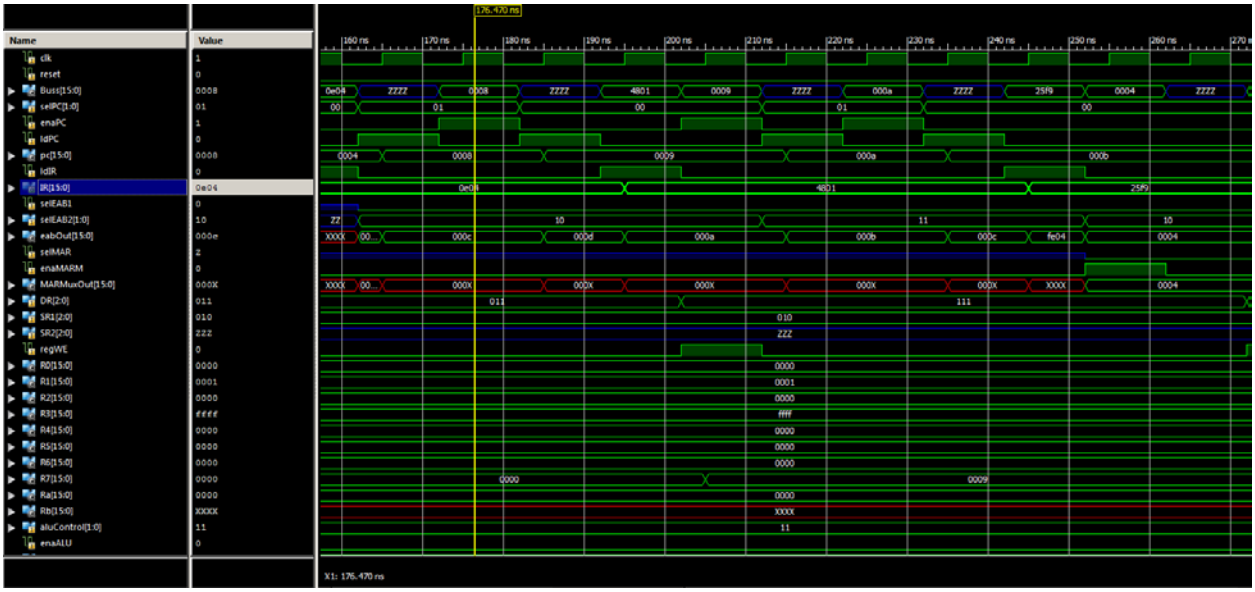
BRANCH2 TCL FILE

```
isim force add selPC 01
isim force add selEAB1 0
isim force add selEAB2 10
isim force add ldPC 1
run 10ns
```

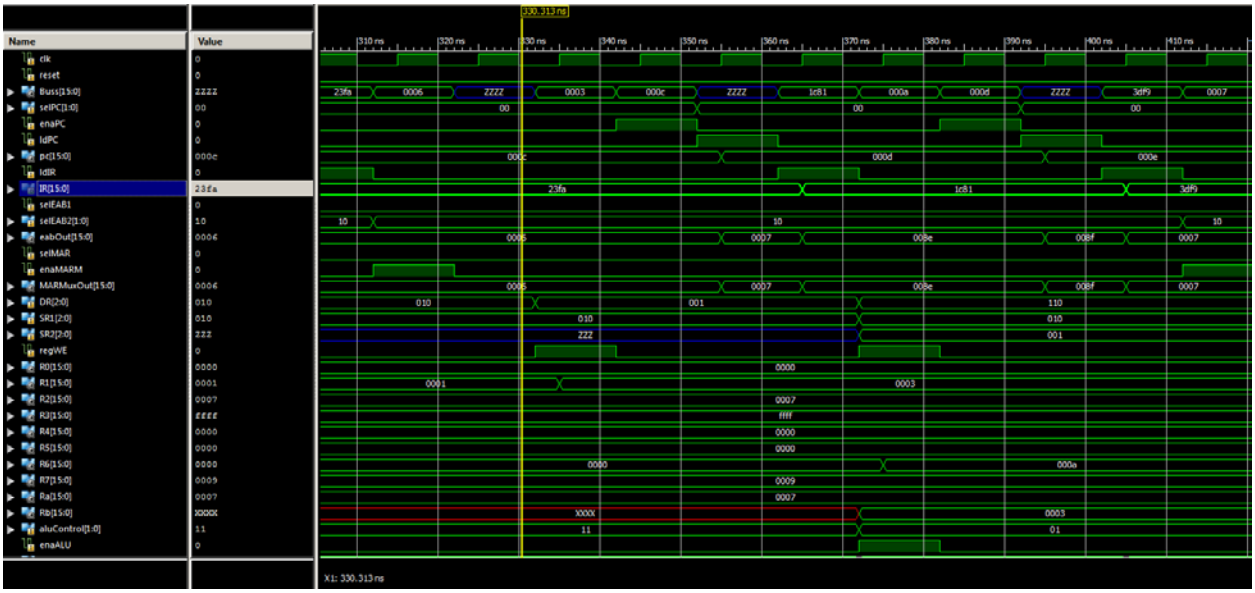
1st three instructions



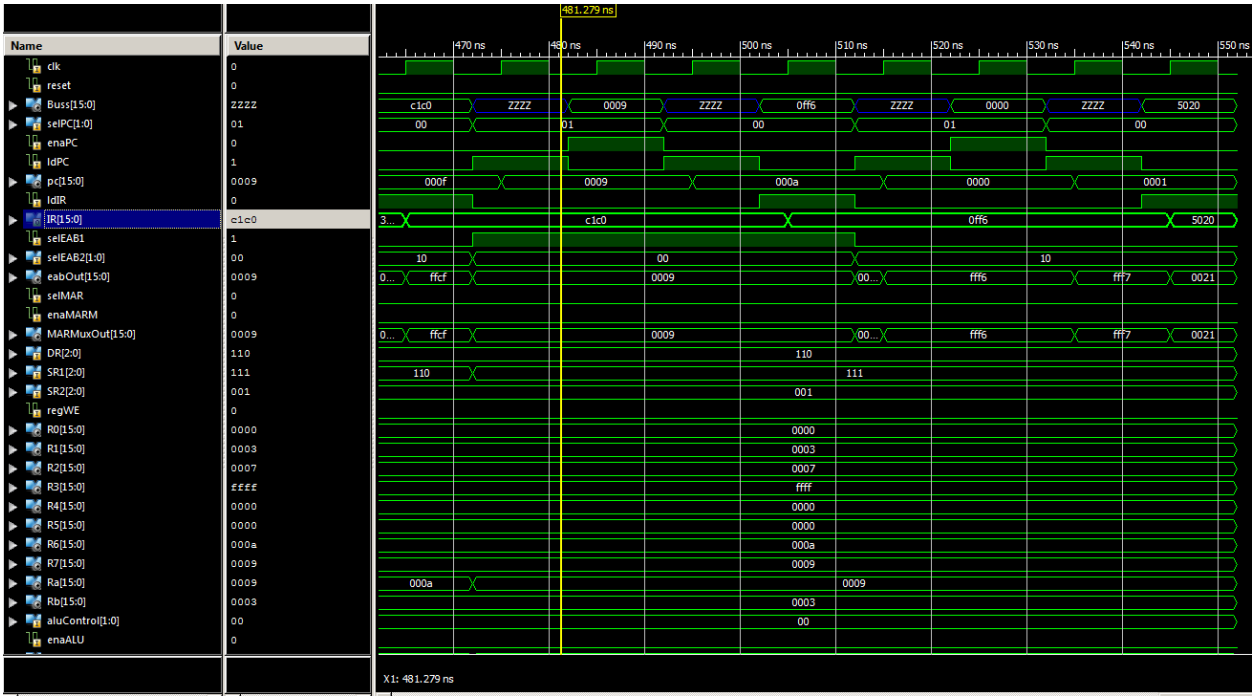
2nd three instructions



3rd three instructions



Last instructions



Anomalies

Our only anomalies were that ISE crashed once or twice and we also got confused by the select symbols on the table in the Homework online of the Datapath signals, specifically selMDR and selMAR because they were mixed in with the enable and load signals.