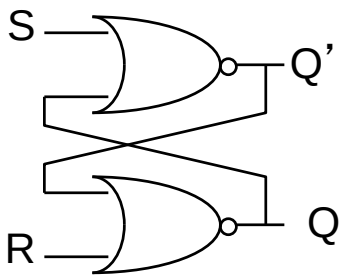
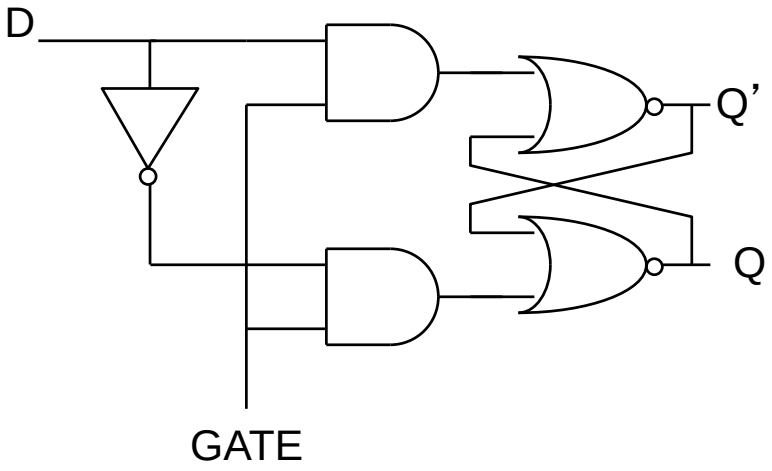
SRAM Controller

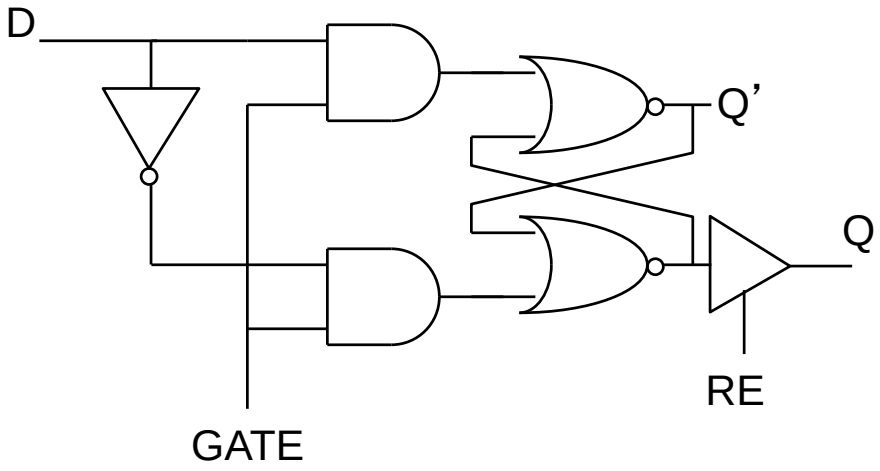
SR Latch

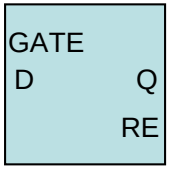


Gated D Latch



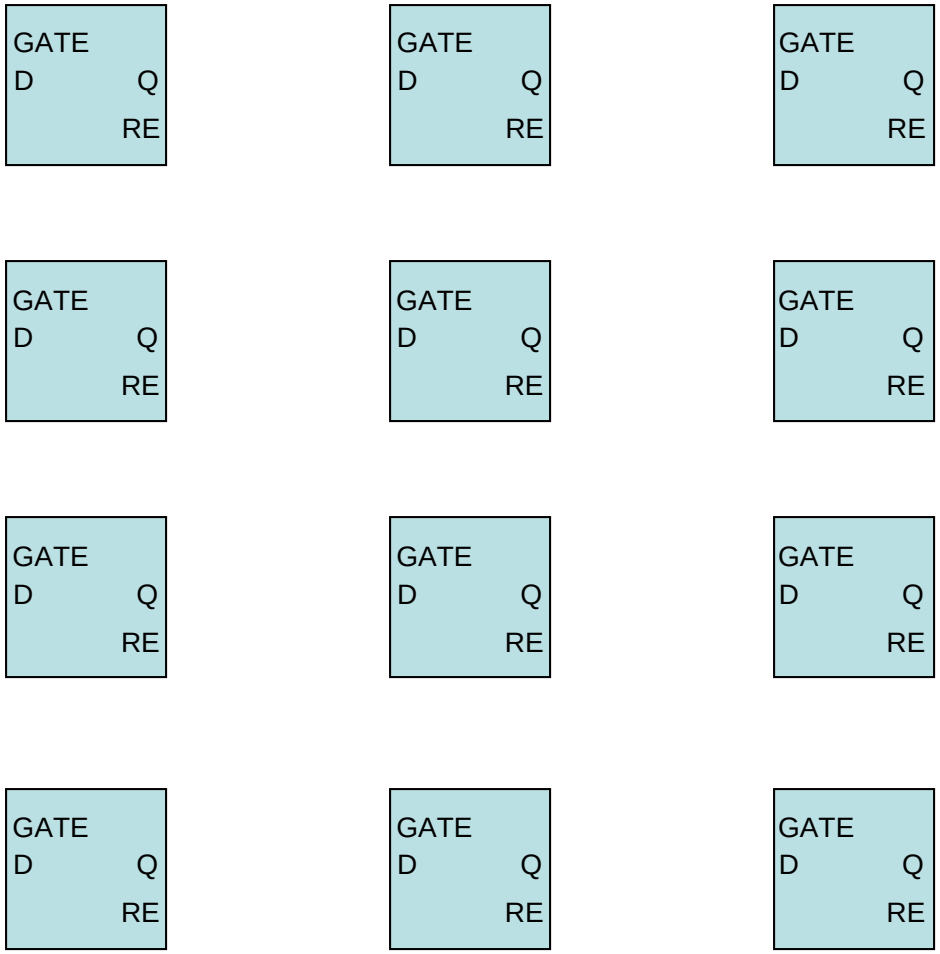
Gated D Latch w/Tristate



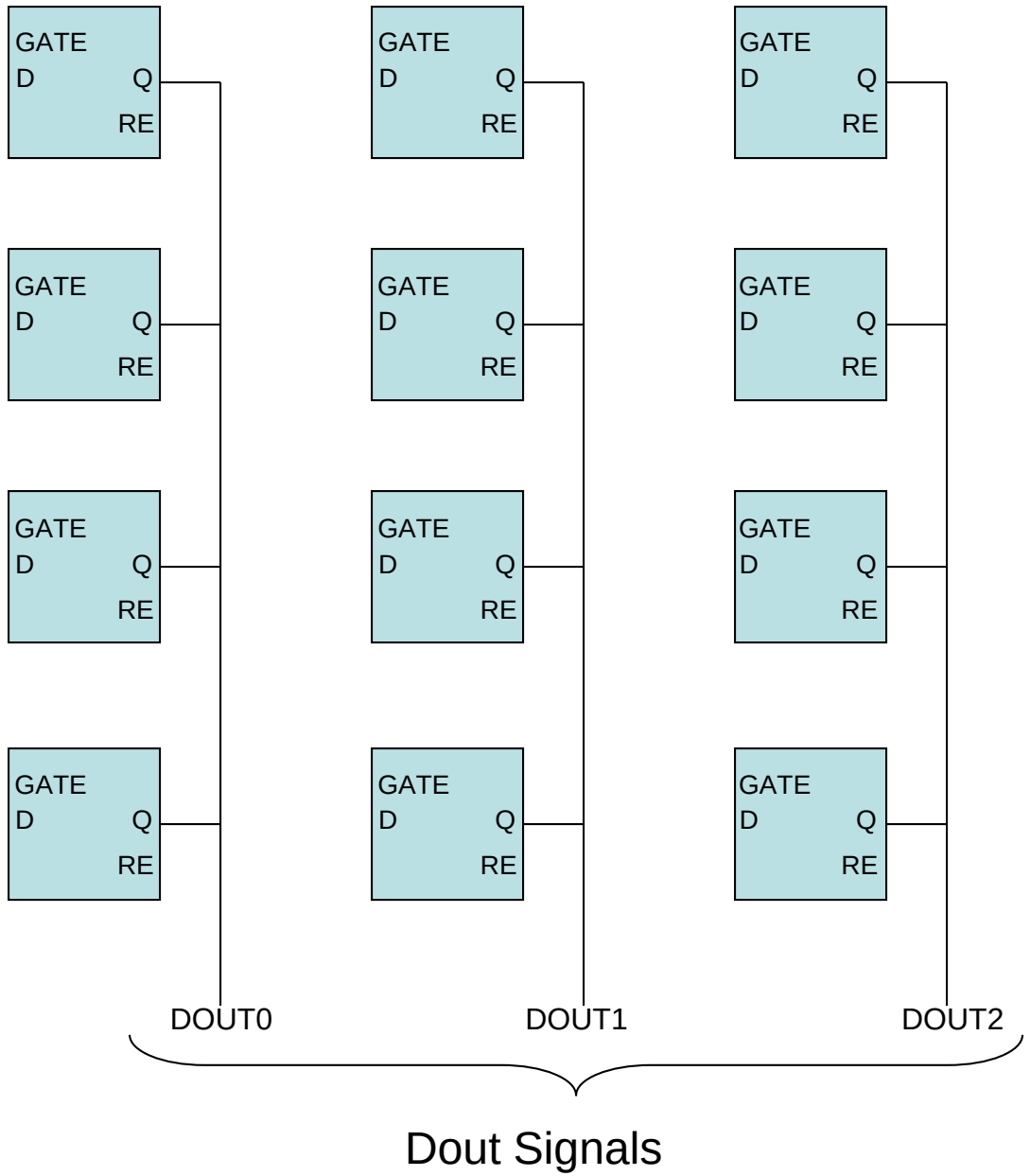


Symbol

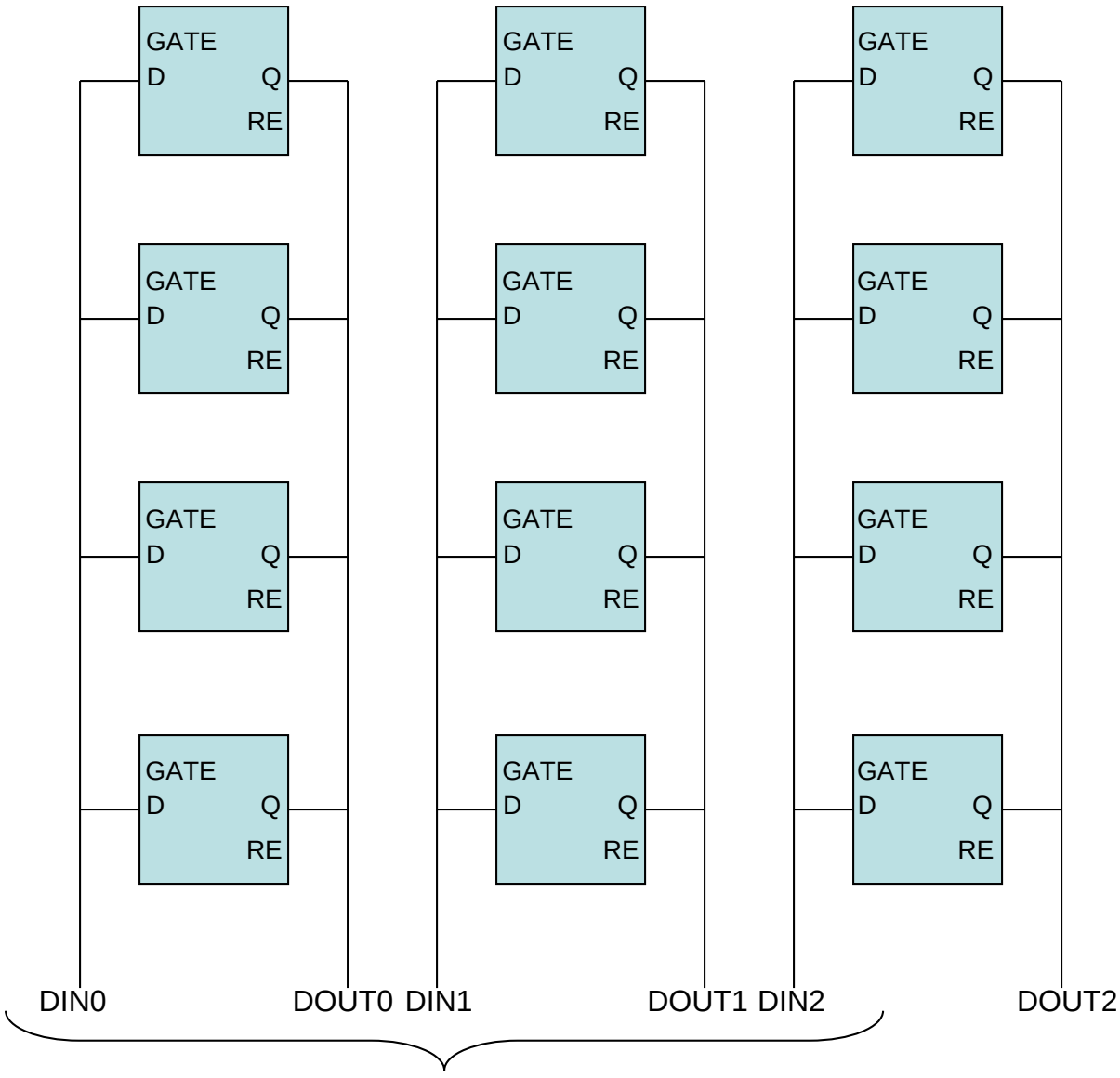
Array of D Latches



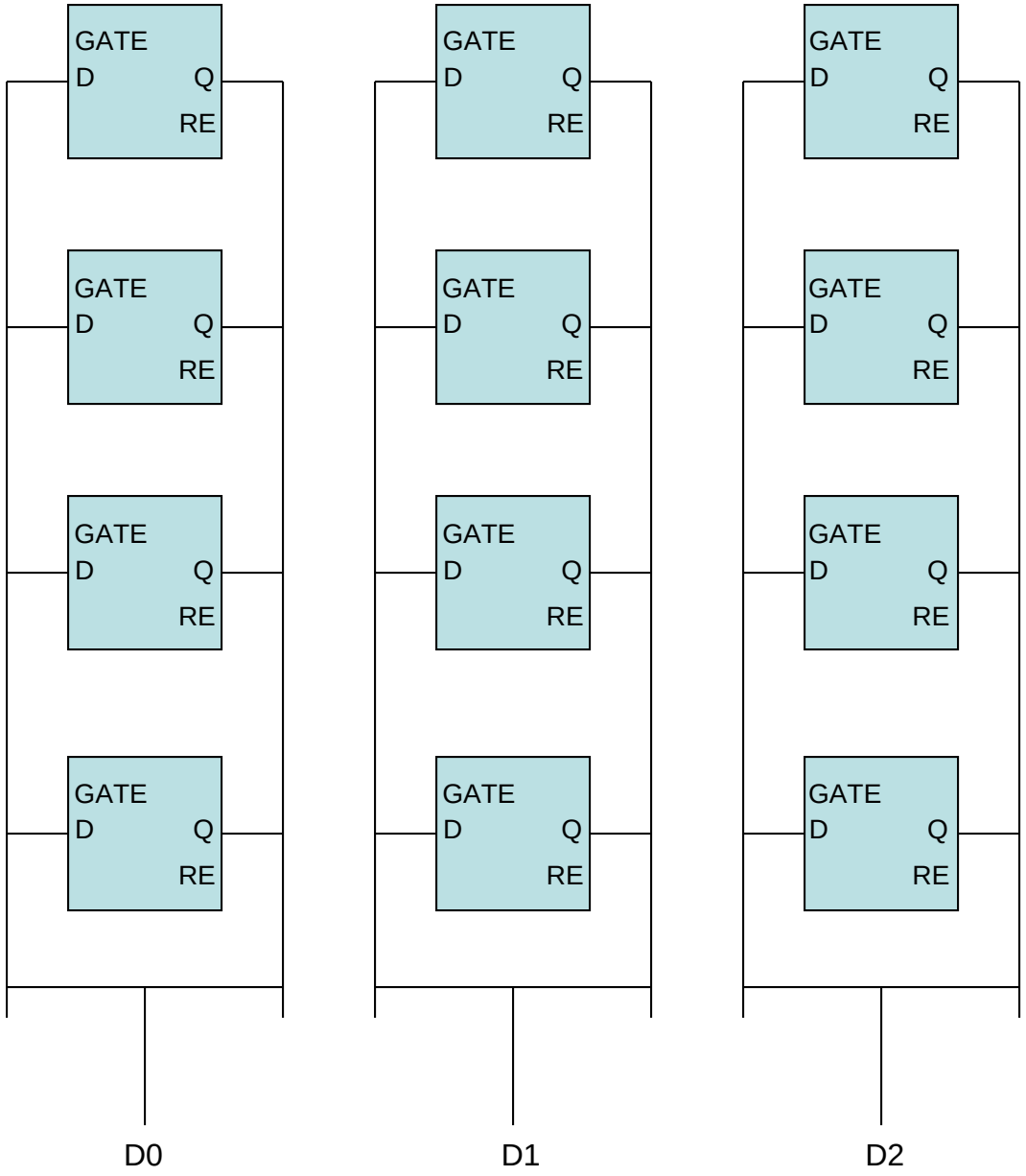
Add Dout Signals



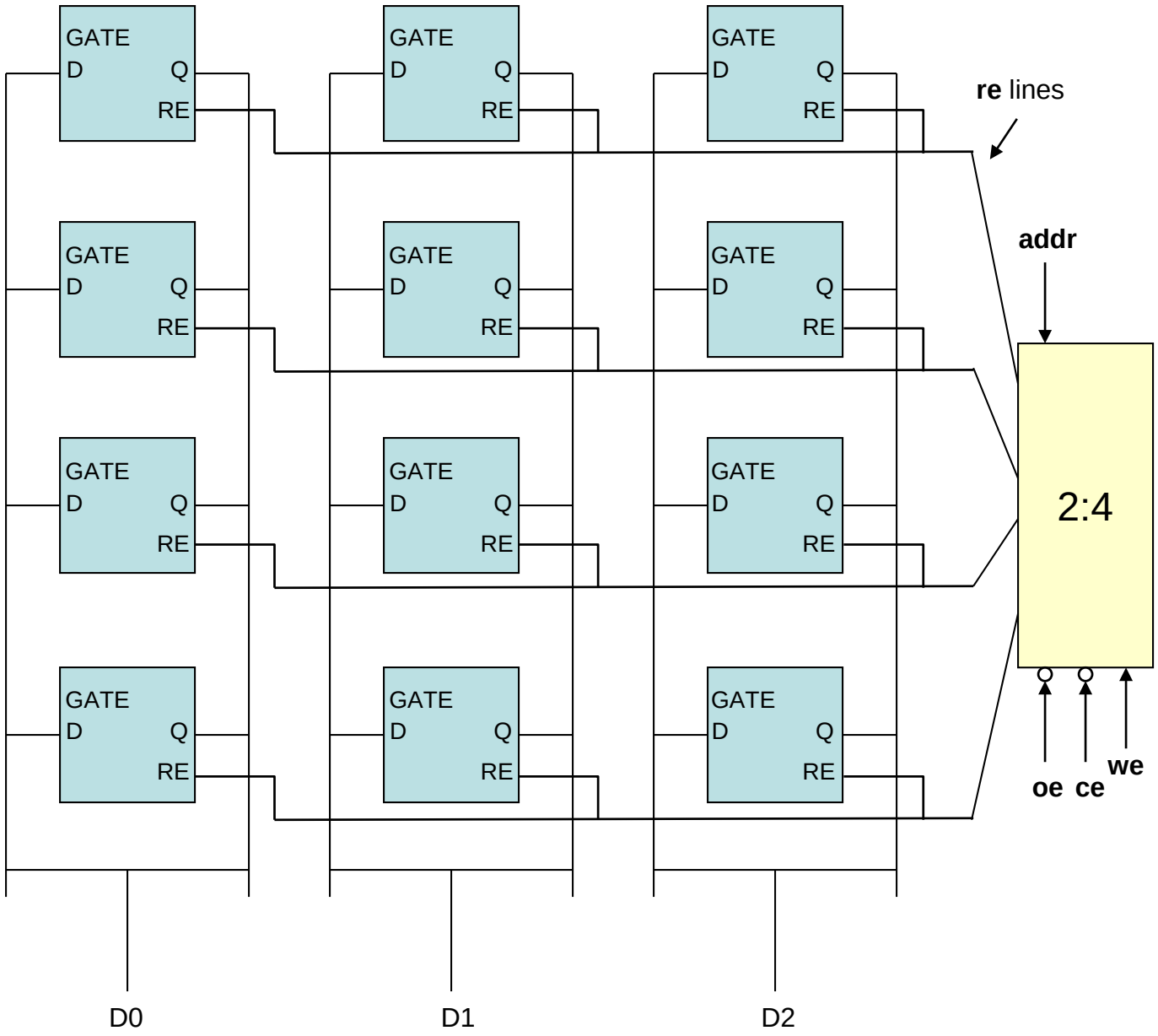
Add Din Signals



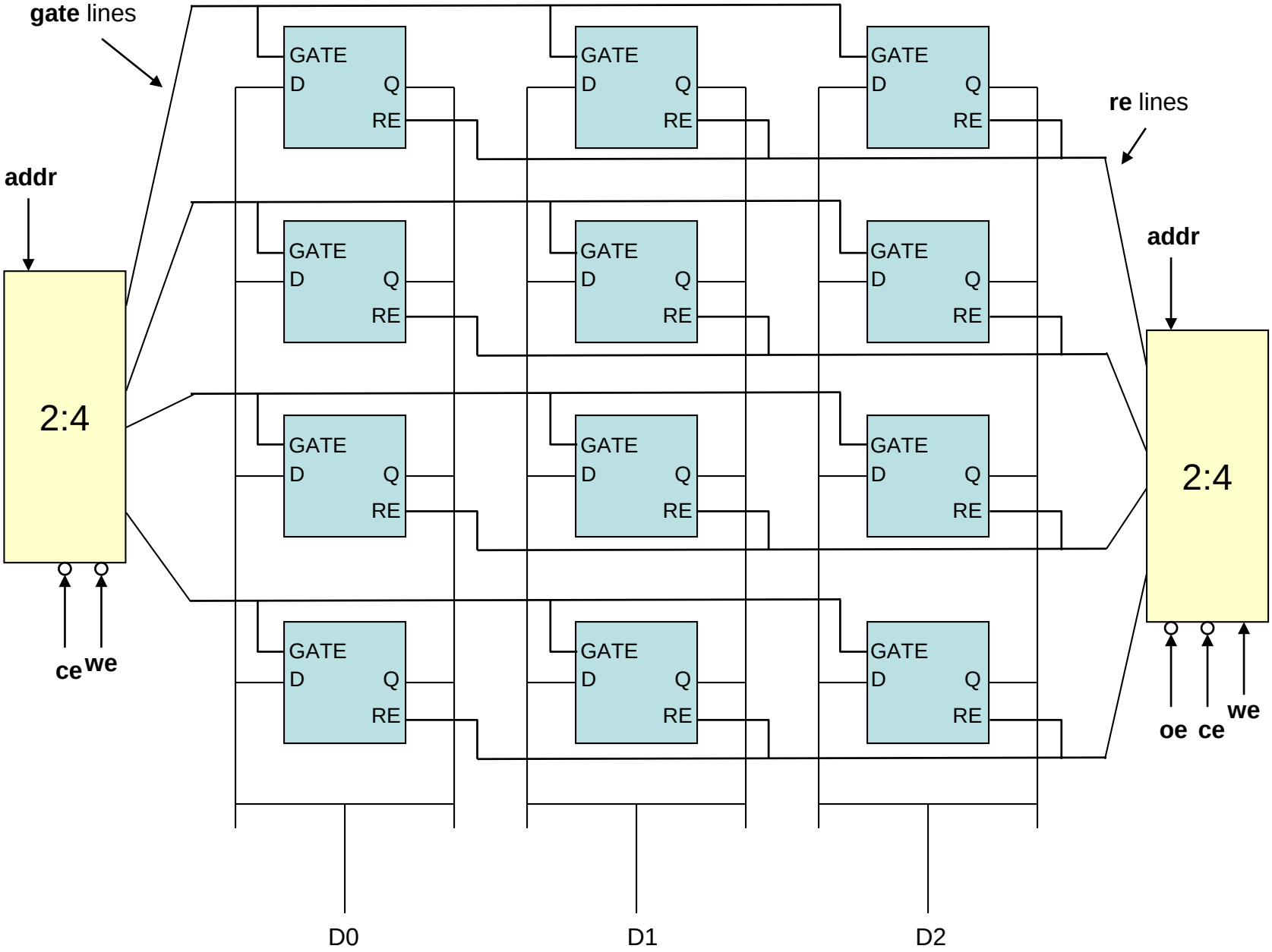
Connect Dout and Din Signals



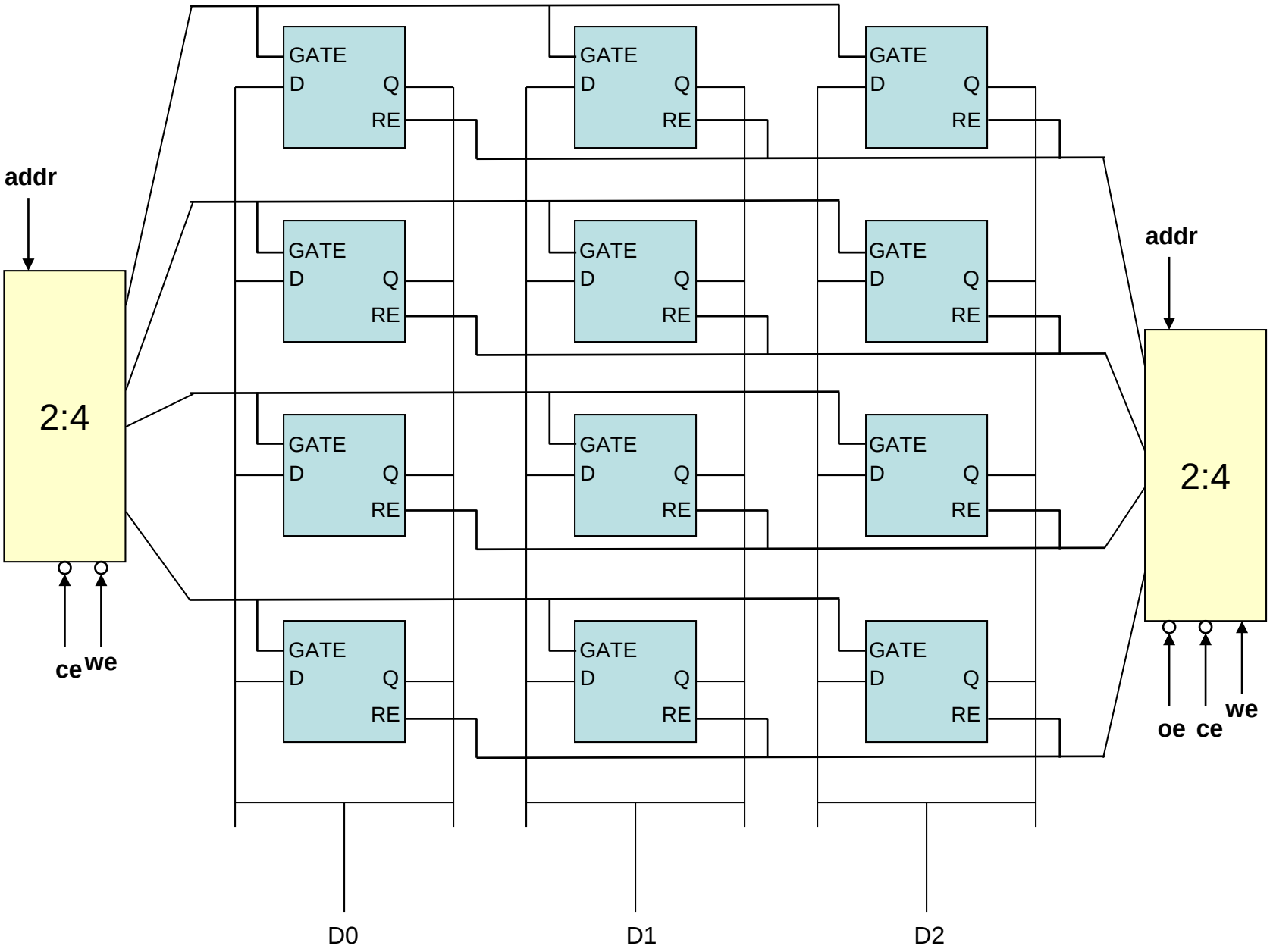
Add Read Decoder

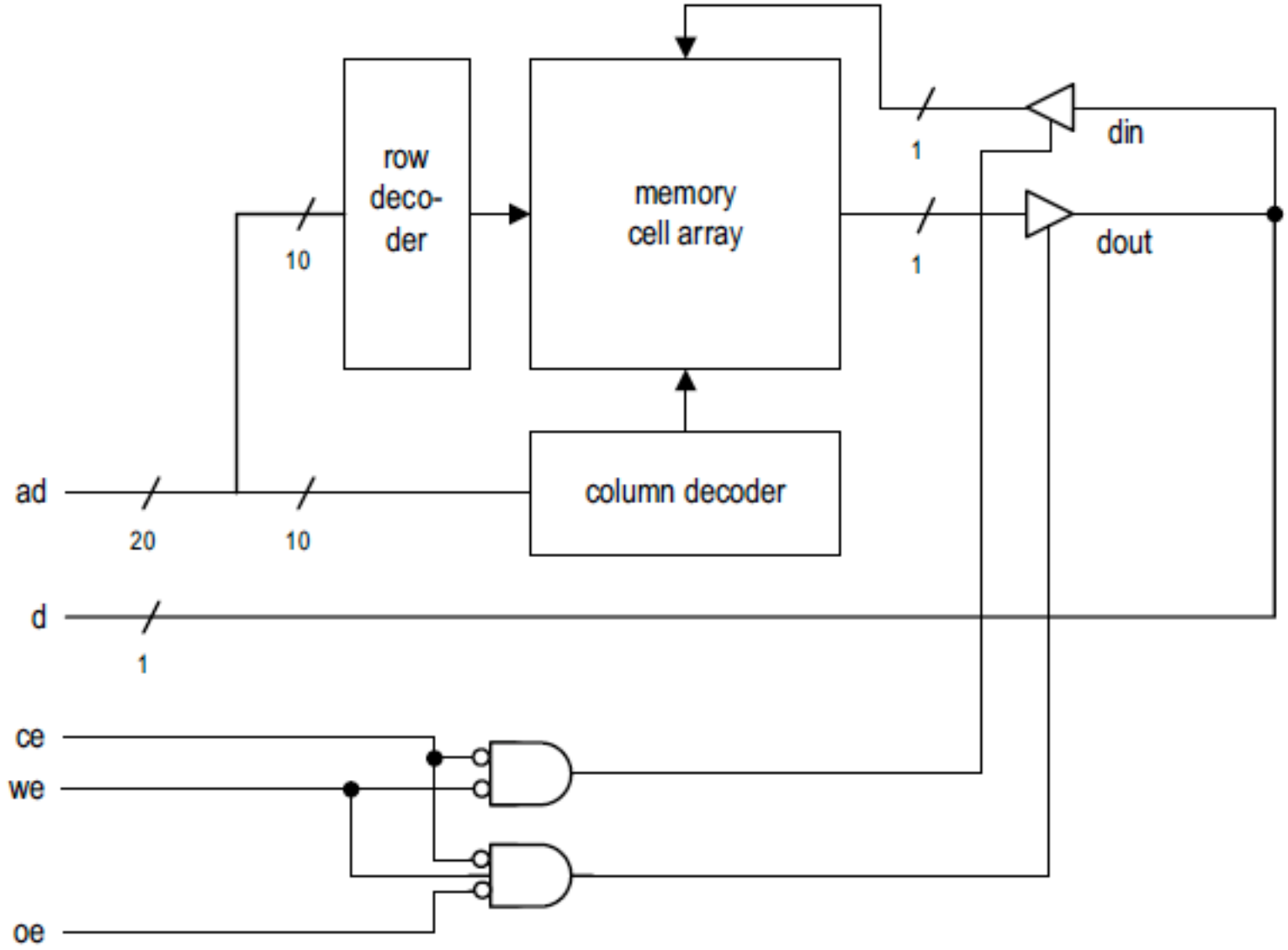


Add Write Decoder



Complete Memory

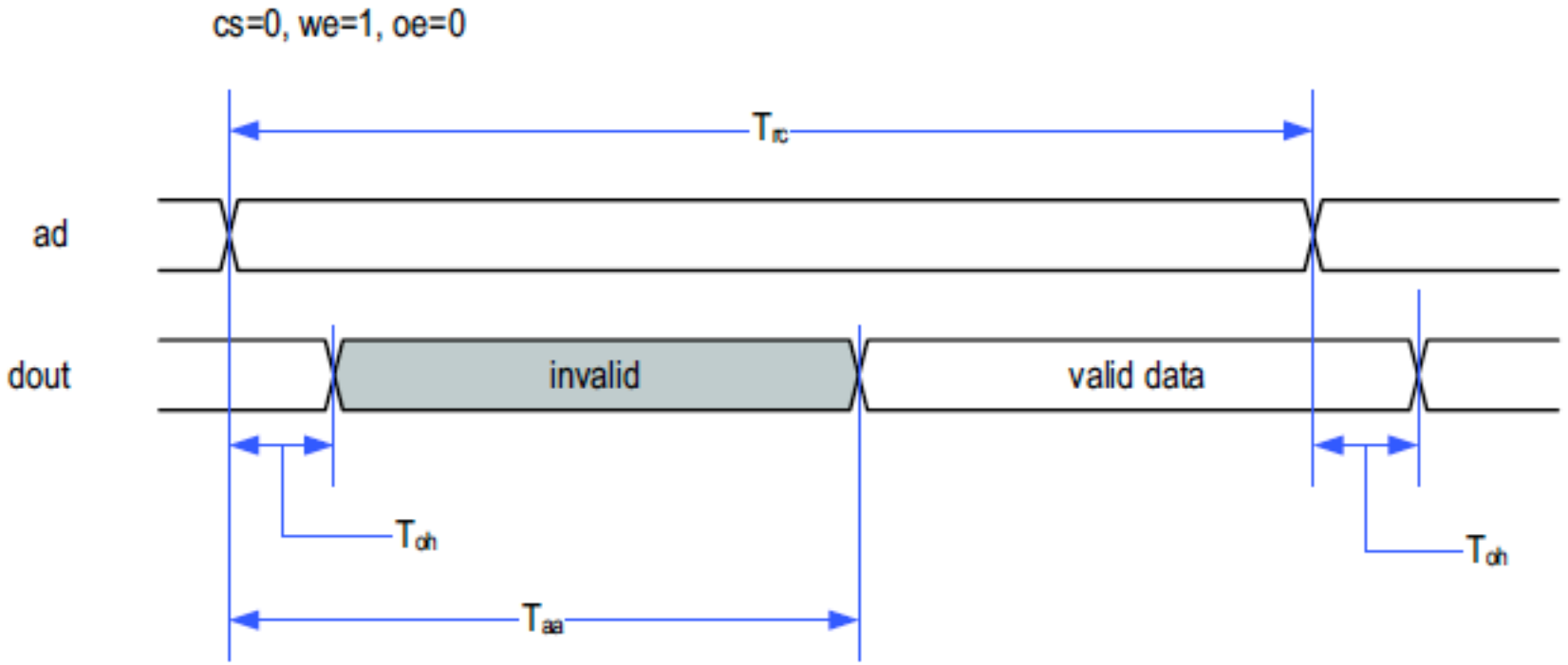




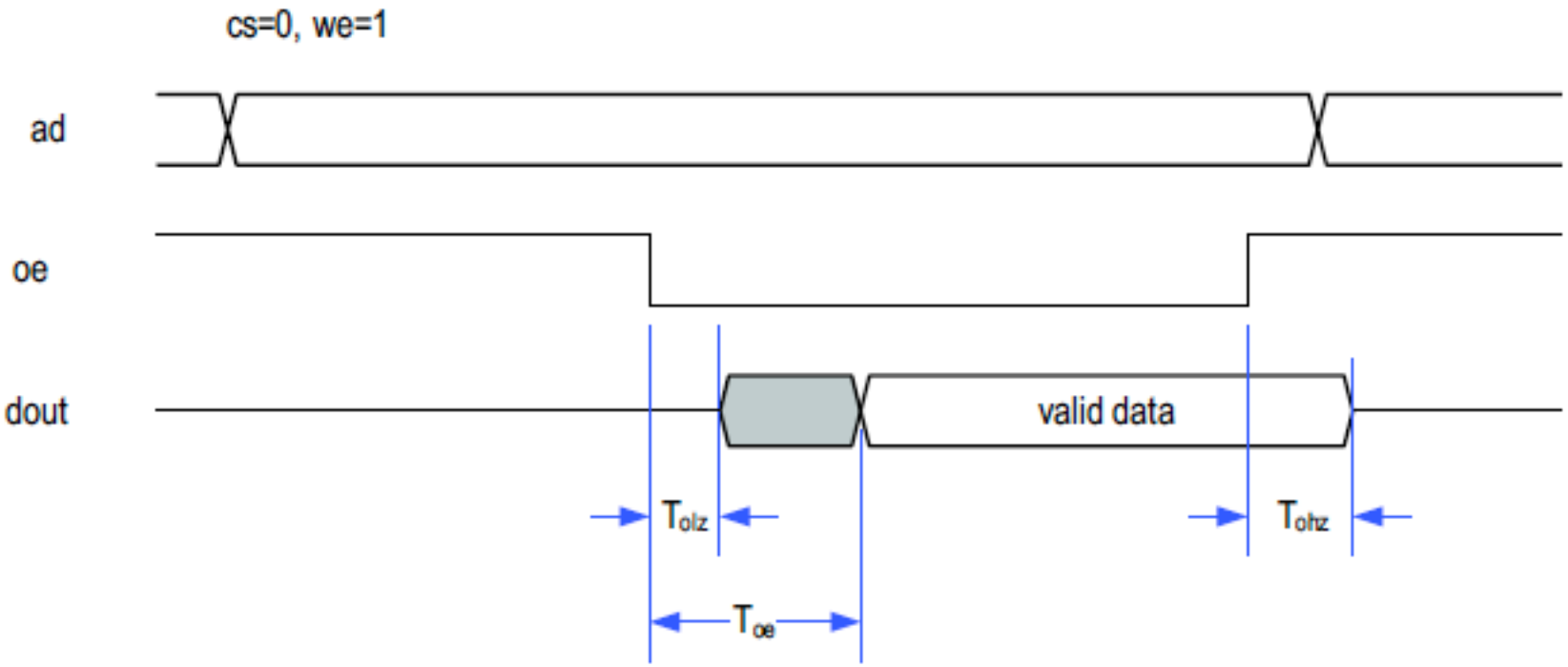
SRAM Block Diagram

ce	we	oe	**Operation**	**Data pin d**
1	-	-	no operation	Z
0	0	-	write	data in
0	1	0	read	data out
0	1	1	no operation	Z

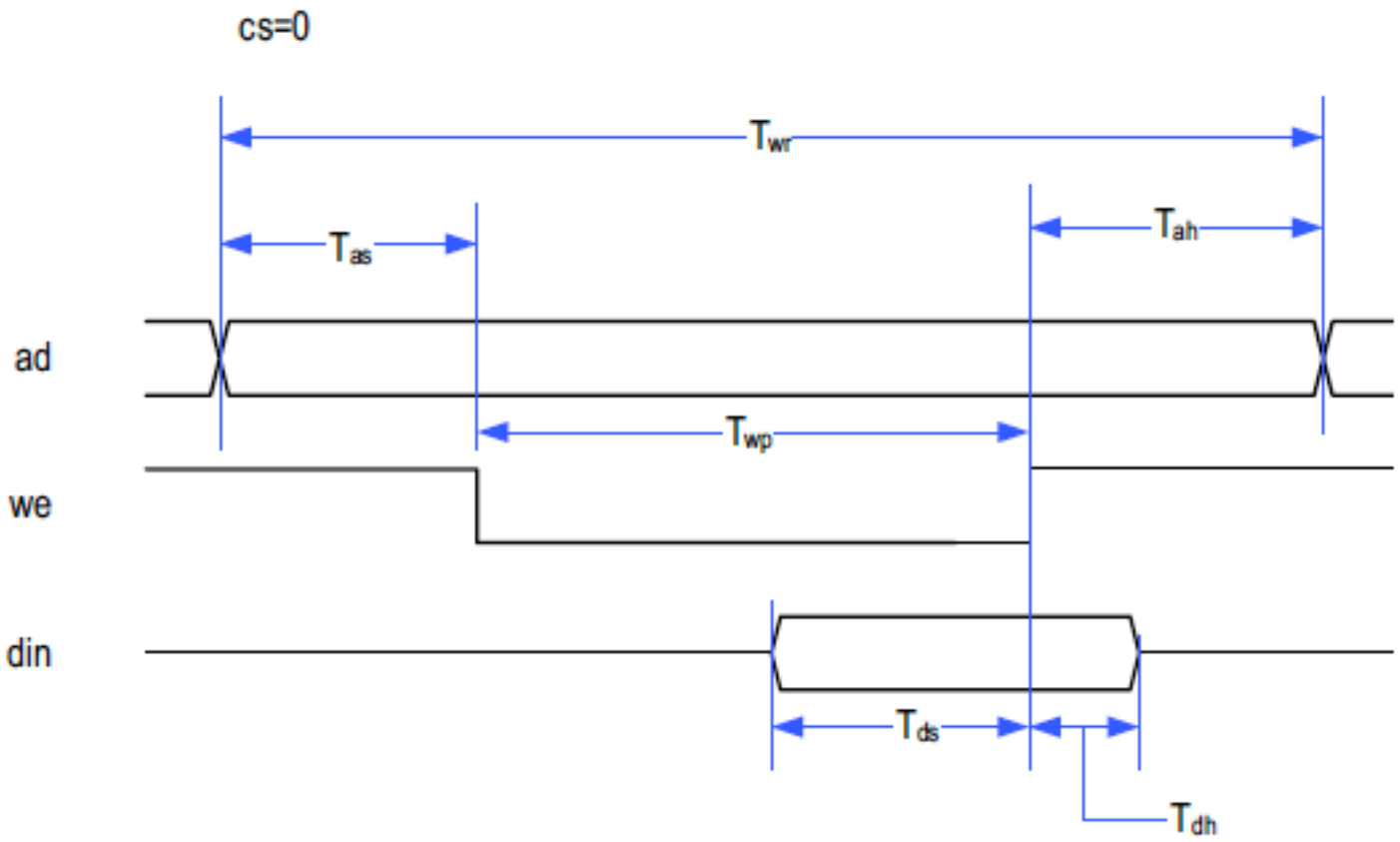
SRAM Control Signal Functionality



(a) Address-controlled read cycle



(b) oe-controlled read cycle



Timing Diagram of SRAM Write Cycle

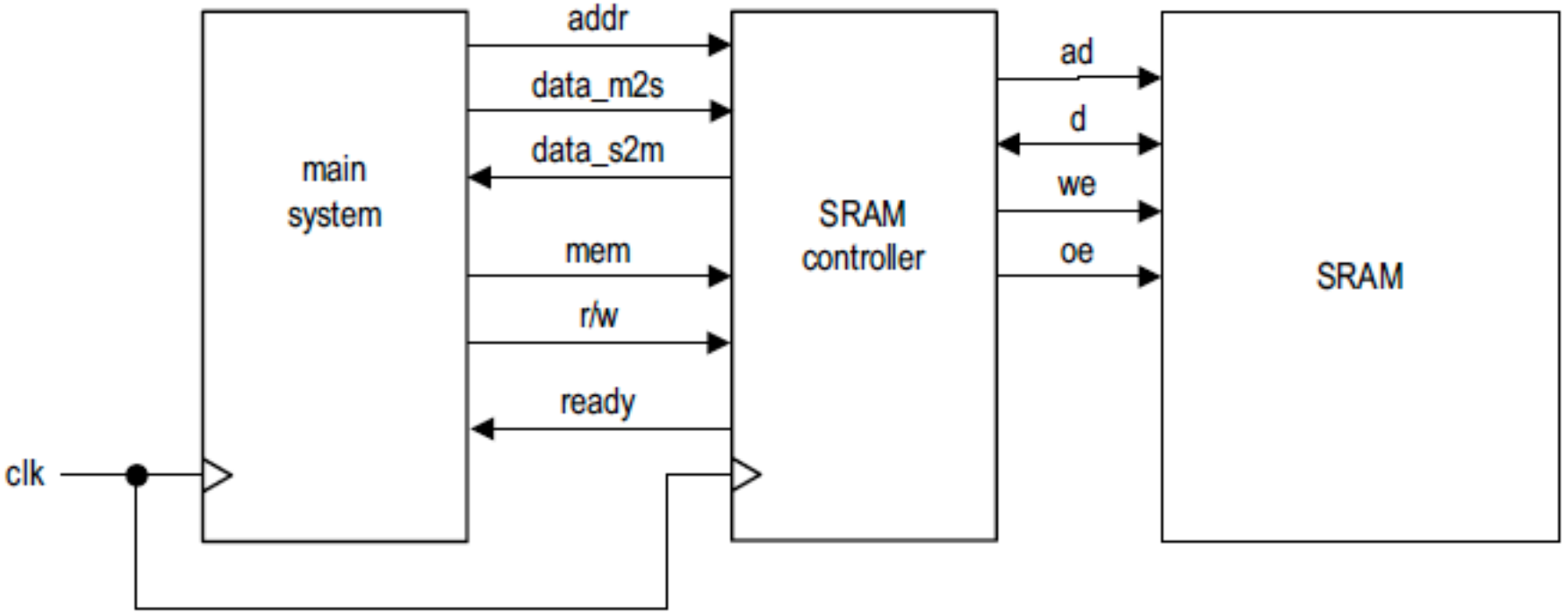


Figure 12.7 Role of an SRAM controller.

Role of SRAM Controller

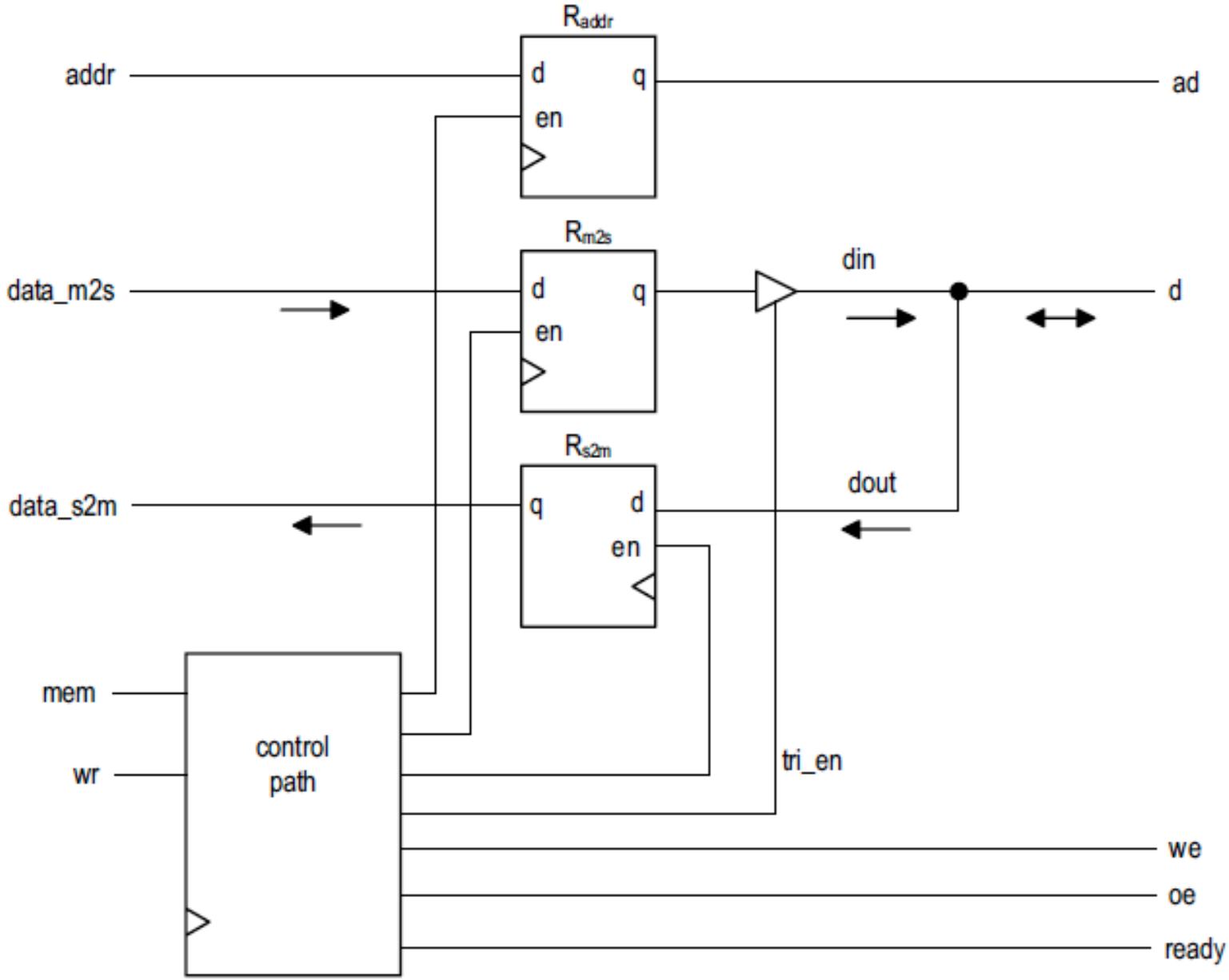
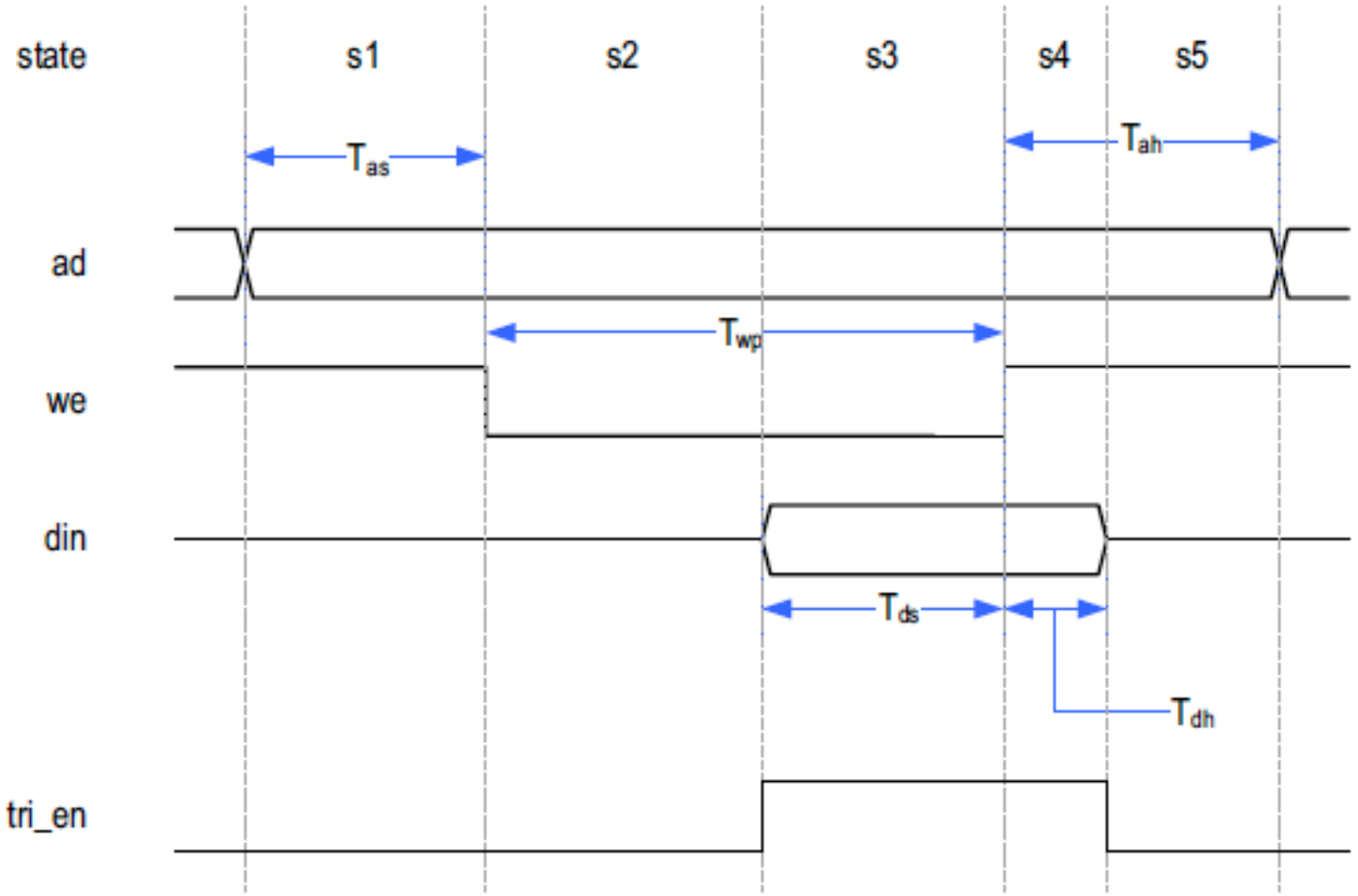
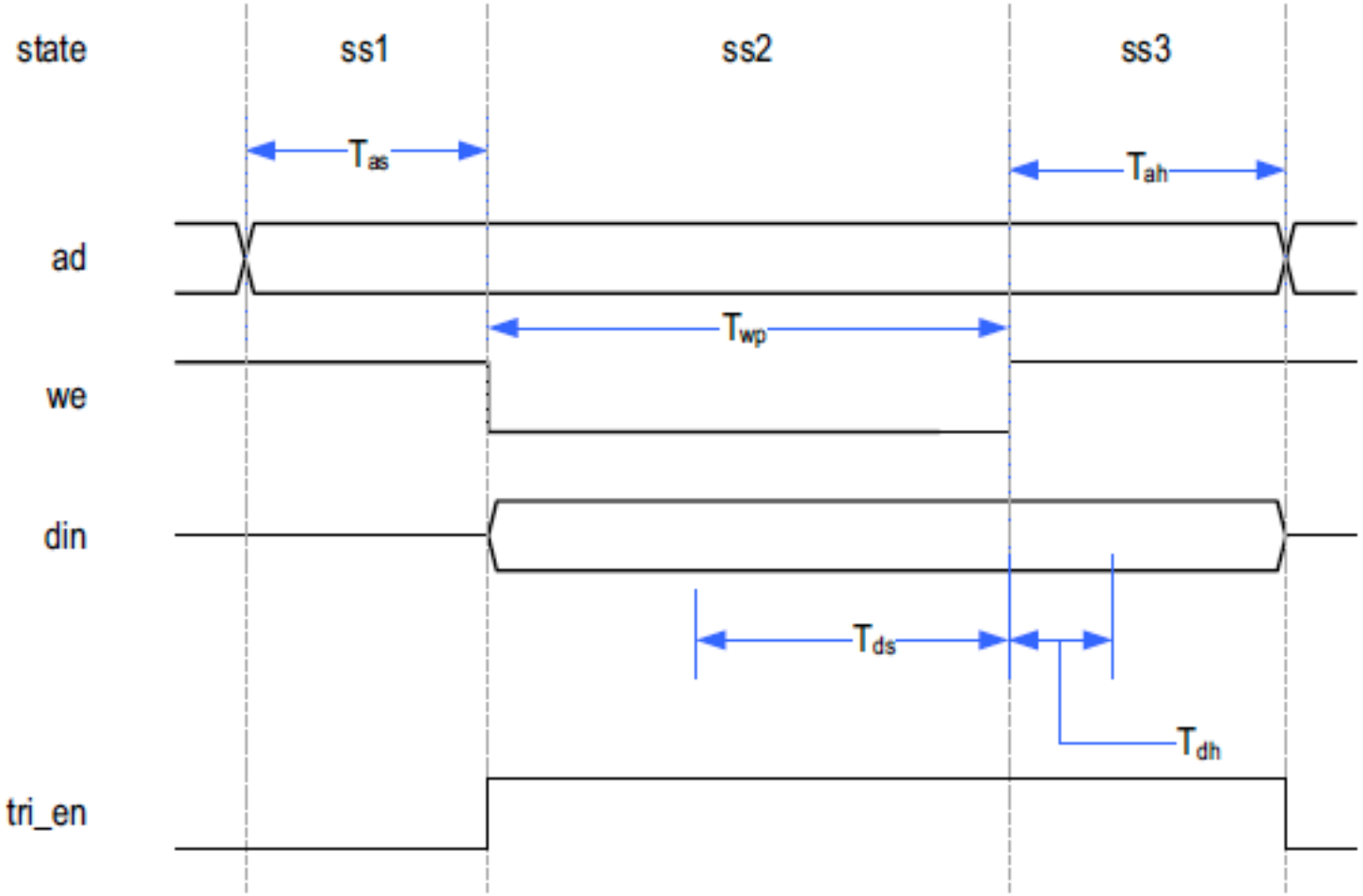


Figure 12.8 Block diagram of an SRAM controller.



(a) Five-state division

Working on the FSM Derivation…

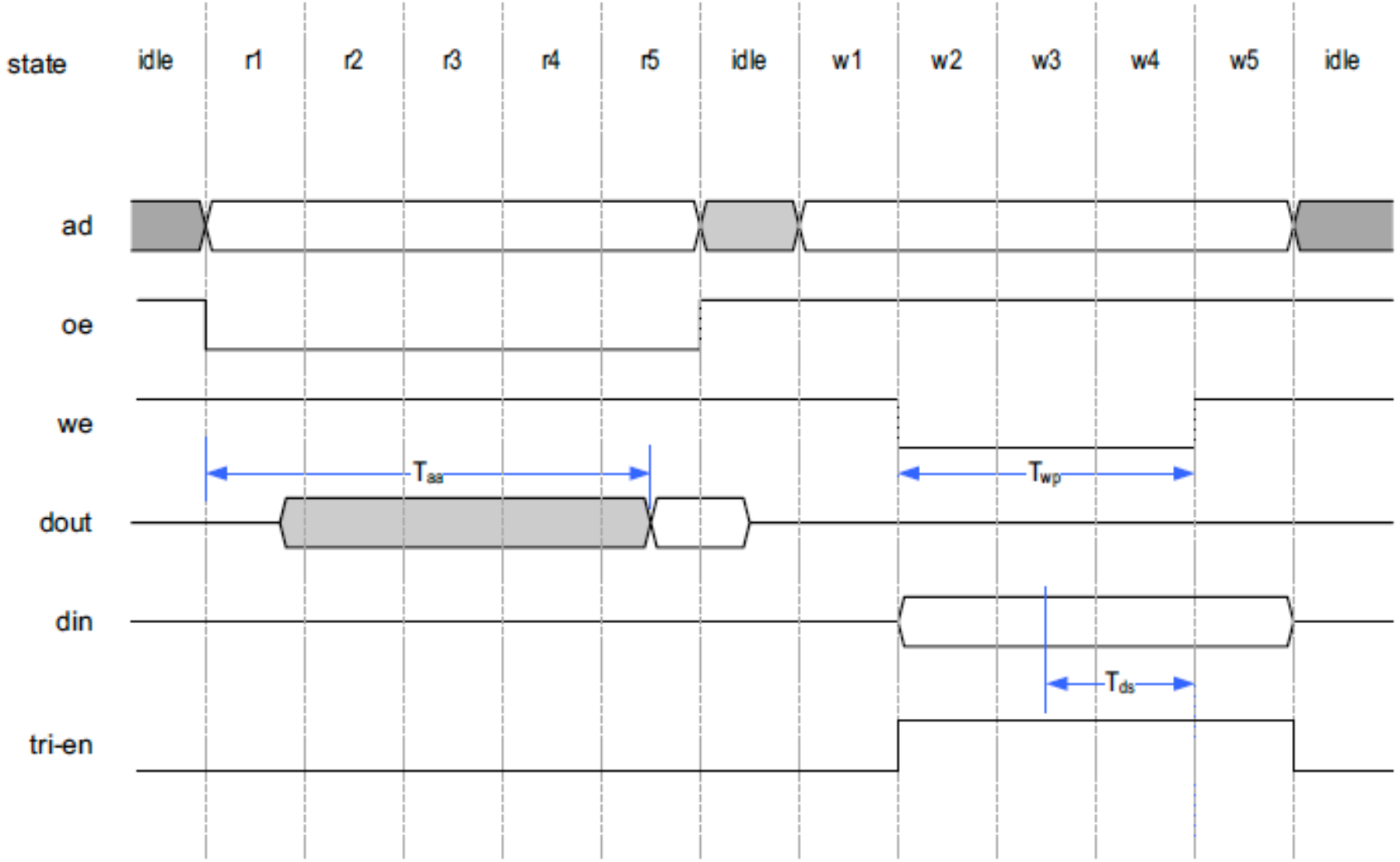


(b) Three-state division

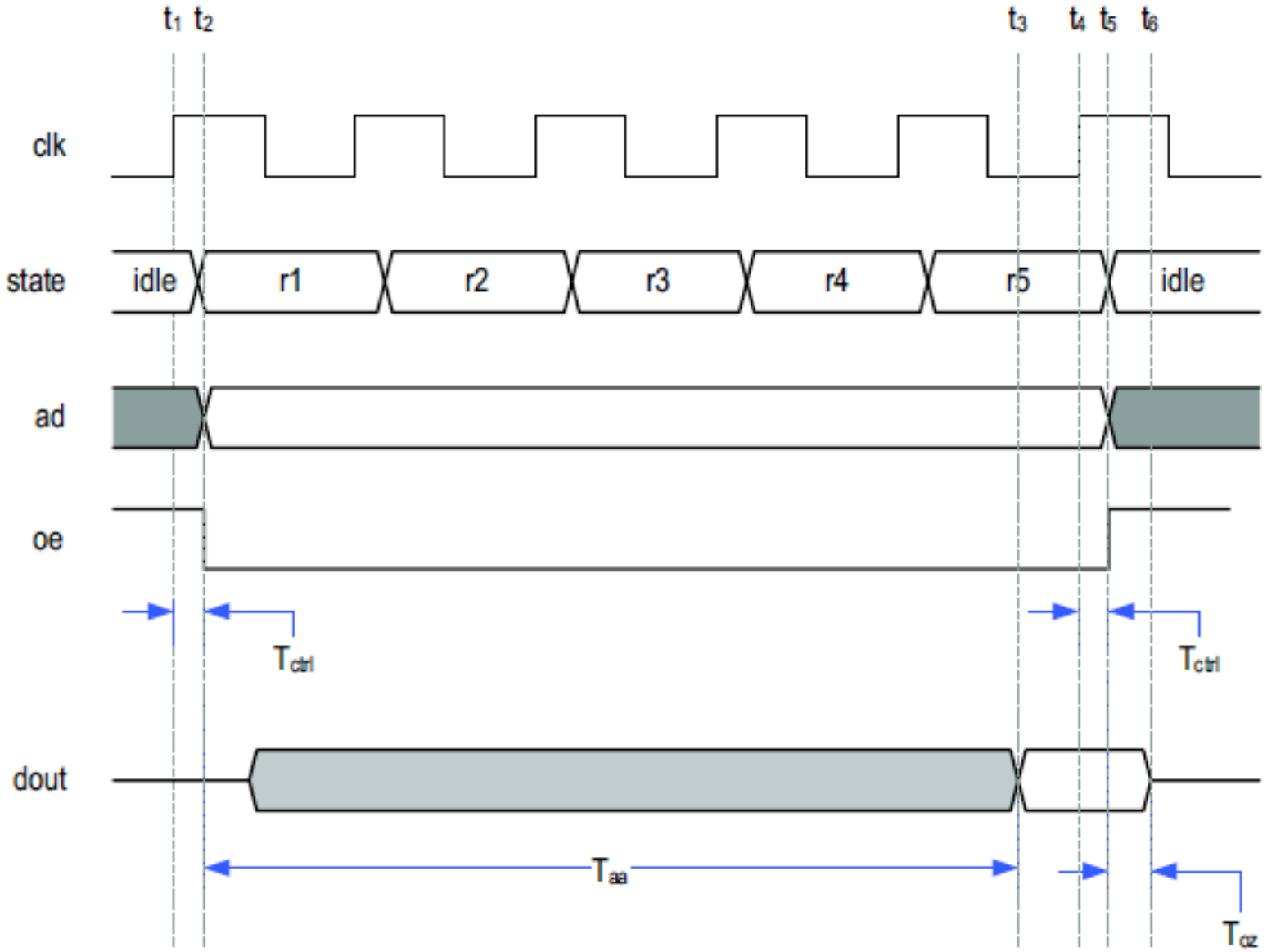
Timing

Parameter	**120 ns SRAM**	**20 ns SRAM**	**10 ns SRAM***	
T_{aa} (max) =	120 ns	20 ns	12 ns	
T_{oh} (min) =	10 ns	3 ns	2 ns	(T_{oha})
T_{olz} (min) =	10 ns	0 ns	0 ns	(T_{lzoe})
T_{oe} (max) =	80 ns	9 ns	5 ns	(T_{doe})
T_{ohz} (max) =	40 ns	9 ns	0 ns	(T_{hzoe})
T_{rc} (min) =	120 ns	20 ns	10 ns	
T_{wp} (min) =	70 ns	12 ns	8 ns	(T_{pwe1})
T_{as} (min) =	20 ns	0 ns	0 ns	(T_{sa})
T_{ah} (min) =	5 ns	0 ns	0 ns	(T_{ha})
T_{ds} (min) =	35 ns	1 ns	6 ns	(T_{sd})
T_{dh} (min) =	5 ns	0 ns	0 ns	(T_{hd})
T_{wr} (min) =	120 ns	20 ns	10 ns	(T_{wc})

System clock rate: 40 Mhz (25 ns clock period)

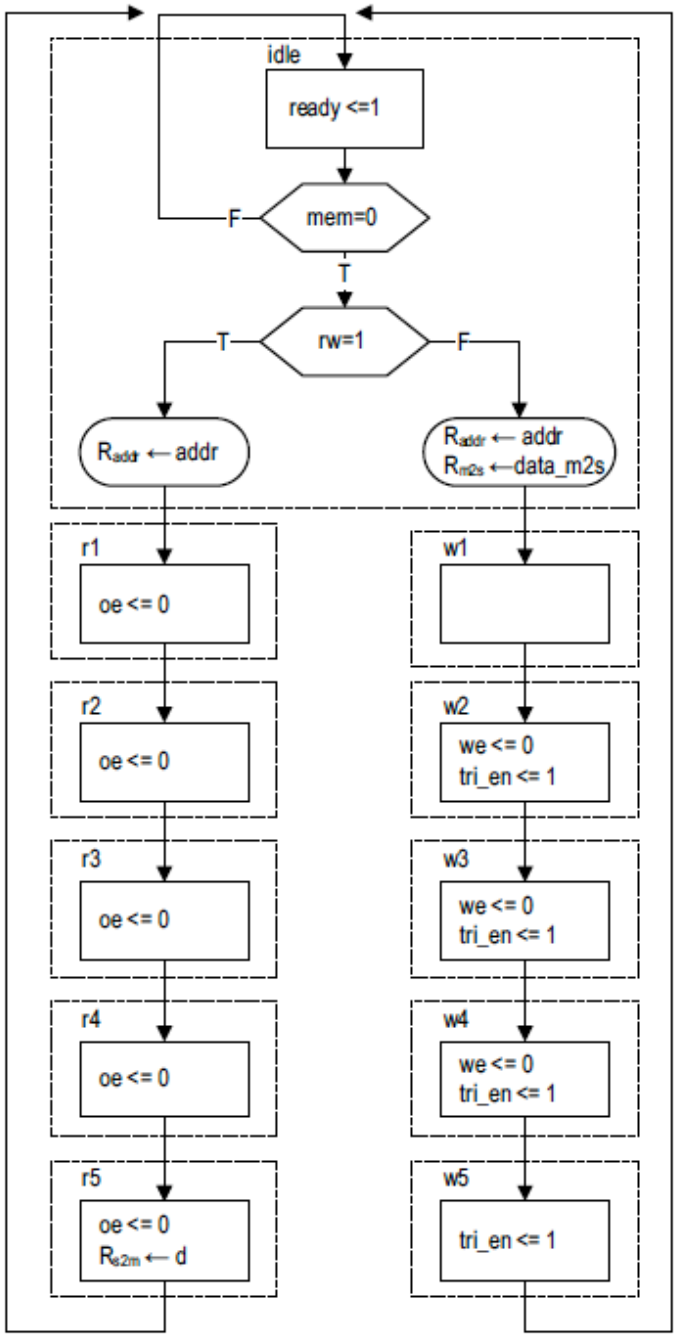


Read Followed by Write (Slow RAM)



Detailed Read Timing

Default: oe <= 1; we <= 1; tri_en <= 0; ready <= 0



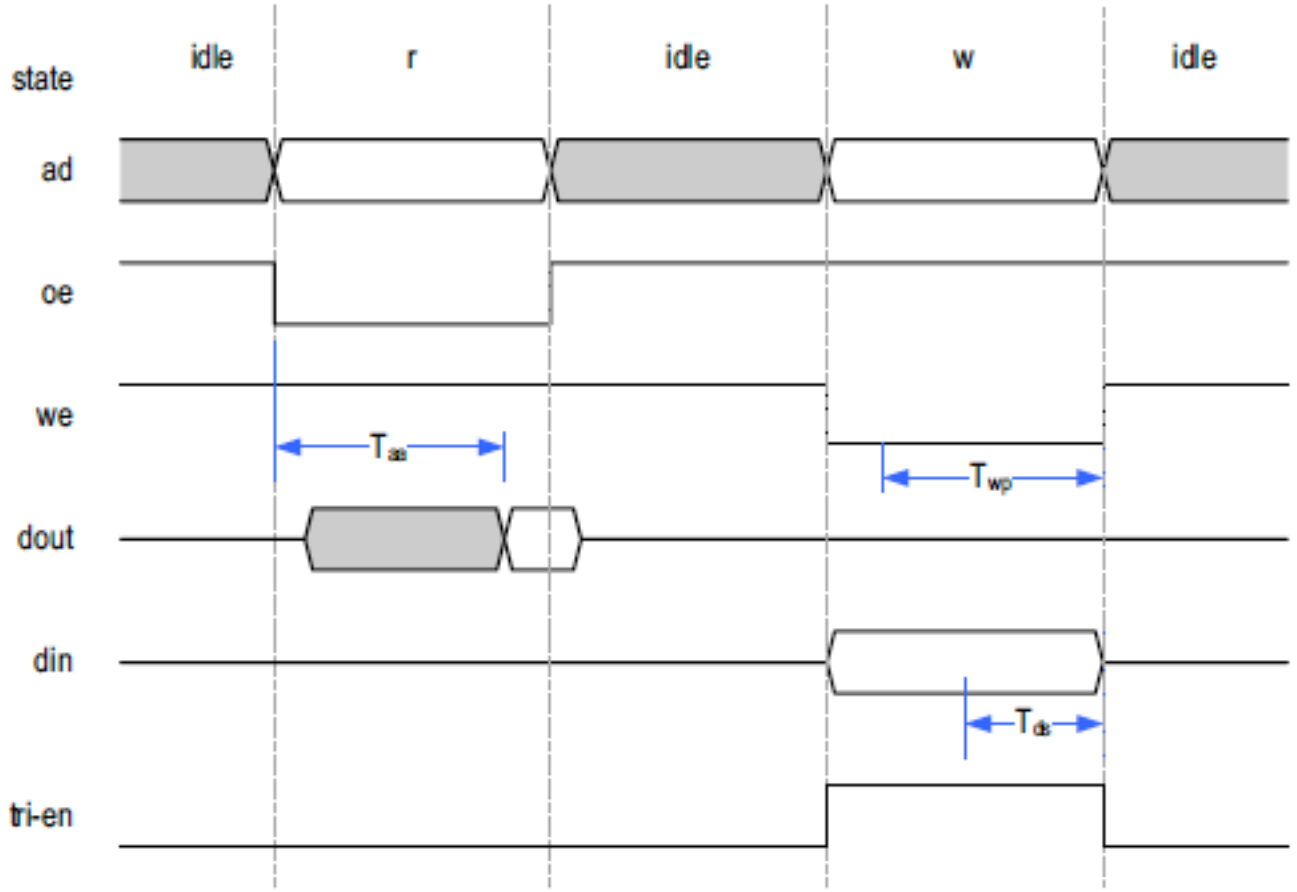


Figure 12.14 Division of read and write cycles of a fast SRAM.

Read and Write in a Fast RAM

Write Setup and Hold Times