N3	N2	N1	N0	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

LAB #4 7 SEGMENT DECODER

Ty Madsen
ECEN 220-03
4-Sept-2013

a (rows: N1N0, columns: N3N2)

N1N0 \ N3N2	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	0	0	0	1
10	0	0	0	0

c (rows: N1N0, columns: N3N1)

N1N0 \ N3N1	00	01	11	10
00	0	0	1	0
01	0	0	0	0
11	0	0	1	0
10	1	0	1	0

e (rows: N1N0, columns: N3N2)

N1N0 \ N3N2	00	01	11	10
00	0	1	0	0
01	1	1	0	1
11	1	1	0	0
10	0	0	0	0

$a = A'B'C'D + A'BC'D' + ABC'D + AB'CD$

$C = A'B'CD' + ABC + ABD'$

$e = A'D + A'BC' + B'C'D$

D 8 6 6
1101 1000|0110|0000

b = 1101|1100|0011|00000
d = 1000 0100 1001 0010
f = 0010 1000 1000 1110
g = 0001 0000 1000 0011

0123 4567 891011 12131415

0001 0011 0010 0101

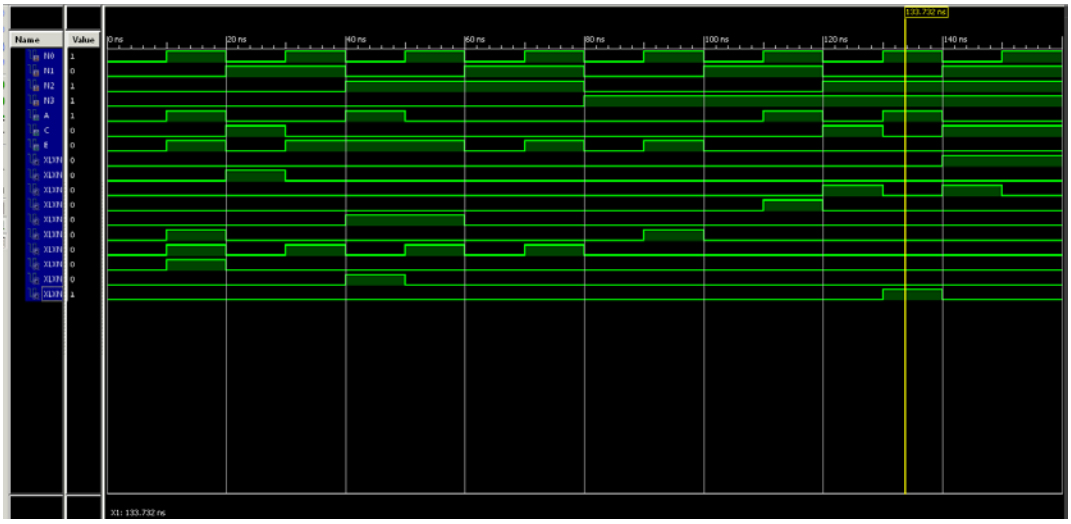
1010 0100 1100 1000

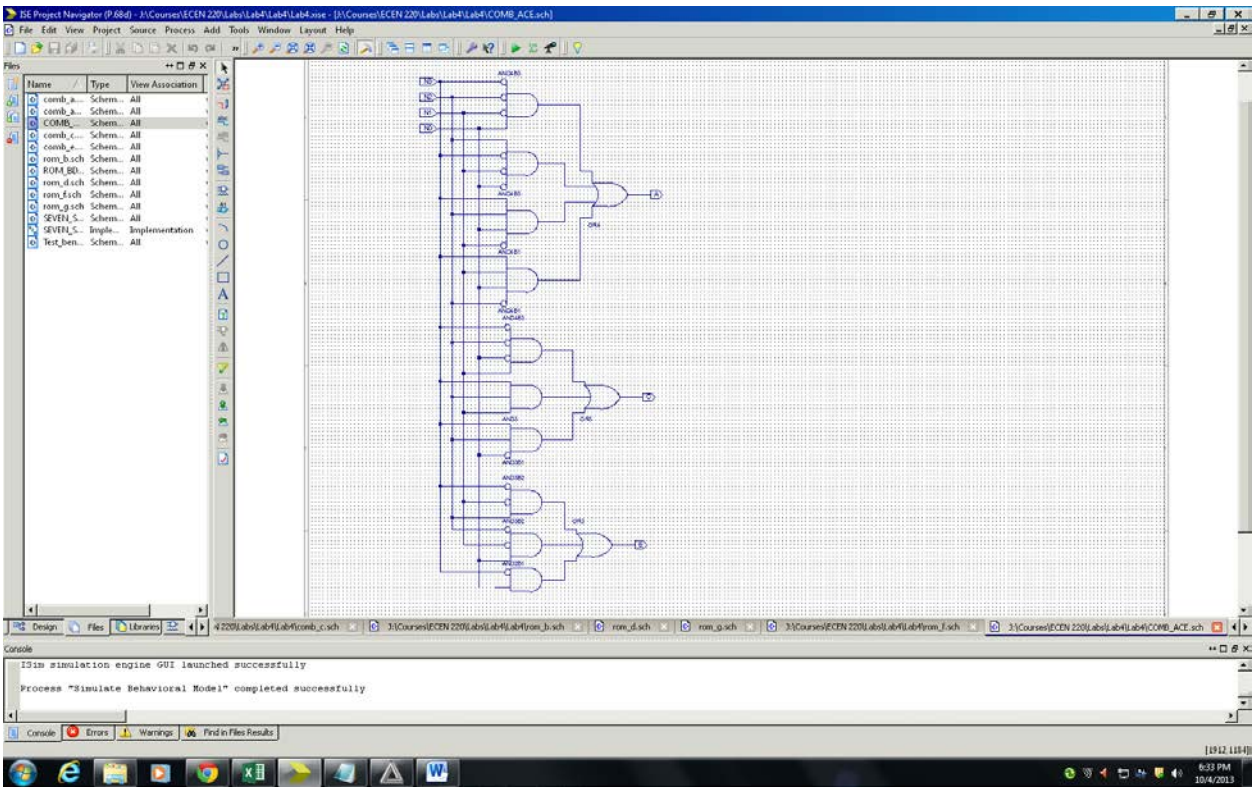
0

- 0) □ ✓
- 1) 1 x
- 2) 2 x
- 3) 3 x
- 4) 4 X
- 5) 5 x
- 6) 6 ✓
- 7) 7 x
- 8) 8 x
- 9) 9 ✓
- A) A x
- b) b x
- c) C x
- d) d x
- e) E x

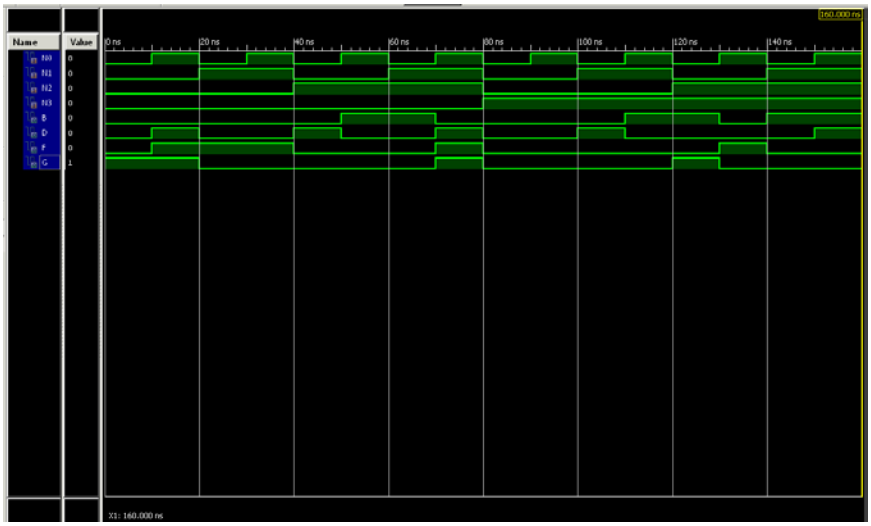
Bin	Character	AN3	AN2	AN1	AN0
0000	0	0	X	X	Y
0001	1	1	X	X	
0010	2	2	X	X	
0011	3	3	X	X	
0100	4	4	X	X	
0101	5	5	X	X	
0110	6	6	X		
0111	7	7	X		
1000	8	8	X		
1001	9	9	X		
1010	A	A	X		
1011	b	b	X		
1100	C	C	X		
1101	d	d	X		
1110	E	E	X		
1111	F	F			

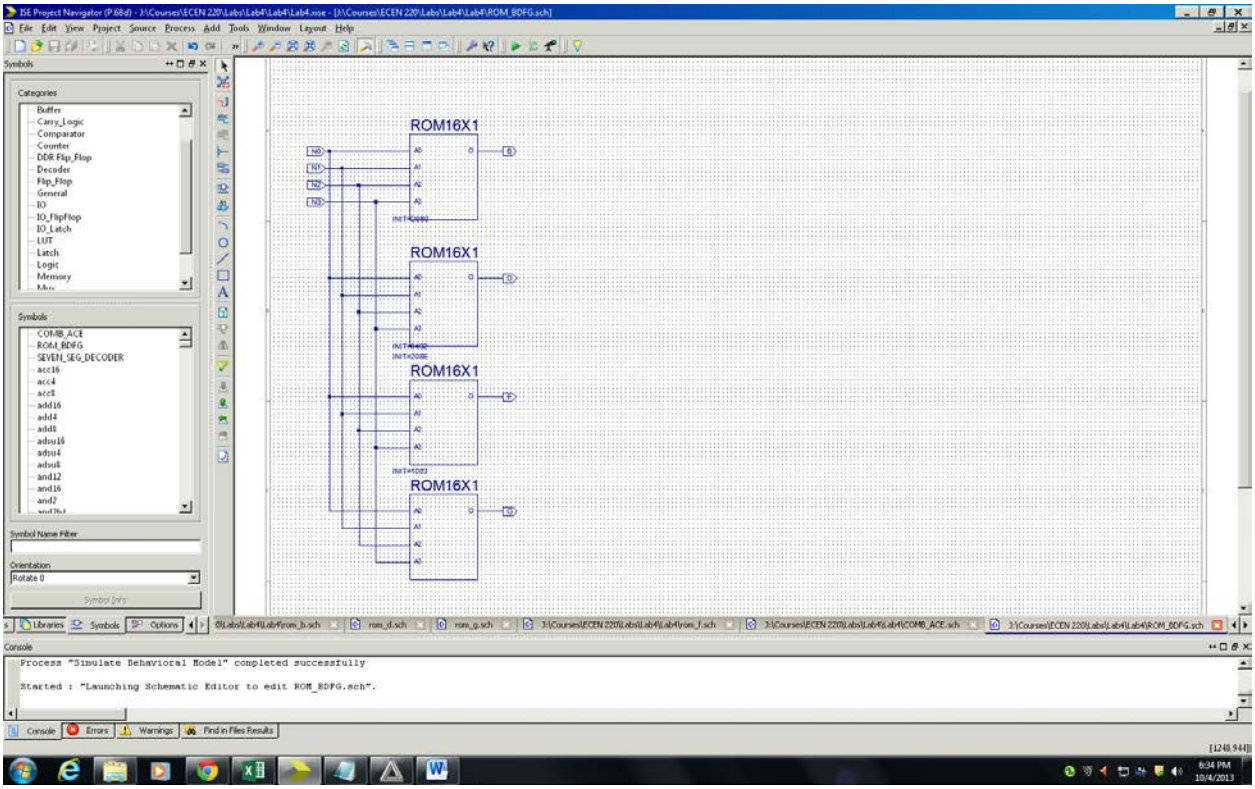
Combinational a, c, e



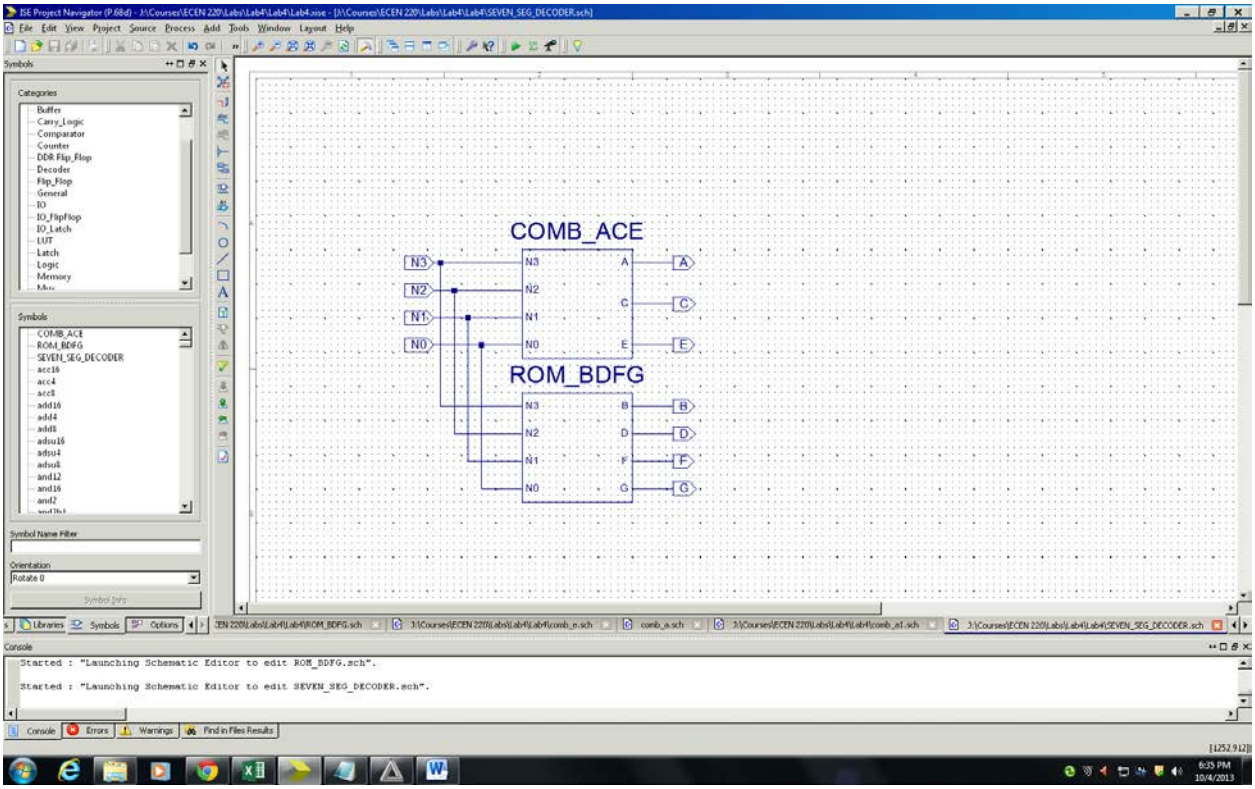


Rom b, d, f, g

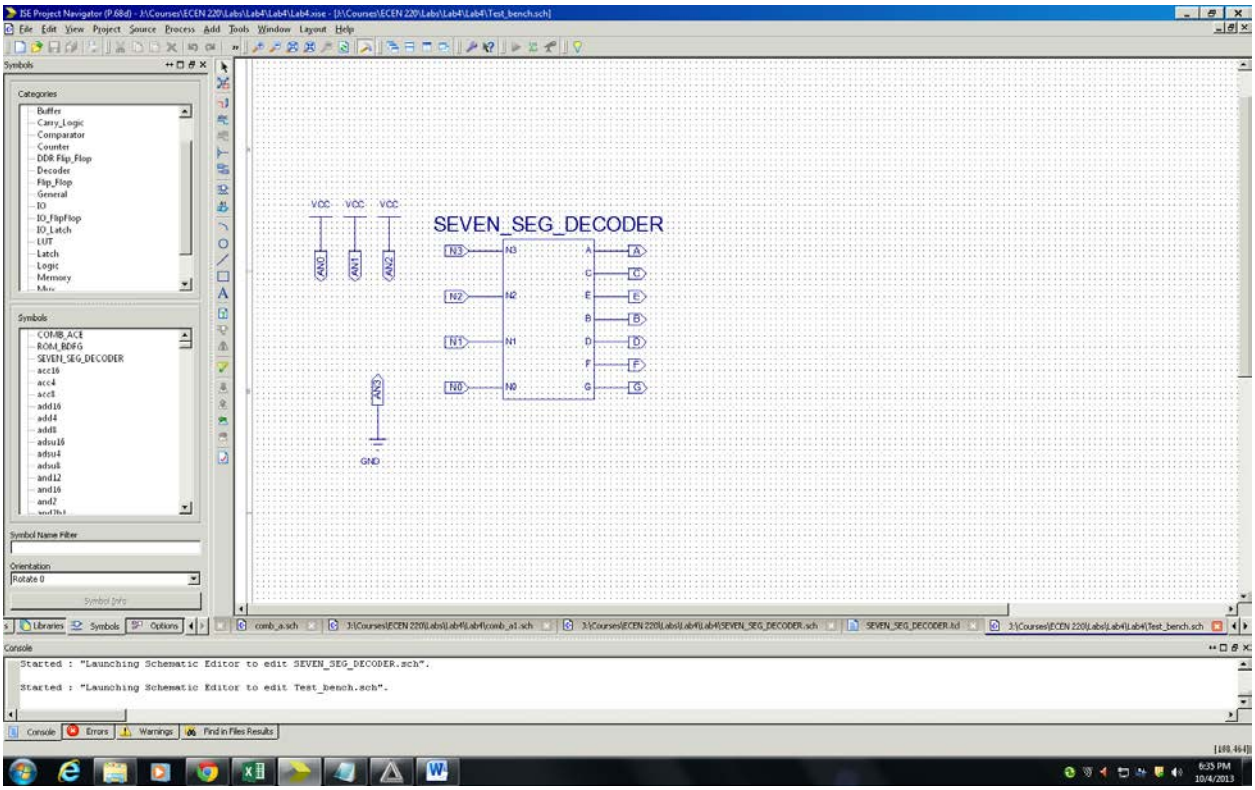

Name
Value
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160.000 ns
X1: 160.000 ns


ISE Project Navigator (P.68d)
File Edit View Project Source Process Add Tools Window Layout Help
Symbols
Categories
Buffer
Carry_Logic
Comparator
Counter
DDR Flip_Flop
Decoder
Flip_Flop
General
IO
IO_FlipFlop
IO_Latch
LUT
Latch
Logic
Memory
Symbols
COMB_ACE
ROM_BDFG
SEVEN_SEG_DECODER
Symbol Name Filter
Orientation
Rotate 0
ROM16X1
ROM16X1
ROM16X1
ROM16X1
Console
Process "Simulate Behavioral Model" completed successfully
Started : "Launching Schematic Editor to edit ROM_BDFG.sch".
Console
Errors
Warnings
Find in Files Results
6:34 PM
10/4/2013

Seven Segment Decoder



Test Bench



UCF

```
## Switches
#NET "sw<0>" LOC = "G18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW0
#NET "sw<1>" LOC = "H18"; # Bank = 1, Pin name = IP/VREF_1, Type = VREF, Sch name = SW1
#NET "sw<2>" LOC = "K18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW2
#NET "sw<3>" LOC = "K17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW3
NET N0 LOC = "L14"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW4
NET N1 LOC = "L13"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW5
NET N2 LOC = "N17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW6
NET N3 LOC = "R17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW7

## Buttons
#NET "btn<0>" LOC = "B18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN0
#NET "btn<1>" LOC = "D18"; # Bank = 1, Pin name = IP/VREF_1, Type = VREF, Sch name = BTN1
#NET "btn<2>" LOC = "E18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN2
#NET "btn<3>" LOC = "H13"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN3

## 7 segment display
NET A LOC = "L18"; # Bank = 1, Pin name = IO_L10P_1, Type = I/O, Sch name = CA
NET B LOC = "F18"; # Bank = 1, Pin name = IO_L19P_1, Type = I/O, Sch name = CB
NET C LOC = "D17"; # Bank = 1, Pin name = IO_L23P_1/HDC, Type = DUAL, Sch name = CC
NET D LOC = "D16"; # Bank = 1, Pin name = IO_L23N_1/LDC0, Type = DUAL, Sch name = CD
NET E LOC = "G14"; # Bank = 1, Pin name = IO_L20P_1, Type = I/O, Sch name = CE
NET F LOC = "J17"; # Bank = 1, Pin name = IO_L13P_1/A6/RHCLK4/IRDY1, Type = RHCLK/DUAL, Sch name = CF
NET G LOC = "H14"; # Bank = 1, Pin name = IO_L17P_1, Type = I/O, Sch name = CG
#NET "dp"     LOC = "C17"; # Bank = 1, Pin name = IO_L24N_1/LDC2, Type = DUAL, Sch name = DP

NET AN0 LOC = "F17"; # Bank = 1, Pin name = IO_L19N_1, Type = I/O, Sch name = AN0
NET AN1 LOC = "H17"; # Bank = 1, Pin name = IO_L16N_1/A0, Type = DUAL, Sch name = AN1
NET AN2 LOC = "C18"; # Bank = 1, Pin name = IO_L24P_1/LDC1, Type = DUAL, Sch name = AN2
NET AN3 LOC = "F15"; # Bank = 1, Pin name = IO_L21P_1, Type = I/O, Sch name = AN3

## VGA Connector
#NET "vgaRed<1>"   LOC = "R9"; # Bank = 2, Pin name = IO/D5, Type = DUAL, Sch name = RED0
#NET "vgaRed<2>"   LOC = "T8"; # Bank = 2, Pin name = IO_L10N_2, Type = I/O, Sch name = RED1
```

TCL file

SEVEN_SEG_DECODER.tcl

```
#add all signals to the waveform viewer
wave add / -radix hex



#define how the data input signals will behave when you run the simulation
#the command "isim force add {signal} 0 -time 0 -value 1 -time 20ns -repeat 40ns" means that {signal}
#will have a value of 0 from time 0, then change to 1 at time 20ns, and then repeat that cycle every 40ns
isim force add N0 0 -time 0 -value 1 -time 10ns -repeat 20ns
isim force add N1 0 -time 0 -value 1 -time 20ns -repeat 40ns
isim force add N2 0 -time 0 -value 1 -time 40ns -repeat 80ns
isim force add N3 0 -time 0 -value 1 -time 80ns -repeat 160ns


#Nothing will change in the waveform viewer until you run the simulation for some period of time.
run 160ns
```

Tool Command Language file | length : 707 | lines : 17 | Ln : 1 | Col : 1 | Sel : 0 | UNIX | ANSI | INS