Ty Madsen
Ecen 220
October 17, 2013

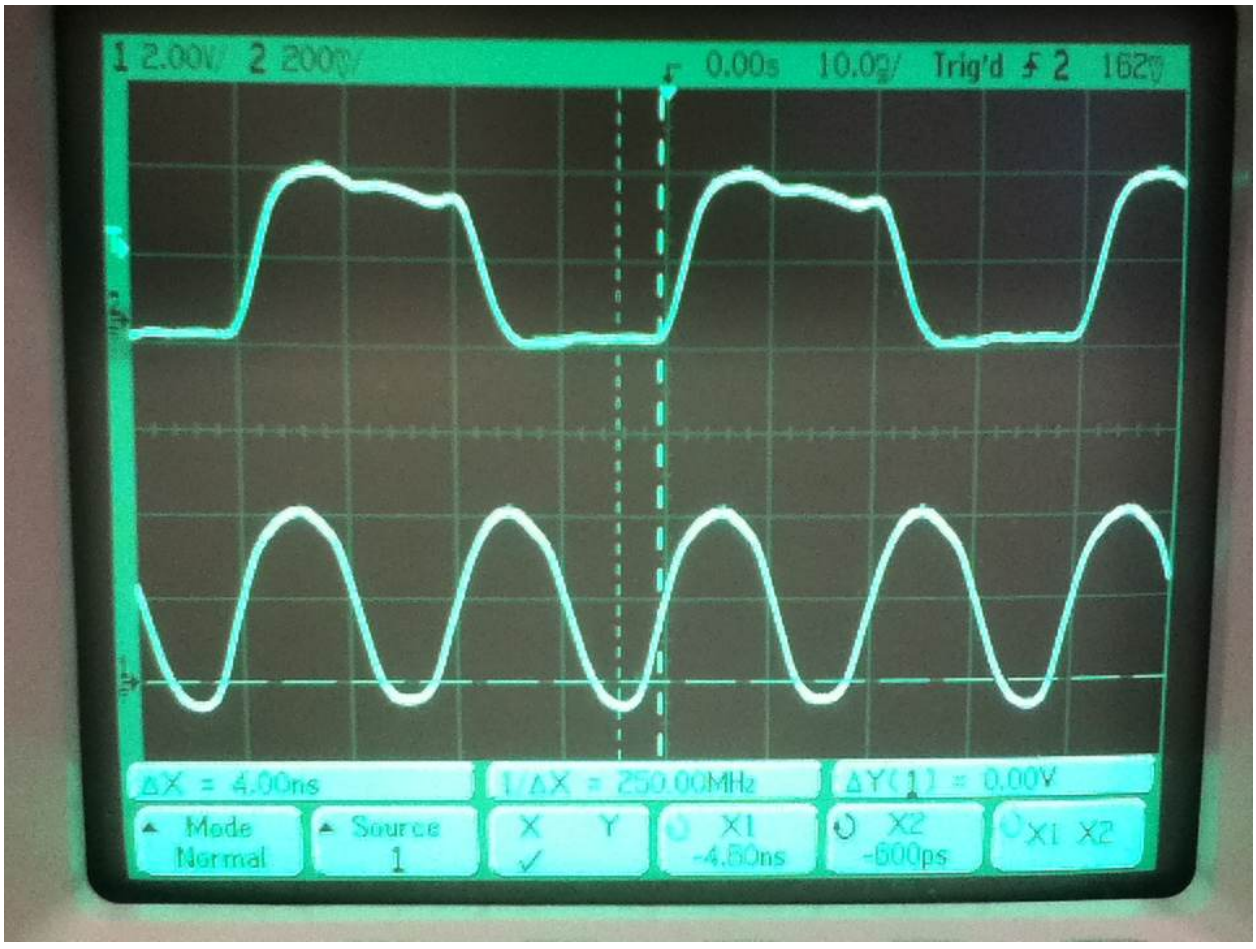
Lab 6 – Oscilloscope/ Logic Analyzer

Toggle Circuit Verilog:

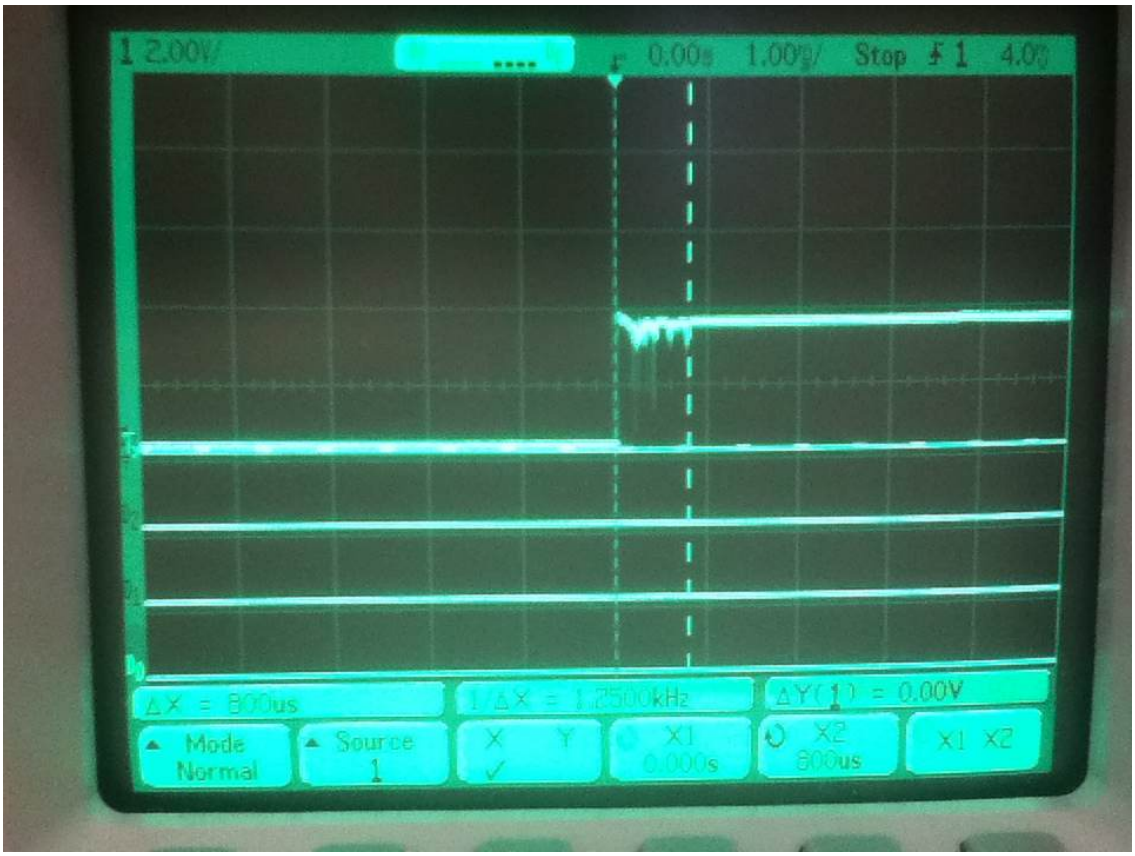
```
module Toggle(
        output Qout,
        output Clk_out,
   input GCLK,
   input CLR
   );
        wire Q_not;
        not(Q_not,Qout);
        buf(Clk_out, GCLK);
        FlipFlop FF(Qout,GCLK,CLR,Q_not);

endmodule
```

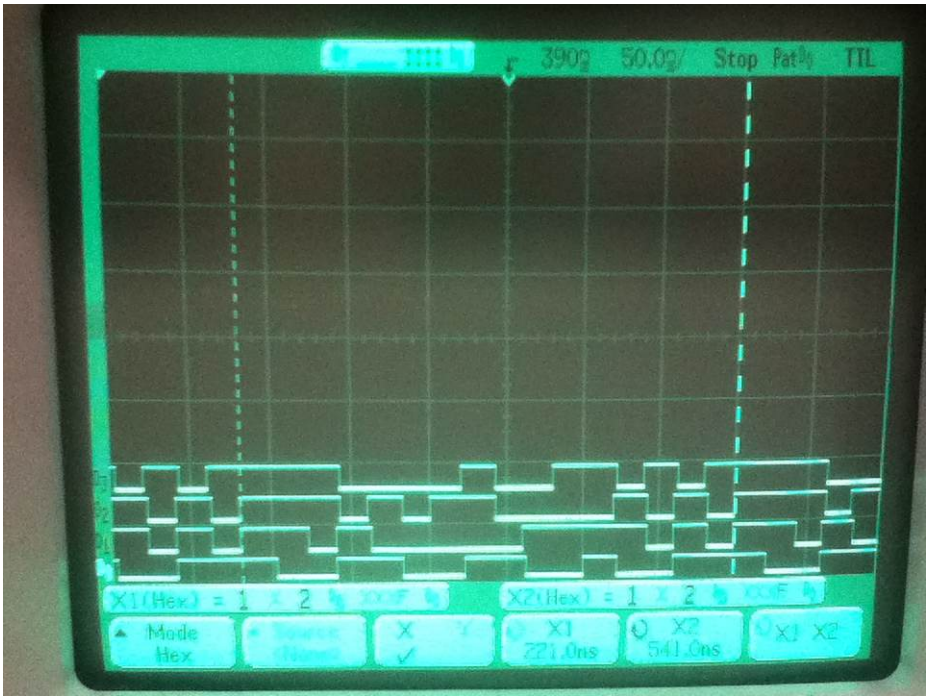
Toggle screen:



Bounce Screen:

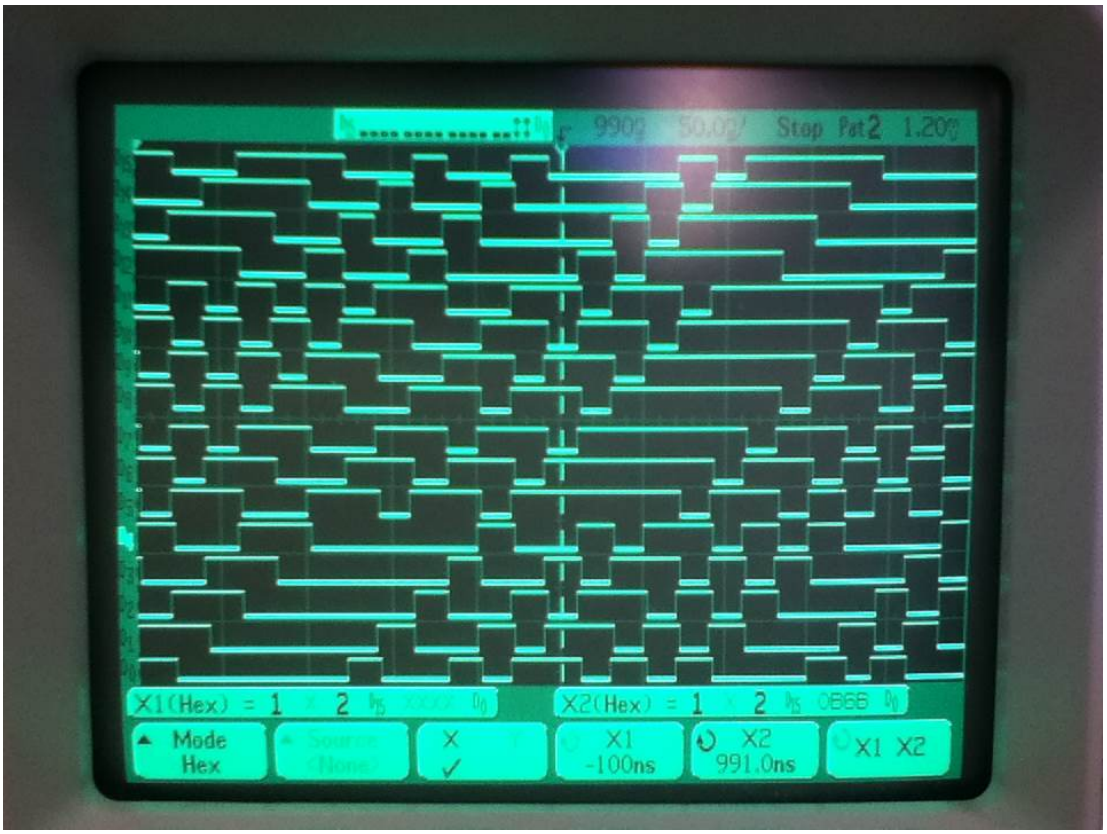


4Bit screen:



16Bit start:

16Bit 990 nS:



16Bit 16.38 micro seconds:

LAB 6 - Oscilloscope/Logic Analyzer

TY MADSEN
ECEN 220

17 OCT 2013

Clock -> Qout rising edge delay: 4.00 ns

Why not square. Signal changes are not immediate high or low, but take time to adjust from one to the other.

Bouncy signal: 800 uS (settling time)

Logic analyzer

1 g) i) Hex: F, E, C, 3, 5, 0, 4, D, 1, 2, A, 5, 6, B, 7, 9

16-bit

2) e) i)

5821
1A43
34A6
694C

f) i) @ 990 ns = [illegible]

ii) @ 16.38 uS = 42981

iii) 899 cycles

50 / 1500 ns

Anomalies: None