LAB 6 - Oscilloscope/Logic Analyzer

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Qout rising edge delay: 7.00 ns

Clk rising edge delay: 10.00 ns

Why not square: Signal changes are not immediate high or low, but take time to adjust from one to the other.

Bouncy signal - 800 us (settling time)

Logic analyzer

1 g) i) 4bit [F, E, C, 3, 5, 0, 4, D, 1, 2, A, 8, 6, B, 7, 9]

50
1000 ns

2) 16-bit

e) i)
1 D391
2 B722
3 7E45
4 FCAA
5 E975
6 C2CA
7 9595
8 3B2A
9 7674
A ECE9
B C9F3
C 83C6
D 178D
E 2F1A
F 5E15
10 BC0B
11 6837
12 D04F
13 B095
14 713E
15 E27D
16 D4FA
17 3984
18 63C8
19 C790

f) i) @ 990 ns = B313

ii) @ 16.38 us = D391

iii) 819 cycles

Anomalies: None