Ty Madsen

Ecen 220

October 17, 2013

Lab 6 – Oscilloscope/ Logic Analyzer

Toggle Circuit Verilog:

module Toggle(

output Qout,

output Clk\_out,

input GCLK,

input CLR

);

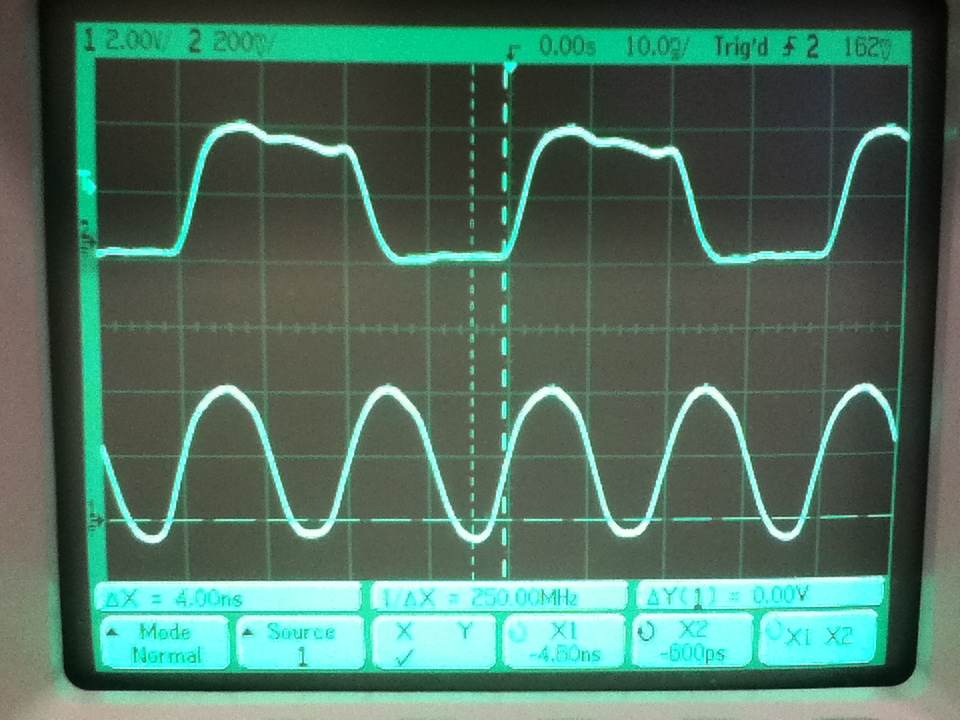
wire Q\_not;

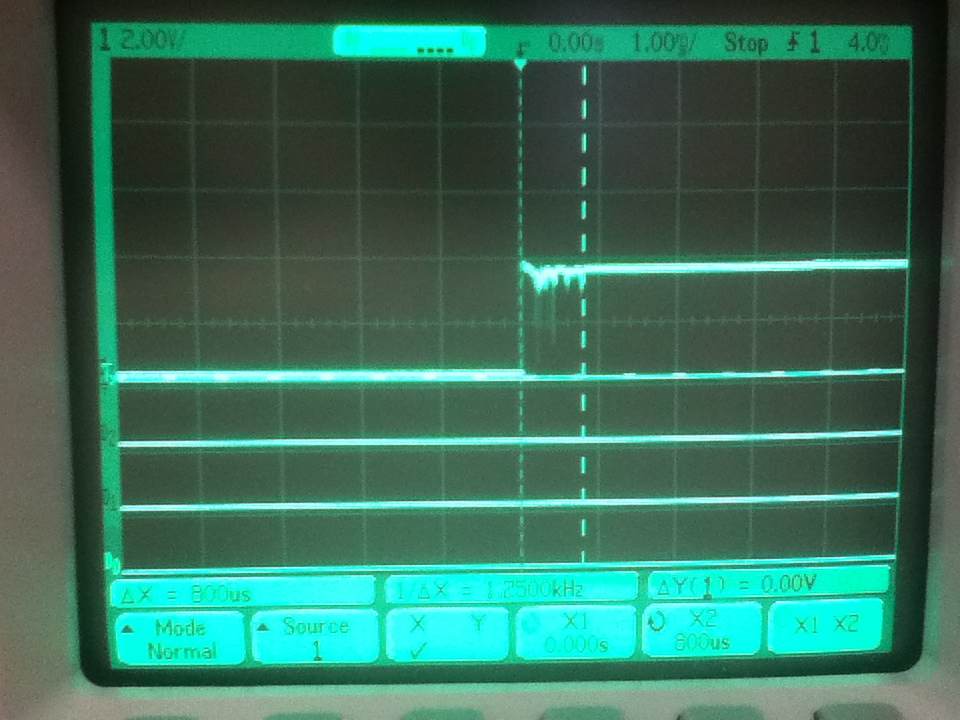
not(Q\_not,Qout);

buf(Clk\_out, GCLK);

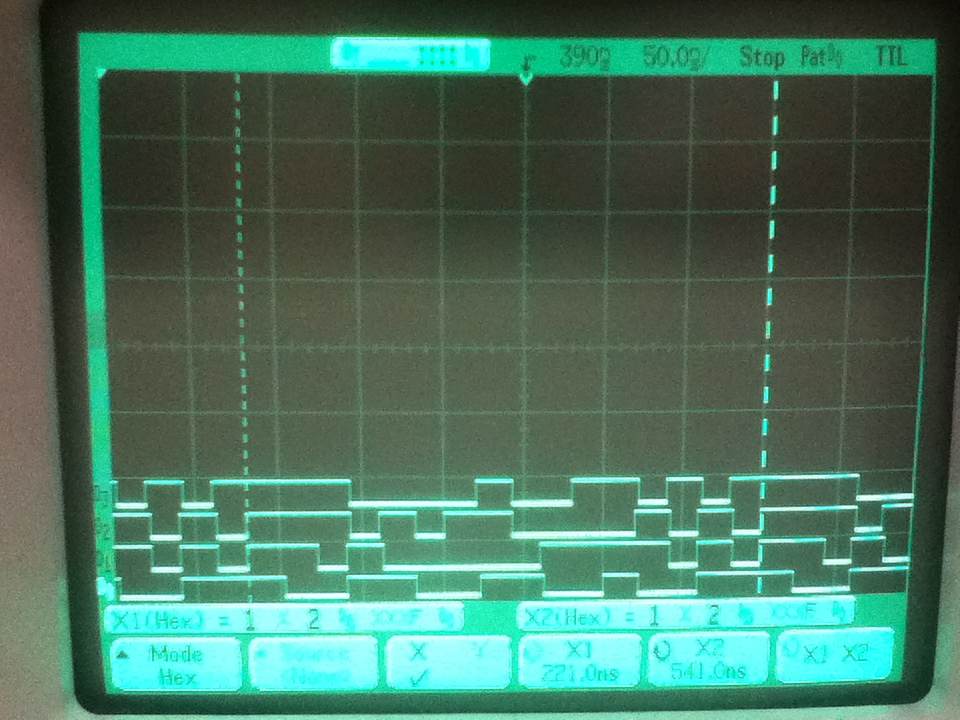
FlipFlop FF(Qout,GCLK,CLR,Q\_not);

endmodule

Toggle screen:

Bounce Screen:

4Bit screen:

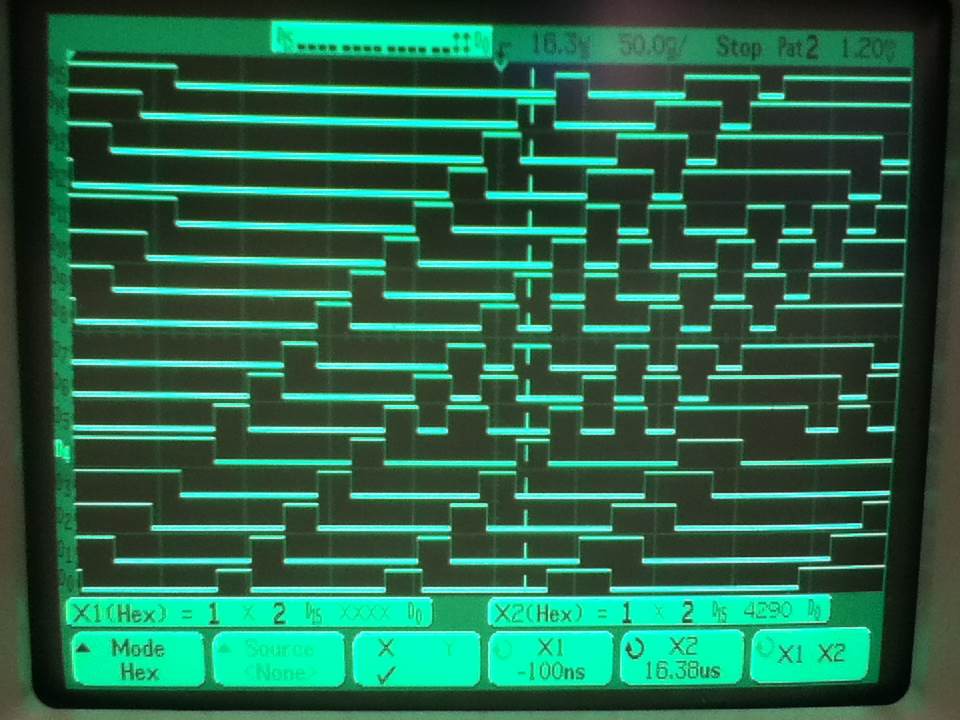


16Bit start:



16Bit 990 nS:

16Bit 16.38 micro seconds:





5821

1A43

34A6

694C