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ECEN 220

15 November 2013

Lab 9 Stopwatch/Controller

SR:

Verilog:

module SR (s, r, q, q\_n);

input s, r;

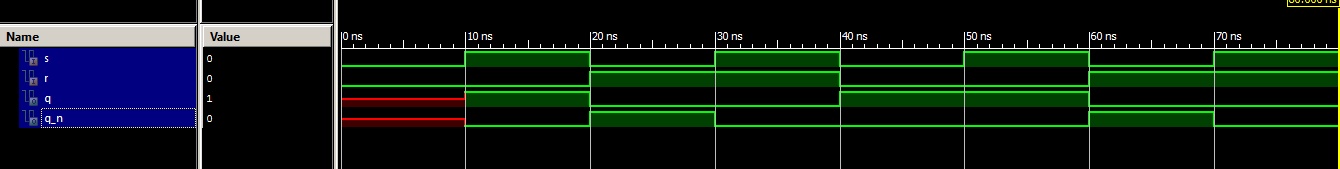
output q, q\_n;

assign q\_n = ~(s | q);

assign q = ~(r | q\_n);

endmodule

Simulation:



TCL:

wave add / -radix hex

isim force add s 0 -time 0 -value 1 -time 10ns -repeat 20ns

isim force add r 0 -time 0 -value 1 -time 20ns -repeat 40ns

run 80 ns



Load Count = 50,000,000/10 = 5,000,000

MOD6:

Verilog:

module MOD6(

input INC,

input Reset,

input CLK,

output Q2,

output Q1,

output Q0,

output ce

);

wire D0,D1,D2,tempce;

assign D2 = ~Reset & (INC & ((Q2 & ~Q0)|(Q1 & Q0)));

assign D1 = ~Reset & (INC & ((~Q2 & ~Q1 & Q0)|(Q1 & ~Q0)));

assign D0 = ~Reset & (INC & ~Q0);

assign tempce = Q2 & ~Q1 & Q0;

FF\_DCE ff0(Q0, CLK, D0, Reset, INC);

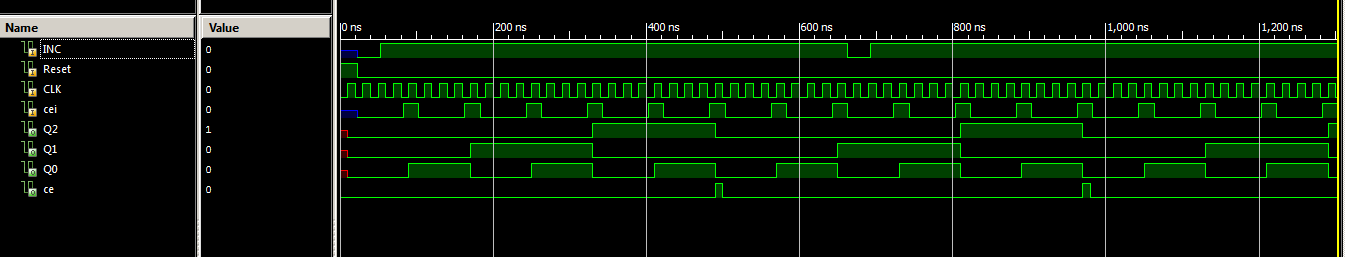
FF\_DCE ff1(Q1, CLK, D1, Reset, INC);

FF\_DCE ff2(Q2, CLK, D2, Reset, INC);

assign ce = Q2 & ~Q1 & Q0 & ~Reset & INC;

endmodule

Simulation:



TCL:

wave add / -radix hex

isim force add CLK 0 -time 0 -value 1 -time 10ns -repeat 20ns

isim force add Reset 1

run 23 ns

isim force add INC 0 -time 0 -value 1 -time 30ns -repeat 640ns

isim force add cei 0 -time 0 -value 1 -time 60ns -value 0 -time 80ns -repeat 80ns

isim force add Reset 0

run 1280ns

MOD10:

Verilog:

module MOD10(

input INC,

input Reset,

input CLK,

output Q3,

output Q2,

output Q1,

output Q0,

output ce

);

wire D0,D1,D2,D3,tempce;

assign D3 = ~Reset & (INC & ((Q2 & Q1 & Q0)|(Q3 & ~Q0)));

assign D2 = ~Reset & (INC & ((~Q2 & Q1 & Q0)|(Q2 & ~Q1)|(Q2 & ~Q0)));

assign D1 = ~Reset & (INC & ((~Q3 & ~Q1 & Q0)|(Q1 & ~Q0)));

assign D0 = ~Reset & (INC & ~Q0);

FF\_DCE ff0(Q0, CLK, D0, Reset, INC);

FF\_DCE ff1(Q1, CLK, D1, Reset, INC);

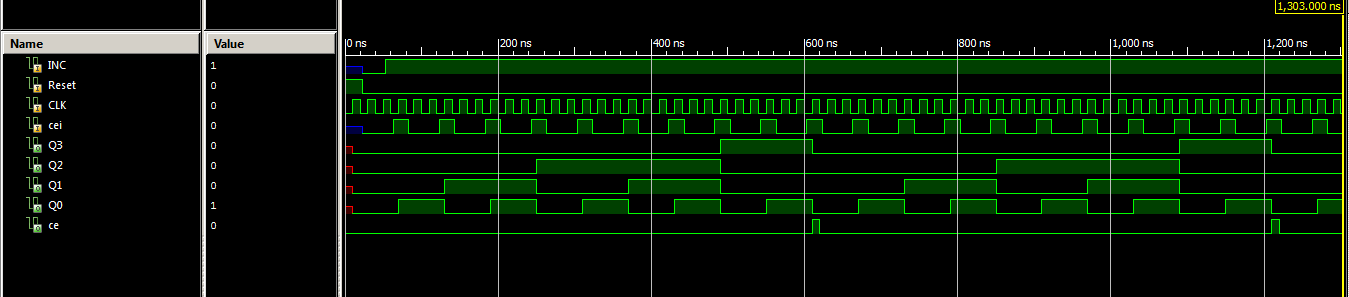
FF\_DCE ff2(Q2, CLK, D2, Reset, INC);

FF\_DCE ff3(Q3, CLK, D3, Reset, INC);

assign ce = Q3 & ~Q2 & ~Q1 & Q0 & ~Reset & INC;

endmodule

Simulation::



TCL:

wave add / -radix hex

isim force add CLK 0 -time 0 -value 1 -time 10ns -repeat 20ns

isim force add Reset 1

run 23 ns

isim force add INC 0 -time 0 -value 1 -time 30ns

isim force add cei 0 -time 0 -value 1 -time 40ns -value 0 -time 60ns -repeat 60ns

isim force add Reset 0

run 1280ns

Counter Block:

Verilog:

module CounterBlock(

input INC,

input Reset,

input CLK,

output [3:0] Q3,

output [3:0] Q2,

output [3:0] Q1,

output [3:0] Q0,

output ce

);

wire ce1, ce2, ce3;

MOD10 mod1(INC, Reset, CLK, Q3[3], Q3[2], Q3[1], Q3[0], ce1);

MOD10 mod2(ce1, Reset, CLK, Q2[3], Q2[2], Q2[1], Q2[0], ce2);

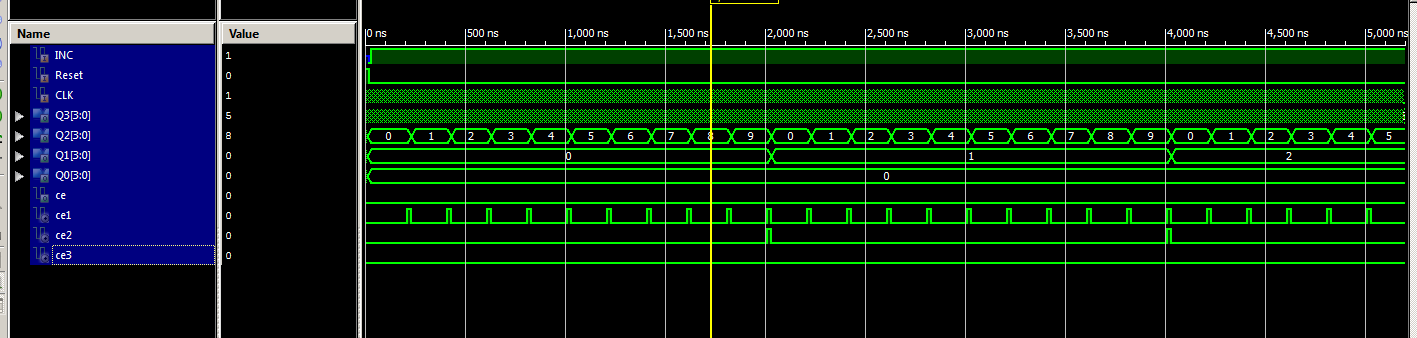
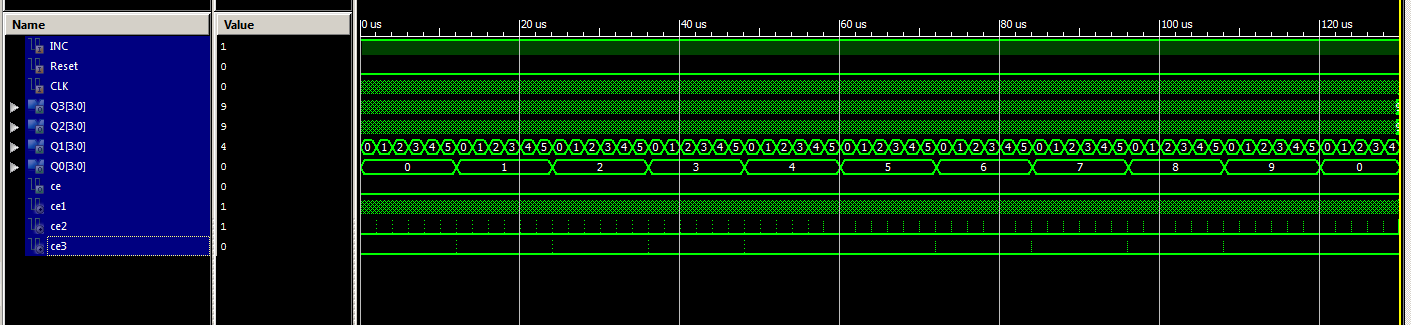
MOD6 mod3(ce2, Reset, CLK, Q1[2], Q1[1], Q1[0], ce3);

assign Q1[3] = 1'b0;

MOD10 mod4(ce3, Reset, CLK, Q0[3], Q0[2], Q0[1], Q0[0], ce);

endmodule

Simulation:



TCL:

wave add / -radix hex

isim force add CLK 0 -time 0 -value 1 -time 10ns -repeat 20ns

isim force add Reset 1

run 23 ns

isim force add INC 0 -time 0 -value 1 -time 10ns

isim force add Reset 0

run 130000ns

Programmable Timer:

Verilog:

module timertest(clk, reset, zero, tp);

input clk, reset;

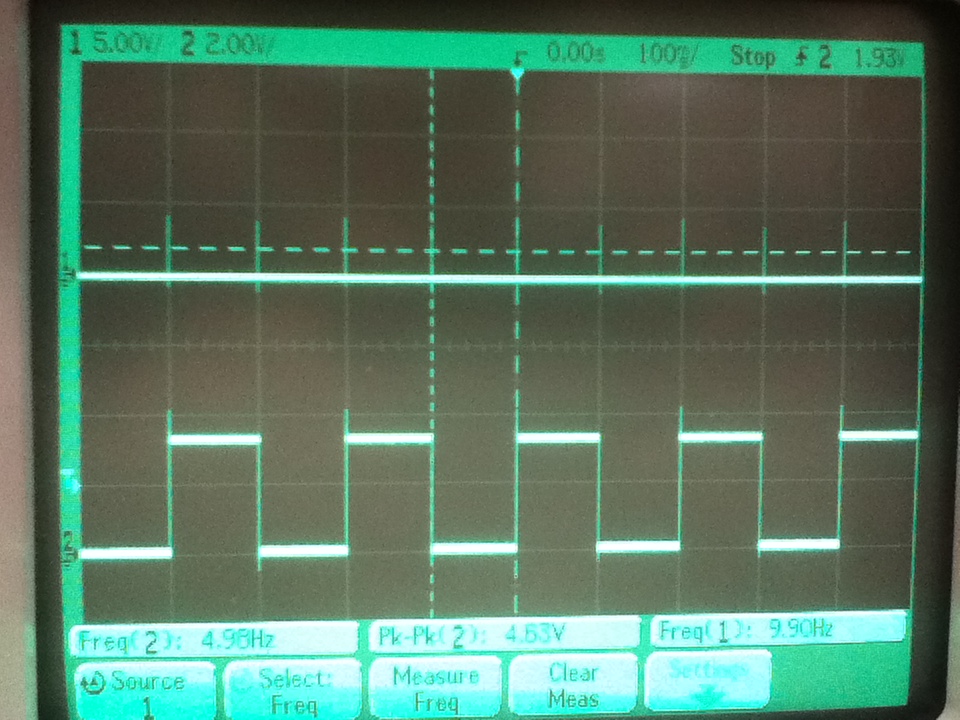
output zero, tp;

wire [23:0] counter;

prog\_timer timer(clk, reset, 1'b1, 24'd5000000, counter, zero, tp);

endmodule

Waveform:



UCF:

NET clk LOC = "B8"; # GCLK

NET reset LOC = "H13"; #BTN3

NET zero LOC = "B4"; # IO0

NET tp LOC = "A4"; # IO1

Stopwatch:

Verilog:

module Stopwatch(start, stop, Reset, CLK, Ca,

Cb, Cc, Cd ,Ce ,Cf ,Cg,

AN3, AN2, AN1, AN0,

DP, tp, tp2, zero, zero2);

input start, stop, Reset, CLK;

output Ca, Cb, Cc, Cd, Ce, Cf, Cg;

output AN3, AN2, AN1, AN0, DP, tp, tp2, zero, zero2;

wire [23:0] counter;

wire ce, q, nq;

wire [3:0] num1, num2, num3, num4;

wire [1:0] mod;

SR sr(start, stop, q, nq);

prog\_timer timer(CLK, Reset, q, 24'd5000000, counter, zero, tp);

CounterBlock cb(zero, Reset, CLK, num4, num3, num2, num1, ce);

segController47 ctrl(num1, num2, num3, num4, CLK, 1'b0, 1'b1,

1'b0, 1'b1, 1'b0, Ca, Cb, Cc, Cd, Ce,

Cf, Cg, AN0, AN1, AN2, AN3, DP, mod, zero2, tp2);

endmodule

UCF:

NET zero LOC = "B4"; # IO0

NET tp LOC = "A4"; # IO1

NET zero2 LOC = "C3"; # IO2

NET tp2 LOC = "C4"; # IO3

## clock pin for Nexys 2 Board

NET CLK LOC = "B8"; # Bank = 0, Pin name = IP\_L13P\_0/GCLK8, Type = GCLK, Sch name = GCLK0

## Buttons

NET start LOC = "B18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN0

NET stop LOC = "D18"; # Bank = 1, Pin name = IP/VREF\_1, Type = VREF, Sch name = BTN1

#NET "btn<2>" LOC = "E18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN2

NET Reset LOC = "H13"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN3

## 7 segment display

NET Ca LOC = "L18"; # Bank = 1, Pin name = IO\_L10P\_1, Type = I/O, Sch name = CA

NET Cb LOC = "F18"; # Bank = 1, Pin name = IO\_L19P\_1, Type = I/O, Sch name = CB

NET Cc LOC = "D17"; # Bank = 1, Pin name = IO\_L23P\_1/HDC, Type = DUAL, Sch name = CC

NET Cd LOC = "D16"; # Bank = 1, Pin name = IO\_L23N\_1/LDC0, Type = DUAL, Sch name = CD

NET Ce LOC = "G14"; # Bank = 1, Pin name = IO\_L20P\_1, Type = I/O, Sch name = CE

NET Cf LOC = "J17"; # Bank = 1, Pin name = IO\_L13P\_1/A6/RHCLK4/IRDY1, Type = RHCLK/DUAL, Sch name = CF

NET Cg LOC = "H14"; # Bank = 1, Pin name = IO\_L17P\_1, Type = I/O, Sch name = CG

NET DP LOC = "C17"; # Bank = 1, Pin name = IO\_L24N\_1/LDC2, Type = DUAL, Sch name = DP

NET AN0 LOC = "F17"; # Bank = 1, Pin name = IO\_L19N\_1, Type = I/O, Sch name = AN0

NET AN1 LOC = "H17"; # Bank = 1, Pin name = IO\_L16N\_1/A0, Type = DUAL, Sch name = AN1

NET AN2 LOC = "C18"; # Bank = 1, Pin name = IO\_L24P\_1/LDC1, Type = DUAL, Sch name = AN2

NET AN3 LOC = "F15"; # Bank = 1, Pin name = IO\_L21P\_1, Type = I/O, Sch name = AN3

ANOMALIES: NONE