

Smart Products Lab 5

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February 28, 2019

Section 1.

a) Algorithm

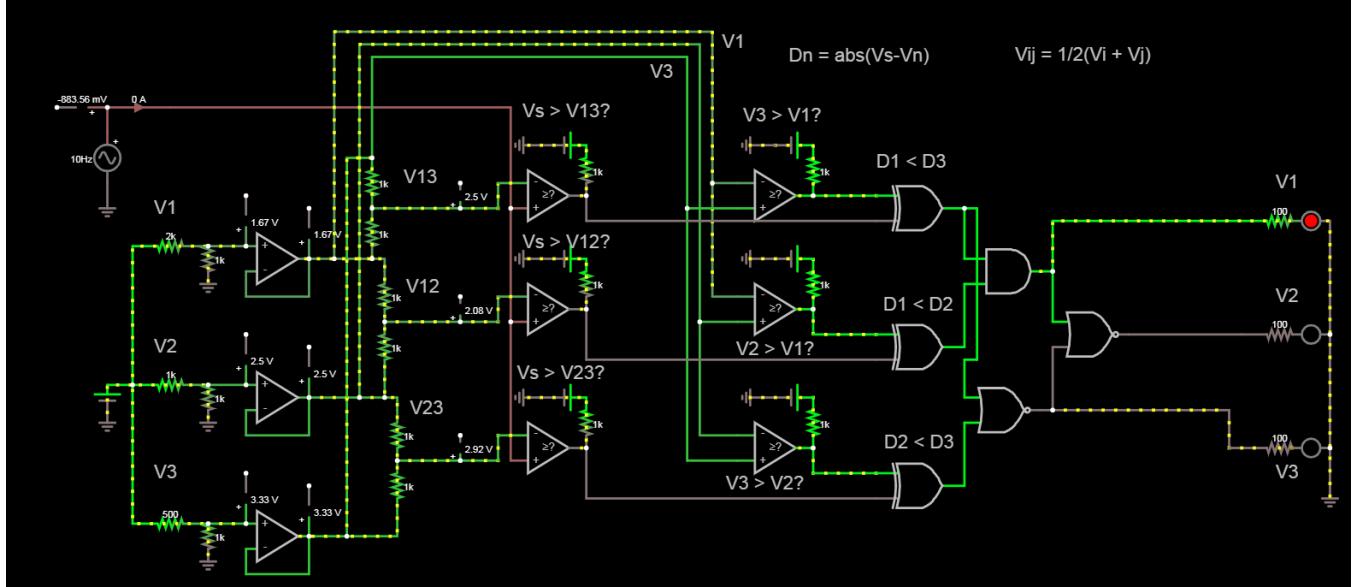


Figure 1: Schematic of circuit.

The op-amps at the start of our circuit isolate the supplied voltages for comparison from the rest of the circuit by providing a constant reference voltage. These are so-called “voltage buffer amplifiers.” The next step in our algorithm is voltage averaging which is accomplished simply by connecting two nodes of the reference voltage together with equal resistance. To understand this method consider the following equation for the averaging of V_1 and V_2 :

$$\frac{V_1 - V_{12}}{R} + \frac{V_2 - V_{12}}{R} = i^- \quad (1)$$

Where V_{12} is the average of V_1 and V_2 , R is the resistance between them, and i^- is the current into the negative input of the comparator. However, because this current must be approximately zero because the impedance of the ideal comparator is infinite,

$$V_1 - V_{12} = V_{12} - V_2 \quad (2)$$

and

$$2V_{12} = V_1 + V_2. \quad (3)$$

Without loss of generality, the same argument applies to the averages of each pair of reference voltages, and the average of each voltage can be obtained without the use of summing amplifiers.

The motivation for obtaining the averages of the reference voltages comes from converting the “nearest voltage problem” to its dual the “which voltage zone” problem. This is like converting a Delaunay triangulation to its corresponding Voroni diagram.

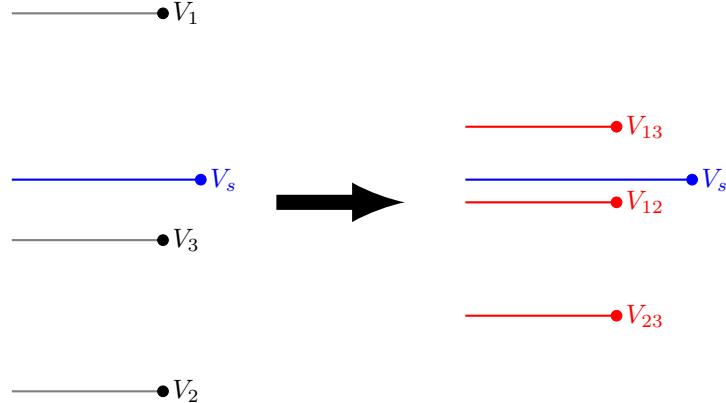


Figure 2: Converting the “nearest voltage problem” to its dual the “which voltage zone” problem.

Converting the problem in this manner allows us to avoid analog differencing operations to determine the distances between V_s and the reference voltages. Instead, we simply need to know the order of the magnitudes of the reference voltages. This can be determined with comparators. Finally, we can easily determine which set of averages V_s is between using comparators. For example, if $V_s > V_{12}$ and $V_{13} > V_s$, it is clear that V_s is somewhere between V_{13} and V_{12} . This allows us to convert the analog problem to a digital problem as soon as possible which limits the amount we had to mess around with analog components. We really liked this aspect of the approach.

Our six comparator outputs are simplified by a digital logic step. The following table demonstrates that by comparing V_s with the average voltage, and XORing it with the comparison between the two voltage levels, we can determine which difference is larger, where the difference is $D_i = |(V_s - V_i)|$.

Table 1: The XOR logic comparing average voltage to the source, and the two voltages together

$V_s > V_{ij}$	$V_i > V_j$	$D_i > D_j$
T	T	F
T	F	T
F	T	T
F	F	F

Now that we have determined $D_i > D_j$ for each combination of reference voltages, we now only need to use a truth table to devise the remaining digital logic.

b) Truth tables

Table 2: The logic of every possible permutation of the order of differences. V_i indicates that LED i should be lit.

$D_3 > D_1$	$D_2 > D_1$	$D_3 > D_2$	Inequalities	Smallest	V_1	V_2	V_3
T	T	T	$D_3 > D_1, D_2 > D_1, D_3 > D_2 \Rightarrow D_3 > D_2 > D_1$	D_1	T	F	F
T	T	F	$D_3 > D_1, D_2 > D_1, D_2 > D_3 \Rightarrow D_2 > D_3 > D_1$	D_1	T	F	F
T	F	T	$D_3 > D_1, D_1 > D_2, D_3 > D_2 \Rightarrow D_3 > D_1 > D_2$	D_2	F	T	F
T	F	F	$D_3 > D_1, D_1 > D_2, D_2 > D_3 \Rightarrow \Leftrightarrow$				False premise
F	T	T	$D_1 > D_3, D_2 > D_1, D_3 > D_2 \Rightarrow \Leftrightarrow$				False premise
F	T	F	$D_1 > D_3, D_2 > D_1, D_2 > D_3 \Rightarrow D_2 > D_1 > D_3$	D_3	F	F	T
F	F	T	$D_1 > D_3, D_1 > D_2, D_3 > D_2 \Rightarrow D_1 > D_3 > D_2$	D_2	F	T	F
F	F	F	$D_1 > D_3, D_1 > D_2, D_2 > D_3 \Rightarrow D_1 > D_2 > D_3$	D_3	F	F	T

Table 3: Logic steps for valid possibilities with $(D_i > D_j) \Leftrightarrow D_{ij}$

D_{31}	D_{21}	D_{32}	$A = D_{31} \wedge D_{21}$	$B = \neg(D_{32} \vee D_{31})$	$V_1 = A$	$V_2 = \neg(A \vee B)$	$V_3 = B$
T	T	T	T	F	T	F	F
T	T	F	T	F	T	F	F
T	F	T	F	F	F	T	F
F	T	F	F	T	F	F	T
F	F	T	F	F	F	T	F
F	F	F	F	T	F	F	T

These tables demonstrate that the NOR and AND logic chips can be used to get the correct output for the circuit from the XOR chip outputs.

c) Components

- 2 Comparator Chips – One for comparisons to V_s one for reference voltage comparison.
- 1 Op-Amp Chip – For buffer amplifiers
- 1 XOR Chip – For $D_i > D_j$ logic
- 1 AND Chip – For final digital logic steps
- 1 NOR Chip – For final digital logic steps

d) Other methodology

The previous sections have more or less completely described our methodology. Averaging was the very first concept that we started with when we thought the reference voltages would be given in order. In order to accommodate arbitrary order, we added logic to the front to switch the references between positions in the original averaging circuit before using logic again at the end. In this approach, we basically found a way to collapse those two sections of logic into one and avoid switches.

e) Incremental testing

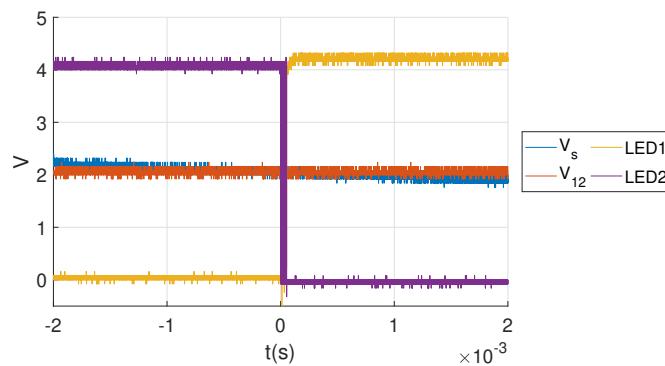
Most of our testing was done in the circuit simulator. In the simulator, we first confirmed we understood the op-amp functionality, the comparator functionality etc. Then, after we had our final design, we assembled the circuit, tested the logic portion manually to confirm it worked and then tested it all together. Some issues with bad connections had to be detected with the multimeter.

f) Future attempts

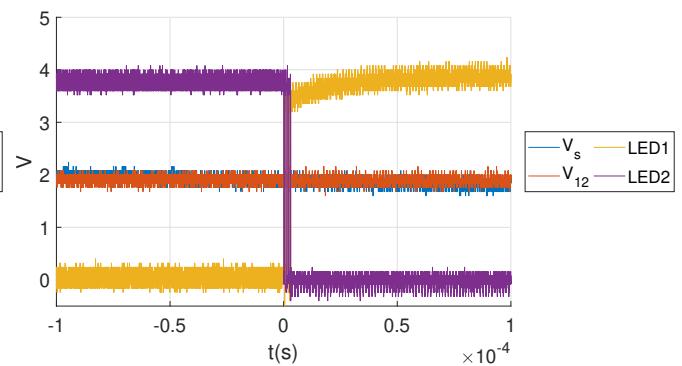
To be honest, I'm not quite sure how we could reduce the component count. There may be a way, but I can't think of anything.

Section 2.

a) Oscilloscope output during testing



(a) Transition from V_2 to V_1 at 5 Hz.

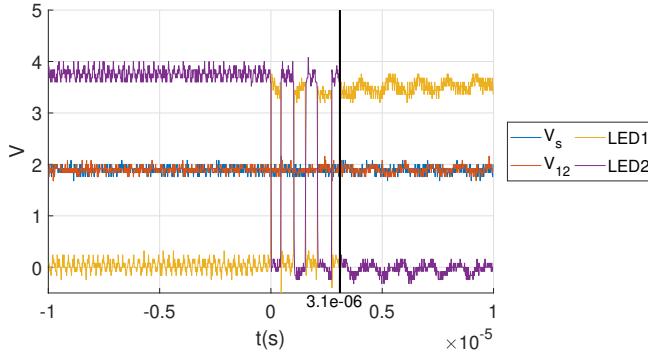


(b) Transition from V_2 to V_1 at 50 Hz.

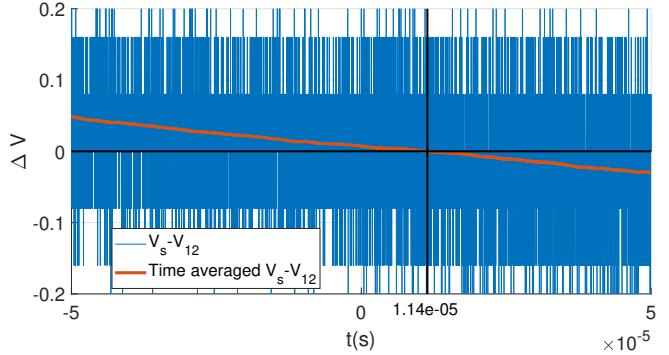
Figure 3: Circuit output with a sine wave V_s falling from V_2 to V_1 .

b) Exercise measurements and graphics

1) Time to switch indicator lines



(a) Transition from V_2 to V_1 at 50 Hz.



(b) Transition from V_2 to V_1 at 50 Hz.

Figure 4: Circuit output with a sine wave V_s falling from V_2 to V_1 .

The above figures show the time at which LED1 finally stays high and the time at which V_s crosses the V_{12} average. These times are actually in the wrong order meaning that the noise in the difference between the voltage levels is too much for us to measure an accurate crossing time to measure the lag. For all intents and purposes it seems instantaneous. However, in hindsight, we should increase the source frequency to narrow the window of time of crossing and better determine the delay time. In this case, all we know is that it is less than 3 μ s.

2) Minimum frequency for simultaneous illumination

While increasing the frequency, at around 14 Hz it was hard to tell whether the LEDs were blinking in unison or sequentially. By around 43 Hz, all three LEDs seemed to be constantly illuminated. LED2, configured for the middle voltage seemed to go steady first and when all the LEDs were steady appeared the dimmest.

The appearance of LED2 is explained by the fact that because it is the middle voltage, for our source sine wave, it is active for a shorter period of time. All three LEDs appear to be illuminated because their blinking exceeds the rate that human eyes can detect. This is, in effect, how lots of modern light sources work.

The fact that when the voltages get near a transition point, noise in the system causes high frequency switching only increases this effect, making it seem as if two lights are illuminated at once because they are switching on and off at the noise frequency which is much higher than the source frequency.

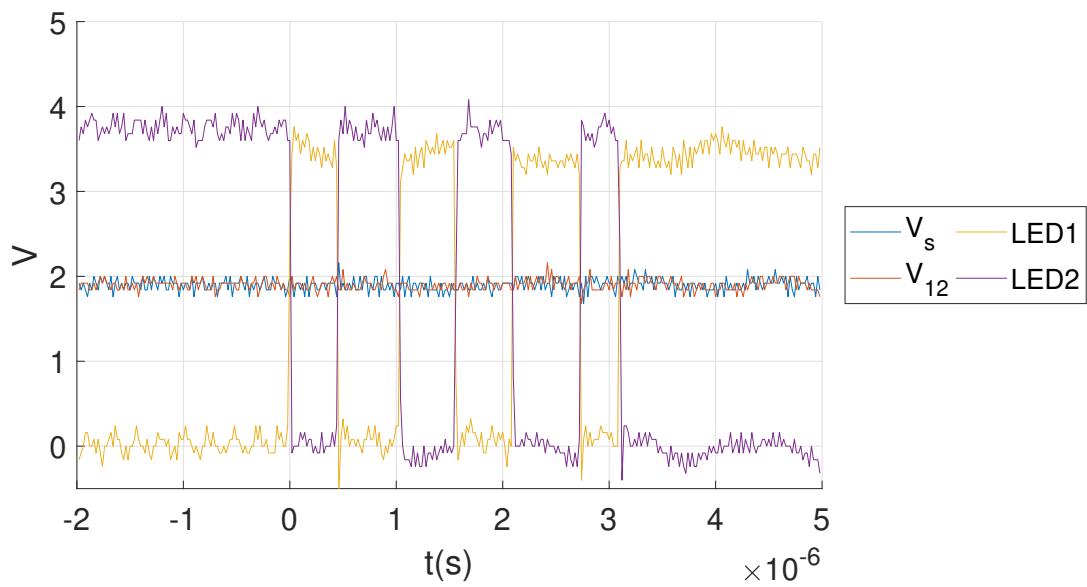


Figure 5: High frequency switching on the digital output line due to noise near the transition point.

c) Picture

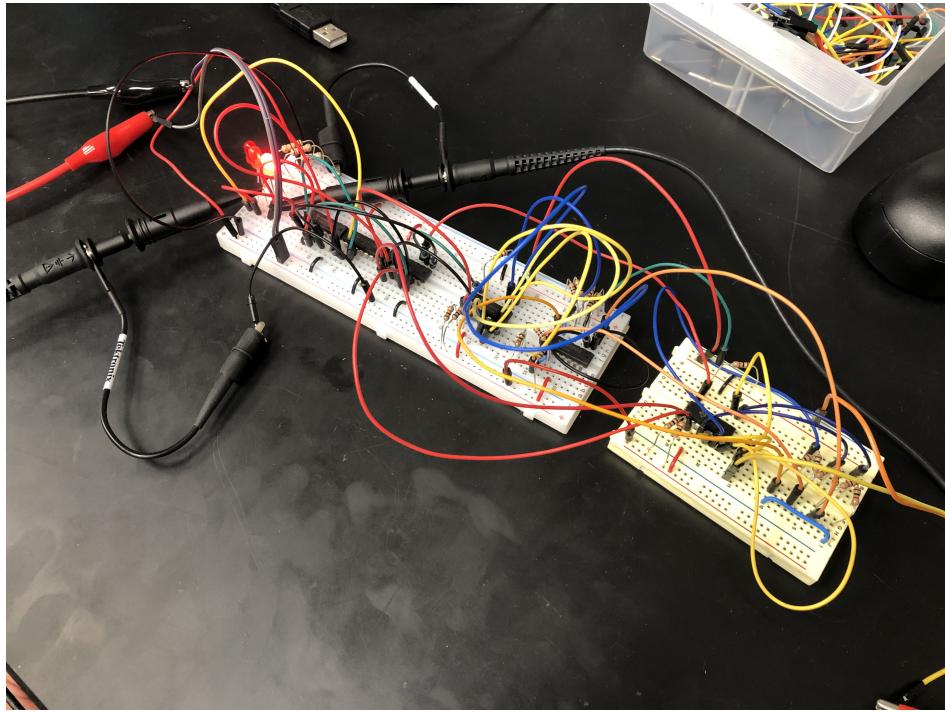


Figure 6: Photo of completed circuit.