AB1565 AB1568 EVK Layout Guide

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Document Revision History

Revision	Date	Description
1.0	29 May 2020	Initial Version. (C738/C742/C744)

Table of contents

Lists of tables and figures

1. Introduction

The AB1565/8 is an advanced single-chip solution which integrates baseband and radio for intensive stereo/mono audio applications. Here is EVK daughterboard for layout guideline example, Figure 1, Figure 2, and the layout guide separated four function:

- ·PCB Specifications
- ·RF Layout Guidelines
- ·Power/GND Layout Guidelines
- ·Audio Layout Guidelines

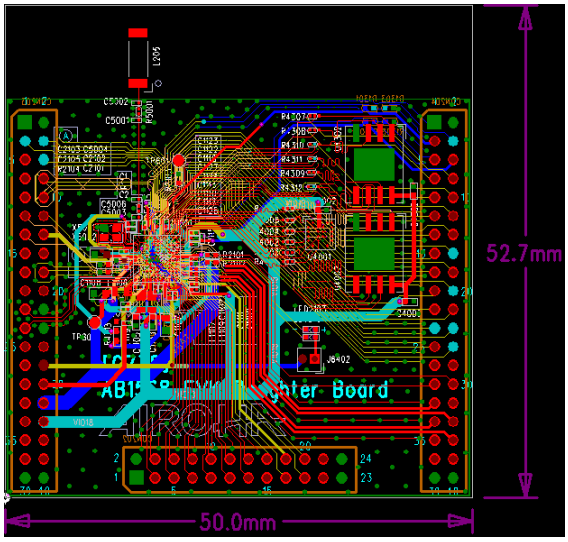

Figure 1. Top view of AB1568 EVK daughter board

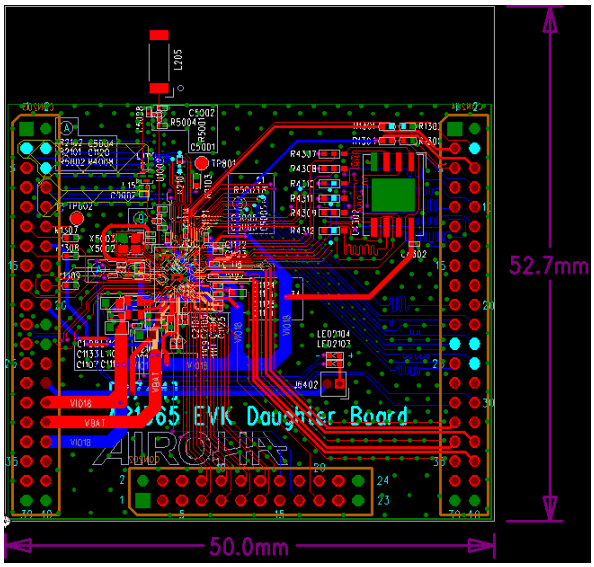

Figure 2. Top view of AB1565 EVK daughter Board

2. PCB Specifications

The AB1568 EVK daughter board has six different layers, as shown in a stack-up layout in Table 1. and the AB1565 EVK daughter board has four different layers, as shown in a stack-up layout in Table 2. Developers can changes to the stack-up layers based on requirements, and the impedance need to calculated wire wide and separation. Please refer to Table 3, Table 4.

Table 1. Stack-up table of the AB1568 EVK daughter board

Top side solder mask				0.80	mils
L1	**TOP**	**Differential and Signal**	**copper and plating**	1.20	mils
			prepreg	2.95	mils
L2			**copper**	1.20	mils
			prepreg	2.95	mils
L3			**copper**	1.25	mils
			core	40.5	mils
L4		**GND**	**copper**	1.25	mils
			prepreg	2.95	mils
L5			**copper**	1.20	mils
			prepreg	2.95	mils
L6	**Bottom**	**Differential and Signal**	**copper and plating**	1.20	mils
Bottom side solder mask				0.80	mils
TOTAL				61.20	mils
				1.55	mm

Total thickness: 1.55mm

Table 2. Stack-up table of the AB1565 EVK daughter board

Top side solder mask				0.80	mils
L1	**TOP**	**Differential and Signal**	**copper and plating**	1.40	mils
			prepreg	3.17	mils
L2		**GND**	**copper**	1.25	mils
			core	48.5	mils
L3			**copper**	1.25	mils
			prepreg	3.17	mils
L4	**Bottom**	**Differential and Signal**	**copper and plating**	1.40	mils
Bottom side solder mask				0.80	mils
TOTAL				61.74	mils
				1.57	mm

Total thickness: 1.57mm

Table 3. PCB design rules of the AB1568 EVK daughter board

Parameter	Value	Comments
Number of layers	6	HDI 2+2+2
Thickness	1.6 mm	N/A
Dielectric	Er=4.4	Er@2.45GHz
Minimum trace width	2.36 mils	Minimum track width can be reduced but the cost would be higher.
Minimum spacing	2.36 mils	Minimum spacing can be reduced but the cost would be higher.
Laser drill diameter	3.94/8.66 mils	N/A
Middle drill diameter	9.84/19.69 mils	N/A
Copper thickness	1 oz	N/A
RF Impedance	Trace wide:4.5 mil Gnd gap: 6.5 mil	50 ohm impedance Gnd reference L2/L5
USB Impedance	Trace wide:4.5 mil Trace gap:7 mil Gnd gap: 6.5 mil	90 ohm impedance Gnd reference L2/L5

Table 4. PCB design rules of the AB1565 EVK daughter board

Parameter	Value	Comments
Number of layers	4	HDI 1+2+1
Thickness	1.6 mm	N/A
Dielectric	Er=4.4	Er@2.45GHz
Minimum trace width	2.95 mils	Minimum track width can be reduced but the cost would be higher.
Minimum spacing	2.95 mils	Minimum spacing can be reduced but the cost would be higher.
Laser drill diameter	3.94/9.84 mils	N/A
Middle drill diameter	9.84/17.72 mils	N/A
Copper thickness	1 oz	N/A
RF Impedance	Trace wide:5 mil Gnd gap: 8 mil	50 ohm impedance Gnd reference L2/L3
USB Impedance	Trace wide:5 mil Trace gap:6 mil Gnd gap: 8 mil	90 ohm impedance Gnd reference L2/L3

3. RF Layout Guidelines

3.1. RF trace

It is essential to provide a correct layout for the RF section (as shown in Figure 3) for the wireless device in order to achieve optimum device performance. A poor layout can cause performance degradation for the output power, the EVM, the harmonic emission, the sensitivity, and the spectral mask. AB1565/8 has an integrated matching and filter, The PI network for RF matching could be remove, and other PI network for Antenna matching should be put close to the antenna.

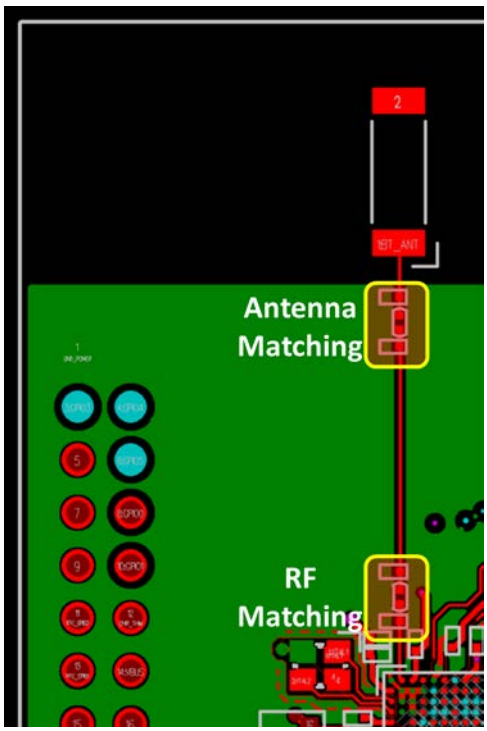

Figure 3. RF trace of the AB1568 EVK daughter board

- Make sure RF path impedance is 50 ohm
- RF trace to antenna should be the top layer and do not let it go through by vias.
- Make sure that the ground plane under the RF trace is solid and increase the vias around the RF trace.
- Add a ground trace close to the package corner-side on the same layer as the chip layer.
- Make sure the return path is solid and good, and the reference layer should be checked also. Refer Figure 4 for more information.

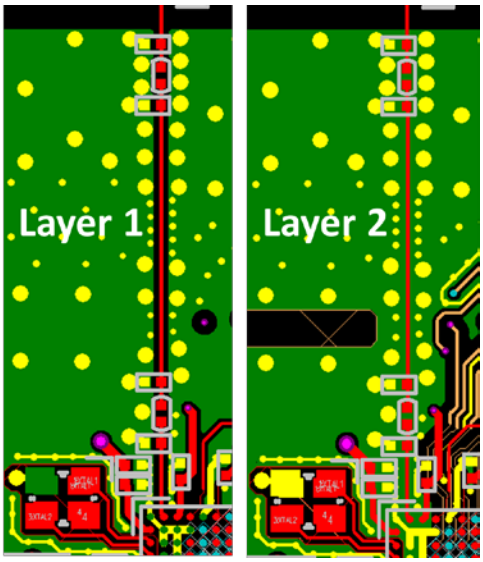

Figure 4. Gnd Via around RF trace of the AB1568 EVK daughter board

3.2. RF circuit decupling Cap

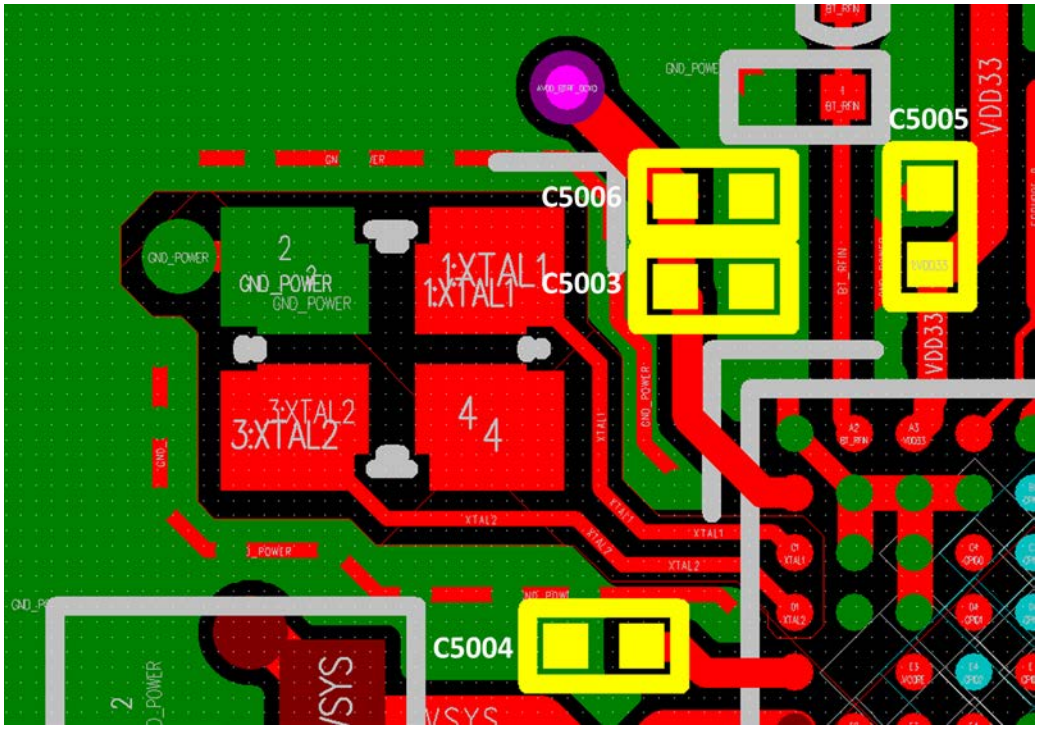

Figure 5. RF circuit decupling Cap of the AB1568 EVK daughter board

- All decoupling caps for AVDD_VBT, AVDD_BTRF, AVDD_DCXO should be at the top layer and close to the pins.
- If limited by PCB size, the C5004 cannot be put at the top layer. Please add C5003(1uF) at the top layer which is for reserved for tuning.

3.3. Crystal 26M

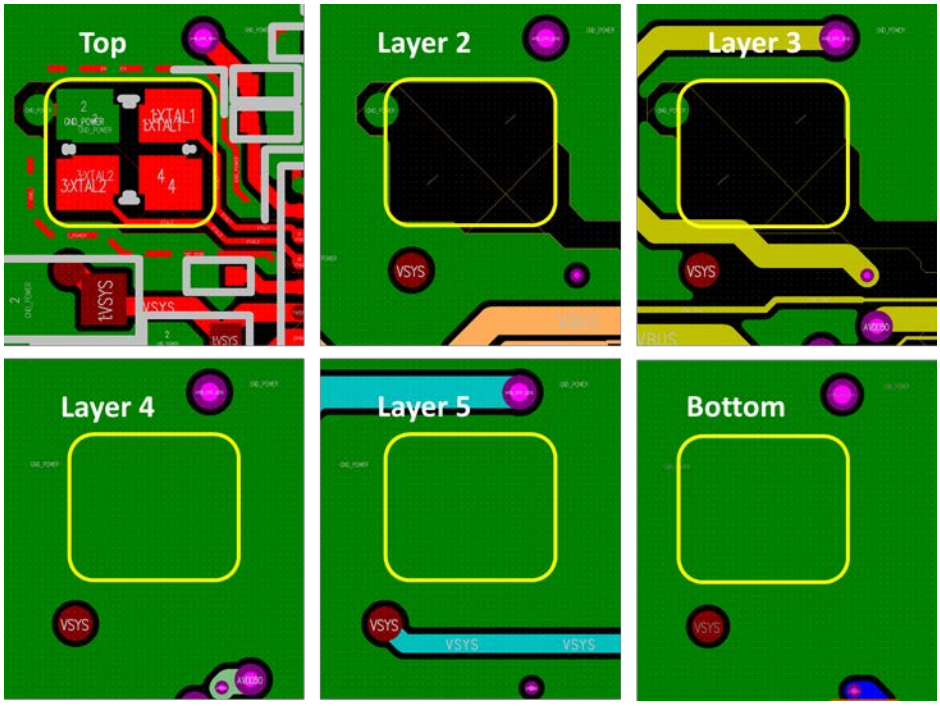

Figure 6. Crystal 26M of the AB1568 EVK daughter board

- XTAL pins must be put at the top layer if possible. If it is not possible, put them at the bottom layer with the shortest trace to crystal.
- The crystal and its trace directly refer to the global ground. Keep out L1&L2&L3 ground, please refer to Figure 6.
- XTAL ground pad directly connects to the global ground. Do not connect to GND on a different layer.
- Add more vias between the crystal and the antenna trace, please refer to Figure 7.

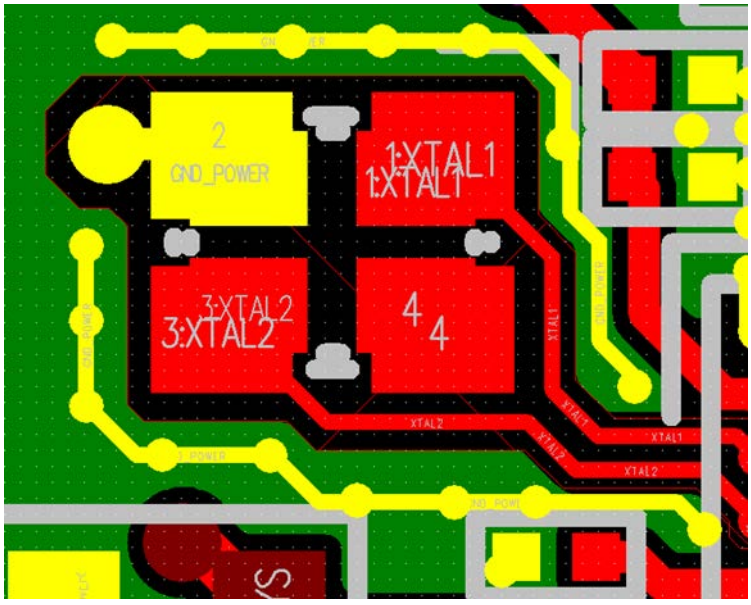

Figure 7. Crystal 26M gnd vias of the AB1568 EVK daughter board

4. Power Layout Guidelines

4.1. Power Trace

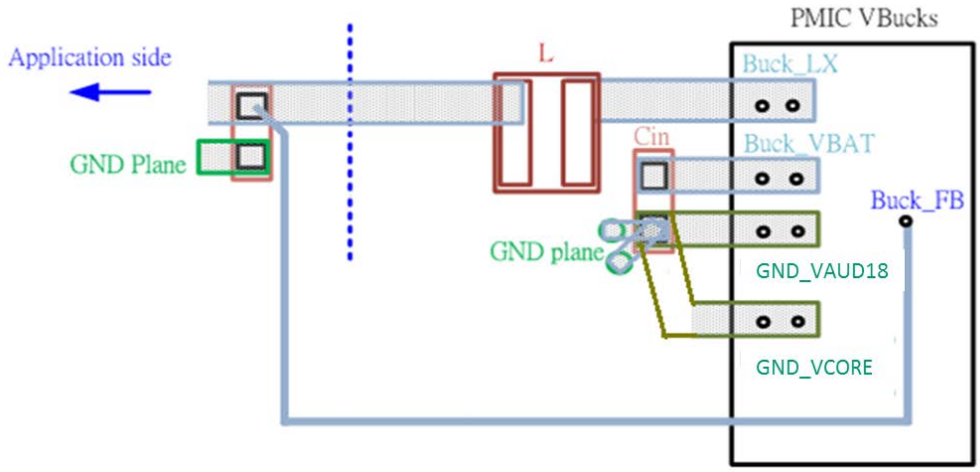

Figure 8. Buck layout guide

- Make the buck inductor trace loop as short as possible, Figure 8 L
- BUCK input cap (Cin) must as close to the VSYS_BUCK pin as possible.
- BUCK input cap GND must star connect with GND_BUCK as shown in Figure 8.
- GND_BUCK must connect directly with the input cap GND.
- BUCK_FB must be shielded with GND and there must be no noise above or below.
- The sensor point of BUCK_FB path must be located at the maximum output capacitor
- Avoid putting the inductor close to the antenna, microphone or speaker.
- The LDO output pin and the farthest cap must less than 200mΩ

4.2. Buck Trace

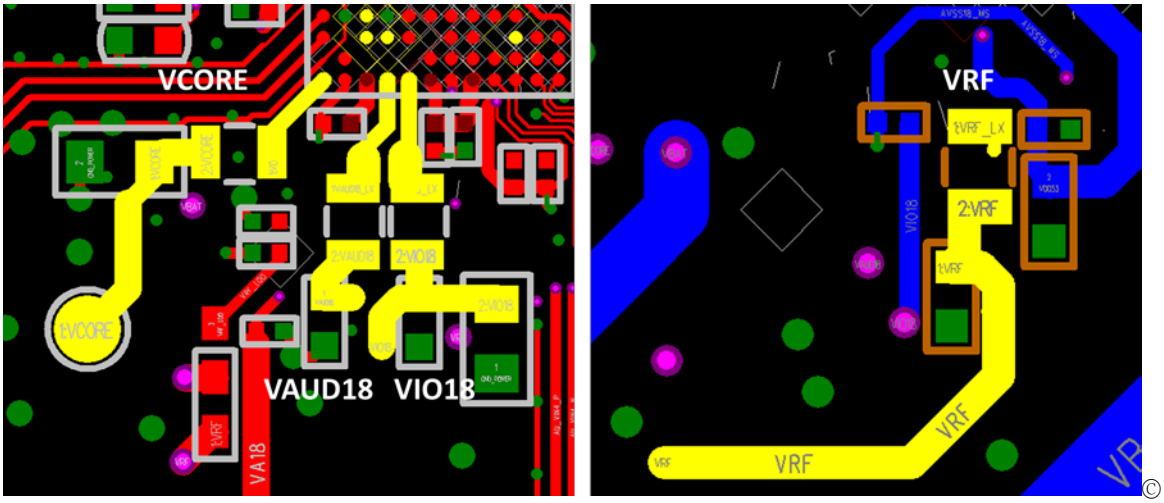

Figure 9. LX Trace of the AB1568 EVK daughter board

- The VIO, Vcore, Vaud, Vrf must be kept as wide as possible. Please refer Table 1Table 5

Table 5.BUCK trace wide of the AB1568 EVK daughter board

Parameter	Trace Width (mil)	GND shielding
VCORE_LX	12	
VCORE_FB	min width	Yes
VIO_LX	16	
VIO_FB	8	Yes
VAUD_LX	10	
VAUD_FB	min width	Yes
VRF_LX	6	
VRF_FB	6	Yes

4.3. LDO Trace

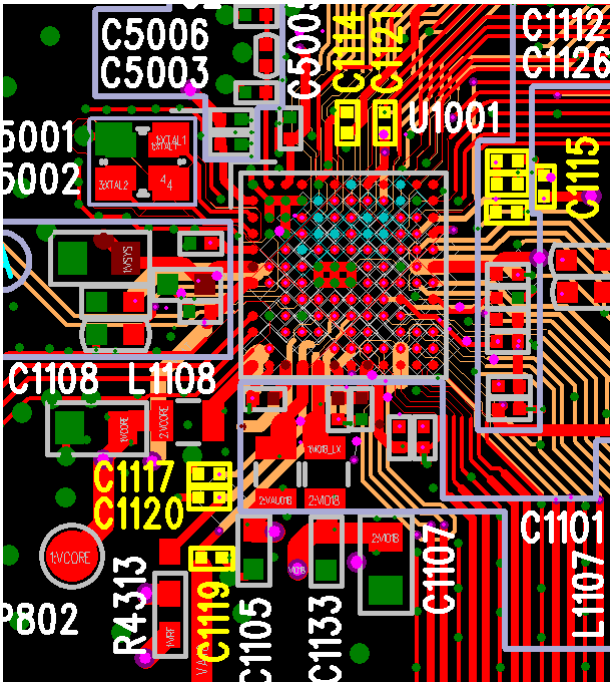

Figure 10. LDO decoupling capacitor of the AB1568 EVK daughter board

- The distance between decoupling capacitor and IC pin must be as short as possible.
- Traces must be routed to through decoupling capacitor pin before the IC pin.
- The LDO trace must be kept as wide as possible. Please refer Table 1Table 6.

Table 6.BUCK trace wide of the AB1568 EVK daughter board

Parameter	Trace Width (mil)	GND shielding
VDIG18	4	
VDD33	6	
VRF	6	
VSRAM	6	
VA18	4	Nice to have
ISINK0	6	
ISINK1	6	

4.4. Charger trace

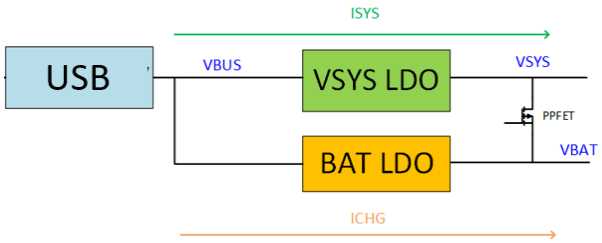

Figure 11. Charger path

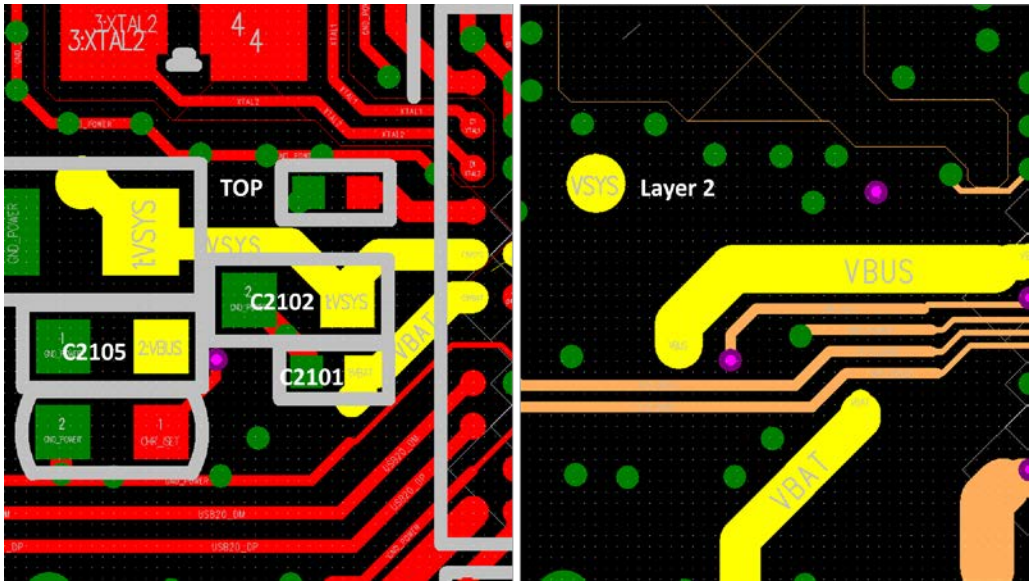

Figure 12. Charger path of the AB1568 EVK daughter board

- The charger trace must be kept as wide as possible.
- Vbus, Vbat and Vsys decoupling capacitor and IC pin must be as short as possible.
- The LDO trace must be kept as wide as possible. Please refer Table 1Table 7.

Table 7.BUCK trace wide of the AB1568 EVK daughter board

Parameter	Trace Width (mil)	GND shielding
VSYS	20	
VBAT	20	
VBUS	20	Nice to have ESD protection

5. Audio Layout Guidelines

For better audio performance and to avoid interference or path loss, you must obey the following rules:

1) The length of microphone path (AU_VIN0_P, AU_VIN0_N, AU_VIN1_P and AU_VIN1_N, AU_VIN2_P and AU_VIN2_N, AU_VIN3_P and AU_VIN3_N, AU_VIN4_P and AU_VIN4_N, AU_VIN5_P and AU_VIN5_N) and speaker path (AU_HPRP, AU_HPRN, AU_HPLP and AU_HPLN) must be as short as possible.

2) Increase the width of the speaker trace to reduce the parasitic resistance that occurs when the speaker trace is too long.

3) The microphone path and speaker path are routed with a solid ground on both sides, and the shield is formed by having the ground on the PCB layers above and below the signals. The surrounding ground planes must be firmly connected with vias to make sure there is a good connection between the ground layers and to the main ground in the PCB.

4) For Hybrid applications, the SPK and FB Mic trace must be isolated to avoid interference each other.

5.1. SPK out trace

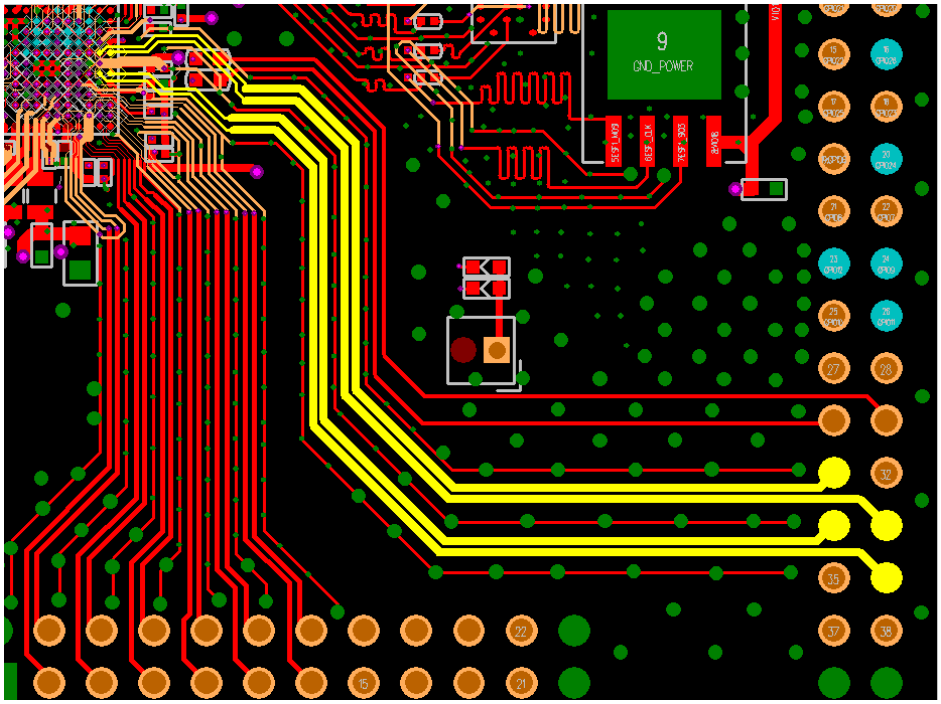

Figure 13. SPK out trace of the AB1568 EVK daughter board

- There should be as many traces for the SPK as possible and be shielded from the ground trace as much possible.
- The trace width must be at least 12 mm wide.

5.2. Mic out trace

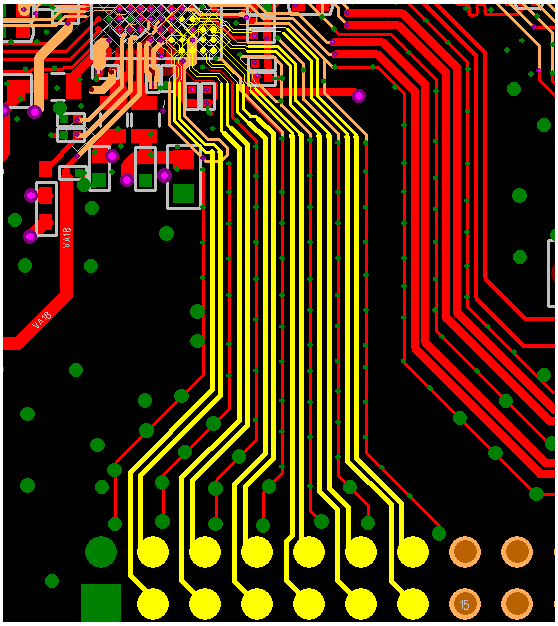

Figure 14. Mic out trace of the AB1568 EVK daughter board

- Trace of MIC should as similar as possible and shielding by ground trace as possible.

5.3. Mic_bias trace

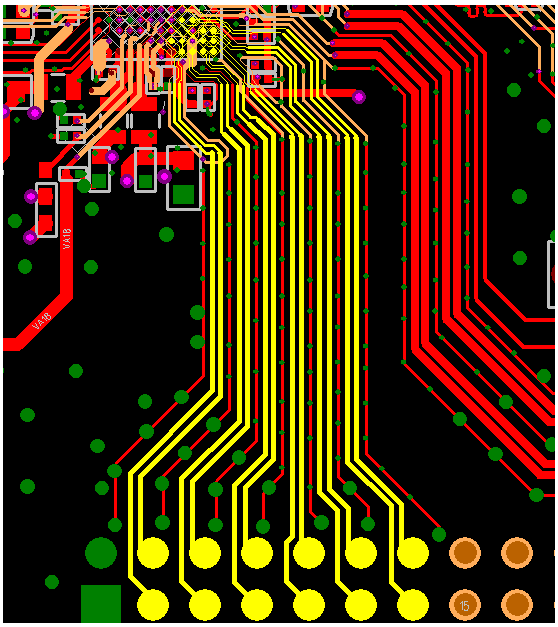

Figure 15. Mic_bias trace of the AB1568 EVK daughter board

- Trace of Mic_bias trace keep as width as possible and shielding by ground trace as possible.

5.4. Touch Pad

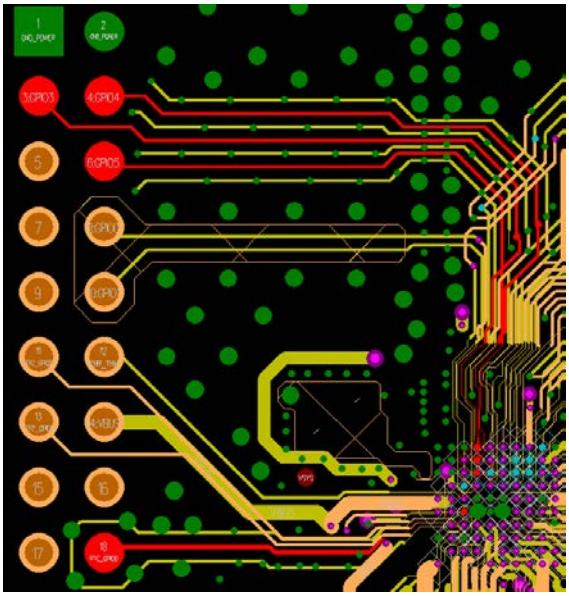

Figure 16. Touch Pad of the AB1568 EVK daughter board

- Trace/Pad of touch should shielding by ground as possible. Suggest to add GND area for shielding to surround the Touch trace. Suggest the trace is layout on bottom layer. The touch sensor is on top layer. The middle layer is suggested to be empty, no signal, and no GND layer. If there is high speed Signal cross Touch Trace, it's better to add GND layer (Grip GND is best) between Touch trace and Signals. Avoid using the via. If necessary, suggest don't let them over two.
- Width between Touch Trace: Suggest is at least two times the trace width; Larger is always better. The width from the Touch Trace to other signals (ex: I²C, SPI, Clock, Power, GND): We strongly suggest it be three times the trace width; Larger is always better. If the touch trace cannot be away from the signal line, put them in a vertical layout, not parallel. Otherwise, add a GND line between them.
- Width from Touch Trace to other signals (ex: I²C, SPI, Clock, Power, GND): We strongly suggest it be three times the trace width; Larger is always better.
- The bigger size of sensor, the more sensibility. But don't let capacitance value of Sensor with trace is over 40pF.Suggest to add GND grid for shielding to surround the Touch Sensor and to cover components. On Top & Bottom, to cover the touch area. The material overlay on the touch sensor should not be conductor or have metal inside.
- The trace from sensor pad to IC pin should be short and thin (3mil~6mil). Add a 0.1uF to Vctp as near as possible. (Power from: Vctp <-- Vrtc <-- VDIG18)
- When touch function are enabled, let the touch channels (GPIO3 / 4 / 5, RTC_GPIO0) be critical line.
- "If there are the branches on GPIO3 / 4 / 5, RTC_GPIO0, keep the branches are short to avoid increasing parasitic cap. Value.
- Total cap value on every channel should be less than 40pF (Sensors + Traces) "
- If more than 2 shared pin function on the GPIO3 / 4 / 5 and RTC_GPIO0, reserve a 0ohm as near as the touch trace for open to avoid increasing parasitic cap. value (Total cap value should be less than 40pF (Sensors + Traces)