CME 433 Lab 2 – Lab Report
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Ripple Carry Adder

Image 1: Ripple Carry Adder counts up

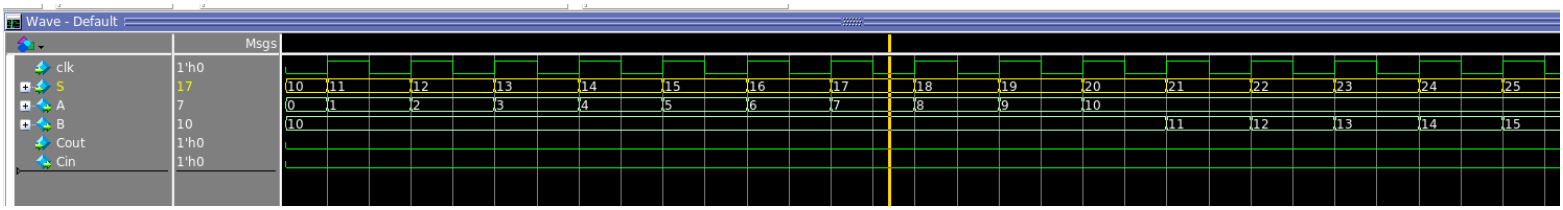
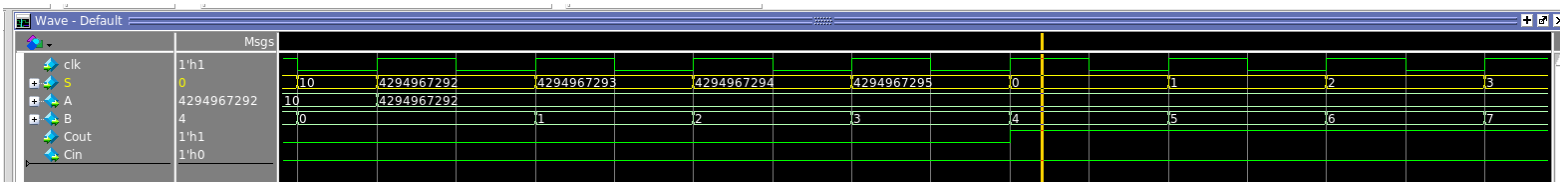


Image 2: Ripple Carry Adder overflows



The max clock frequency (at 1200mV and 85C) that Quartus determined was 120.63MHz for this design.

Carry Look-Ahead Adder

Image 1: CLA Adder counts up

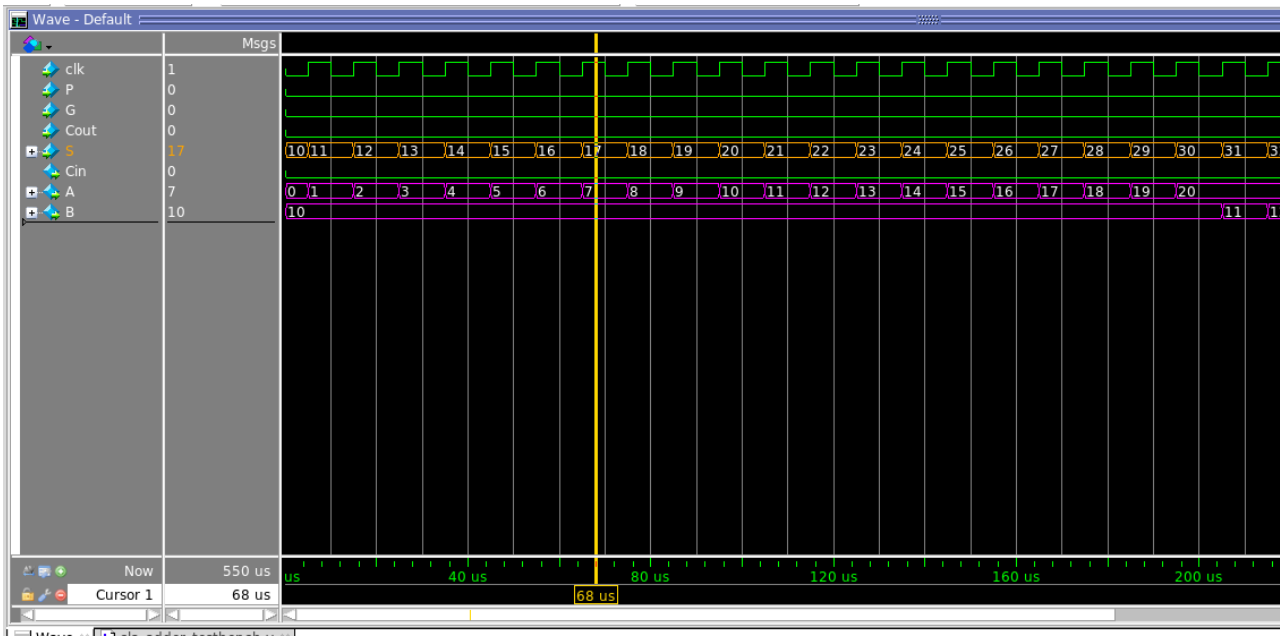
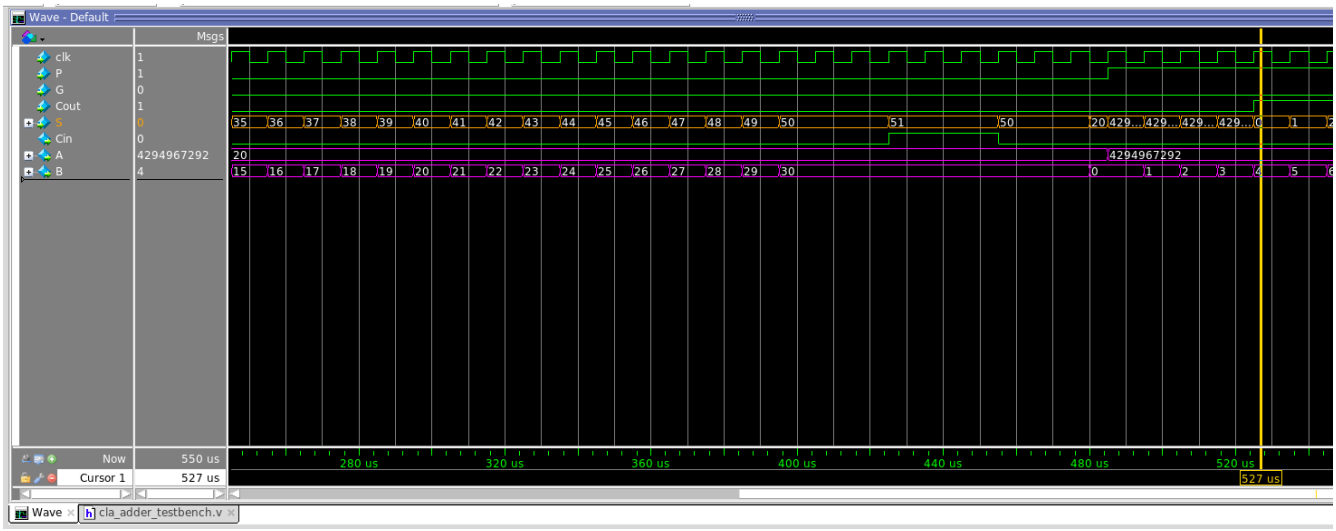


Image 2: CLA Adder overflows



The max clock frequency (at 1200mV and 85C) that Quartus determined was 62.59MHz for this design.

Obviously these results were not what was expected – the CLA adder was expected to be relatively faster, not slower than the ripple carry adder. The explanation comes from the reason the cla was expected to be faster: the improved performance is due to the large fan-out of the cla adder (with the cla logic using c[0] as the main Cin, rather than propogating it all the way through).

Unfortunately, upon inspection of the RTL viewer in Quartus, my carry look-ahead adder did not achieve these large fanout effect, meaning it did not see the performance improvements that were expected. Despite my efforts, the carry bit was still being “propagated” through the circuit. In a redesign, I would need to be more careful in my logic definition, to ensure that C[0] was used as the main carry bit driver (using the P and G internal signals to propagate the effects internally).