CME 433 – Lab 4
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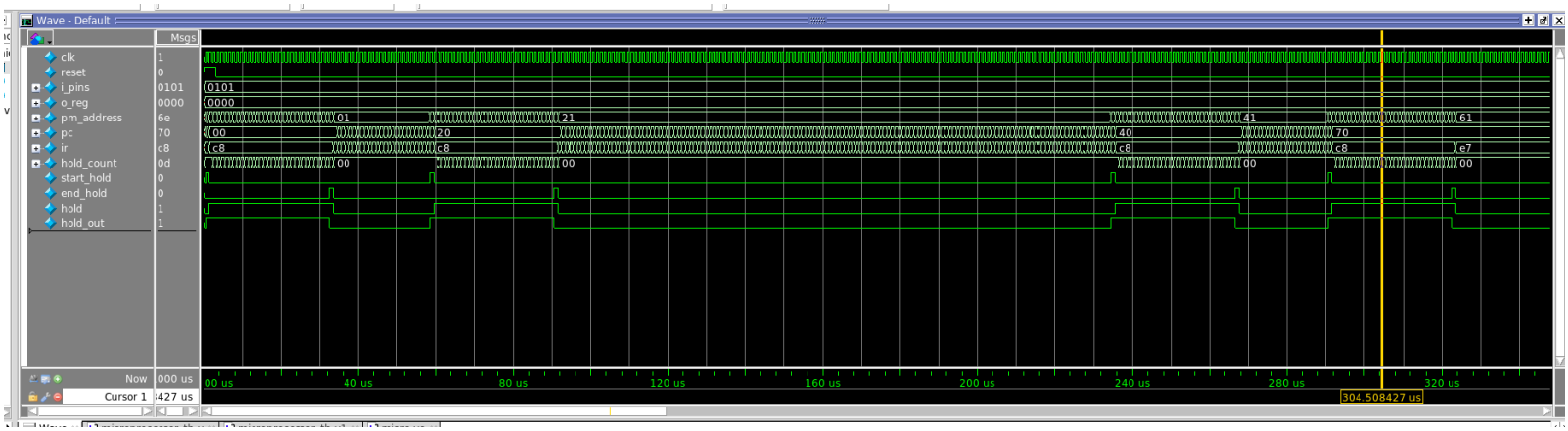
Part 1 – Single Line Cache



1. Typically, the main advantage of a cache is that it can speed up the performance of a CPU by reducing latency during read operations, by making certain instructions available with very fast read times (different cache schemes have different methods of determining which instructions to store).

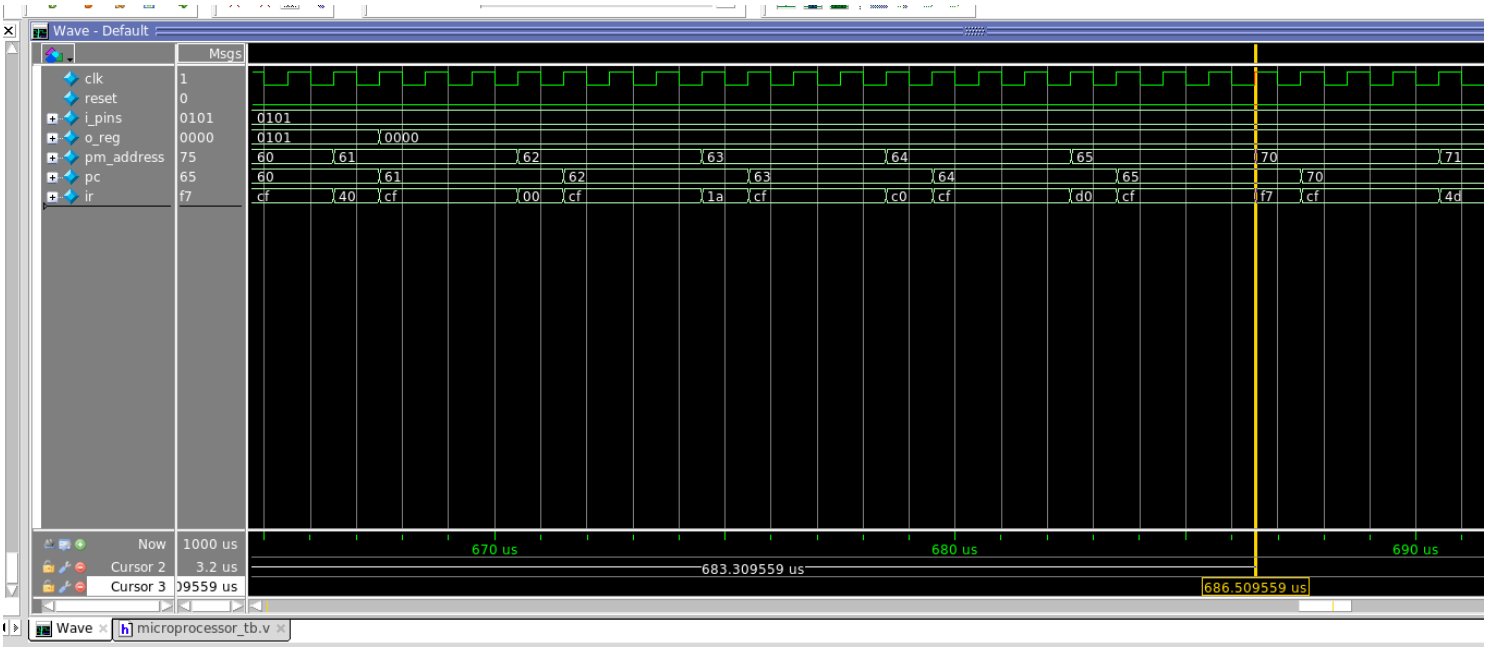
2. Common disadvantages include increased hardware complexity and increased cost. Another disadvantage is based on what kind of program is being cached – if it is a long series of sequentially ordered code without any (or very few) repeating instructions, then the cache may actually increase the latency instead of decreasing.

3. You can overcome these disadvantages by being careful & smart in your selection of cache schemes/properties (i.e. where the cache covers in memory, its placement/replacement scheme, etc). You can also try to implement the cache in a way such that it will be more likely to use parallel/cyclical code sets (GPUs, popular memory locations, etc.)

Part 2

rom_more_clk

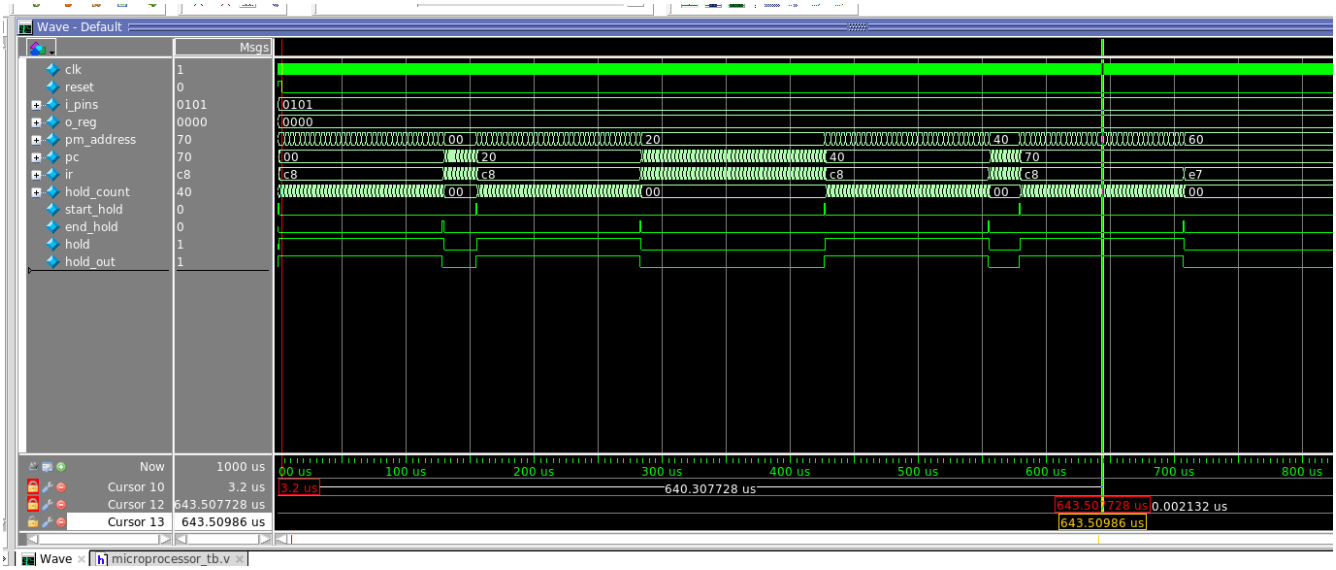
completion time: **683.510 us**

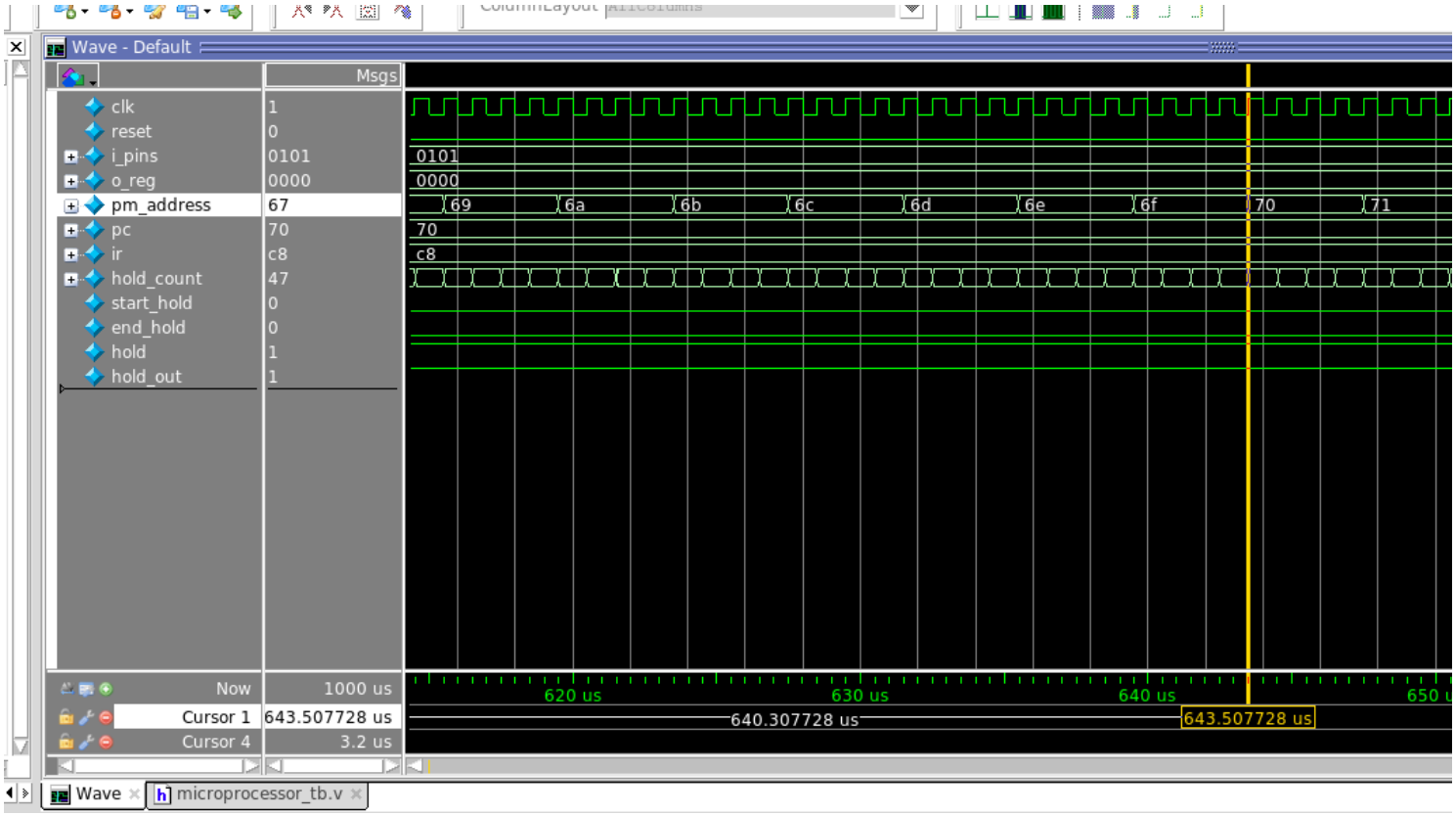


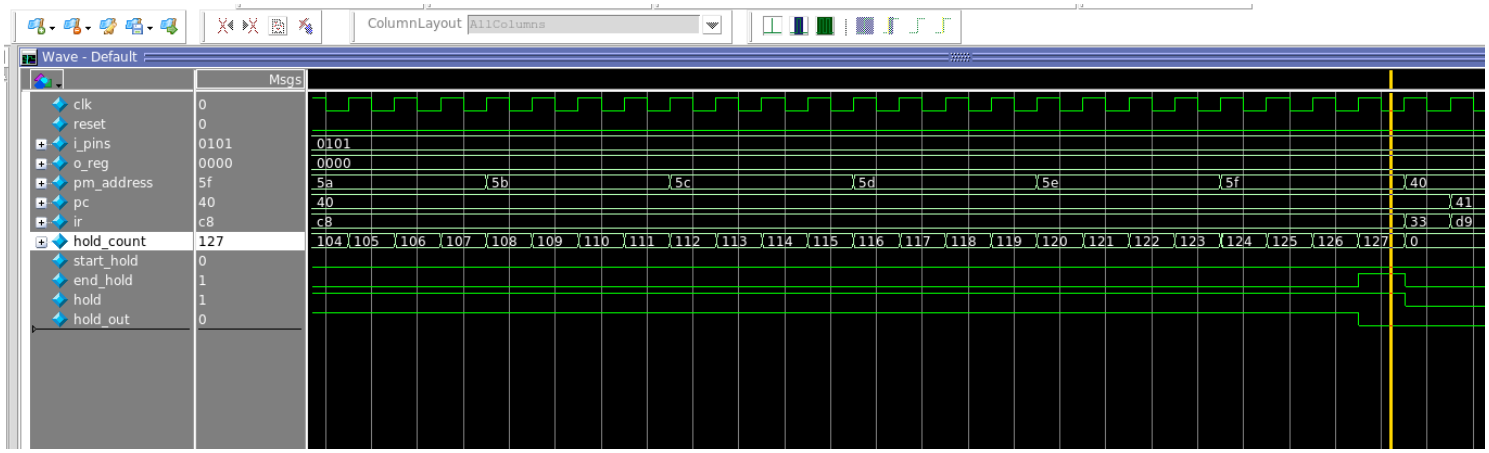
rom_more_clk_cache

successfully got the micro to suspend for 128 clk cycles while it loads instructions for the cache; duriong this time, the IR reg is stuck at C8 (NOP instruction).

Completion time: **643.308us**







Questions:

1. the difference in completion time from the micro that takes 4 clock cycles (683.510 us) and the micro with the instruction cache (643.308us) is almost exactly 40 us. The instruction cache has less latency, which is good, however the design is slightly more complex and more time is spent doing nothing (which is a design limitation).

2. Programs with lots of the exact same instructions grouped together spatially (closer in memory – i.e. loops, etc) will have much more to gain from this type of cache. Purely sequential programs with few repeating instructions might see performance decreases from a single line cache.