CME 435 – Lab 1 Document
Tyrel Kostyk – tck290 – 11216033

vlib:
Creates a design library with the name specified immediately after the command. Will return with error code if design library already exists.

vmap:
Creates a mapping between a “logical library name” and a directory (modifies the modelsim.ini file)

vlog:
compiles verilog source code and systemverilog extensions (into the work library by default)

vcom:
compiles VHDL source code (into the work library by default)

vopt:
globally optimizes designs (after vcom or vlog) in the working directory

vsim:
invokes the vsim simulator, to either view the results of the previous sim or of the one specified in the command

run:
advances the current simulation by the specified timesteps

step:
An alias for the run command with the -step switch. Steps the simulator to the next HDL or C statement

bp:
Either sets or returns a set of fine-line breakpoints

log:
creates a wave (.WLF) file containing simulation data

show:
lists HDL objects and subregions visible from the current environment

do:
Executes the commands in a *.do macro file

restart -f:
Specifies that the simulation will be restarted without requiring confirmation in a popup window

view:
Opens the specified window