Lab 4: Synchronous Sequential Circuits

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Part I

2. Export the subcircuit schematic as an image and include it in your report.

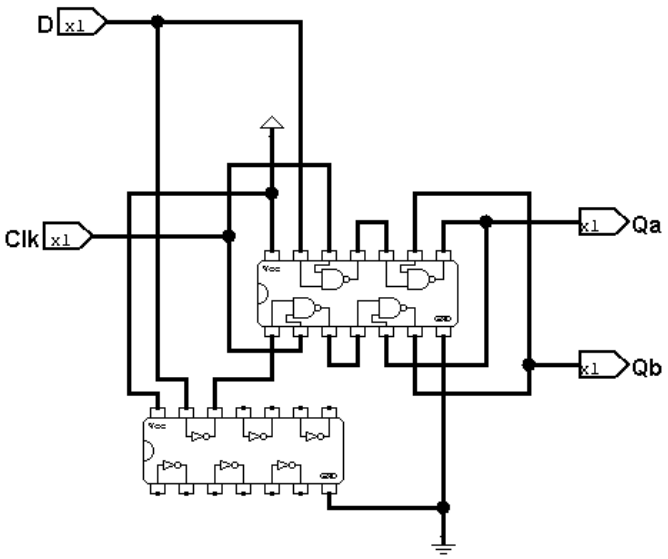

Figure 1: A schematic of the gated D-latch.

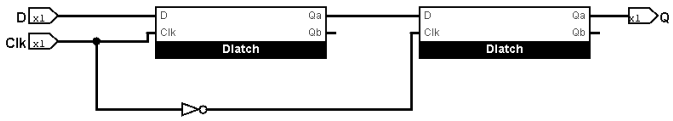

Figure 2: A schematic of the D flip-flop.

3. For the D latch and the flip flop, are there any input combinations of Clk and D that should NOT be the first you test with the *Poke* tool? List them if applicable.
When we are testing the gated D latch we should first ensure that the clock is set to ON while toggling the input for D. This is because the latch requires the clock to be active/ high at least once to capture and reflect the D input on the output. This then sets the output, which can then hold its state when the clock is subsequently set to low. In other words, these combinations cause undefined outputs because the initial values of Qa and Qb are set yet

Part IIa

2. Export the subcircuit schematic as an image and include it in your report.
3. Include a screenshot of your simulated test vectors for op5, op6, and op7.

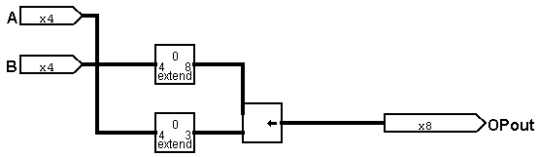

Figure 3: A schematic of op5.

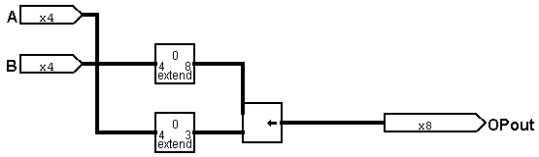

Figure 4: A schematic of op6.

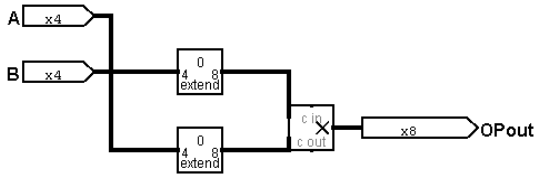

Figure 5: A schematic of op7.

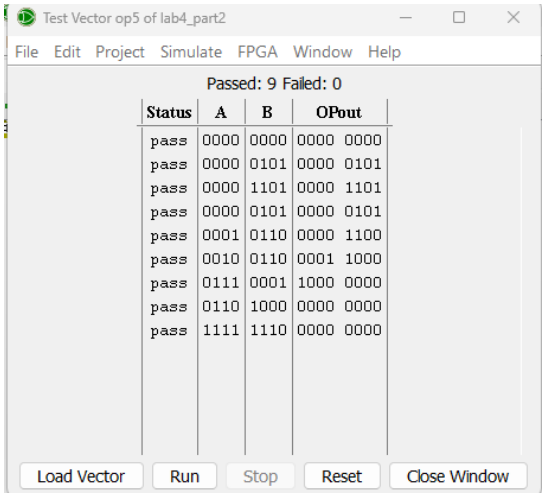

Figure 6: A simulation of op5.

Part IIb

3. Include a screenshot of your simulated timing diagram demonstrating ALUreg starting at 0x0 and increasing by 1 until 0x0f.
4. Include a screenshot of your simulated timing diagram demonstrating a shifting operation where ALUreg goes from at 0x01 and doubling until 0x00.

Part III

2. What is the behavior of the 8-bit shift register when *Load_n = 1* and *ShiftRight = 0*? Briefly explain in your prelab. When load_n is 1 and ShiftRight is = 0 the register, nothing will change. This is because load is active and it will not do its task when its 1. ShiftRight is 0 so no shifting will happen so this results in nothing happening in general.

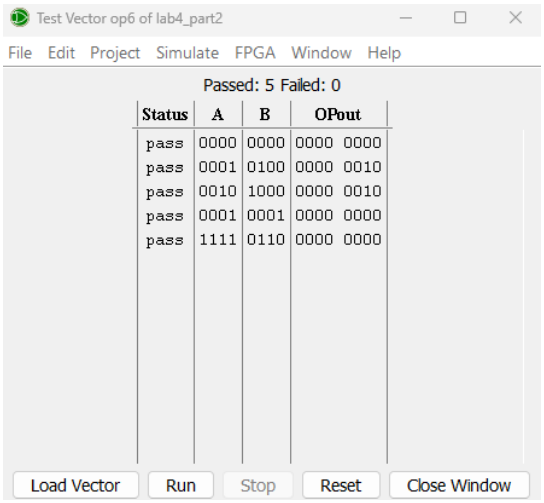

Figure 7: A simulation of op6.

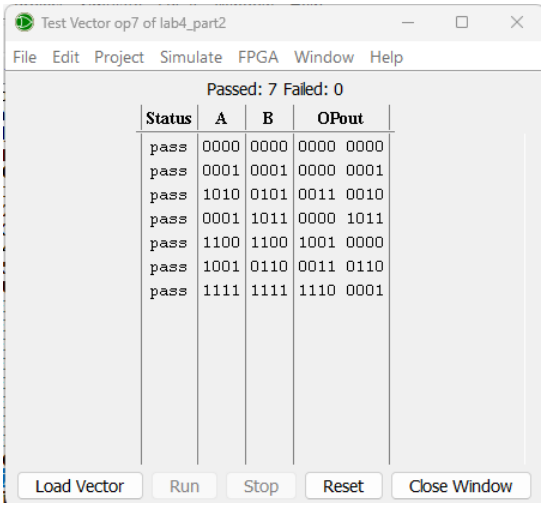

Figure 8: A simulation of op7.

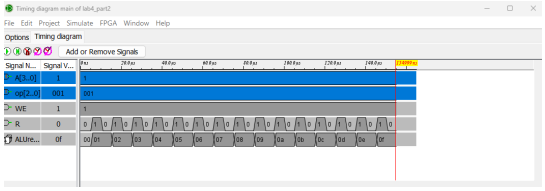

Figure 9: A timing simulation demonstrating incrementing.

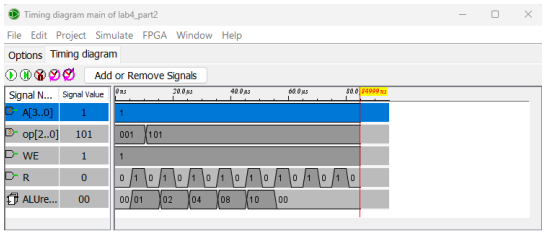

Figure 10: A timing simulation demonstrating doubling.

3. Export the subcircuit schematic as an image and include it in your report.

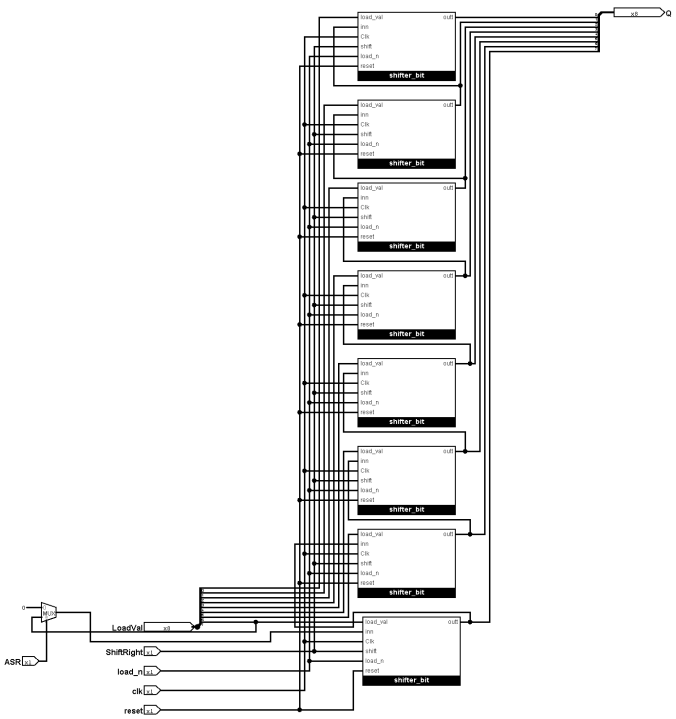

Figure 11: A schematic of the 8-bit shift register.

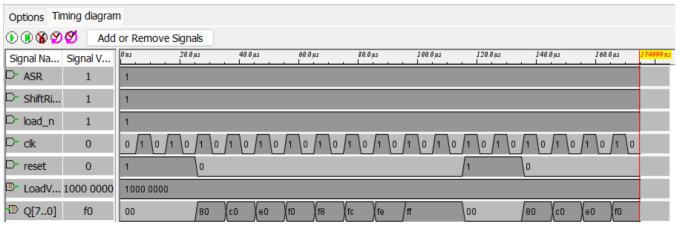

Figure 12: 8-bit shift register's test case #1

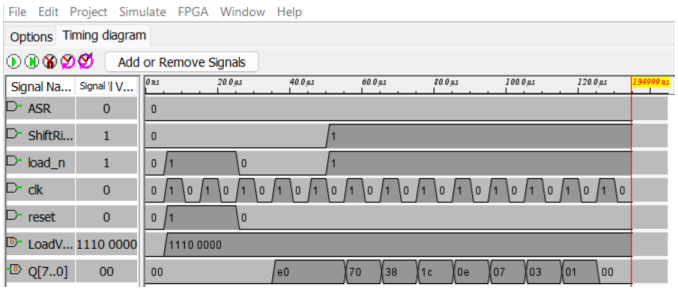

Figure 13: 8-bit shift register's test case #2

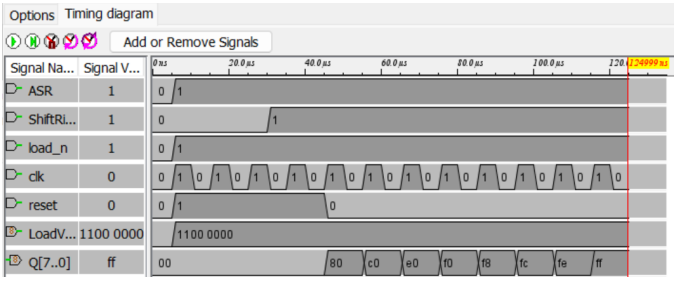

Figure 14: 8-bit shift register's test case #3