

Lab 2: The Design Hierarchy

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Part I

1. If the truth table in Table 2.1 of the handout was given in full, how many rows would it have?

Since we have 2 selection lines (s_0 and s_1) and we also have 4 inputs (u,v,w,x) we will have a total of 6 lines to consider. Since each line can be either a 0 or a 1, we have in total $2^6 = 64$

2. Export the schematic of the mux4to1 subcircuit as an image and include it in your report.

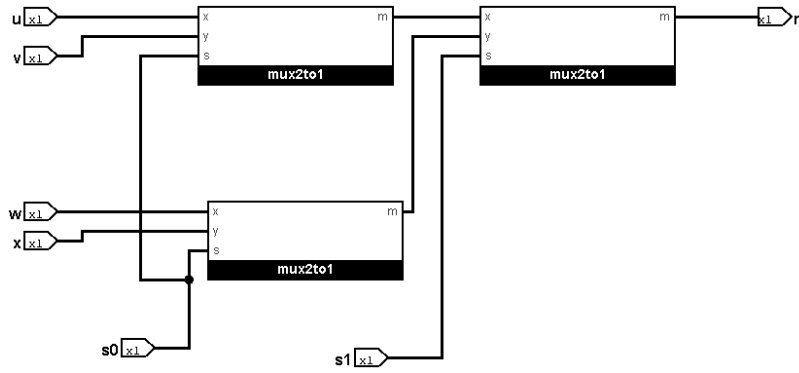


Figure 1: A schematic of the 4-to-1 multiplexer

Part II

1. Derive seven truth tables, one for each segment of the 7-segment decoder.

$D_{3:0}$	Character	S_0	S_1	S_2	S_3	S_4	S_5	S_6
0000	0	1	1	1	1	1	1	0
0001	1	0	1	1	0	0	0	0
0010	2	1	1	0	1	1	0	1
0011	3	1	1	1	1	0	0	1
0100	4	0	1	1	0	0	1	1
0101	5	1	0	1	1	0	1	1
0110	6	1	0	1	1	1	1	1
0111	7	1	1	1	0	0	0	0
1000	8	1	1	1	1	1	1	1
1001	9	1	1	1	0	0	1	1
1010	A	1	1	1	0	1	1	1
1011	b	0	0	1	1	1	1	1
1100	c	1	0	0	1	1	1	0
1101	d	0	1	1	1	1	0	1
1110	E	1	0	0	1	1	1	1
1111	F	1	0	0	0	1	1	1

Table 1: Your Table Caption

2. Use Karnaugh maps to write seven Boolean functions for each segment so that they are optimized.

$$\begin{aligned}
 S_0 &= (\overline{B} \cdot \overline{D}) + (\overline{A} \cdot C) + (B \cdot C) + (A \cdot \overline{D}) + (\overline{A} \cdot B \cdot D) + (A \cdot \overline{B} \cdot \overline{C}) \\
 S_1 &= (\overline{A} \cdot \overline{B}) + (\overline{D} \cdot \overline{B}) + (\overline{D} \cdot \overline{C} \cdot \overline{A}) + (\overline{A} \cdot C \cdot D) + (A \cdot \overline{C} \cdot D) \\
 S_2 &= (\overline{A} \cdot \overline{C}) + (\overline{A} \cdot D) + (\overline{C} \cdot D) + (\overline{A} \cdot B) + (A \cdot \overline{B}) \\
 S_3 &= (\overline{A} \cdot \overline{B} \cdot \overline{D}) + (\overline{B} \cdot C \cdot D) + (B \cdot \overline{C} \cdot D) + (B \cdot C \cdot \overline{D}) + (A \cdot \overline{C} \cdot \overline{D}) \\
 S_4 &= (\overline{B} \cdot \overline{D}) + (C \cdot \overline{D}) + (A \cdot C) + (A \cdot B) \\
 S_5 &= (\overline{C} \cdot \overline{D}) + (B \cdot \overline{D}) + (A \cdot \overline{B}) + (A \cdot C) + (\overline{A} \cdot B \cdot \overline{C}) \\
 S_6 &= (\overline{B} \cdot C) + (C \cdot \overline{D}) + (A \cdot \overline{B}) + (A \cdot D) + (\overline{A} \cdot B \cdot \overline{C})
 \end{aligned}$$

3. Use the naming scheme HEX0, HEX1, ..., HEX6 for each subcircuit. Export each subcircuit schematic as an image and include it in your report.

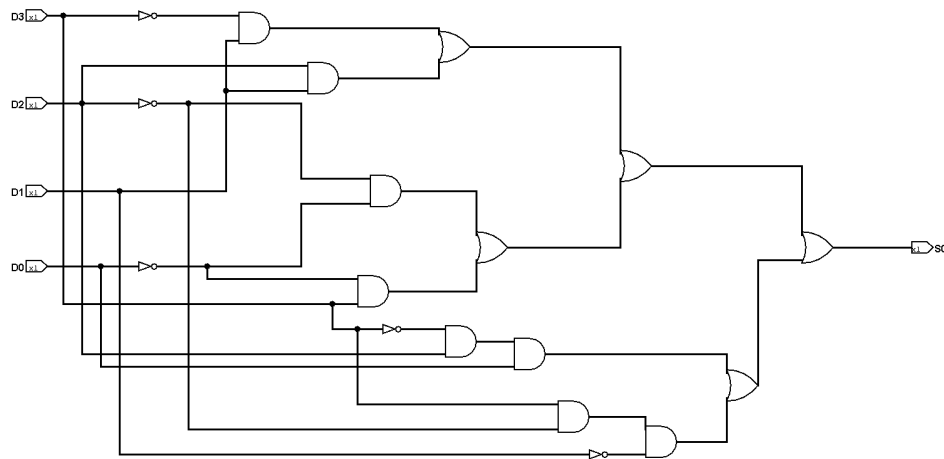


Figure 2: A schematic of HEX0

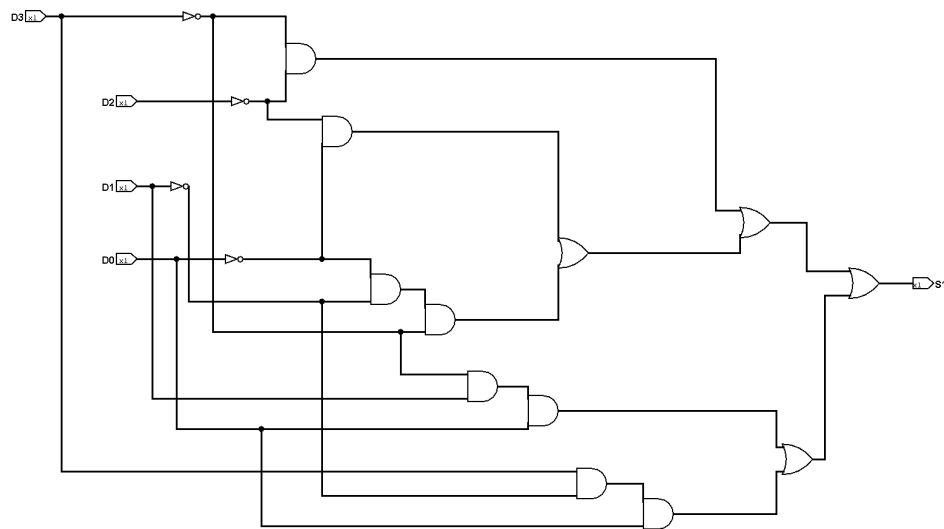


Figure 3: A schematic of HEX1

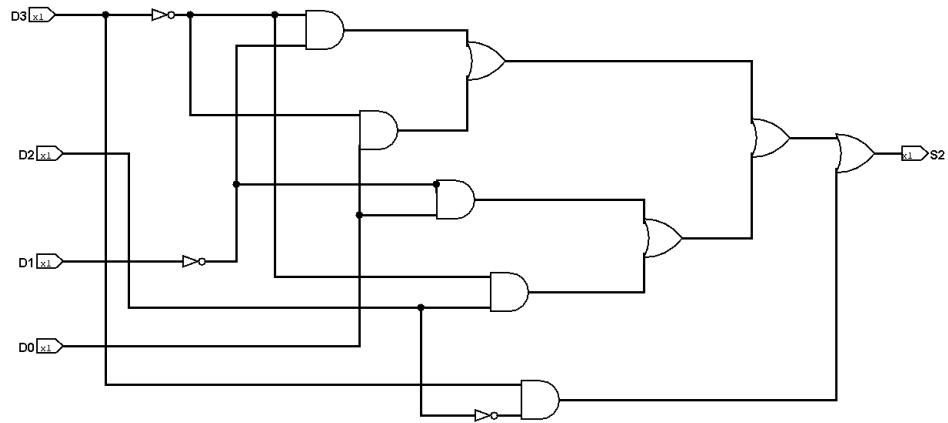


Figure 4: A schematic of HEX2

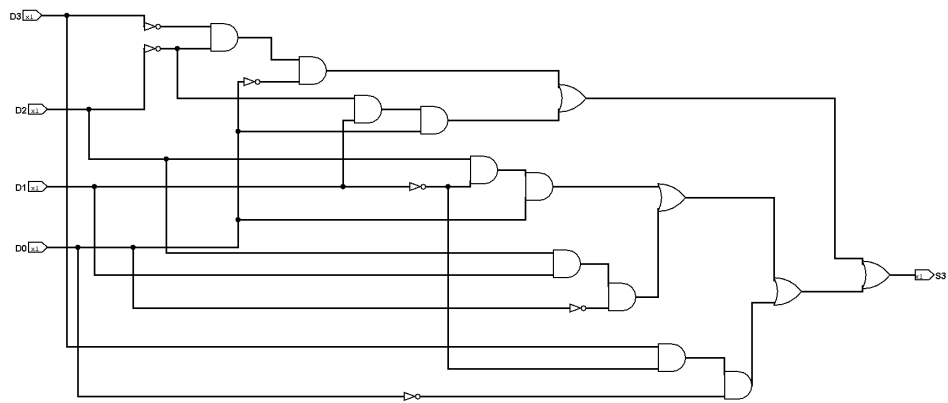


Figure 5: A schematic of HEX3

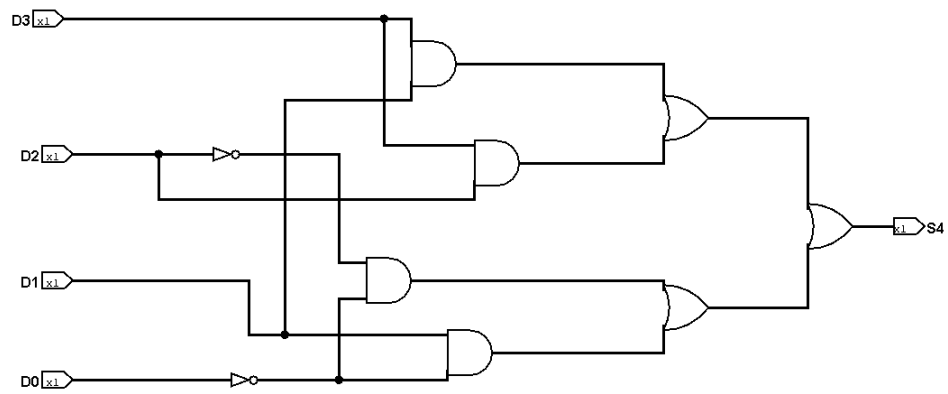


Figure 6: A schematic of HEX4

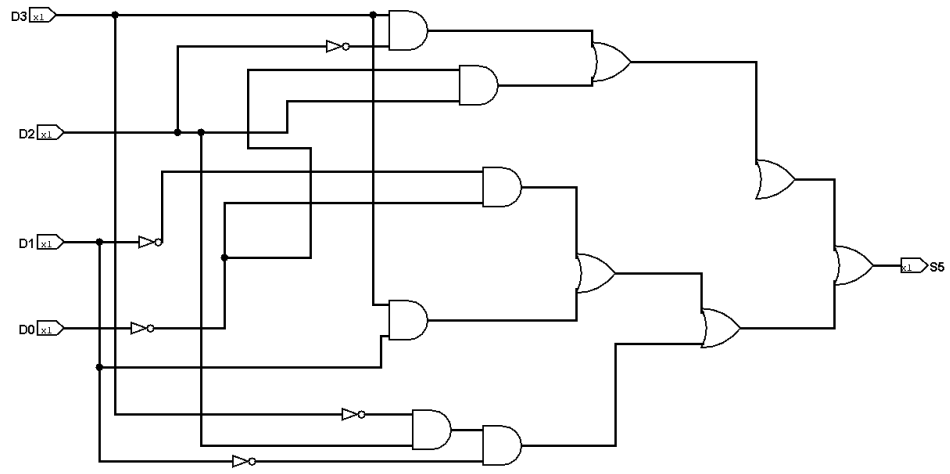


Figure 7: A schematic of HEX5

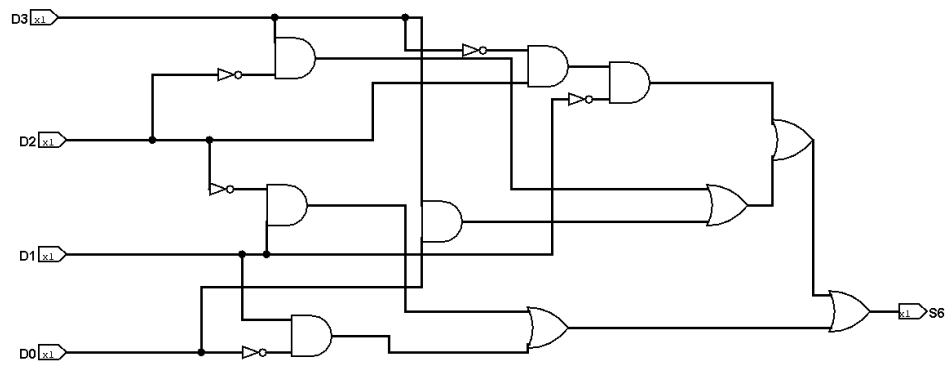


Figure 8: A schematic of HEX6