	300100 (300100))))))))))))))	1 2 3 3 4 4 4 5 5 6 6 6 7 7 8 8 9 9 C D E F F O D D E F F O D D E F F O D D D D D D D D D D D D D D D D D
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440 BOHD 2	0x0220D 0x0223B 0x0223B 0x0224A 0x0229C 0x023B 0x023B 0x022B 0x022B 0x022C 0x022D 0x022D 0x022D 0x022D 0x022D	D
March Marc	0x022D 0x0231 0x0214 0x0213 0x0216 0x0217 0x0218	D :
0x002 = Pin 10 (CMON) only signals source current (PS) in 0x003 = Current (PS) on pin 10 (ull range)]; 0x0003 = Current (PS) on pin 10 (ull range)]; 0x0004 = Current (PS) on pin 10 (ull range)]; 0x0005 = Pin 10 (CMON) signals ELPS current (PS) on pin 10 and sink current (EL) on pin 10 (ull range)]; 0x0005 = Pin 10 (CMON) signals ELPS current (0.10 V = 100%0.100%, half range signal) 488 0x01F2	0x0213 0x0216 0x0217 0x0218	
1P: 0x15 = Ethernet 2P; 0x16 = Modius TCP 2P; 0x16 = Modius TCP 2P; 0x17 = Profine 12P; 0x16 = GPB: 0x19 = CAP\$: 0x16 = EtherCAT: 0x1C = free		3 6 7
(due to communication timeout (CTO)) Bit 6		
Bit 21 Power fail 0 = none; 1 = active Bit 32 REM-SB 0 = none; 1 = active Bit 33 REM-SB 0 = none; 1 = active Bit 30 REM-SB 0 = none; 1 = active Bit 30 REM-SB 0 = none; 1 = active Bit 30 REM-SB 0 = none; 1 = active Bit 30 REM-SB 0 = none; 1 = active Bit 30 REM-SB 0 = none; 1 = active Bit 30 REM-SB 0 = none; 1 = active Device state 2 Device state 3 Device state 4 Device state 5 Devic	0x021B 0x021C 0x021D 0x0212	C D 112
521 0x0209 x Court of OC alarms since power up(PSB/PSBE devices: source mode) R unit(16) 2 1 0x0000 - 0xFFFF 3 3 21 0x0000 - 0xFFFF 3 3 3 3 3 3 3 3	0x0313 0x0314 0x0315 0x0316 0x0317 0x0318 0x0319 0x02FE 0x0301 0x0304 0x0302	3 4 5 6 7 8 9 E 1 4 2
570 0.023A x x x Sink mode: Overpower protection threshold OPP RW uint(16) 2 1 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 2 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 3 7 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 4 9 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 4 9 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 4 9 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 4 9 0.00000 - 0.0£147 (0 - 110%) OPP threshold (for translation see programming guide) 4 9 0.00000 - 0.0£147 (0 - 110%) OPP thresh	0x0305	5 3 0 1
656 0x029	0x0404 0x0405 0x0406 0x0407 0x0408 0x021E 0x021F 0x0220 0x0221 0x0222	4 5 6 7 8 F 1 2 3
	Dx0227	
2225 2255 2225 2255 2225	0x07F9 0x07FA 0x07FB 0x07FC 0x07FD 0x07FE 0x07FF	B C D
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Description		
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	0x0234	34
Word 1 = House (0-23) Word 2 = Mirruse (0-59)	0x0235 0x0236 0x0237 0x0238 0x0238	36 37 38 39