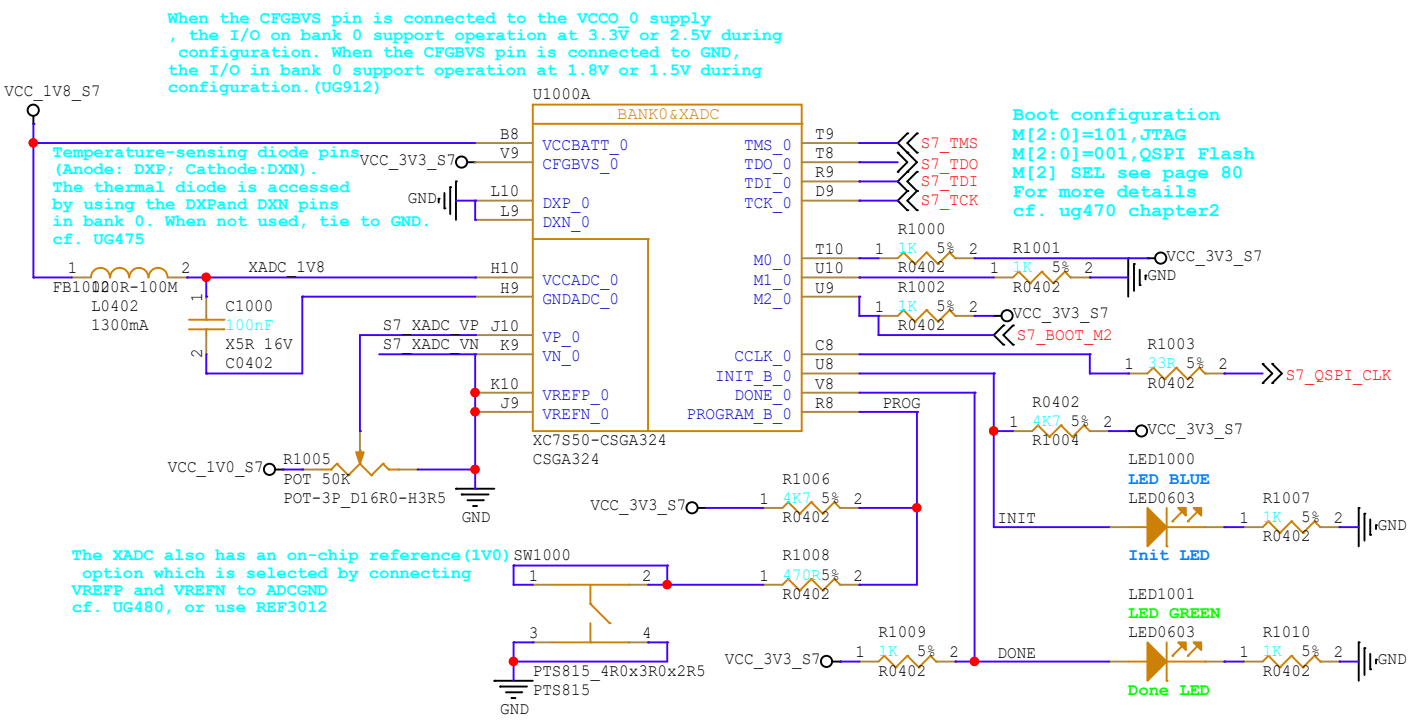
XC7S50 Bank0



Designed by: tz61@illinois.edu	
Reviewed by: Tongning Zhang	
Date: Monday, November 11, 2024	
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File: XC7S50Main	
Project:10.S7_BANK0	

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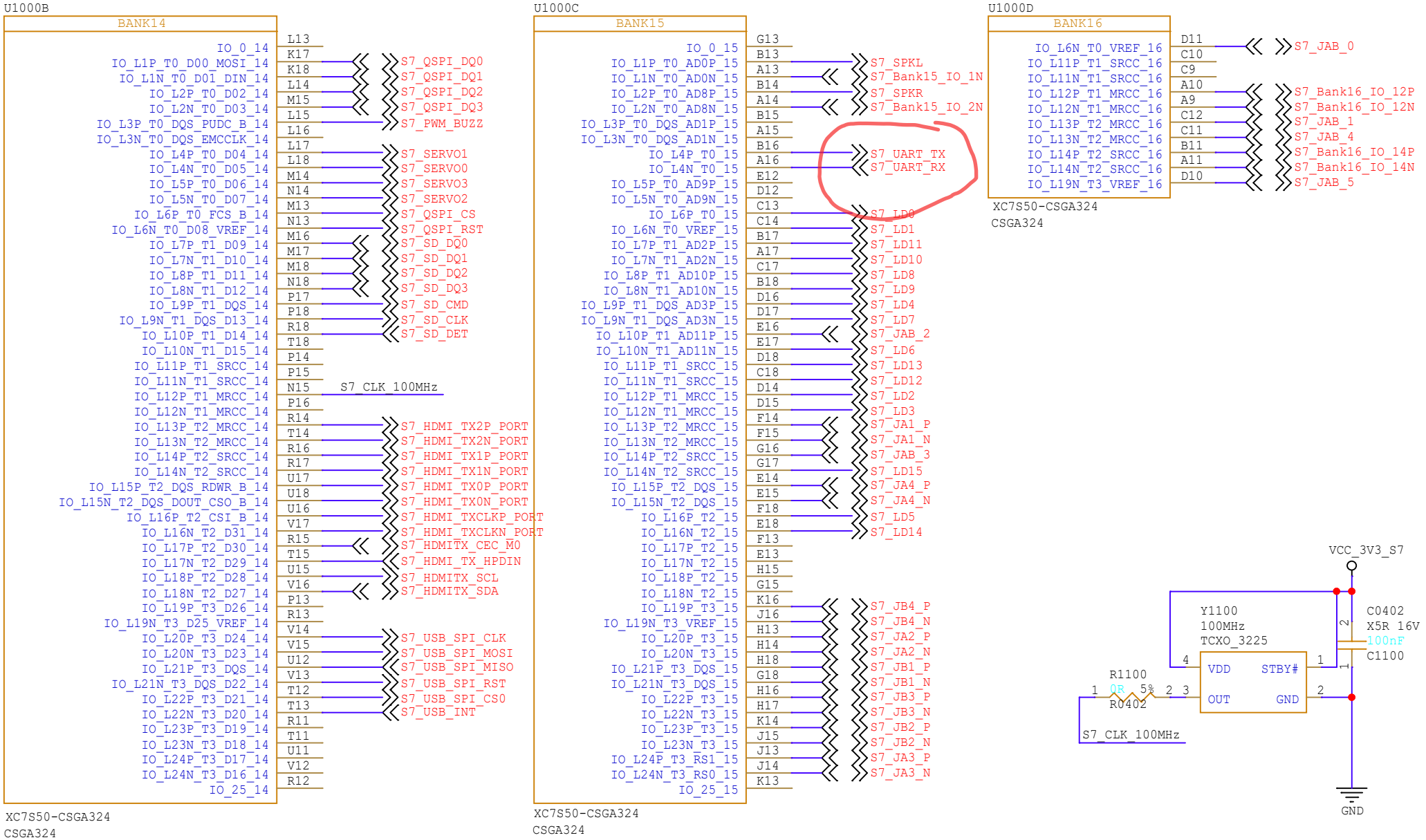
XC7S50 Bank14/15/16



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Reviewed by: Tongning Zhang	
Date: Monday, November 11, 2024	
Rev: v0.1	
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File: XC7S50Main	
Project: 11.S7_BANK14/15/16/PLCLK	

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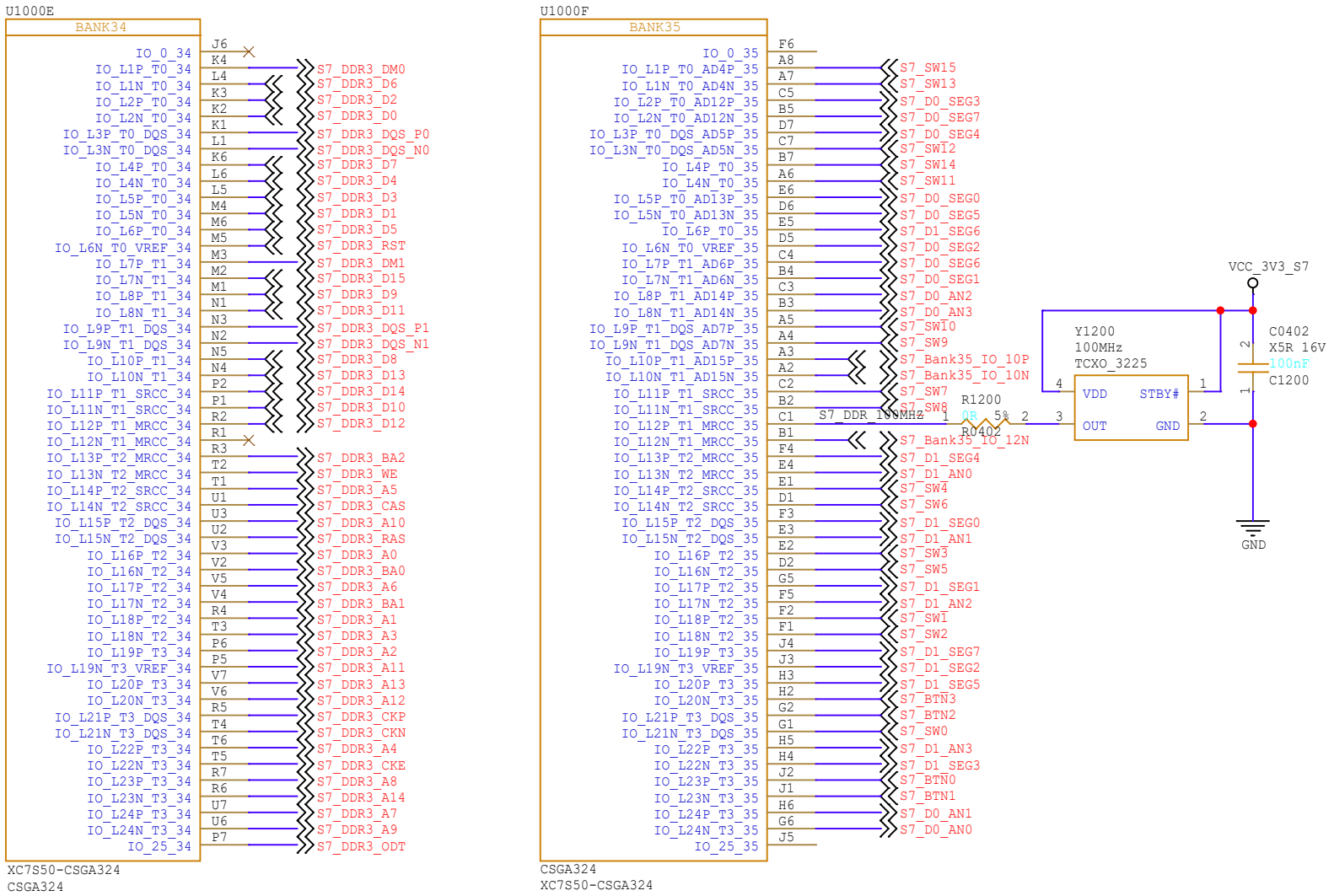
XC7S50 Bank34/35/DDRCLK



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Date: Monday, November 11, 2024	
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File: XC7S50Main	
Project:12.S7_BANK34/35/DDRCLK	

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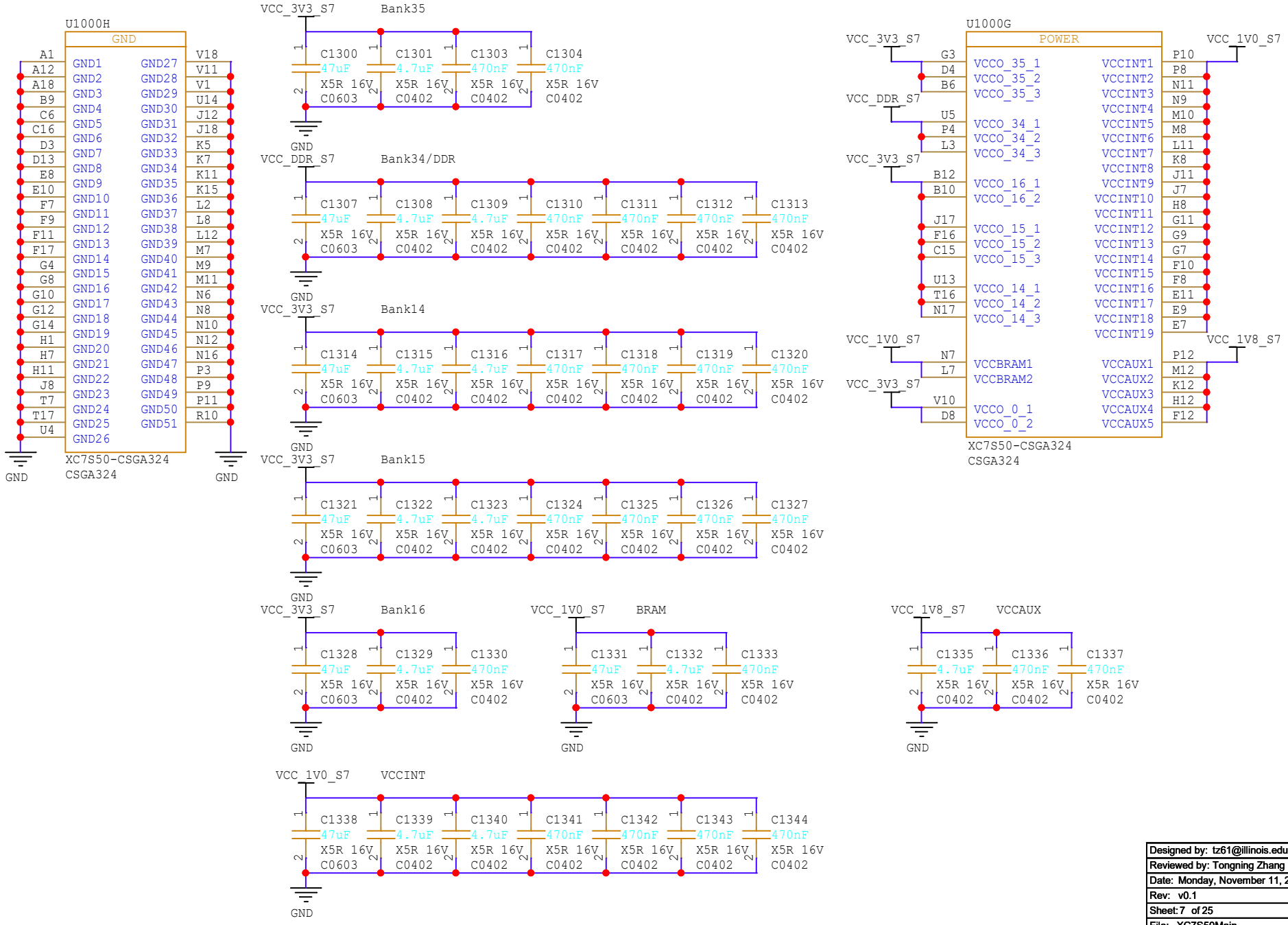
XC7S50 Power/Gnd



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Reviewed by:	Tongning Zhang
Date:	Monday, November 11, 2024
Rev:	v0.1
Sheet:	7 of 25
File:	XC7S50Main
Project:	13.S7_Power/Gnd

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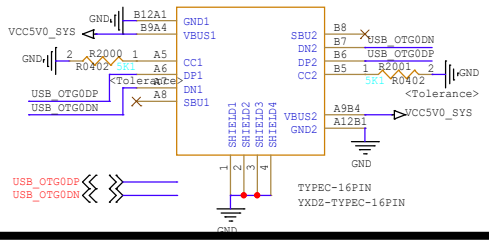
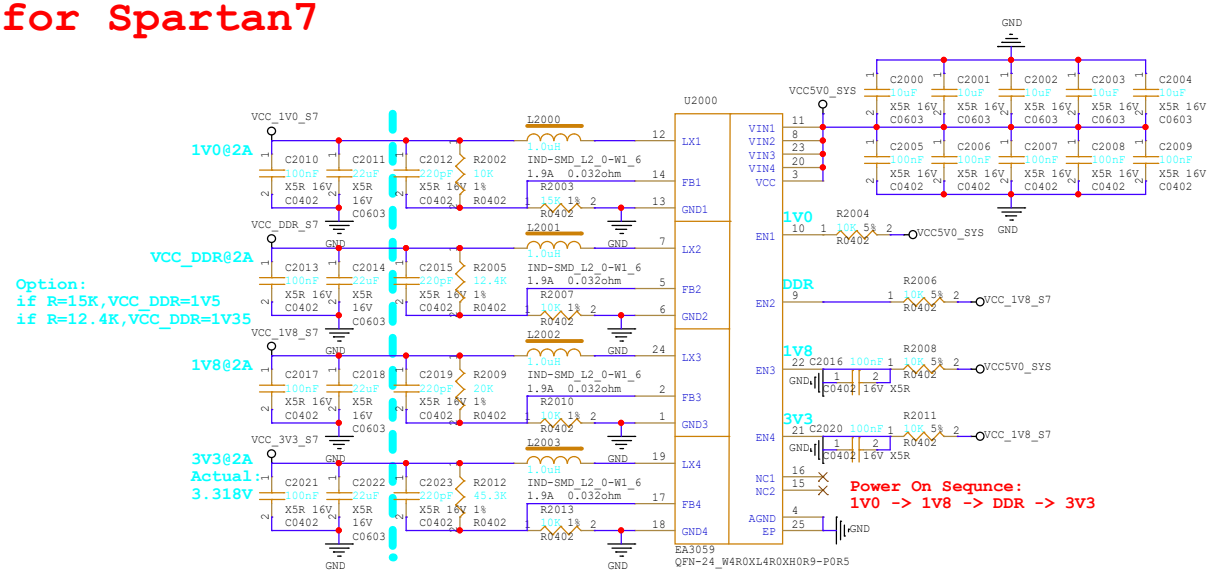
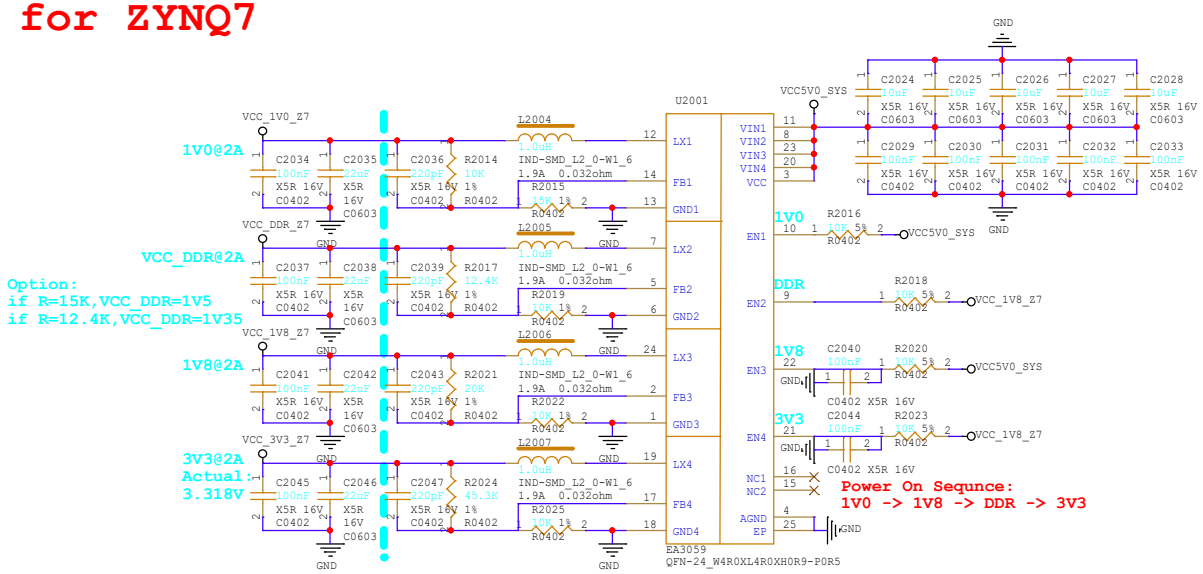
5V Input/USB In(Type-C connector)



Power for Spartan7



Power for ZYNQ7



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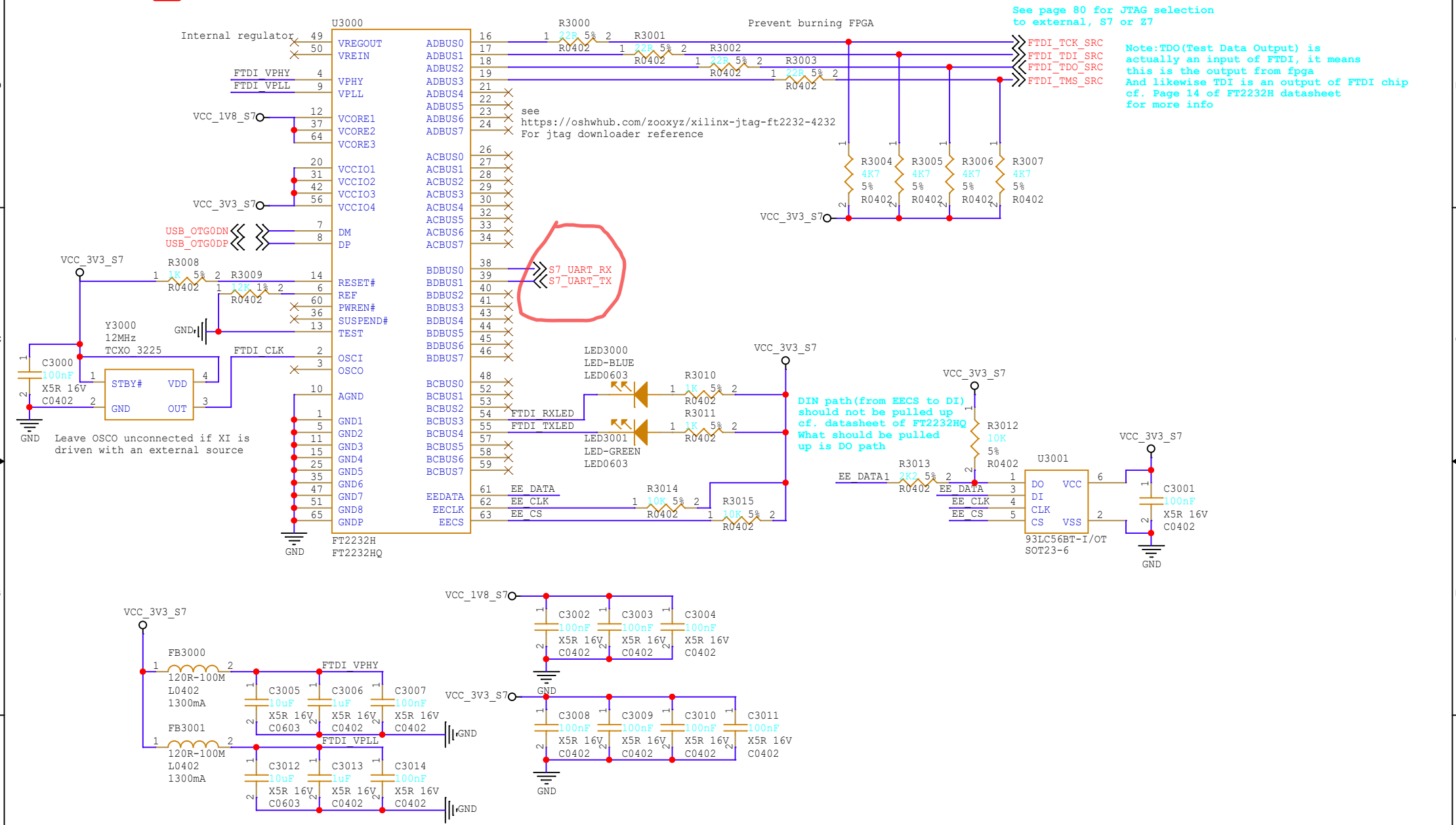
Date: Monday, November 11, 2024	
Rev: v0.1	ZJU-UIUC INSTITUTE
Sheet: 8 of 25	
File: XC7S50Main	
Project:20.PowerIN	

FT2232_HQ JTAG Debugger/UART



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Reviewed by: Tongning Zhang	
Date: Monday, November 11, 2024	
Rev: v0.1	
Sheet:9 of 25	
File: XC7S50Main	
Project:30.JTAG Debugger/UART	

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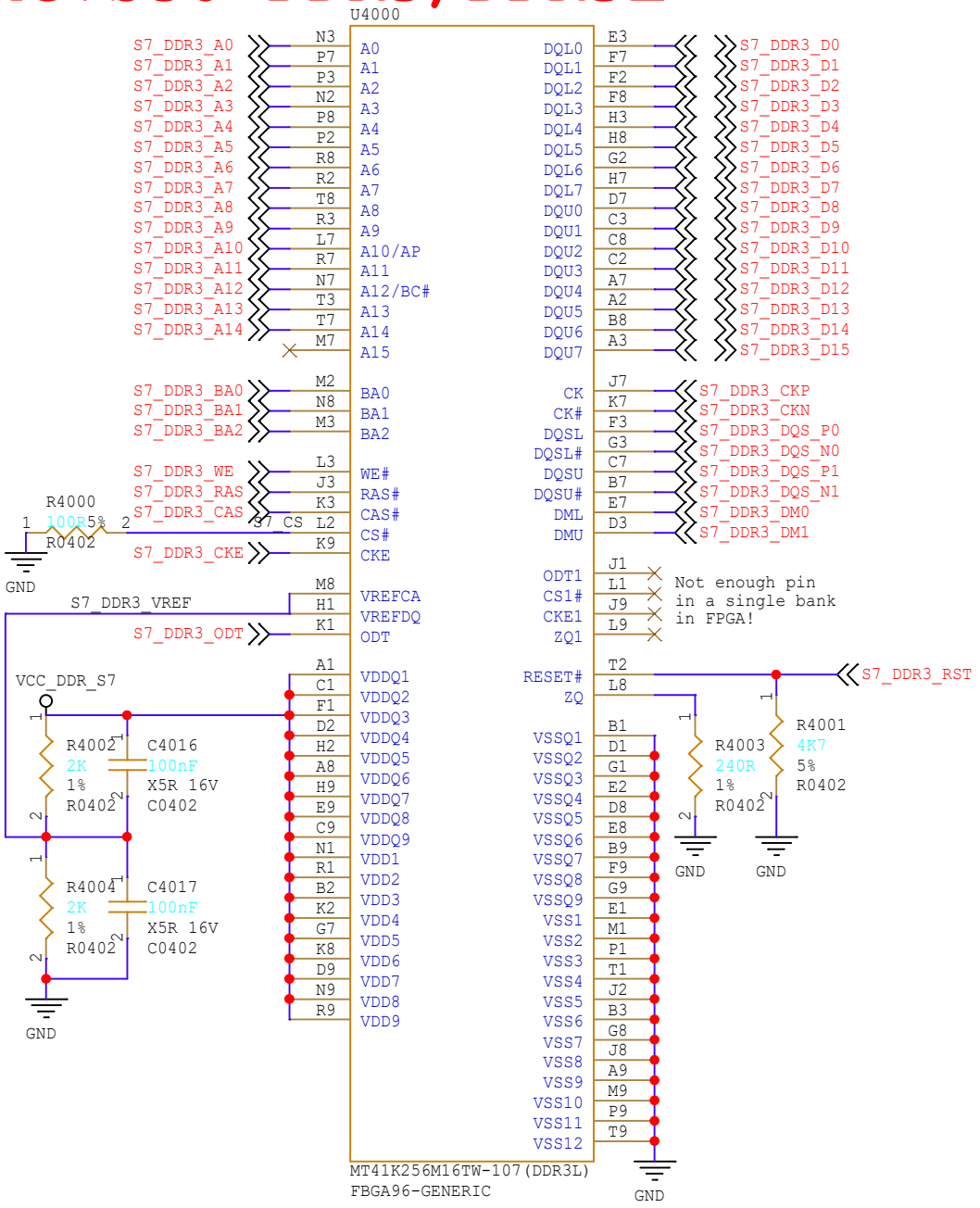
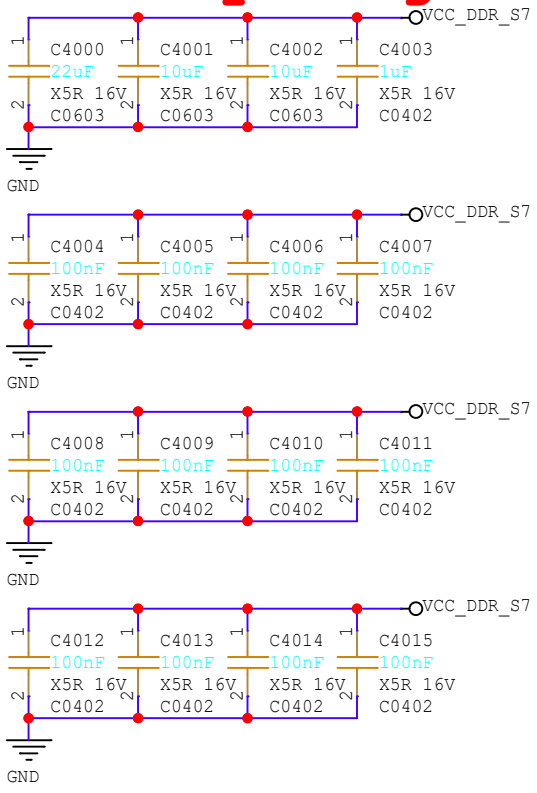
XC7S50 DDR3/DDR3L



DDRCheck done by tz61

Decoupling Capacitors



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Reviewed by:	Tongning Zhang
Date:	Monday, November 11, 2024
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File:	XC7S50Main
Project:	40.S7_DDR3

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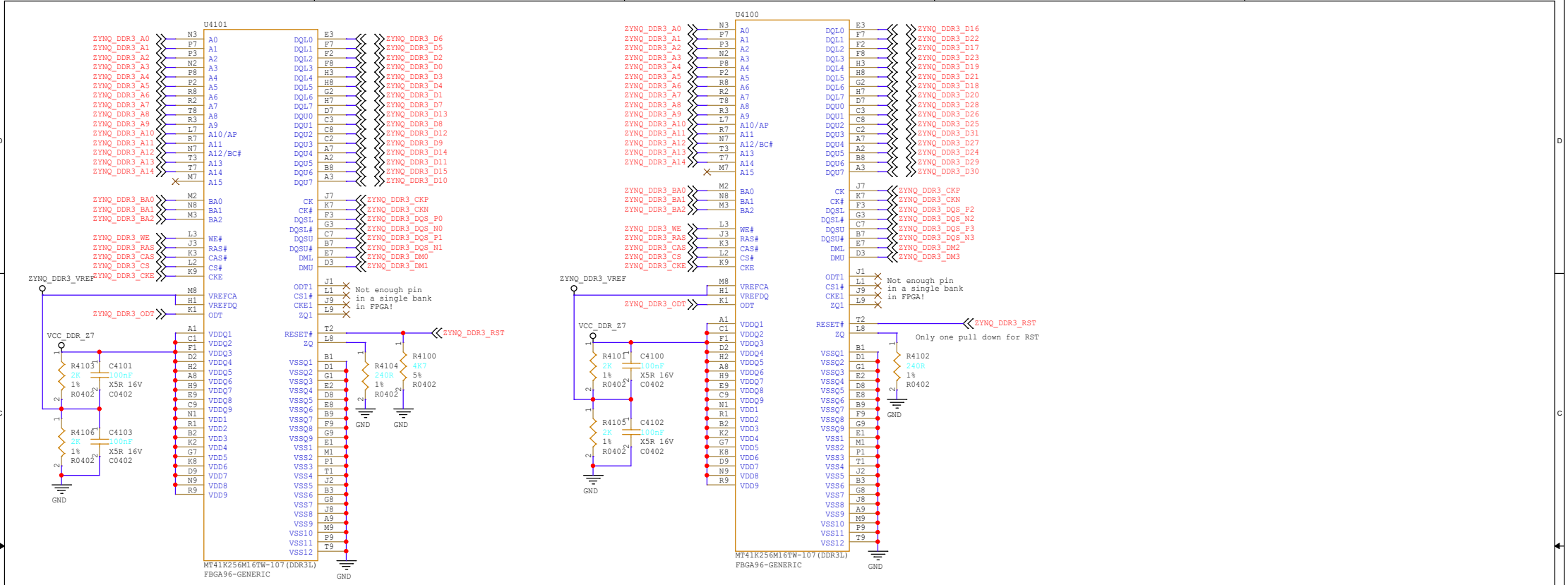
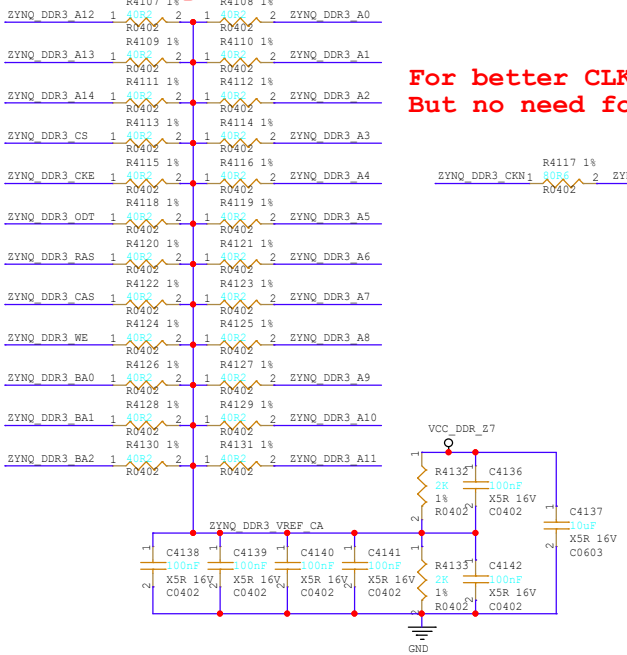
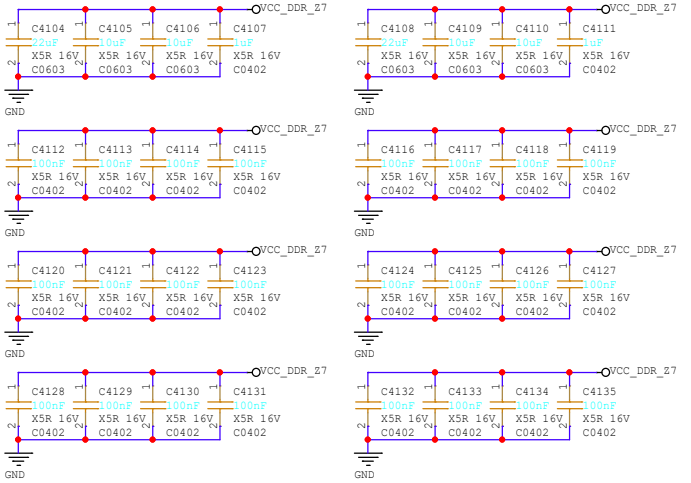


Terminating Resistor for Address/Control



For better CLK, add RC filter at T point
But no need for design of CLK at 400/333MHz

Decoupling Capacitors
Ch1 Ch2



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Date: Monday, November 11, 2024	
Rev: v0.1	
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File: XC7S50Main	
Project: 41_27_DDR3	

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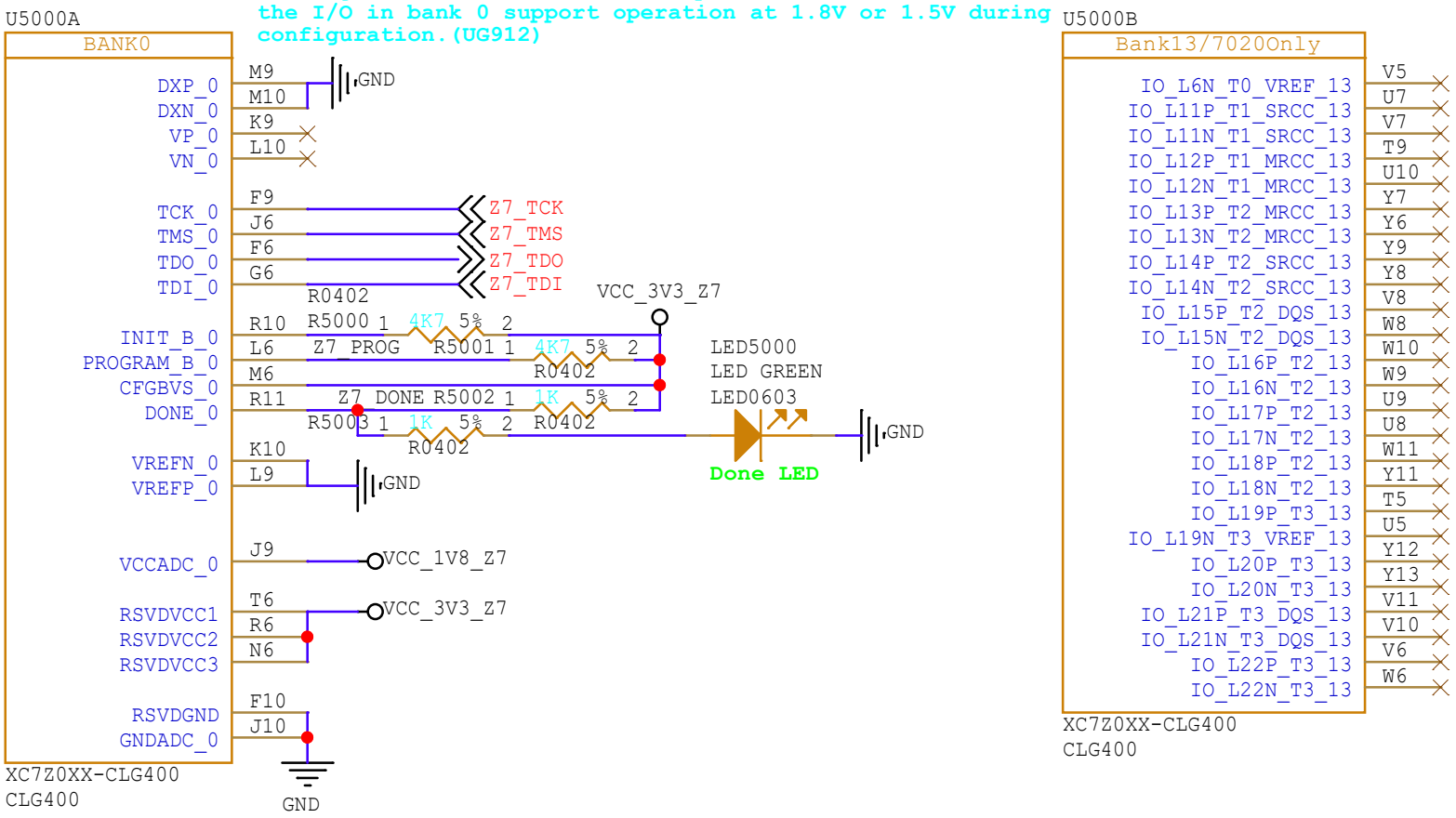
XC7Z010 Bank0/13

When the CFGBVS pin is connected to the VCCO_0 supply , the I/O on bank 0 support operation at 3.3V or 2.5V during configuration. When the CFGBVS pin is connected to GND, the I/O in bank 0 support operation at 1.8V or 1.5V during configuration.(UG912)



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Reviewed by:	Tongning Zhang
Date:	Monday, November 11, 2024
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File:	XC7S50Main
Project:	50.Z7_Bank0/13

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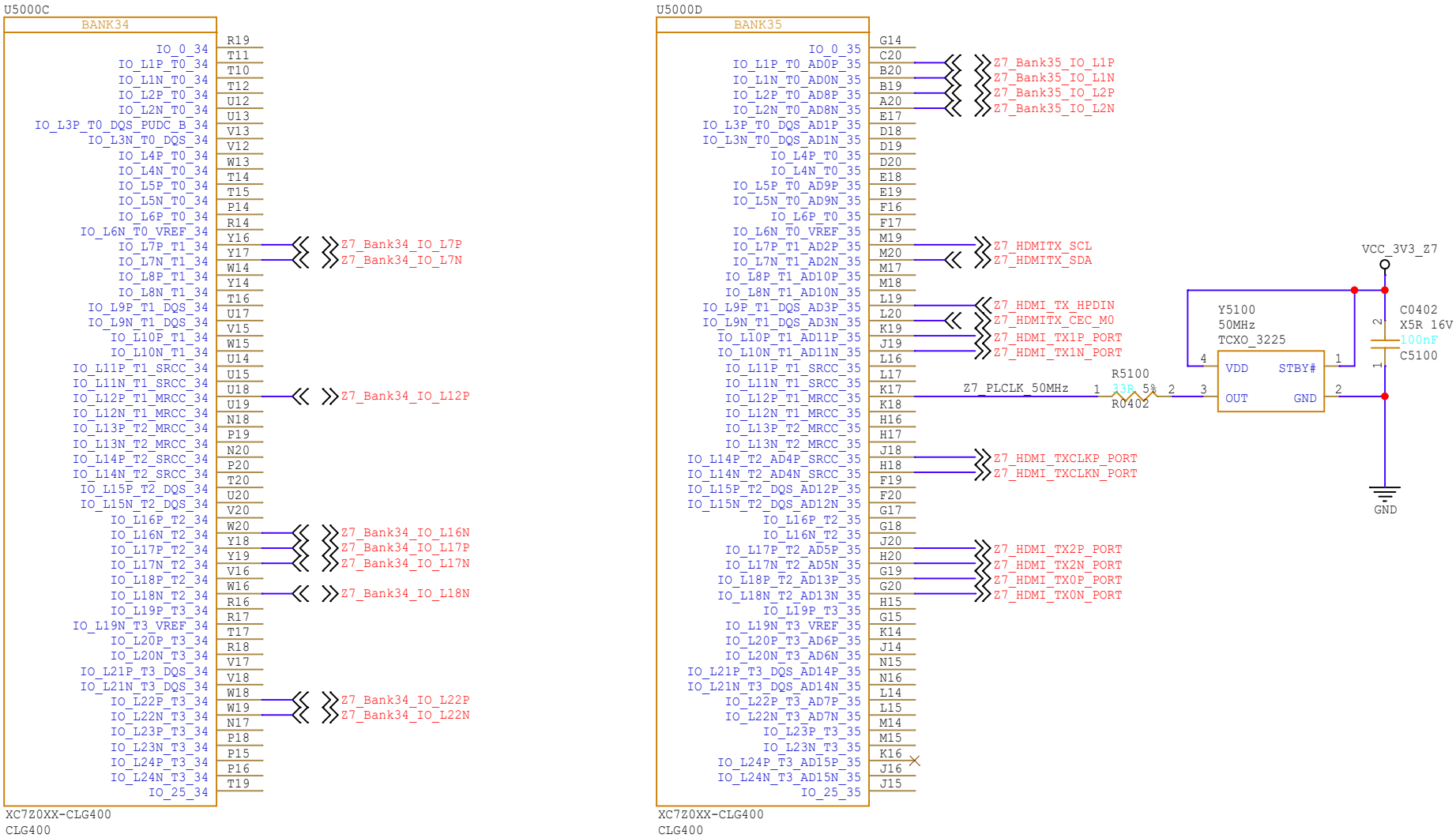
XC7Z010 Bank34/35



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Reviewed by: Tongning Zhang	
Date: Monday, November 11, 2024	
Rev: v0.1	
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File: XC7S50Main	
Project: 51.Z7_Bank34/35	

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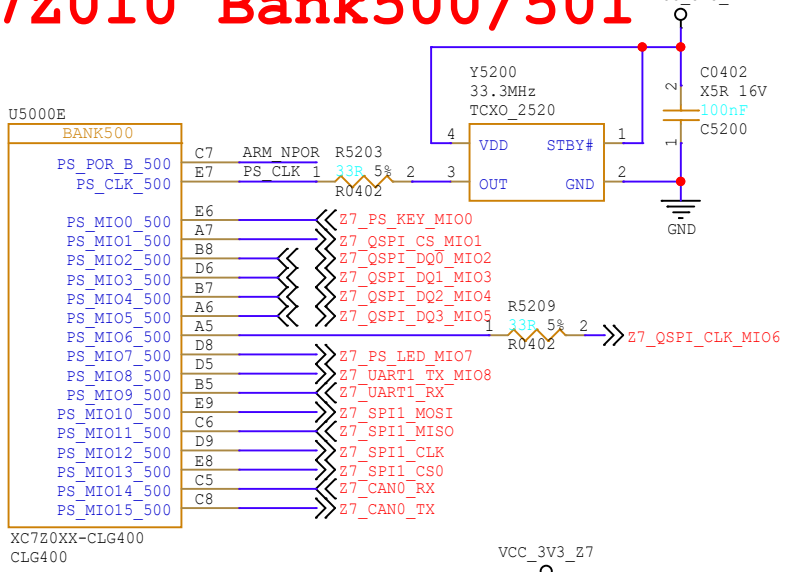
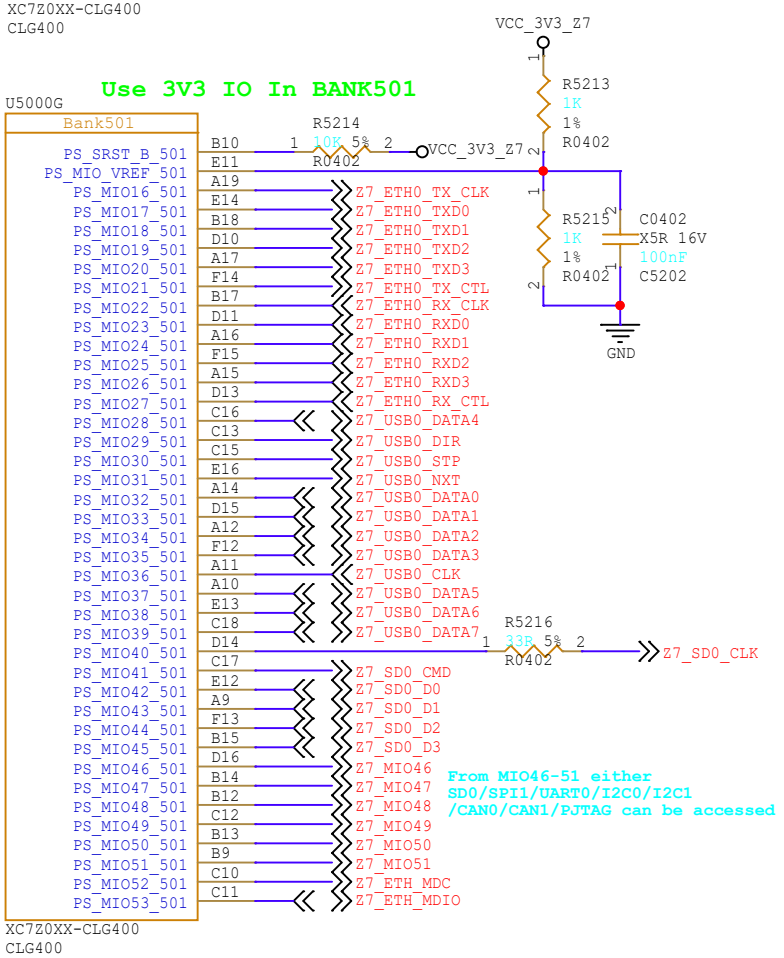
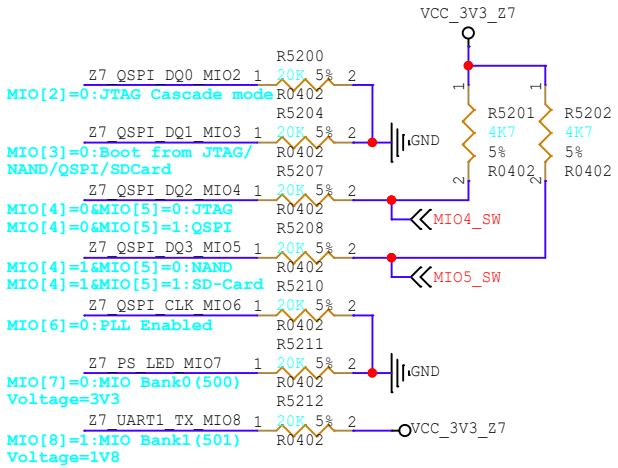
XC7Z010 Bank500/501

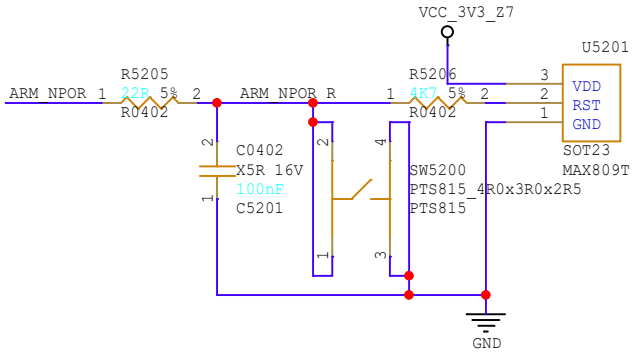




Boot mode SEL



Reset Signal



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Date: Monday, November 11, 2024	
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File: XC7S50Main	
Project:52.Z7_Bank500/501	

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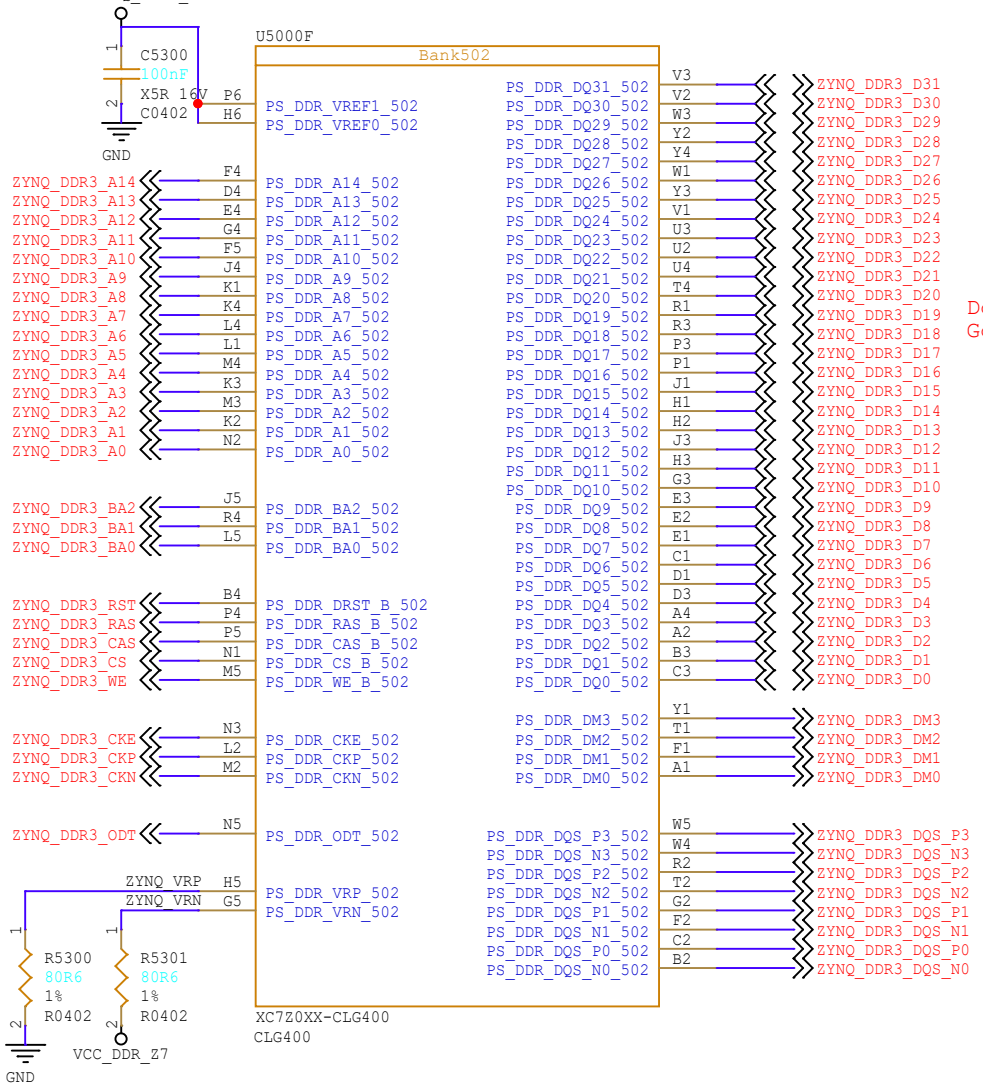

Dont' exchange DQ net here
Goto page 41 to exchange DQ pins

DDRCheck done by tz61

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Date: Monday, November 11, 2024	
Rev: v0.1	
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File: XC7S50Main	
Project:53.Z7_Bank502	

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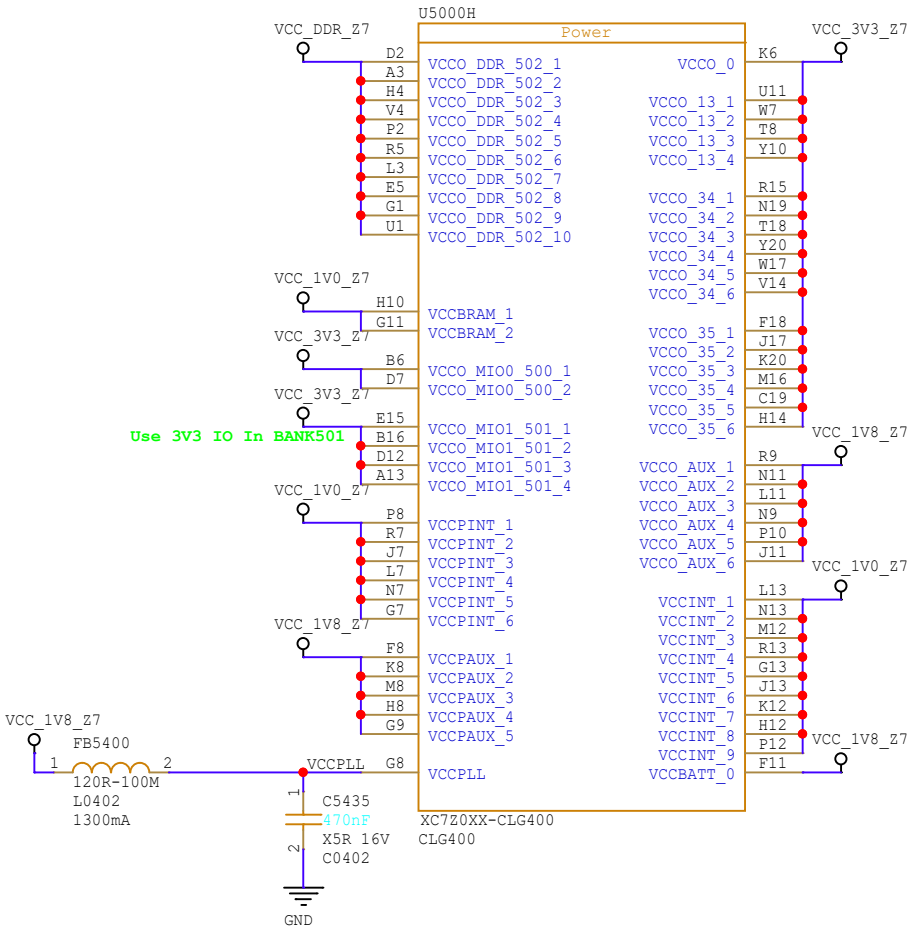
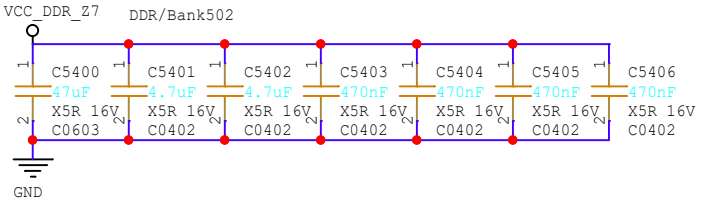
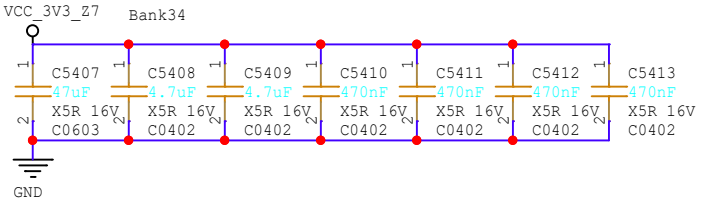
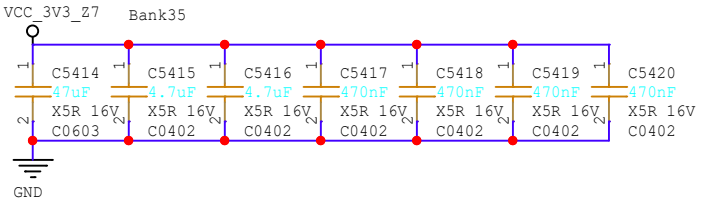
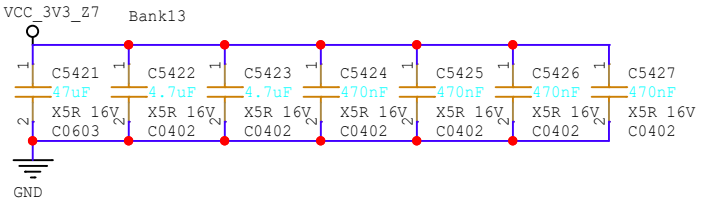
XC7Z010 Power/Gnd

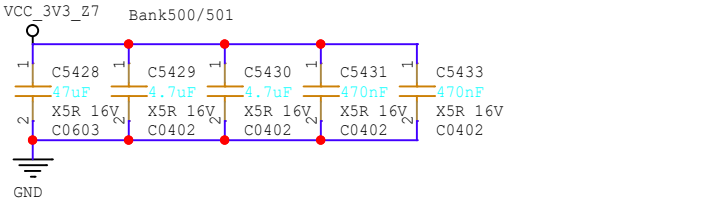


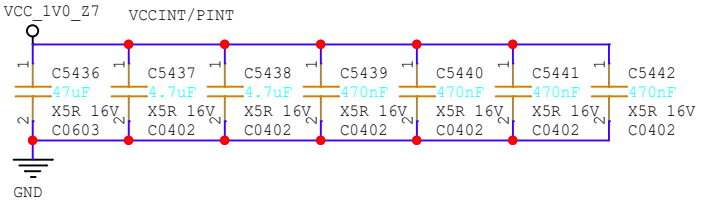


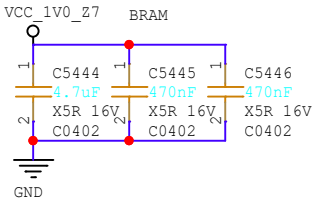


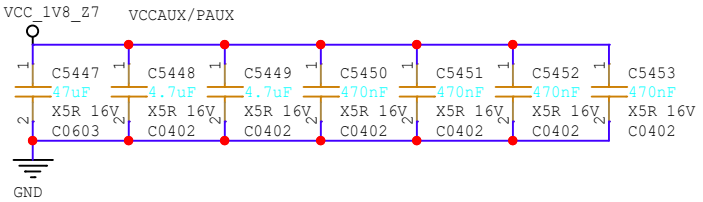


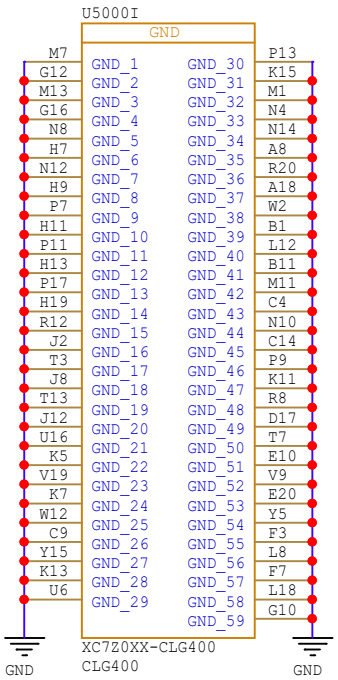












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Date: Monday, November 11, 2024	
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File: XC7S50Main	
Project:54.Z7_Power/Gnd	

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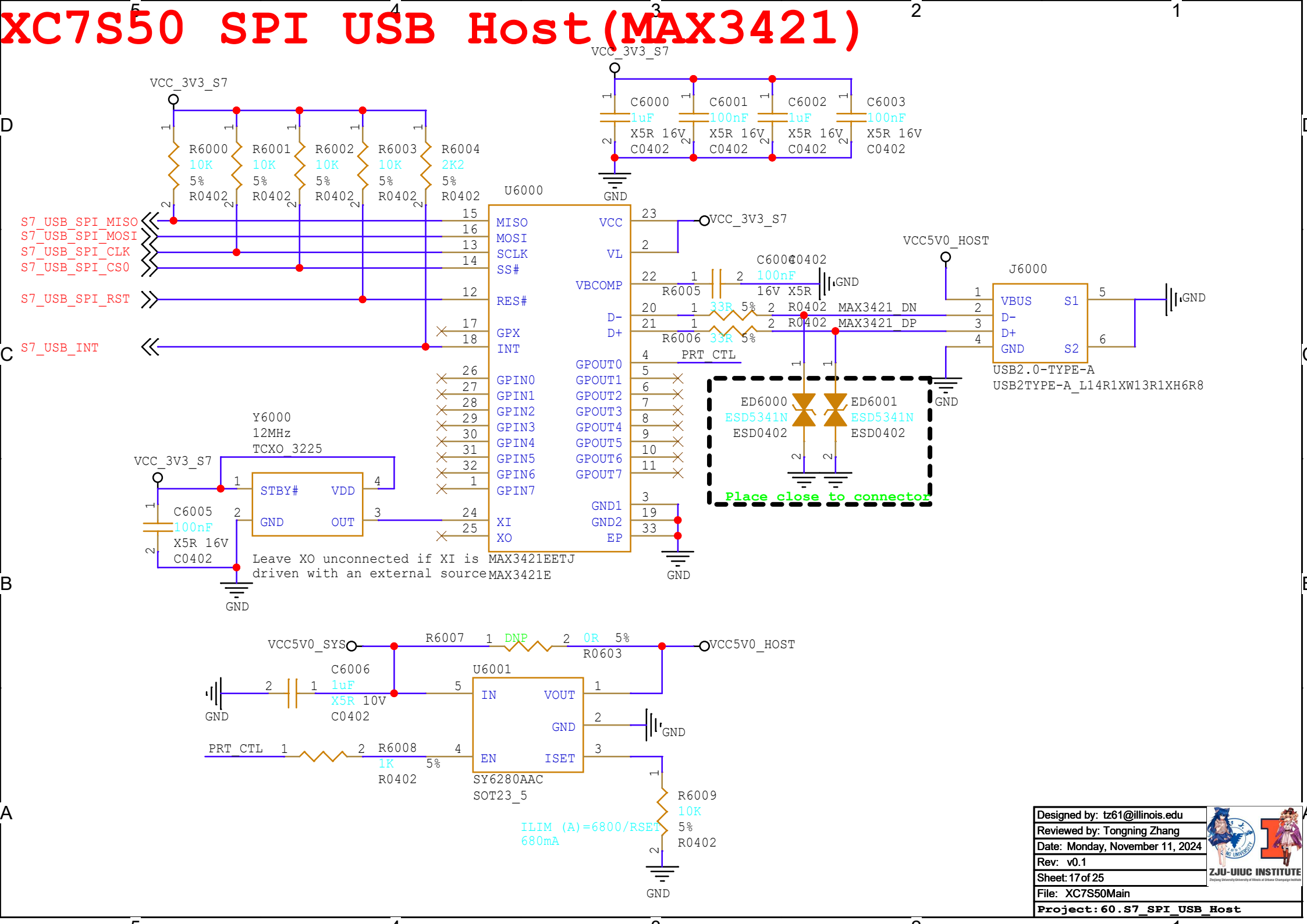
XC7S50 SPI USB Host(MAX3421)



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Date:	Monday, November 11, 2024
Rev:	v0.1
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File:	XC7S50Main
Project:	60.S7_SPI_USB_Host

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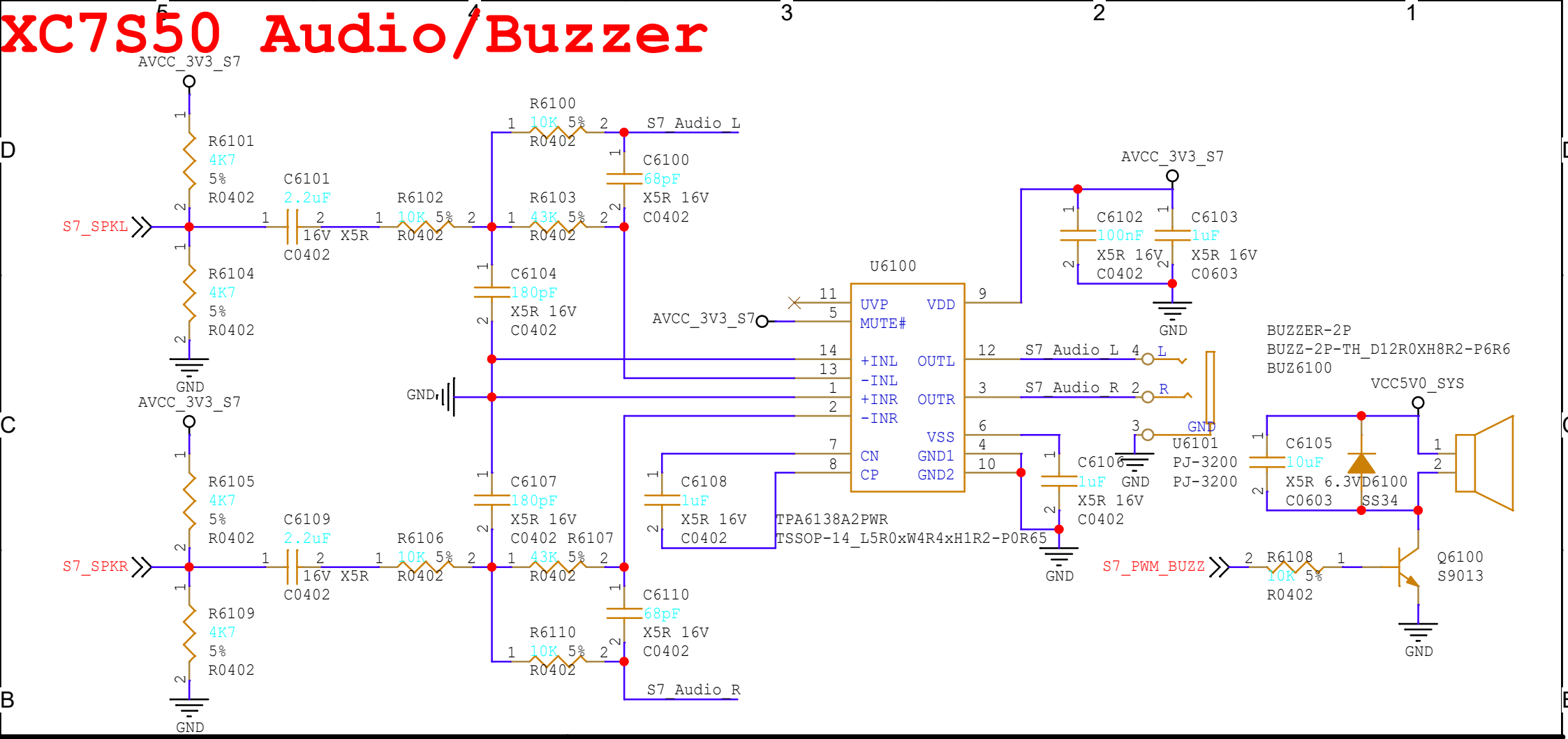
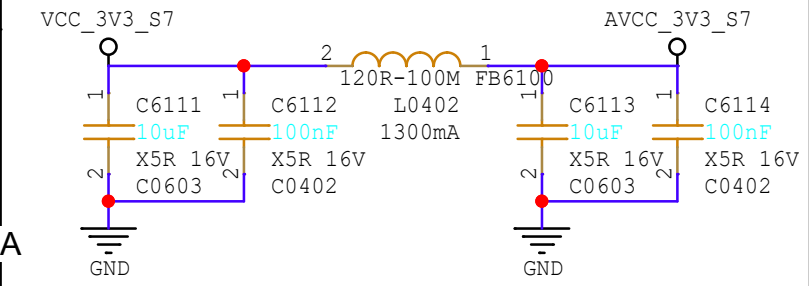
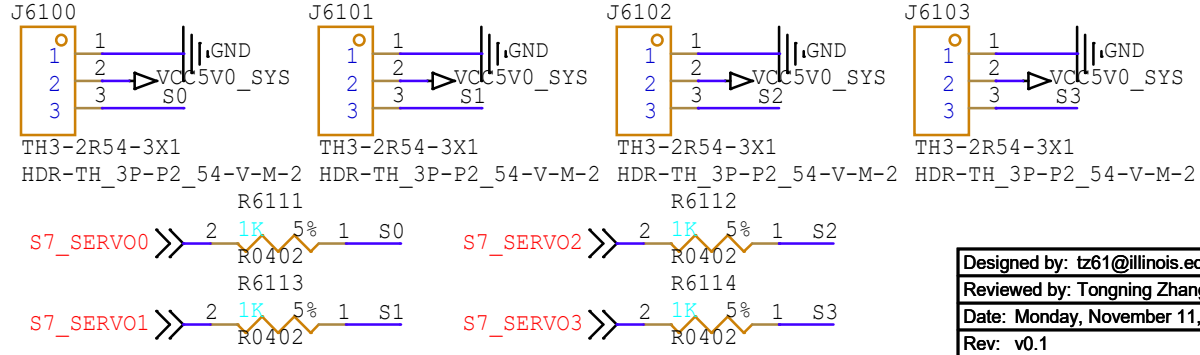
XC7S50 Audio/Buzzer



Audio Power



XC7S50 Servo



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Reviewed by:	Tongning Zhang
Date:	Monday, November 11, 2024
Rev:	v0.1
Sheet:	18 of 25
File:	XC7S50Main
Project:	61.S7_Audio/Buzzer/Servos

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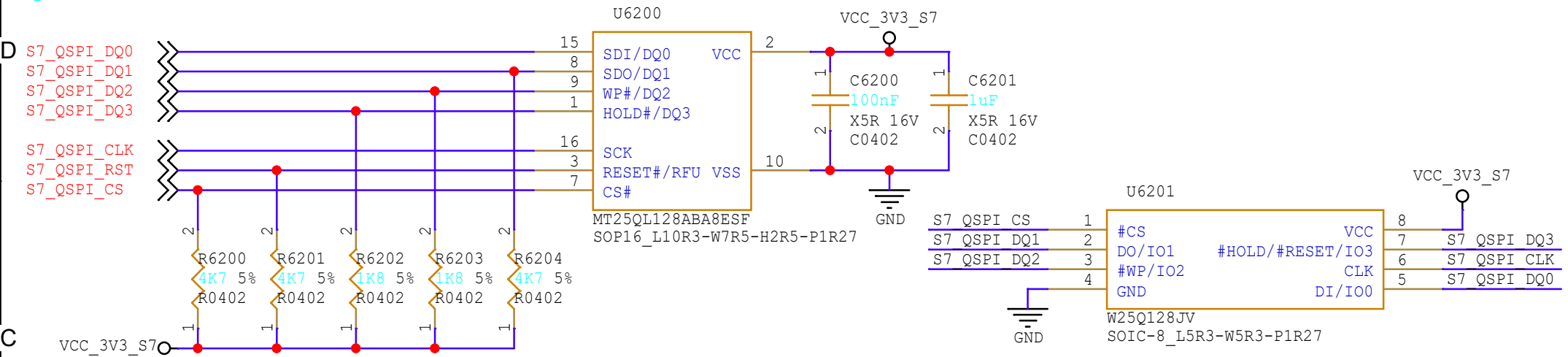
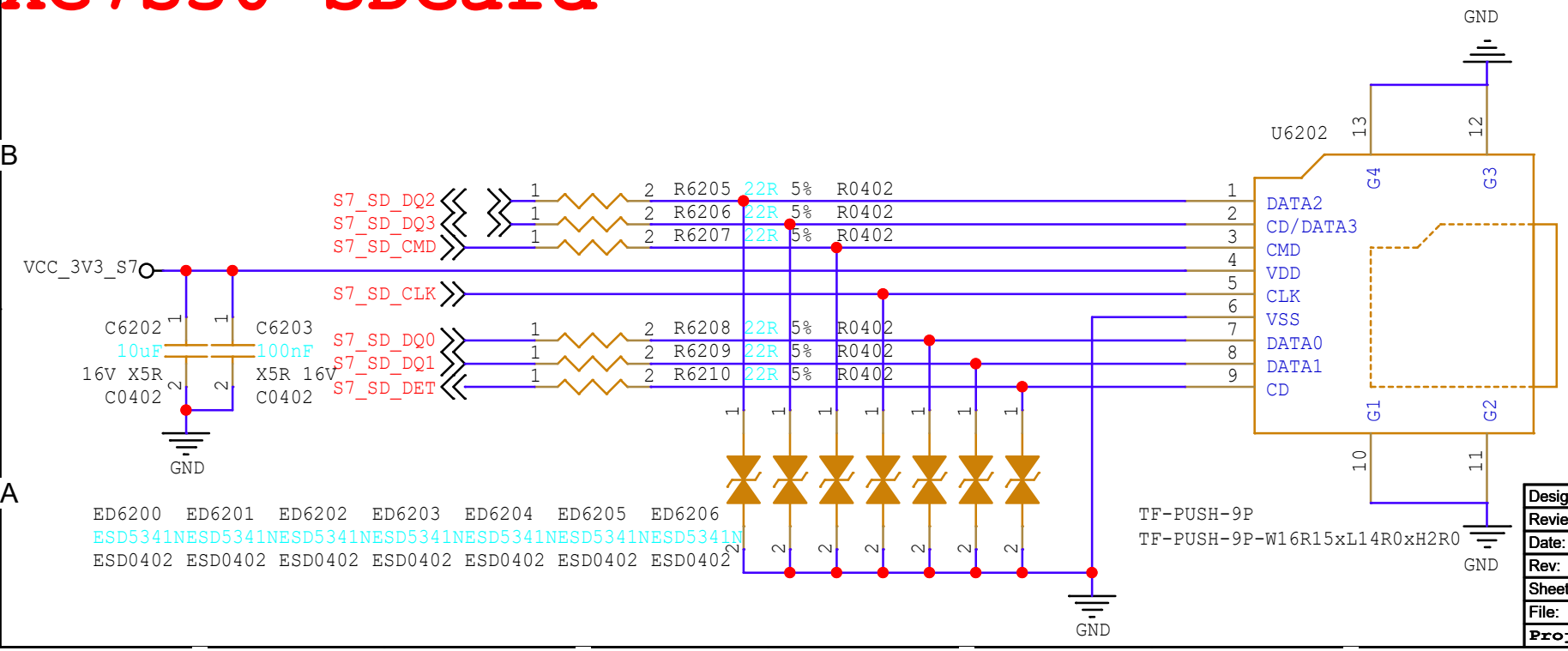
XC7S50 QSPI Flash

Option 1:Micron
Option 2:Winbond



Note:
In design from zynq_mini, only CS is pulled up using 4K7
in urbana board, DQ2 DQ3 are pulled up withj 1K8, RST is pulled up with 4K7
In NarviS7 DQ1 is also pulled up with 4K7

XC7S50 SDCard



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Date:	Monday, November 11, 2024
Rev:	v0.1
Sheet:	19 of 25
File:	XC7S50Main
Project:	62.S7_FLASH

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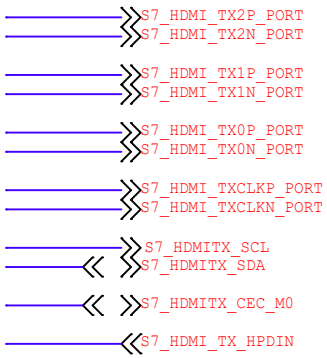
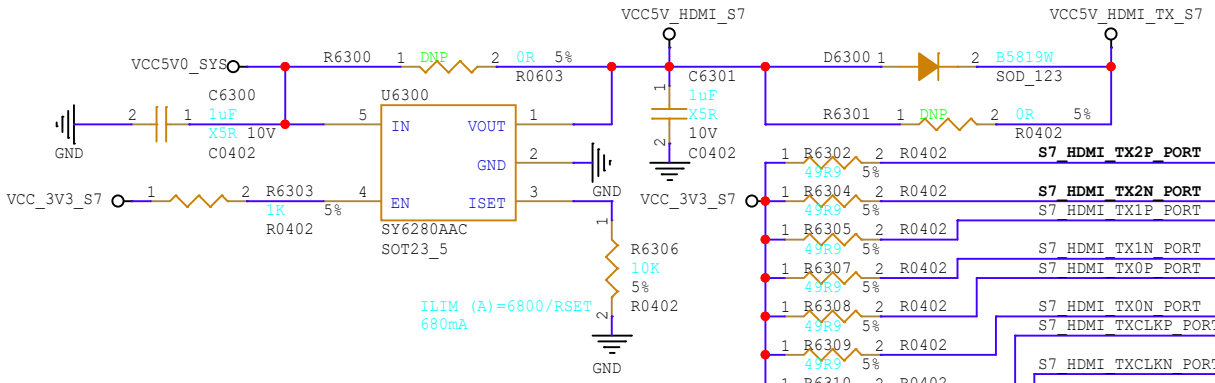
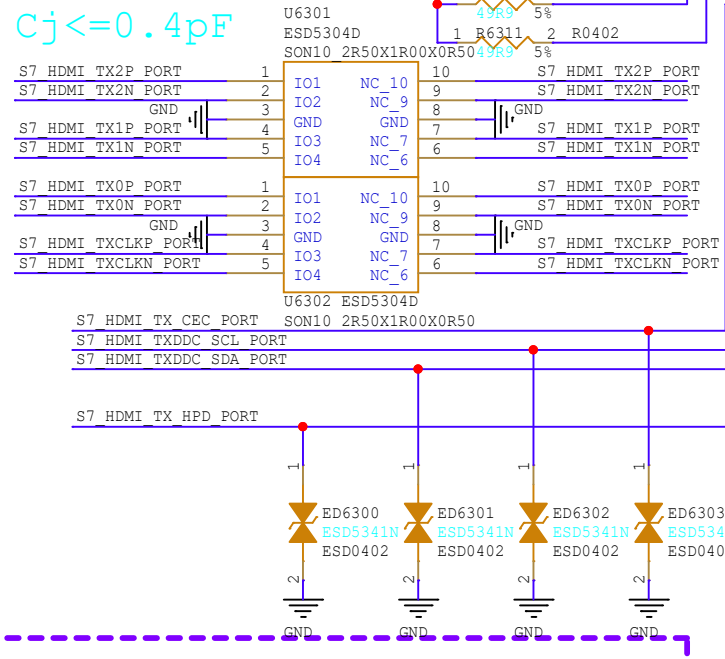
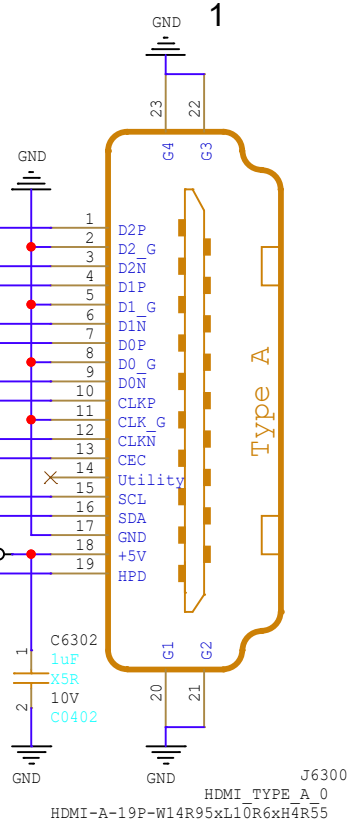
XC7S50 HDMI TX



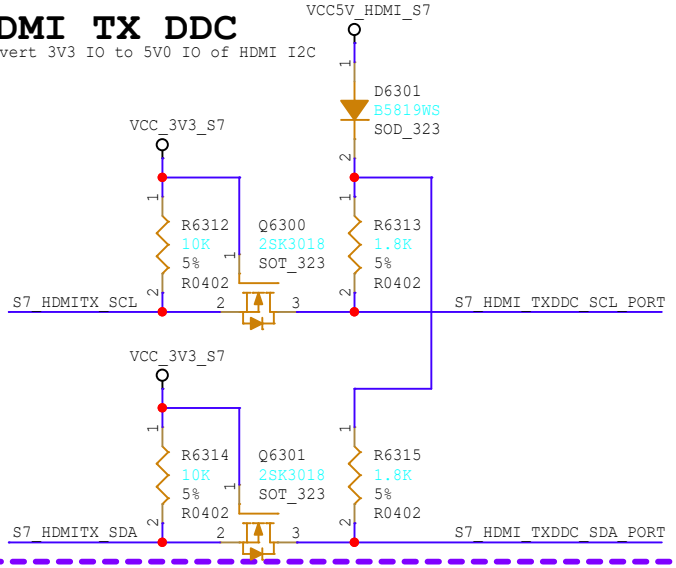






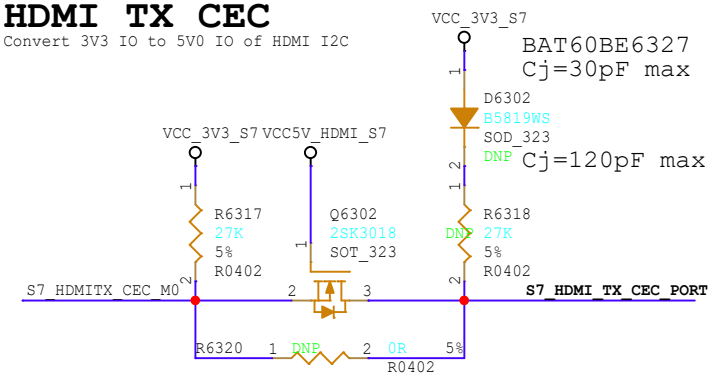
HDMI TX DDC

Convert 3V3 IO to 5V0 IO of HDMI I2C

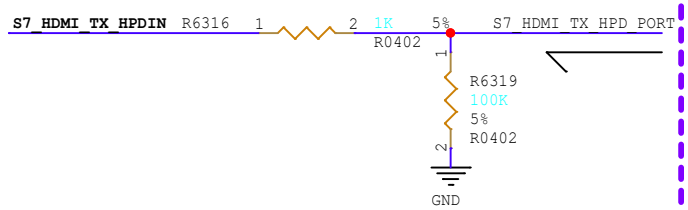


HDMI TX CEC

Convert 3V3 IO to 5V0 IO of HDMI I2C



HDMI TX HPD



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Reviewed by: Tongning Zhang	
Date: Monday, November 11, 2024	
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Project:63.S7_HDMI_TX	

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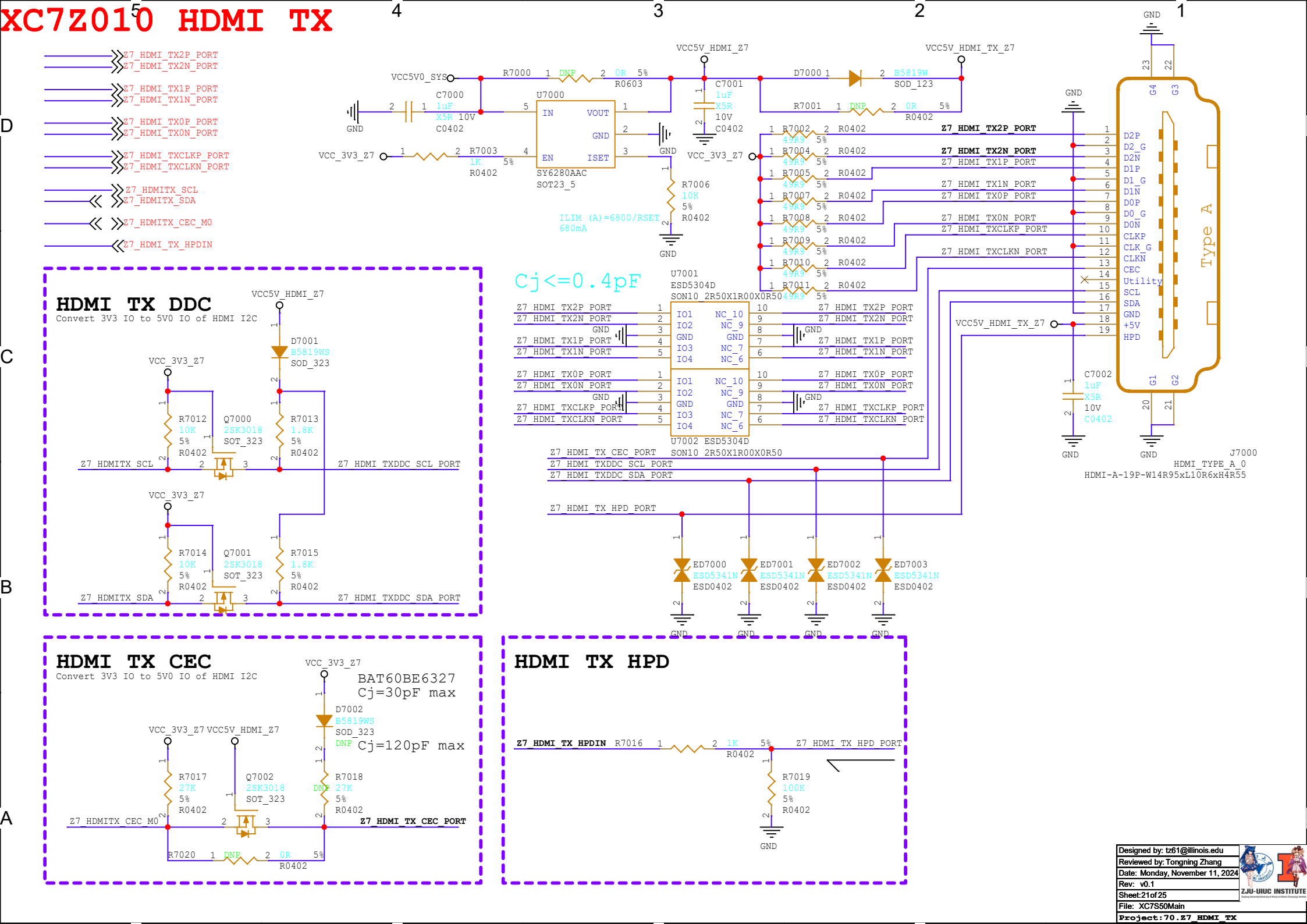
XC7Z010 HDMI TX



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Project:70.Z7_HDMI_TX	

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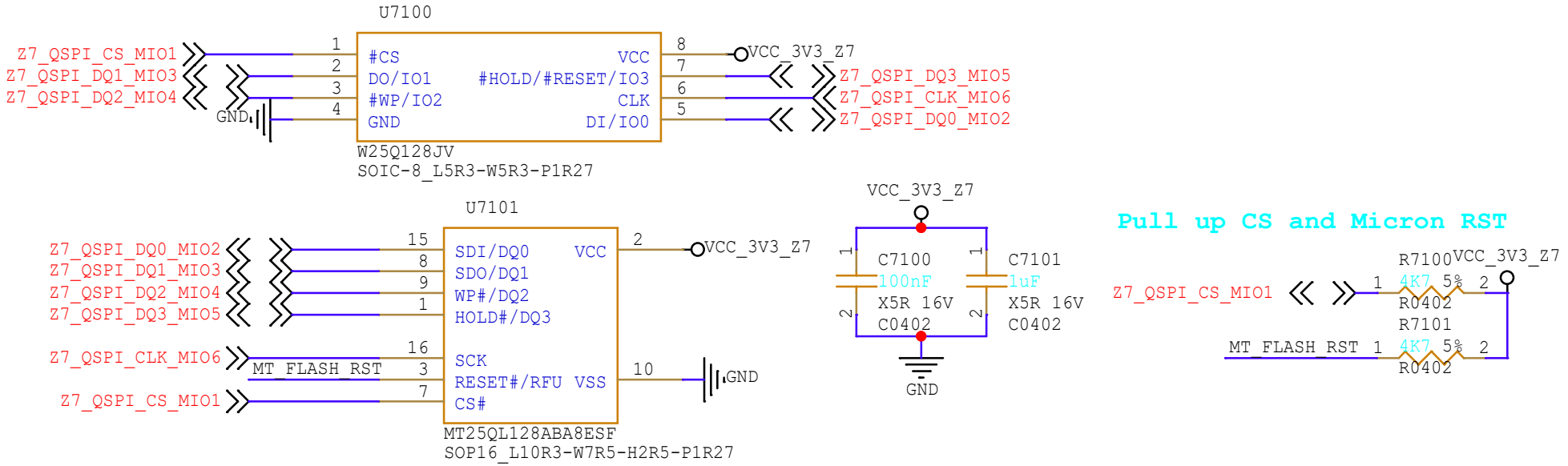
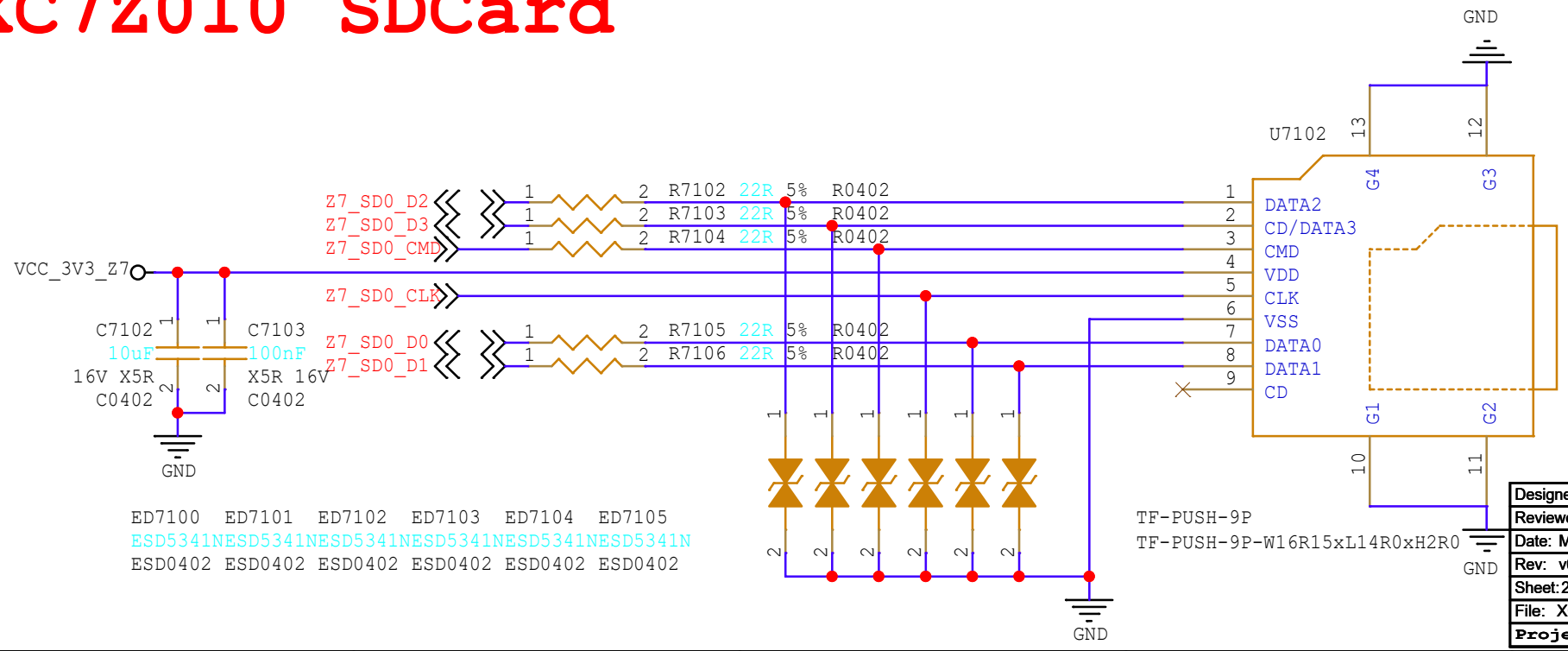
XC7Z010 QSPI Flash

Option 1:Micron
Option 2:Winbond



XC7Z010 SDCard



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File:	XC7S50Main
Project:	71.Z7_FLASH

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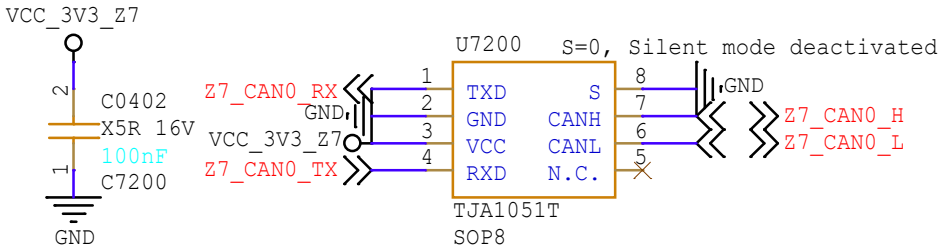
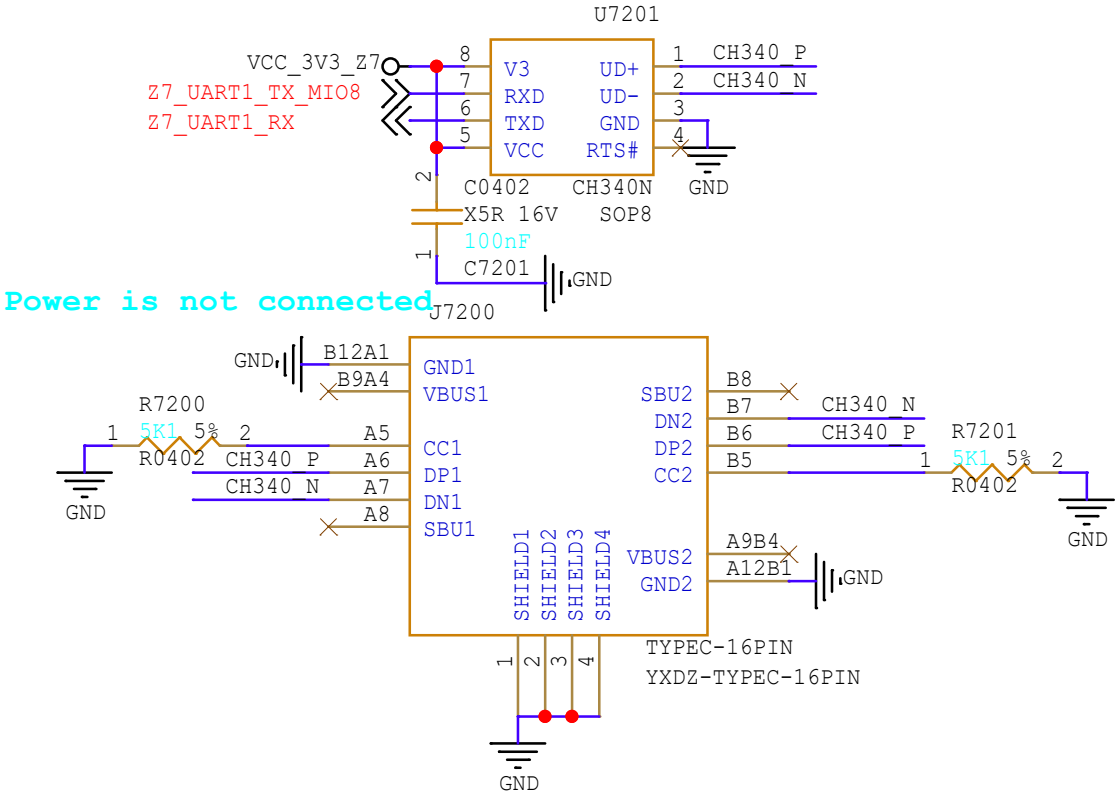
XC7Z010_CAN0



XC7Z010_UART1&Conn



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File:	XC7S50Main
Project:	72.Z7_CAN0/UART1/SPI1

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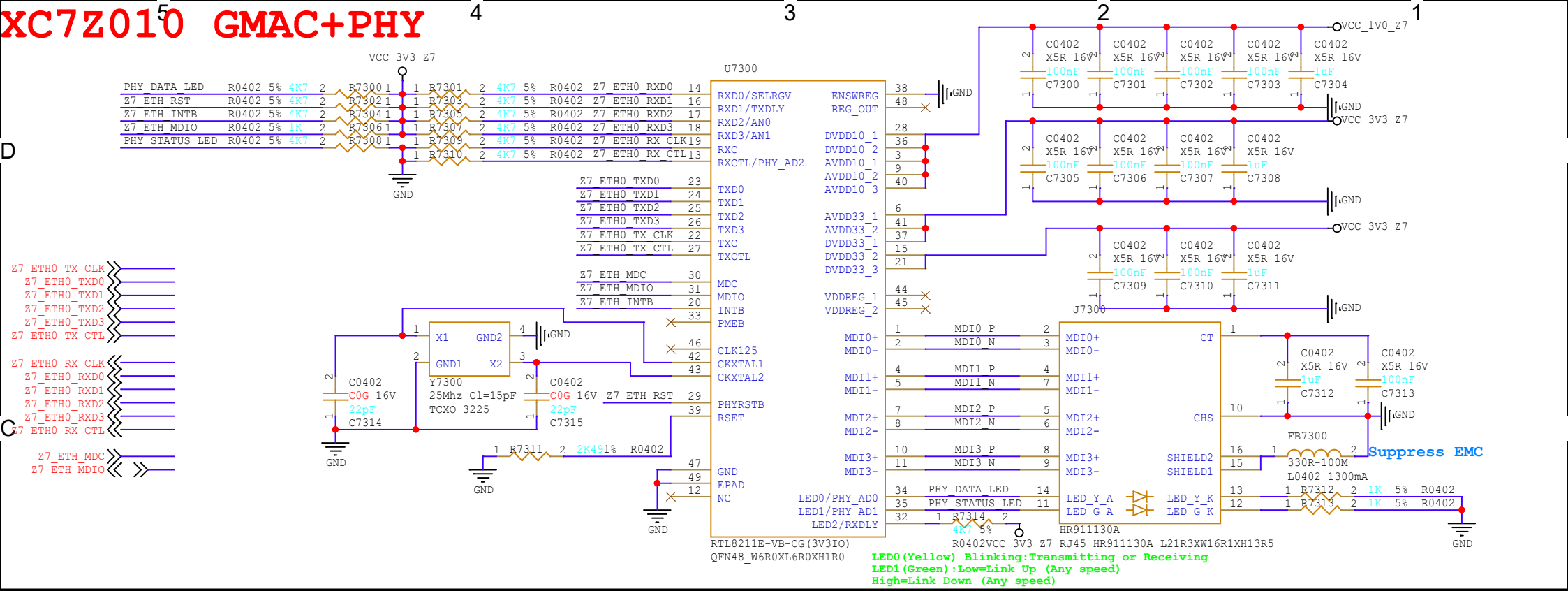
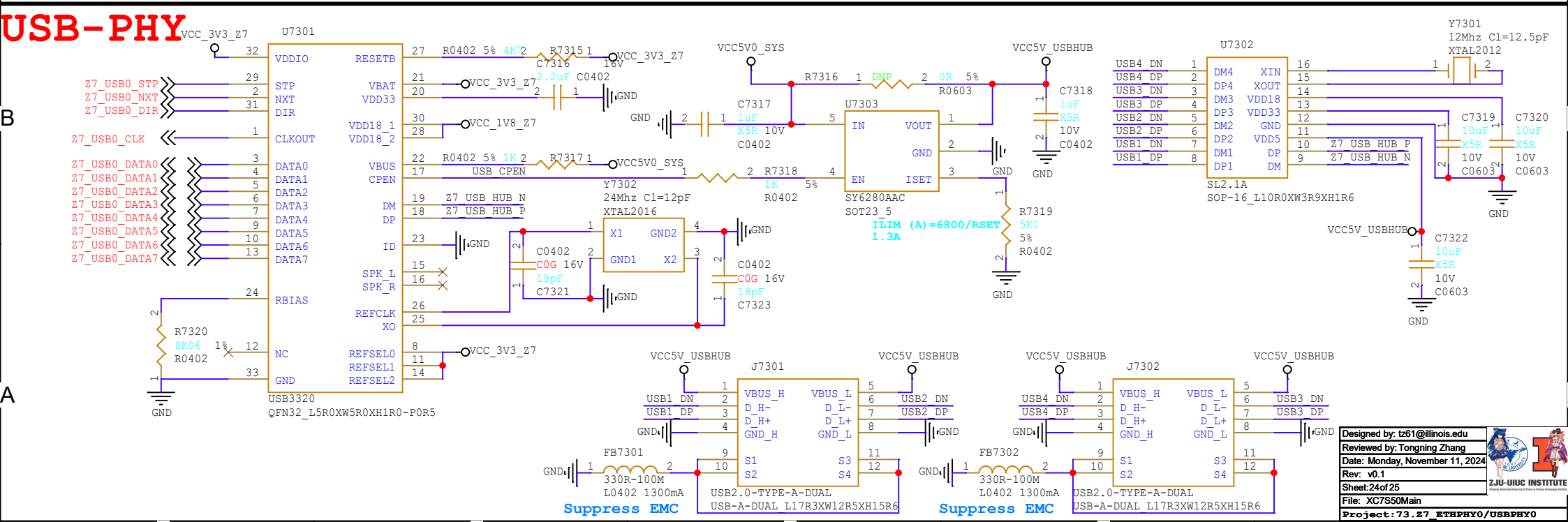
XC7Z010 GMAC+PHY



USB-PHY



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File:	XC7S50Main
Project:	73.Z7_ETHPHY0/USBPHY0

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Overall Keys/LED/Switches/PMODs

Boot SEL&JTAG Path SEL

When MIO is switched to open, connect to GND

SW8001 — 76SB08T

When you press the button to the left JTAG connects to S7
When you press the button to the right JTAG connects to Z7

SW8000 — 76SC04T

No connection to power otherwise causing damage to urbana board

CN8000 — TH30-2R54-15x2
HDR-TH_30P-P2R54-V-M-R2-C15

J8000 — 12P-2x6-2.54
HDR-TH_12P-P2r54-V-M-R2-C6-S2

ED8000 ED8001 ED8002 ED8003 ED8004 ED8005 ED8006 ED8007 ED8008 ED8009 ED8010 ED8011 ED8012 ED8013 ED8014 ED8015 ED8016 ED8017 ED8018 ED8019 ED8020 ED8021
ESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341NESD5341N
ESD0402 ESD0402

D8000 MV5X164 MV5X164
D8001 MV5X164 MV5X164

DISP8000 — 7SEG-4DIGIT-DISP_CA
4D-7SEG_L30R0XW14R0XH7R2-P2R54

DISP8001 — 7SEG-4DIGIT-DISP_CA
4D-7SEG_L30R0XW14R0XH7R2-P2R54

SW8002 SW8003 SW8004 SW8005 — BTN4P PTS815

SW8006 SW8007 — 76SB08T

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Project: 80.Key/LED/Switches/PMOD	

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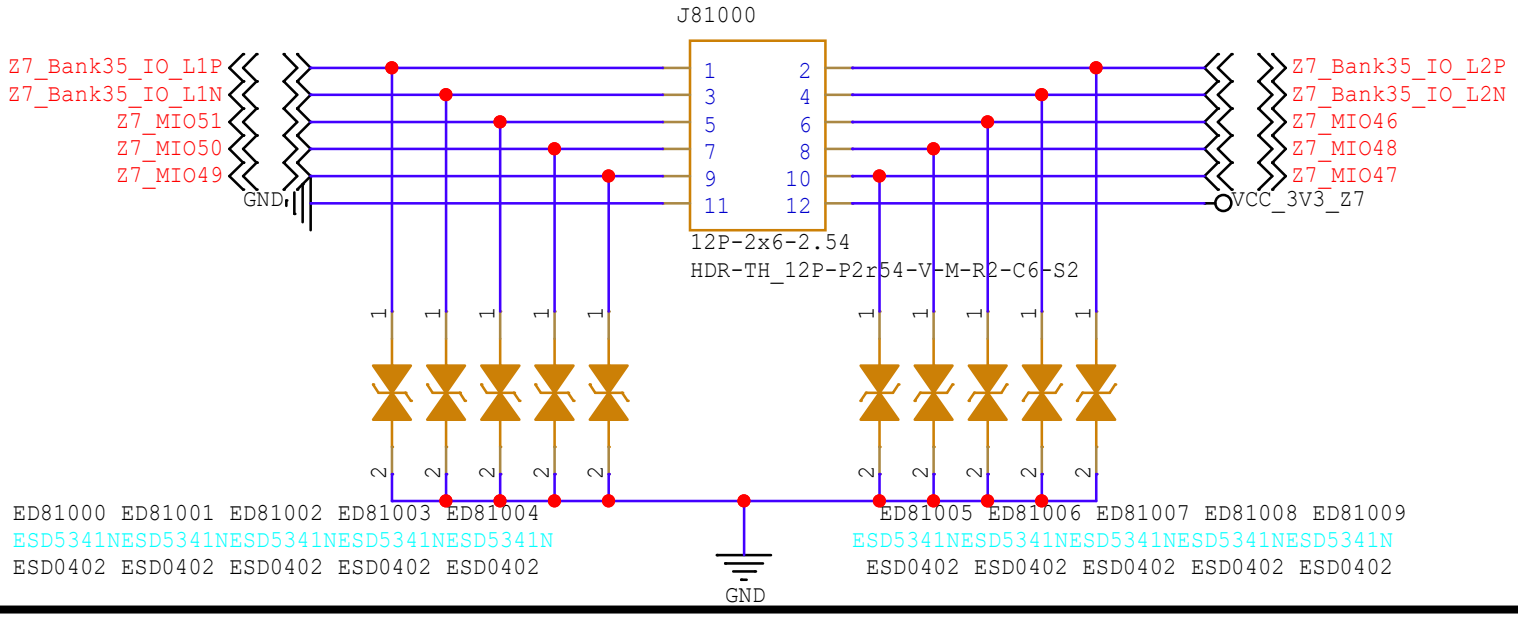
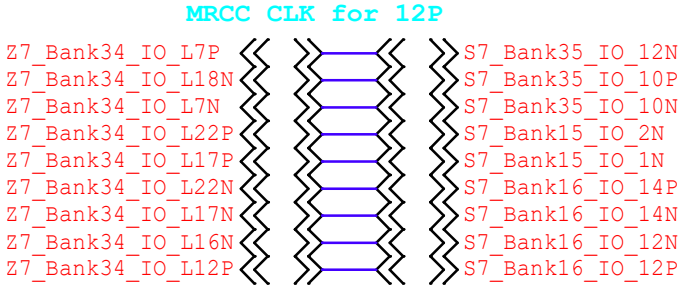
XC7Z010 IO Extension



XC7S50-XC7Z010-Interconnection



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Reviewed by: Tongning Zhang	
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Project: 81.IO_Ext	

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