18650 Battery Capacity Tester

Design Summary Document

Overview

This circuit tests 18650 lithium cell capacity by charging and discharging through a known load while measuring voltage over time. It supports automated multi-cycle testing with USB power connected continuously. The design uses software-controlled switching to isolate the charger during discharge cycles.

Microcontroller

Heltec WiFi Kit 32 V3 (ESP32-S3 based) with integrated 0.96" OLED display. Powered via USB-C at 5V. The onboard display eliminates external display wiring.

GPIO Assignments

GPIO	Function	Direction	Description
GPIO2	V_SENSE	Input (ADC)	Battery voltage via divider (ADC1_CH1)
GPIO6	CHRG_STAT	Input	TP4056 charge status (LOW = complete)
GPIO7	CHARGE	Output	Enable charging (HIGH = charge ON)
GPIO8	DISCHARGE	Output	Enable discharge (HIGH = load ON)

Charge Switch Circuit

A P-channel MOSFET (Q1: IRF9540) isolates the TP4056 charger output from the battery during discharge. Since the P-FET source connects to the charger output (~4V), a level-shifting circuit is required to drive the gate from the 3.3V MCU GPIO.

Circuit operation:

• R4 (10k) pulls Q1 gate to source, keeping Q1 OFF by default
• Q3 (2N2222 NPN) pulls Q1 gate to ground when activated
• R5 (1k) limits current through Q3 collector
• R6 (1k) limits base current to Q3 from GPIO7
• When GPIO7=HIGH: Q3 ON → Q1 gate LOW → Q1 conducts → charger connected
• When GPIO7=LOW: Q3 OFF → R4 pulls Q1 gate HIGH → Q1 OFF → charger isolated

Discharge Circuit

An N-channel logic-level MOSFET (Q2: IRLZ44N) switches the discharge load. The IRLZ44N has a low gate threshold (~2V) allowing direct drive from 3.3V GPIO. R3 (100Ω) limits gate current and reduces ringing.

Load resistor: 4Ω 10W power resistor. At 4.2V this draws ~1.05A, dropping to ~0.75A at 3.0V cutoff. Average current estimate: 0.9A for capacity calculations.

Voltage Sensing

A resistor divider (R1=10k, R2=10k) scales battery voltage to safe ADC range:

- Vout = Vin / 2
- Full charge (4.2V) → 2.1V at ADC
- Cutoff (3.0V) → 1.5V at ADC
- ESP32-S3 ADC is 12-bit with ~3.1V reference

Battery Charger

TP4056 module with integrated protection circuit. Charges at 1A constant current, then tapers to constant voltage (4.2V). CHRG pin indicates status: HIGH during charge, LOW when complete. The protection circuit prevents over-discharge and short circuit.

Bill of Materials

Ref	Value	Description
U1	TP4056 module	1A Li-ion charger with protection
Q1	IRF9540	P-channel MOSFET, TO-220
Q2	IRLZ44N	N-channel logic-level MOSFET, TO-220
Q3	2N2222	NPN transistor, TO-92
R1	10kΩ	Voltage divider upper
R2	10kΩ	Voltage divider lower
R3	100Ω	Q2 gate resistor
R4	10kΩ	Q1 gate pull-up
R5	1kΩ	Q3 collector resistor
R6	1kΩ	Q3 base resistor
R_LOAD	4Ω 10W	Discharge load, wirewound
BT1	18650 holder	Single cell holder with leads

Schematic Net Labels

The schematic is split into two sheets connected by net labels:

Net Label	Description
+5V	USB 5V power rail
CHARGE	Charge enable signal from GPIO7
CHRG_STAT	Charge status from TP4056 to GPIO6
V_SENSE	Divided battery voltage to GPIO2
DISCHARGE	Discharge enable signal from GPIO8

Operating Modes

Mode	GPIO7	GPIO8	Q1 State	Q2 State	Result
Charge	HIGH	LOW	ON	OFF	Charger → Battery
Discharge	LOW	HIGH	OFF	ON	Battery → Load
Idle	LOW	LOW	OFF	OFF	Battery isolated

Auto-Cycle Test Algorithm

1. Insert battery, USB remains connected throughout
2. Set CHARGE mode (GPIO7=HIGH, GPIO8=LOW)
3. Wait for CHRG_STAT to go LOW (charge complete)
4. Optional: rest period (30-60 minutes) for accurate OCV
5. Set DISCHARGE mode (GPIO7=LOW, GPIO8=HIGH)
6. Sample voltage periodically, accumulate mAh (estimated current × time)
7. Stop when voltage drops below 3.0V cutoff
8. Record cycle capacity
9. Repeat from step 2 for N cycles
10. Report average capacity and per-cycle data

Capacity Calculation (Simplified)

Without a current sensor, capacity is estimated using the known load resistance:

- I = V / R (instantaneous current)
- With 4Ω load: I ranges from 1.05A (at 4.2V) to 0.75A (at 3.0V)
- For simplicity, use average current estimate of 0.9A
- Capacity (mAh) = 900mA × discharge_time_hours
- Expected accuracy: ±15-20% (sufficient to identify fake cells)

Design Notes

• The IRLZ44N was chosen because it's logic-level (low Vgs threshold) and commonly available
• The IRF9540 P-channel requires the NPN level shifter because its gate must be pulled to near-source voltage to turn off
• 10W load resistor rating provides margin (max dissipation ~4.4W at 4.2V)
• TP4056 module includes DW01 protection IC - handles over-discharge if software fails
• Ground symbols used locally rather than connected rails for schematic clarity
• Net labels allow schematic to be split across multiple sheets