VE320 Introduction to Semiconductor Physics and Devices

Recitation Class

VE320 Teaching Group SU2022

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Contents

Subthreshold Conduction

- For NMOS, ideally we assume $I_D = 0$ when $V_{GS} < V_T$.
- Experimentally, there is subthreshold current.

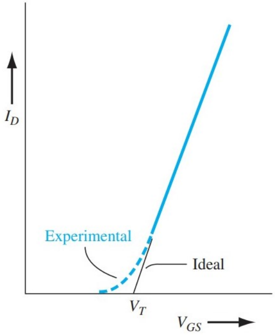


Figure: Comparison of ideal and experimental plots of $\sqrt{I_D}$ versus V_{GS}. Assume saturation region.

Subthreshold Conduction

- Under weak inversion ($\phi_{fp} < \phi_s < 2\phi_{fp}$), E_F is closer to E_C.
- The semiconductor surface develops a lightly doped n-type material.

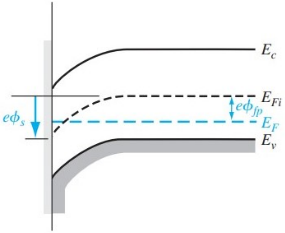


Figure: Energy-band diagram when $\phi_{fp} < \phi_s < 2\phi_{fp}$.

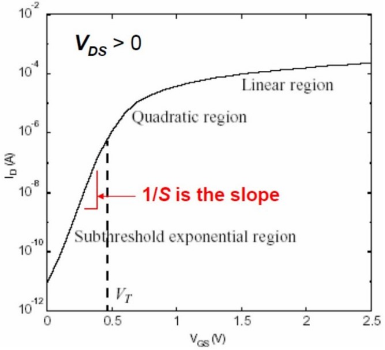
Subthreshold Conduction

- There is a potential barrier between the n source and channel region which the electrons must overcome to generate current.
- $I_D(\text{sub}) \propto \left[\exp\left(\frac{eV_{GS}}{kT}\right)\right] \cdot \left[1 - \exp\left(\frac{-eV_{DS}}{kT}\right)\right]$
- If V_{DS} is larger than a few (kT/e) volts, the subthreshold current is independent of V_{DS}.
- When $V_{GS} < V_T$, $I_D(\text{sub}) \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$, where n (an experimental factor) is ideally 1.

Figure: Energy-band diagrams along channel length at weak inversion.

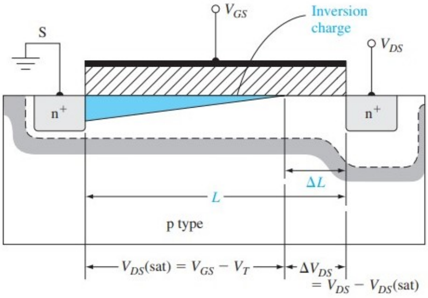
Subthreshold Conduction

- Slope Factor (S): the inverse slope of the $\log(I_D)$ vs. V_{GS} characteristic in the subthreshold region.
- $S = n\left(\frac{kT}{q}\ln(10)\right)$ (volts per decade)
- At room temperature, $\frac{kT}{q}\ln(10) = 60\text{mV}$.



Channel Length Modulation

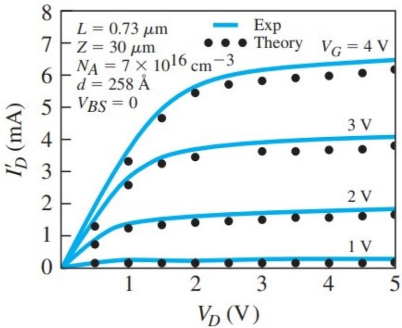
- We assume that the channel length L was a constant.
- However, in the saturation region, the depletion region at the drain extends into the channel.
- The effective channel length is reduced.



Channel Length Modulation

- I_D increases with decreasing L.
- $I'_D = \frac{L}{L - \Delta L} I_D$
- For saturation region, we have increasing current.
- For NMOS: $I_D = \mu_n C_{ox} \frac{W}{2L} \left[(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \right]$, λ is the channel length modulation parameter.
- For PMOS: the same, but with μ_p and I_{SD}, λ is negative.

Channel Length Modulation



- $I'_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \right]$
- Output resistance: $r_o = \left(\frac{\partial I'_D}{\partial V_{DS}} \right)^{-1} = \left\{ \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot \lambda \right\}^{-1}$
- Since λ is normally small, $r_o \cong \frac{1}{\lambda I_D}$.

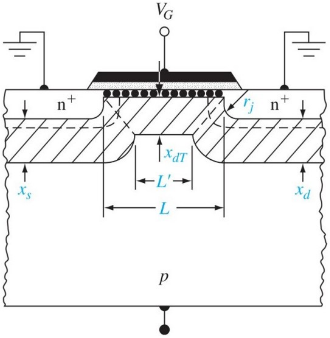
Velocity Saturation

- When electric field increases, carrier velocity will saturate, especially in short-channel devices.
- With velocity saturation first, pinch-off can still happen if continuing increasing V_{DS}.
- With pinch-off happening first, there will not be velocity saturation since the voltage across the effective channel length will be constant.

$$I_{DSAT} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{1}{2} V_{DSAT} \right) V_{DSAT}$$

Short Channel Effect

- In long channel devices, the depletion regions of source and drain are very small parts of the entire channel.
- In short channel devices, the depletion region of the drain reduces the channel length effectively.



Short Channel Effect

- For NMOS, as the channel length decreases, the threshold voltage shifts in the negative direction.
- For PMOS, as the channel length decreases, the threshold voltage shifts in the positive direction.
- The both move towards depletion mode.

NMOS

- Determine V_T, and sometimes consider substrate bias effects.
- When $V_{GS} < V_T$, $I_{DS} = 0$ or consider subthreshold current.
- Determine the minimum of velocity saturation voltage V_{DSAT} and pinch off voltage $V_{GS} - V_T$. Denote as V_{SAT}.
- If $V_{DS} < V_{SAT}$, $I_{DS} = \frac{W\mu_n C_{ox}}{2L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right]$.
- If $V_{DS} > V_{SAT}$, $I_{DS,\text{ideal}} = \mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_T - \frac{1}{2}V_{SAT}\right)V_{SAT}$. If it is in pinch off region and we consider channel length modulation (remember even with velocity saturation, we can still reach pinch off), $I_{DS} = I_{DS,\text{ideal}}(1 + \lambda V_{DS})$.

PMOS

- Determine V_T, and sometimes consider substrate bias effects. Remember that for an enhancement mode PMOS, $V_T < 0$.
- When $V_{GS} > V_T$, $I_{SD} = 0$ or consider subthreshold current.
- Determine the minimum of velocity saturation voltage V_{DSAT} and pinch off voltage $V_{SG} + V_T$. Denote as V_{SAT}. The both are positive values.
- If $V_{SD} < V_{SAT}$, $I_{SD} = \frac{W\mu_p C_{ox}}{2L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right]$ or $I_{SD} = \frac{W\mu_p C_{ox}}{2L}[2(V_{SG} + V_T)V_{SD} - V_{SD}^2] > 0$.
- If $V_{SD} > V_{SAT}$, $I_{SD,\text{ideal}} = \mu_p C_{ox}\frac{W}{L}\left(V_{SG} + V_T - \frac{1}{2}V_{SAT}\right)V_{SAT}$. If it is in pinch off region and we consider channel length modulation (remember even with velocity saturation, we can still reach pinch off), $I_{SD} = I_{SD,\text{ideal}}(1 + |\lambda V_{SD}|)$.

Example

Consider an n-channel silicon MOSFET. The parameters are $k_n' = 75\mu\mathrm{A}/\mathrm{V}^2$, $W/L = 10$, and $V_T = 0.35\ \mathrm{V}$. The applied drain-to-source voltage is $V_{DS} = 1.5\ \mathrm{V}$. (a) For $V_{GS} = 0.8\ \mathrm{V}$, find (i) the ideal drain current, (ii) the drain current if $\lambda = 0.02\ \mathrm{V}^{-1}$, and (iii) the output resistance for $\lambda = 0.02\ \mathrm{V}^{-1}$. (b) Repeat part (a) for $V_{GS} = 1.25\ \mathrm{V}$.

Solution

(a) (i) $I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \left(V_{GS} - V_T\right)^2 = \left(\frac{0.075}{2}\right)(10)(0.8 - 0.35)^2 = 0.07594 \text{ mA} = 75.94\mu\text{A}$

(ii) $I_D' = I_D \left(1 + \lambda V_{DS}\right) = (75.9375)[1 + (0.02)(1.5)] = 78.22\mu\text{A}$

(iii) $r_o = \frac{1}{\lambda I_D} = \frac{1}{(0.02)(75.94)} = 0.658\text{M}\Omega = 658\text{k}\Omega$

(b) (i) $I_D = \left(\frac{0.075}{2}\right)(10)(1.25 - 0.35)^2 = 0.30375 \text{ mA}$

(ii) $I_D' = (0.30375)[1 + (0.02)(1.5)] = 0.3129 \text{ mA}$

(iii) $r_o = \frac{1}{(0.02)(0.30375)} = 165\text{k}\Omega$

Questions?