VE320 Intro to Semiconductor Devices Chapter 10

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UM-SJTU Joint Institute

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- The Two-terminal MOS Structure
 - Energy-Band Diagrams
 - Depletion Layer Thickness
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- Capacitance-Voltage Characteristics
- The Basic MOSFET Operation
 - MOSFET Structure
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 - Substrate Bias Effects
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Basic Structure

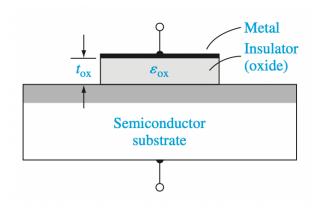


Figure: The basic MOS capacitor structure

NMOS: P-type substrate, N-type channel

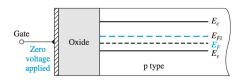


Figure: Energy-band diagram for ideal case (zero gate voltage)

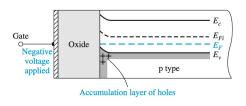


Figure: Energy-band diagram for a negative gate bias (accumulation mode)

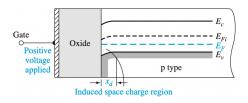


Figure: Energy-band diagram for a moderate positive gate bias (depletion mode)

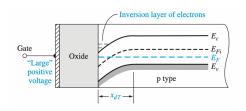


Figure: Energy-band diagram for a large positive gate bias (inversion mode)

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PMOS: N-type substrate, P-type channel

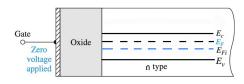


Figure: Energy-band diagram for ideal case (zero gate voltage)

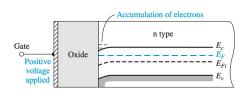


Figure: Energy-band diagram for a positive gate bias (accumulation mode)

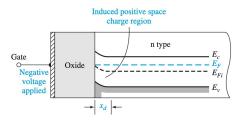


Figure: Energy-band diagram for a moderate negative gate bias (depletion mode)

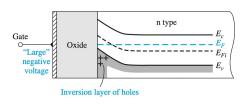


Figure: Energy-band diagram for a large negative gate bias (inversion mode)

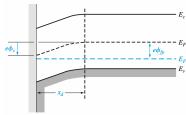
Depletion Layer Thickness

- Surface potential ϕ_s : the difference (in V) between E_{Fi} measured in the semiconductor and E_{Fi} measured at the surface
- ullet Potential difference ϕ_{fp} : the difference (in V) between E_{Fi} and E_{F}

$$\phi_{fp} = V_t \ln \left(\frac{N_a}{n_i} \right)$$

Space charge width x_d:

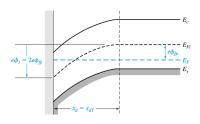
$$x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a}\right)^{1/2}$$



Depletion Layer Thickness

- Threshold inversion point: for p-type semiconductor, the electron concentration at the surface equals to the hole concentration in the semiconductor
- Maximum space charge width x_{dT} :

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a}\right)^{1/2}$$



Quiz

- Could you write the formulas for PMOS (N-type semiconductor)?
 - \bullet ϕ_{fn} :
 - X_d:
 - X_{dT}:



Work Function Difference

- Modified metal work function $\phi_{\it m}^{'}$
- Modified electron affinity χ'
- ullet Potential drop across the oxide for zero applied gate voltage V_{ox0}
- Surface potential ϕ_{s0}

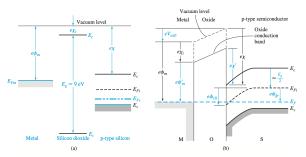


Figure 10.13 | (a) Energy levels in a MOS system prior to contact and (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.

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Work Function Difference

- NMOS: $\phi_{\textit{ms}} = \phi_{\textit{m}}^{'} \left(\chi^{'} + \frac{\textit{E}_{\textit{g}}}{2\textit{e}} + \phi_{\textit{fp}}\right)$
- PMOS: $\phi_{\textit{ms}} = \phi_{\textit{m}}^{'} \left(\chi^{'} + \frac{\textit{E}_{\textit{g}}}{2\textit{e}} \phi_{\textit{fn}}\right)$
- When n^+ polysilicon is used as metal (NMOS): $\phi_{ms} = \left[\chi^{'} \left(\chi^{'} + \frac{E_g}{2e} + \phi_{fp}\right)\right] = -\left(\frac{E_g}{2e} + \phi_{fp}\right)$
- When p^+ polysilicon is used as metal (NMOS): $\phi_{\textit{ms}} = \left[\left(\chi^{'} + \frac{\textit{E}_g}{2\textit{e}} \right) \left(\chi^{'} + \frac{\textit{E}_g}{2\textit{e}} + \phi_{\textit{fp}} \right) \right] = \left(\frac{\textit{E}_g}{2\textit{e}} \phi_{\textit{fp}} \right)$

Flat-Band Voltage

- **Flat-band voltage** V_{FB} : the applied gate voltage such that there is no band bending in the semiconductor
- Fixed charge density in the oxide $Q_{ss}^{'}$
- Charge density on the metal $Q_m^{'}$

$$extstyle V_{FB} = \phi_{ extstyle ms} - rac{ extstyle Q_{ extstyle ss}^{'}}{ extstyle C_{ extstyle ox}}$$

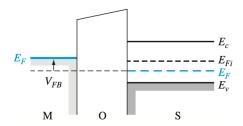


Figure: Energy-band diagram of a MOS capacitor at flat band

Threshold Voltage

- Threshold voltage V_T: the gate voltage needed at the threshold inversion point
- ullet Charge density on the metal at the inversion point $Q_{mT}^{'}$
- Maximum charge density in depletion region $Q'_{SD}(\max)$: $|Q'_{SD}(\max)| = eN_ax_{dT}$
- NMOS:

$$egin{aligned} V_{TN} &= rac{|Q_{SD}^{'}(\mathsf{max})|}{C_{ox}} - rac{Q_{ss}^{'}}{C_{ox}} + \phi_{ms} + 2\phi_{fp} \ V_{TN} &= (|Q_{SD}^{'}(\mathsf{max})| - Q_{ss}^{'}) \left(rac{t_{ox}}{\epsilon_{os}}
ight) + \phi_{ms} + 2\phi_{fp} \ V_{TN} &= rac{|Q_{SD}^{'}(\mathsf{max})|}{C_{ox}} + V_{FB} + 2\phi_{fp} \end{aligned}$$

Threshold Voltage

- PMOS: $|Q'_{SD}(\text{max})| = eN_dx_{dT}$
- PMOS:

$$egin{aligned} V_{TP} &= -rac{|Q_{SD}^{'}(ext{max})|}{C_{ox}} - rac{Q_{ss}^{'}}{C_{ox}} + \phi_{ms} - 2\phi_{fn} \ V_{TP} &= (-|Q_{SD}^{'}(ext{max})| - Q_{ss}^{'}) \left(rac{t_{ox}}{\epsilon_{os}}
ight) + \phi_{ms} - 2\phi_{fn} \ V_{TP} &= -rac{|Q_{SD}^{'}(ext{max})|}{C_{ox}} + V_{FB} - 2\phi_{fn} \end{aligned}$$

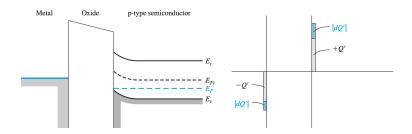


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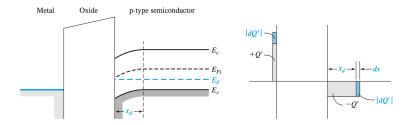
In accumulation mode:

$$C^{'}(\mathsf{acc}) = C_{ox} = rac{\epsilon_{ox}}{t_{ox}}$$



• In depletion mode:

$$C^{'}(\mathsf{depl}) = rac{\epsilon_{\mathit{OX}}}{t_{\mathit{OX}} + \left(rac{\epsilon_{\mathit{OX}}}{\epsilon_{\mathit{S}}}
ight) x_{\mathit{d}}}$$

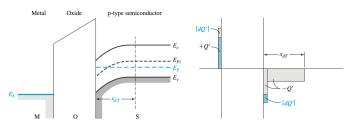


In inversion mode:

$$oldsymbol{C}^{'}(\mathsf{inv}) = oldsymbol{C}_{\mathit{ox}} = rac{\epsilon_{\mathit{ox}}}{t_{\mathit{ox}}}$$

• The minimum capacitance (at threshold inversion point):

$$C'(\min) = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_{s}}\right) x_{dT}}$$



 The flat-band capacitance (between the accumulation mode and the depletion mode):

$$C^{'}(\mathsf{FB}) = rac{\epsilon_{\mathsf{OX}}}{t_{\mathsf{OX}} + \left(rac{\epsilon_{\mathsf{OX}}}{\epsilon_{\mathsf{S}}}
ight)\sqrt{\left(rac{k\mathsf{T}}{e}
ight)\left(rac{\epsilon_{\mathsf{S}}}{e\mathsf{N}_{a}}
ight)}}$$

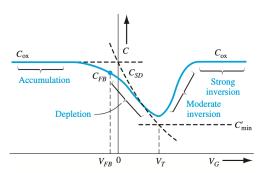


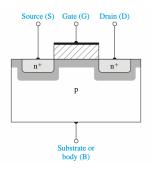
Figure: The low frequency capacitance of NMOS vs the gate voltage

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N-channel MOSFET Structure

- Enhancement mode: the semiconductor substrate is not inverted directly under the oxide with zero gate voltage
- Depletion mode: a channel region exists under the oxide with zero gate voltage



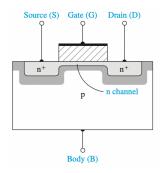
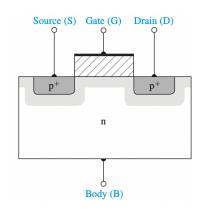


Figure: NMOS enhancement mode

Figure: NMOS depletion mode

P-channel MOSFET Sturcture



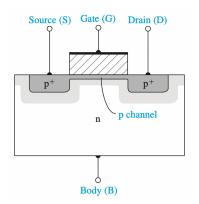
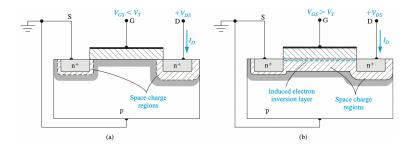


Figure: PMOS enhancement mode

Figure: PMOS depletion mode

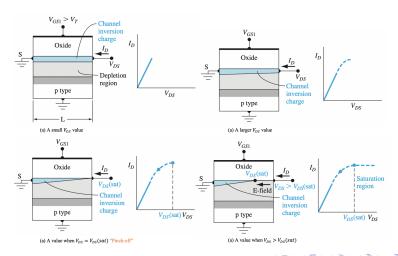
Current-Voltage Relationship

- For NMOS in enhancement mode, when V_{DS} is close to 0
- $V_{GS} < V_T$: no inversion layer, no current
- $V_{GS} > V_T$: inversion layer created, current flow from drain to source



C-V Relationship with Different V_{DS}

• When V_{DS} increases, the inversion charge density around the drain decreases. When $V_{DS} = V_{DS}(\text{sat})$, it reaches "pinch off"



Current-Voltage Relationship

- For NMOS
 - $V_{GS} < V_T$:

$$I_{DS}=0$$

• $V_{GS} > V_T$ and $V_D < V_{GS} - V_T$:

$$I_{DS} = \frac{W \mu_n C_{ox}}{2L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

• $V_{GS} > V_T$ and $V_D \ge V_{GS} - V_T$:

$$I_{DS} = \frac{W\mu_n C_{ox}}{2L} (V_{GS} - V_T)^2$$



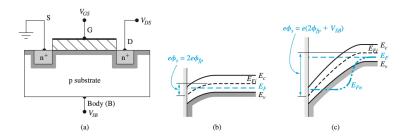
Transconductance

 Transconductance: the change in drain current with respect to the corresponding change in gate voltage

$$g_{m} = \frac{\partial I_{D}}{\partial V_{GS}}$$

$$= \begin{cases} \mu_{n} C_{ox} \frac{W}{L} V_{DS} & 0 < V_{DS} < V_{GS} - V_{T} \\ \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{T}) & V_{DS} > V_{GS} - V_{T} \end{cases}$$

Substrate Bias Effects



- When $V_{SB}=0$: $Q_{SD}^{\prime}(\max)=-\sqrt{2e\epsilon_sN_a(2\phi_{fp})}$
- When $V_{SB}>0$: $Q_{SD}^{'}=-\sqrt{2\it{e}\epsilon_s\it{N}_a(2\phi_{fp}+V_{SB})}$



Substrate Bias Effects

The change in threshold voltage

$$\Delta V_T = V_T (V_{SB} > 0) - V_T (V_{SB} = 0)$$
:

$$\begin{split} \Delta V_T &= -\frac{\Delta Q_{SD}'}{C_{ox}} \\ &= \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right] \\ &= \gamma \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right] \end{split}$$

where $\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}$ is defined as the body-effect coefficient.



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