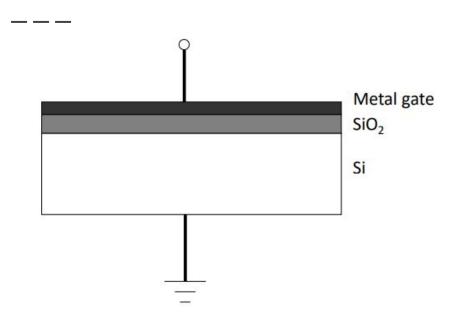
VE320 RC - Charpter 10

louyukun@umich.edu

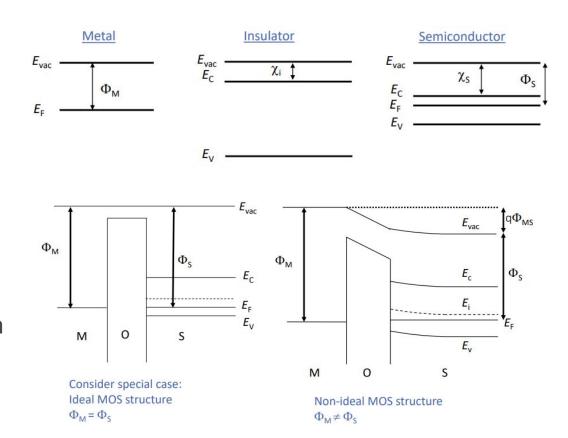
Outline

- MOS Structure
- MOS Capacitance
- MOSFET

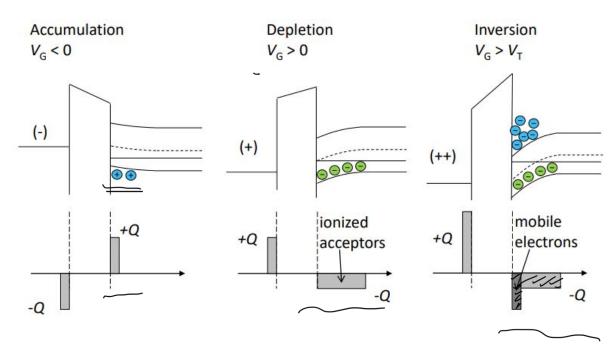


Rules:

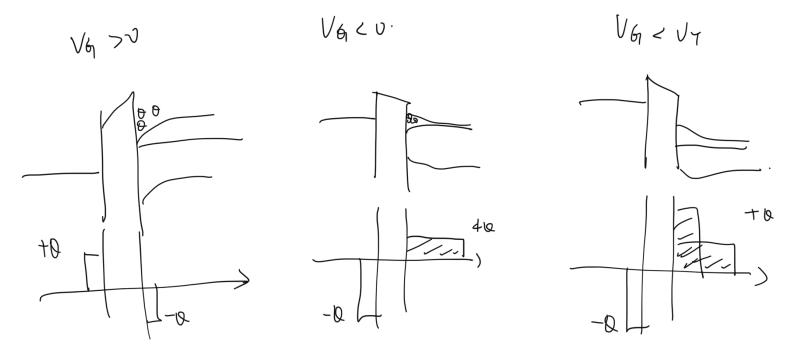
- 1. Constancy of Fermi level in equilibrium
- 2. Continuity of vacuum level across interfaces.
- 3. Equilibrium configuration depends on metal and semiconductor work function



p-type NMOS



n-type PMOS?



Surface Potential:
$$\phi_s = \frac{1}{q} \left[E_{i,bulk} - E_{i,surface} \right]$$

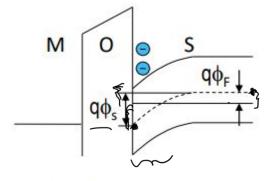
n-type Semiconductor

 ϕ_{F} Potential Difference:

$$\phi_F$$

Space charge width: $x_d = \left(\frac{2\epsilon \left(\phi_s\right)}{eN_c}\right)$

$$x_d = \left(\frac{2\epsilon \phi_s}{eN_a}\right)^{1/2}$$



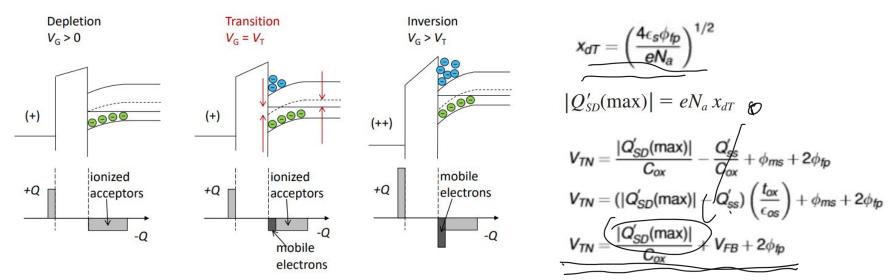
p-type Semiconductor

$$\phi_F = -\frac{kT}{q} ln \left(\frac{N_D}{n_i} \right) \qquad \phi_F = +\frac{kT}{q} ln \left(\frac{N_A}{n_i} \right)$$

Threshold inversion point:

$$\phi_S = 2\phi_F$$

Concentration of electrons at surface = Concentration of holes in bulk



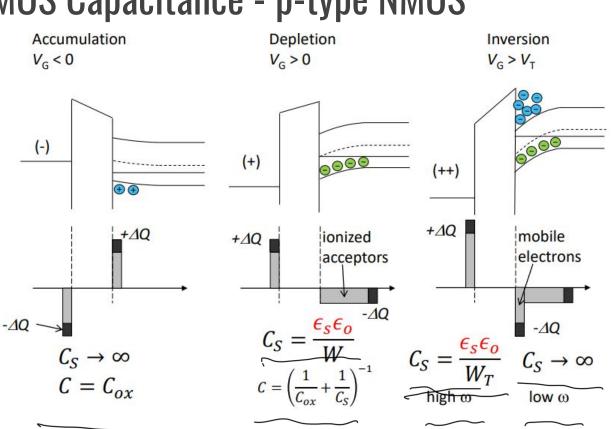
metal-semiconductor work function difference:

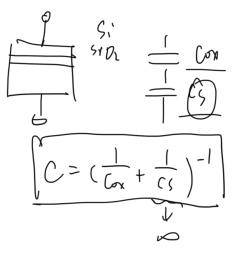
p-type
$$\phi_{ms} \equiv \left[\phi_m' - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$
 n-type $\phi_{ms} = \phi_m' - \left(\chi' + \frac{E_g}{2e} - \phi_{fn}\right)$

$$V_{FB} = \text{Voltage needed for flat energy bands (analogous to Vbi)}$$

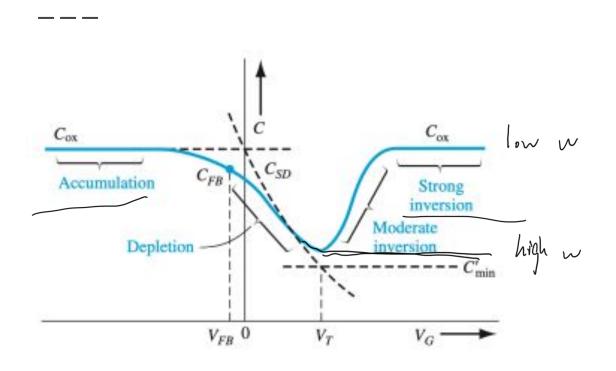
$$V_{FB} = \phi_{ms} - \frac{Q_{ss}'}{C}$$

MOS Capacitance - p-type NMOS



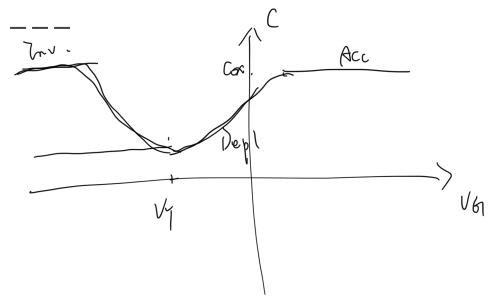


MOS Capacitance - p-type NMOS



$$C'(\mathsf{acc}) = C_{ox} = rac{\epsilon_{ox}}{t_{ox}}$$
 $C'(\mathsf{depl}) = rac{\epsilon_{ox}}{t_{ox} + \left(rac{\epsilon_{ox}}{\epsilon_{s}}
ight) x_{d}}$
 $C'(\mathsf{inv}) = C_{ox} = rac{\epsilon_{ox}}{t_{ox}}$
 $C'(\mathsf{min}) = rac{\epsilon_{ox}}{t_{ox} + \left(rac{\epsilon_{ox}}{\epsilon_{s}}
ight) x_{dT}}$
 $C'(\mathsf{FB}) = rac{\epsilon_{ox}}{\left(\epsilon_{ox}\right) \sqrt{\epsilon_{ox}}}$

MOS Capacitance - n-type PMOS

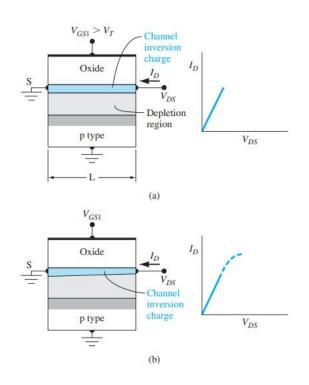


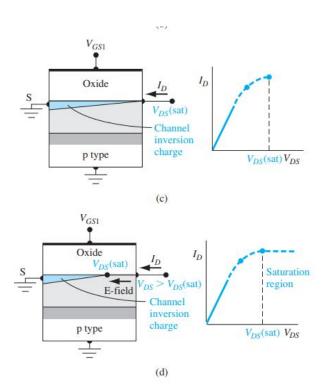
MOSFET

Enhancement mode: the semiconductor substrate is not inverted directly under the oxide with zero gate voltage

Depletion mode: a channel region exists under the oxide with zero gate voltage

MOSFET





When VDS increases, the inversion charge density around the drain decreases.

When VDS = VDS(sat), it reaches "pinch off"

MOSFET

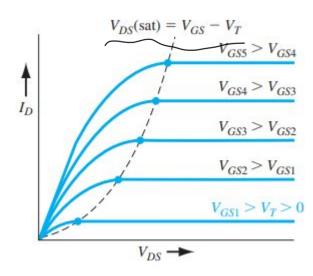
 $V_{GS} < V_T$: $I_{DS} = 0$

 $V_{GS} > V_T$ and $V_D < V_{GS} - V_T$:

$$I_D = \frac{W\mu_n C_{\text{ox}}}{2L} \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2 \right]$$

V_{GS} > V_T and VD ≥ V_{GS} - V_T:

$$I_D = \frac{W\mu_n C_{\text{ox}}}{2L} (V_{GS} - V_T)^2$$



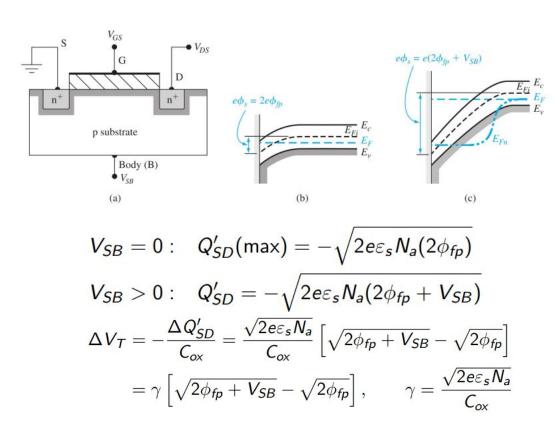
Transconductance

The change in drain current with respect to the corresponding change in gate voltage.

$$g_{m} = \frac{\partial I_{D}}{\partial V_{GS}}$$

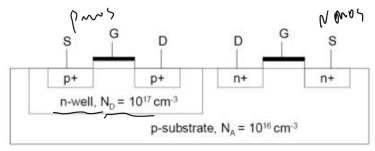
$$= \begin{cases} \mu_{n} C_{ox} \frac{W}{L} V_{DS}, & 0 < V_{DS} < V_{GS} - V_{T} \\ \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{T}), & V_{DS} > V_{GS} - V_{T} \end{cases}$$

Substrate Bias Effects



Practice

Consider the following Si CMOS Transistor. Calculate the threshold voltage for both NMOS and PMOS.



$$x_{ox}$$
 = 40 nm
 ϕ_{ms} = -0.6 V, NMOS
 ϕ_{ms} = -0.4 V, PMOS

Thanks