VE320 – Summer 2021

Semiconductor Physics

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Chapter 10 Fundamentals of Metal-Oxide-Semiconductor Field Effect Transistors

Outline

Outline

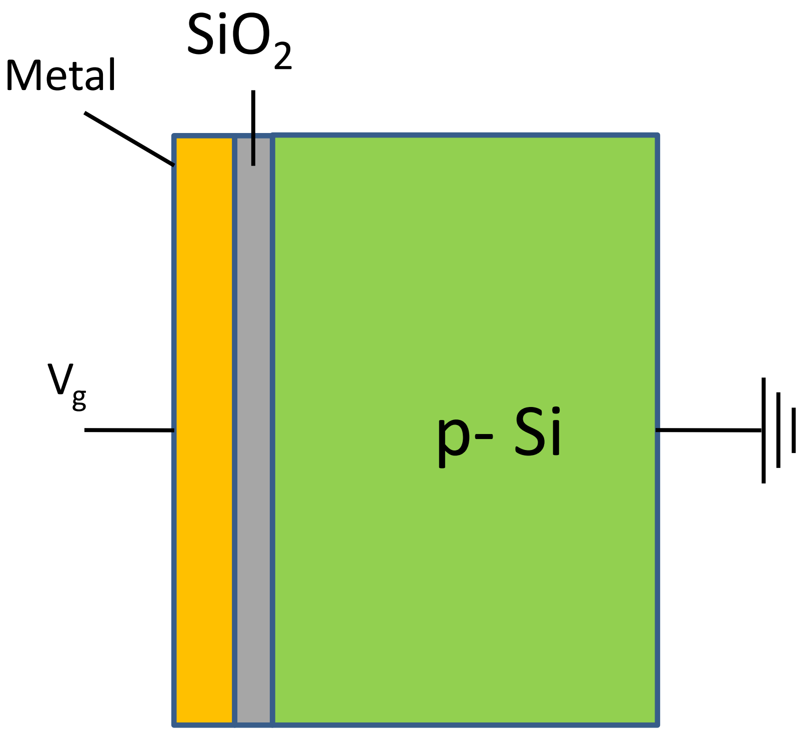
10.1 The two-terminal MOS structure

10.2 Capacitance-voltage characteristics

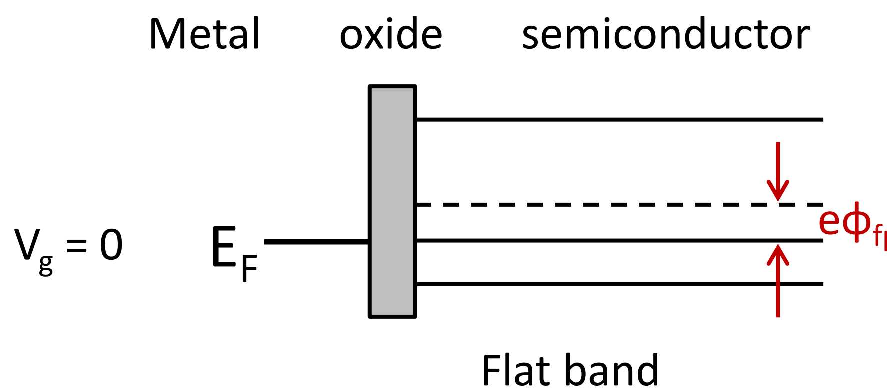
10.3 Non-ideal effects

10.4 The basic MOSFET operation

10.1 The two-terminal MOS structure

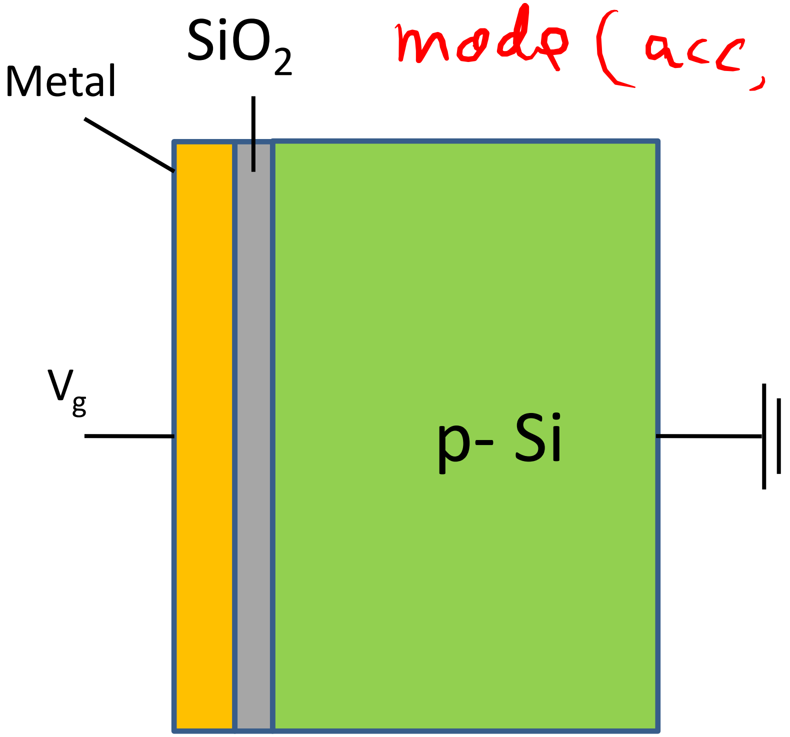


Metal-insulator-semiconductor (MIS)



① energy diagram

mode (acc, dep, w inv, s inv)



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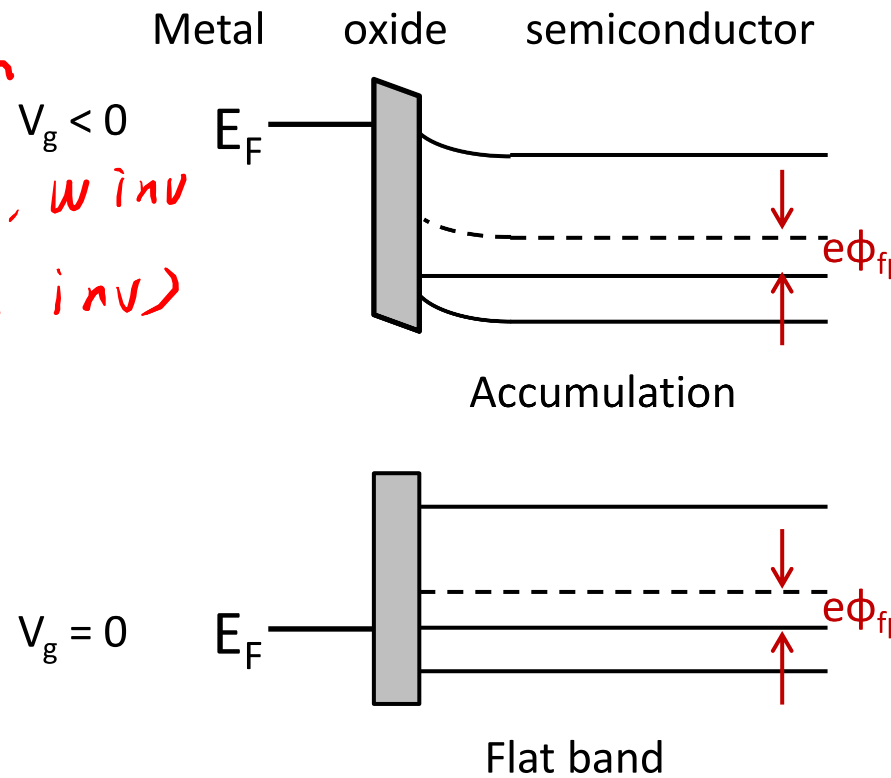
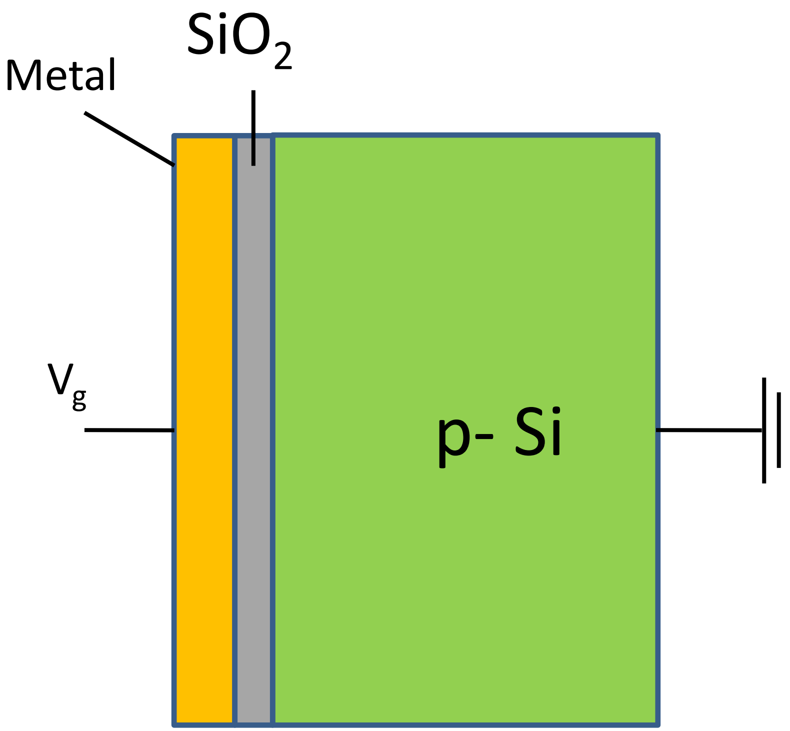


10.1 The two-terminal MOS structure



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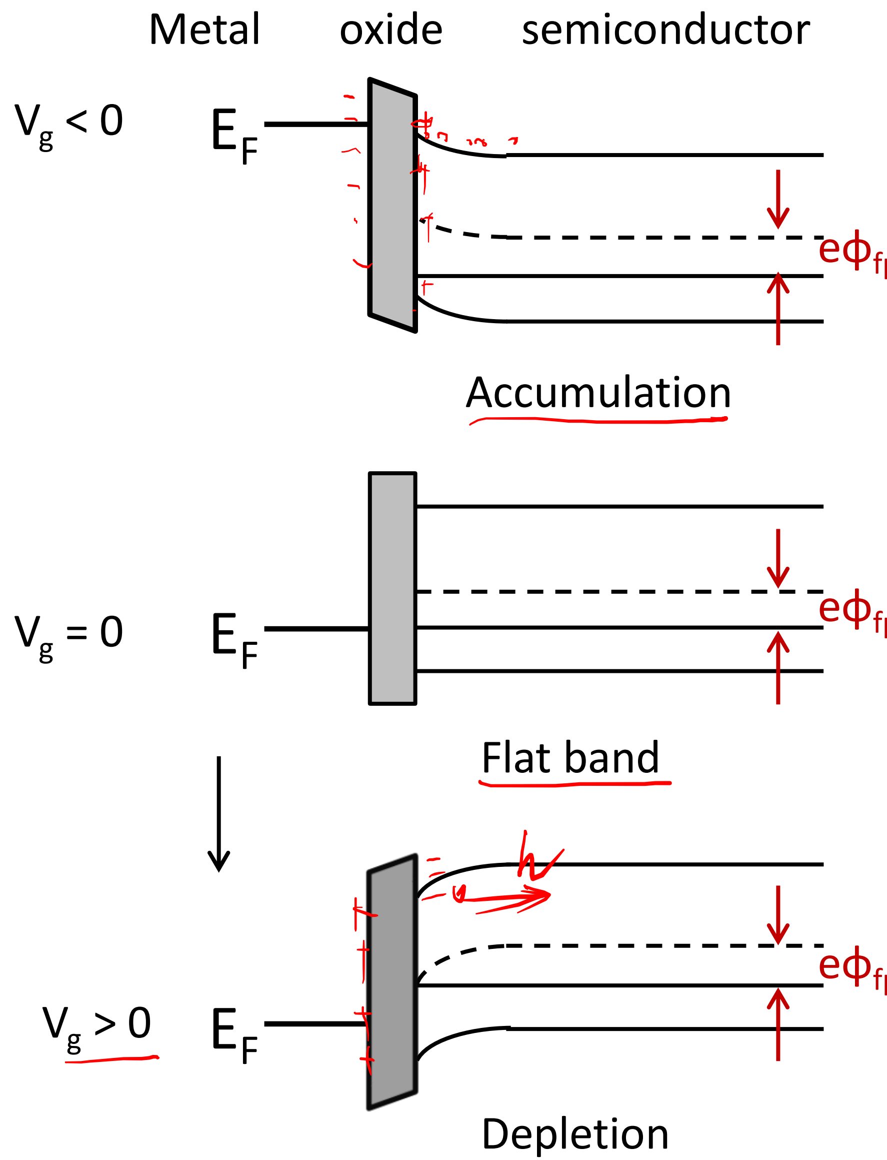

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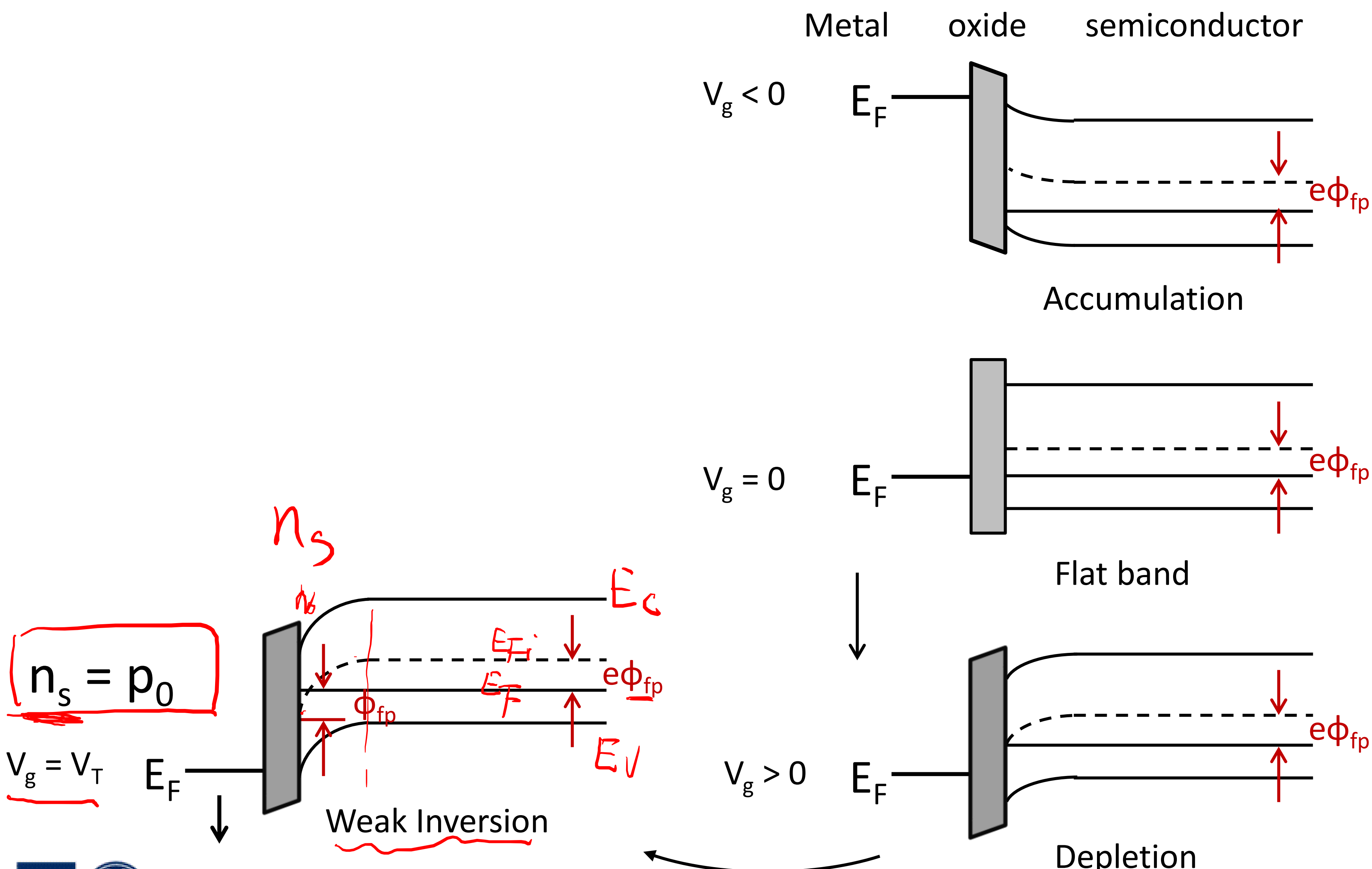

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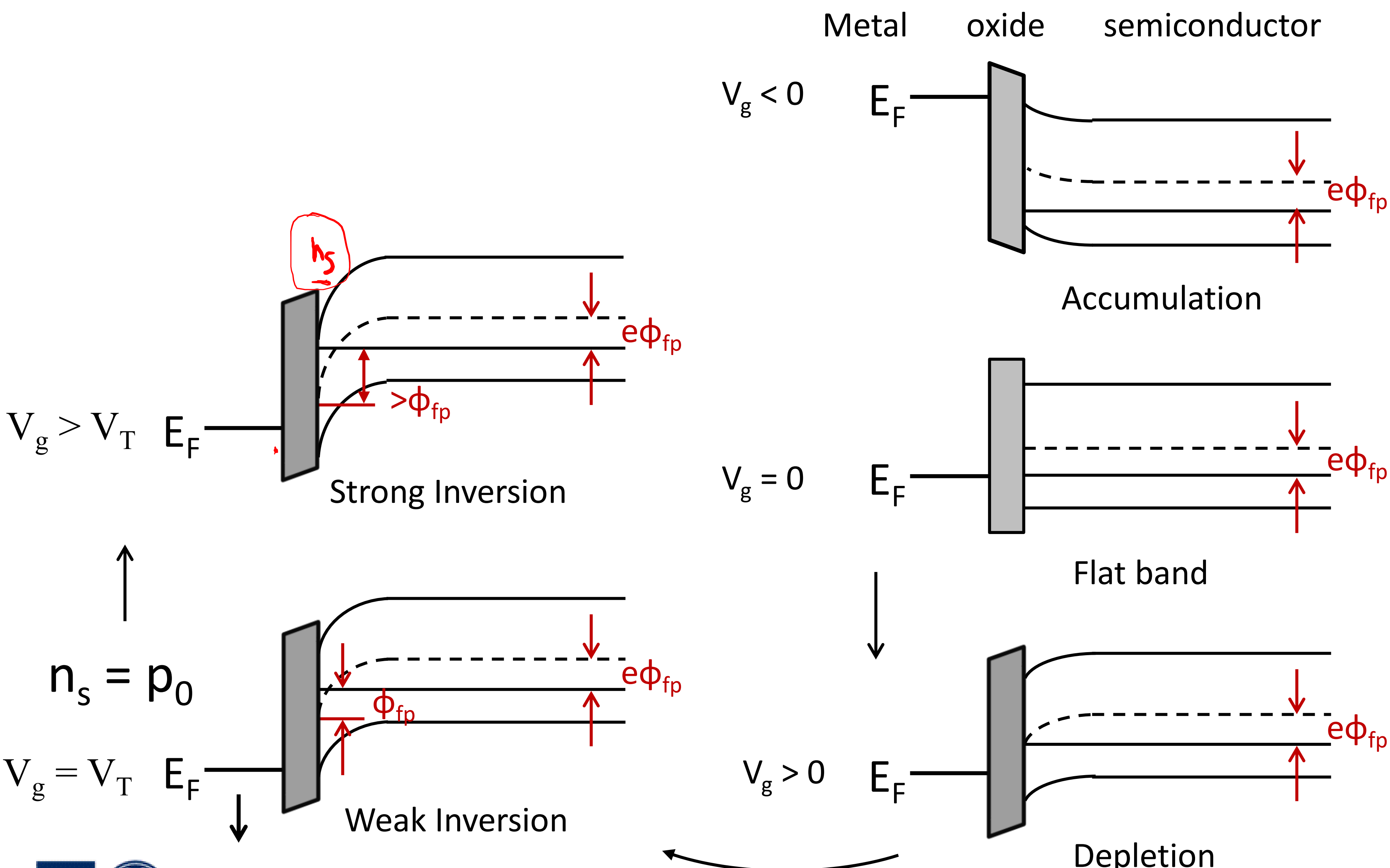
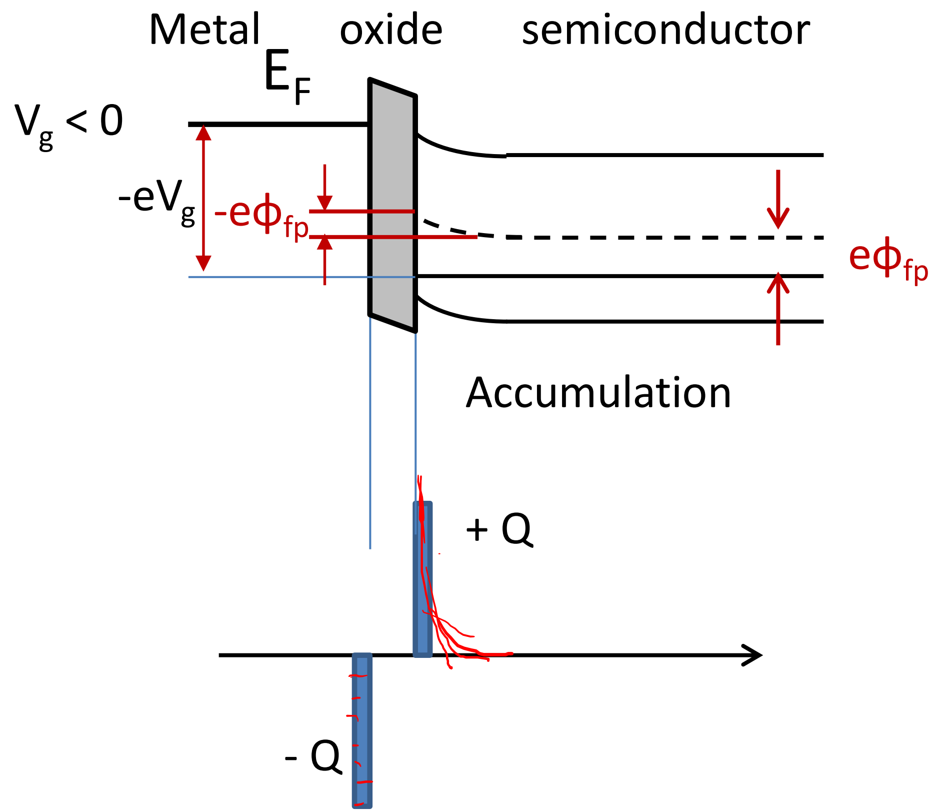


10.1 The two-terminal MOS structure

2) Charge distribution



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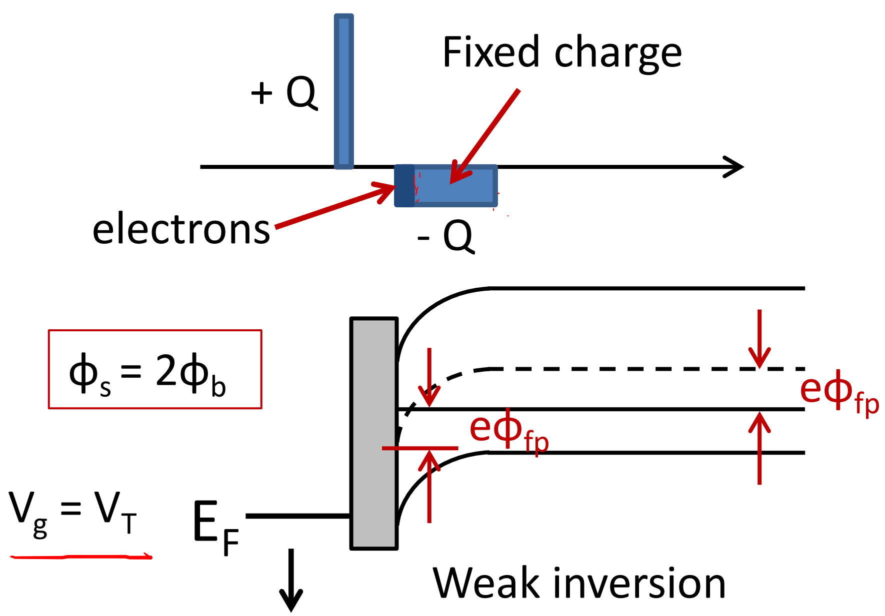
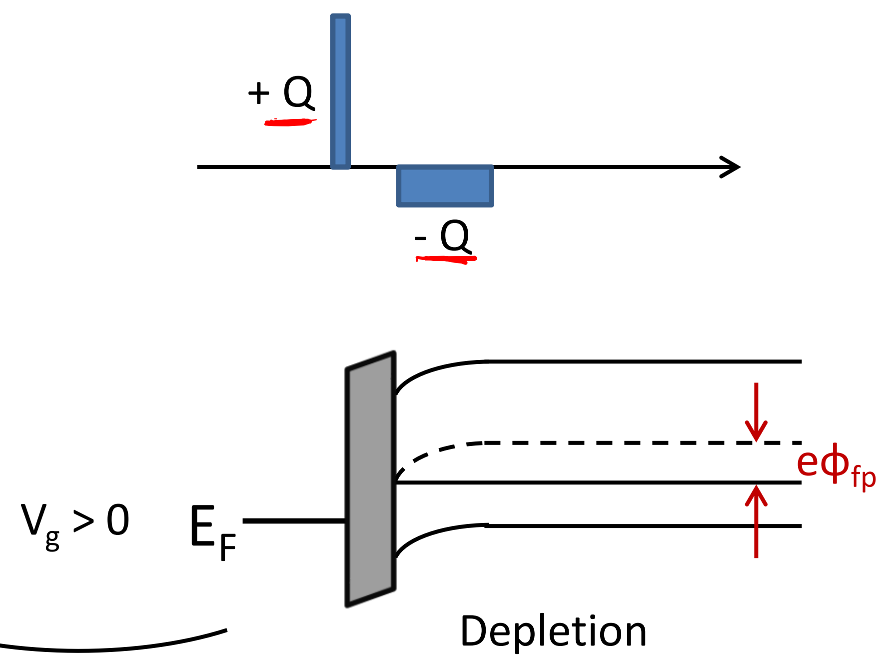
Charge distribution





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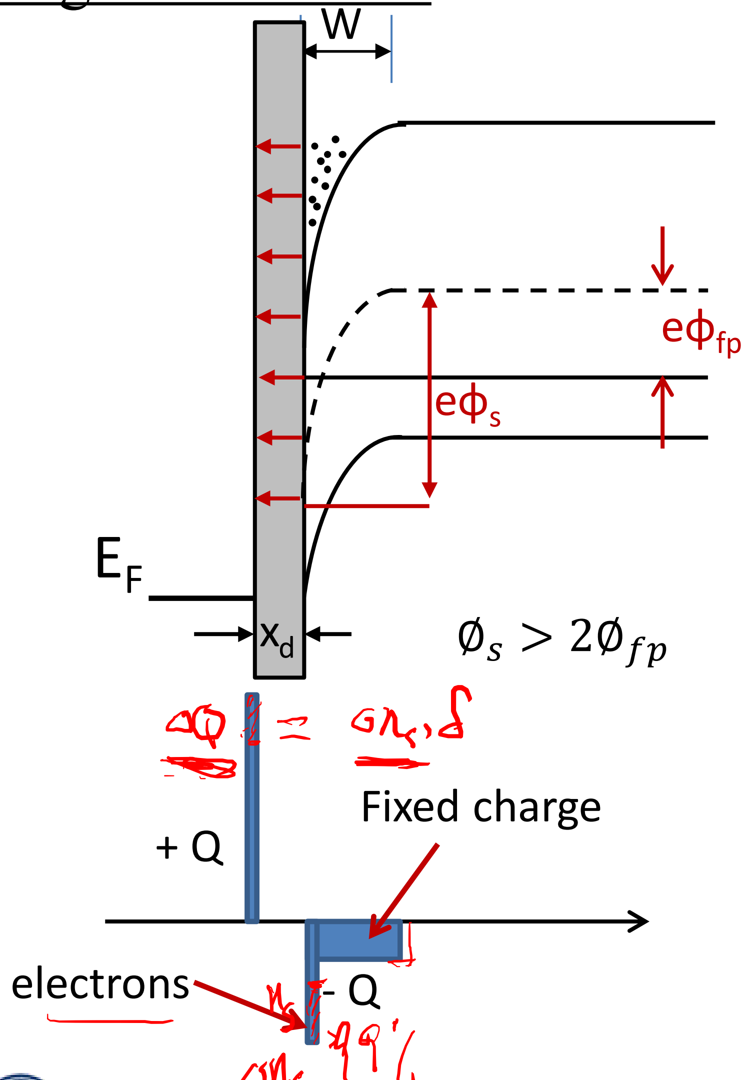
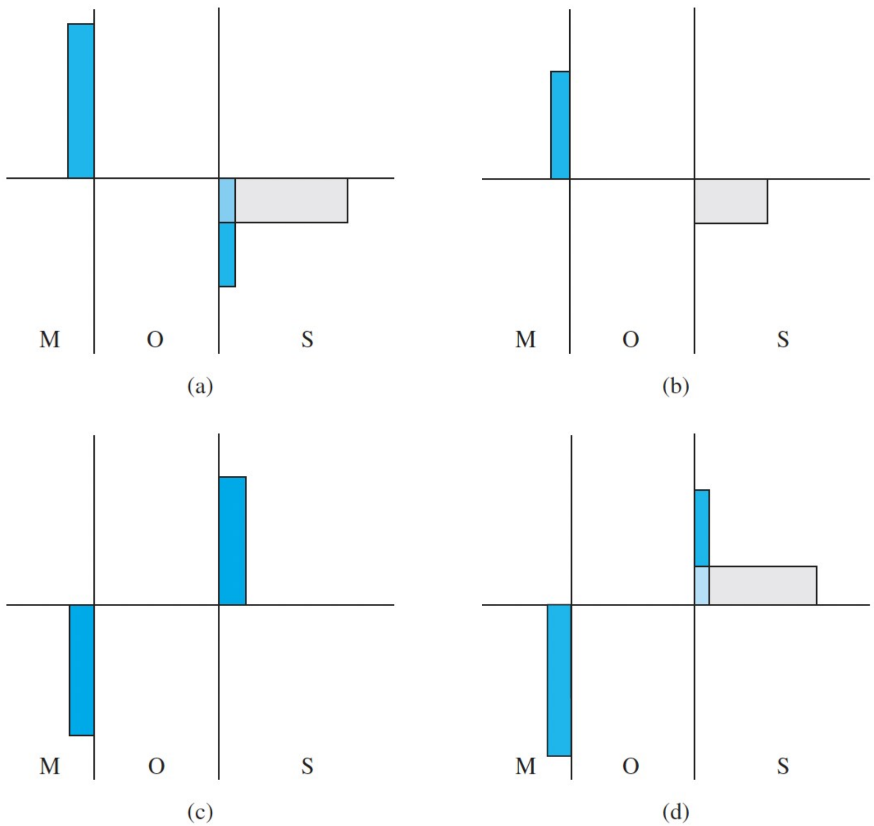
Charge distribution



Check your understanding

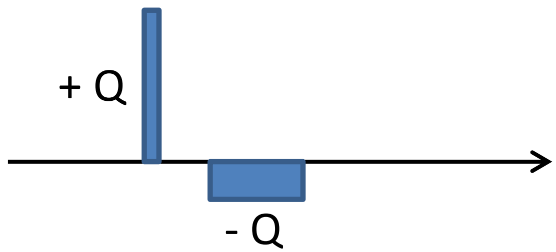
Example Problem #1

The dc charge distributions of four ideal MOS capacitors are shown in Figure P10.1. For each case: (*a*) Is the semiconductor n or p type? (*b*) Is the device biased in the accumulation, depletion, or inversion mode? (*c*) Draw the energy-band diagram in the semiconductor region.

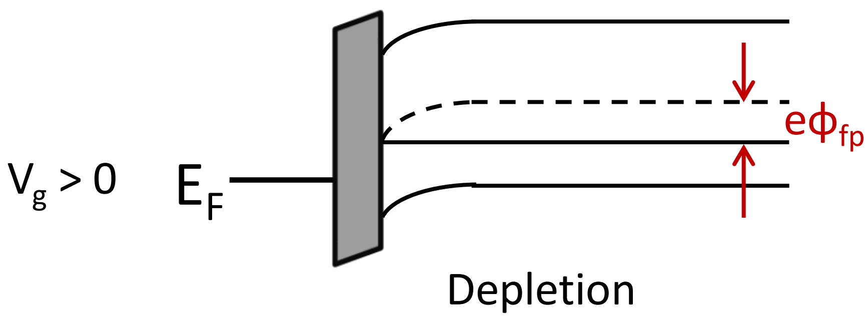


10.1 The two-terminal MOS structure

③ Depletion layer thickness



$$x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a} \right)^{1/2}$$



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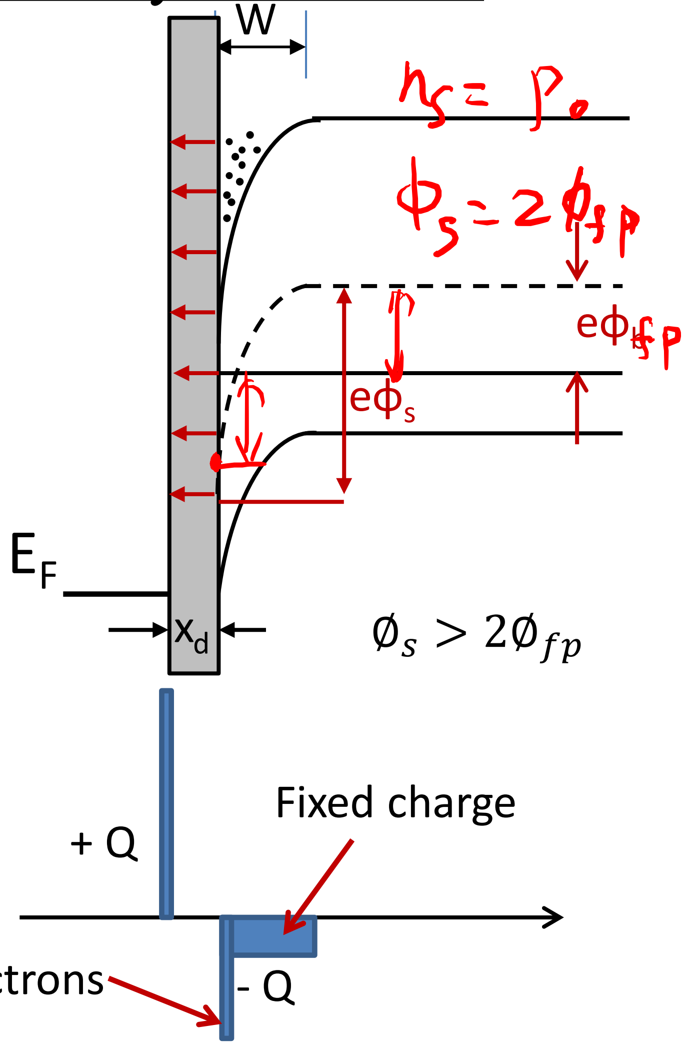
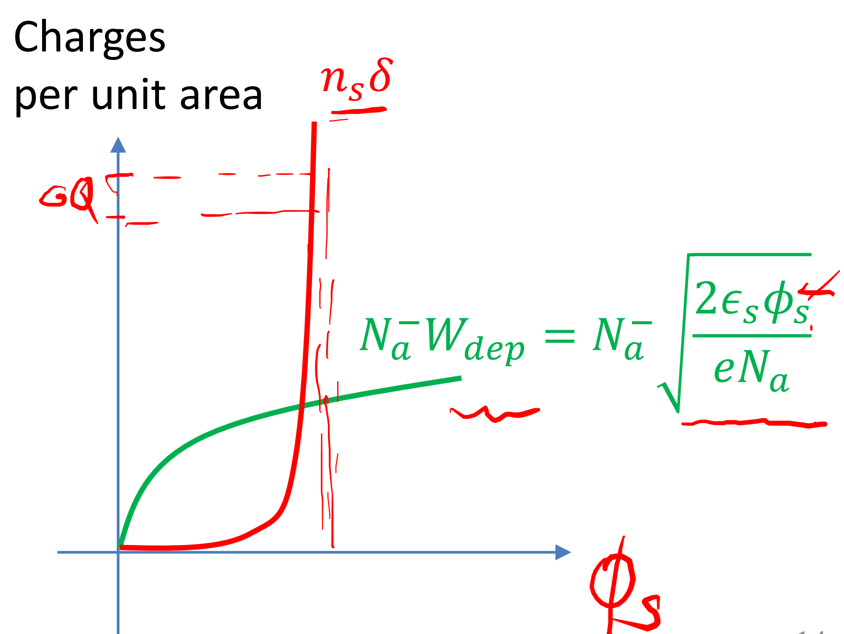
Depletion layer thickness



Maximum depletion layer

$$\boxed{x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a}\right)^{1/2}}$$



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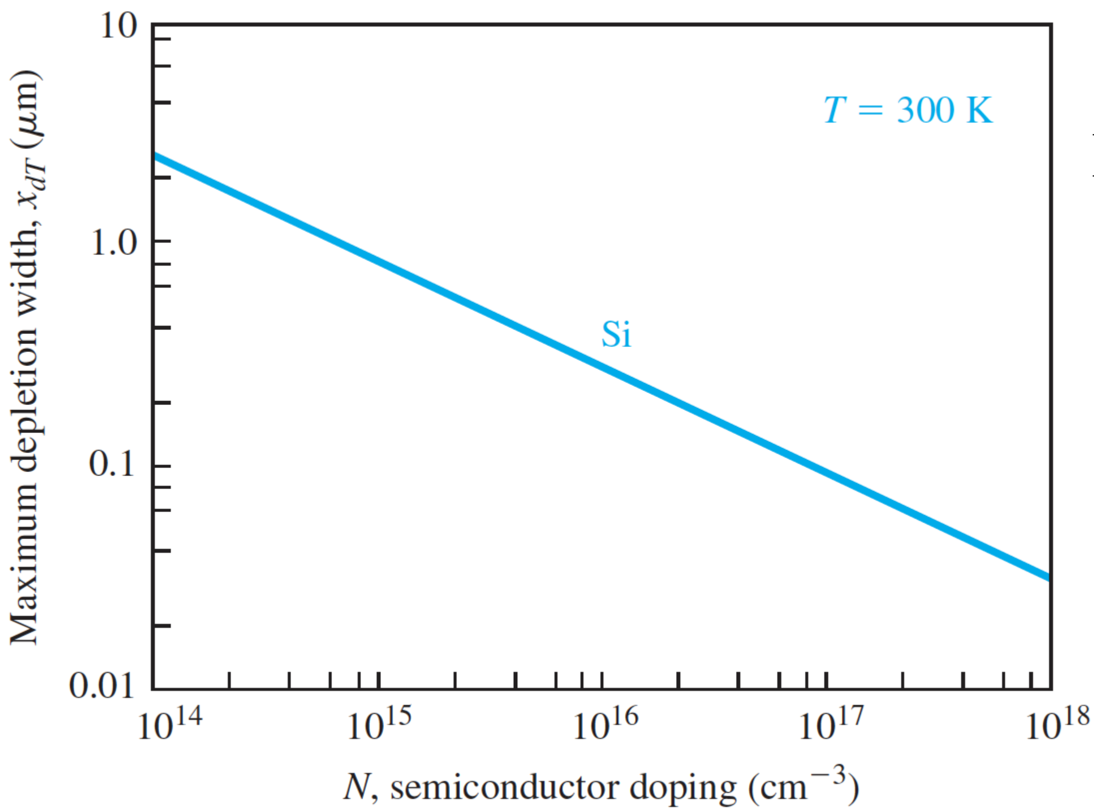

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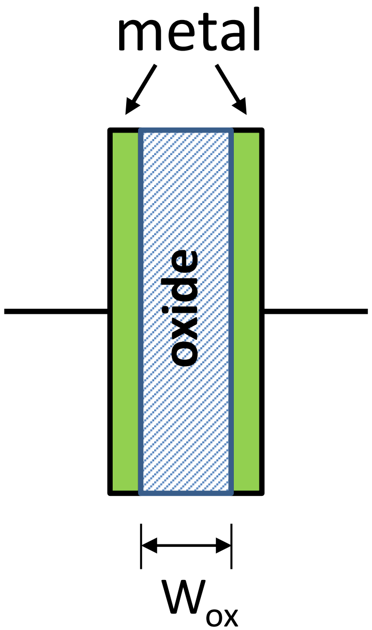
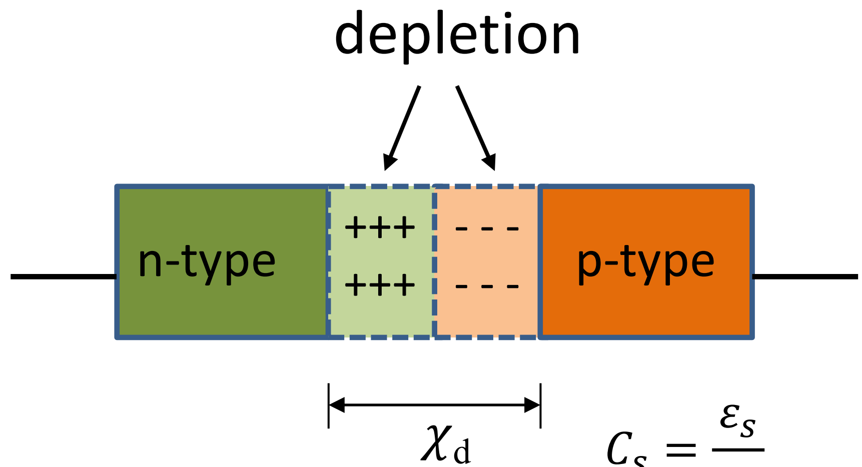
10.2 The capacitance-voltage characteristics



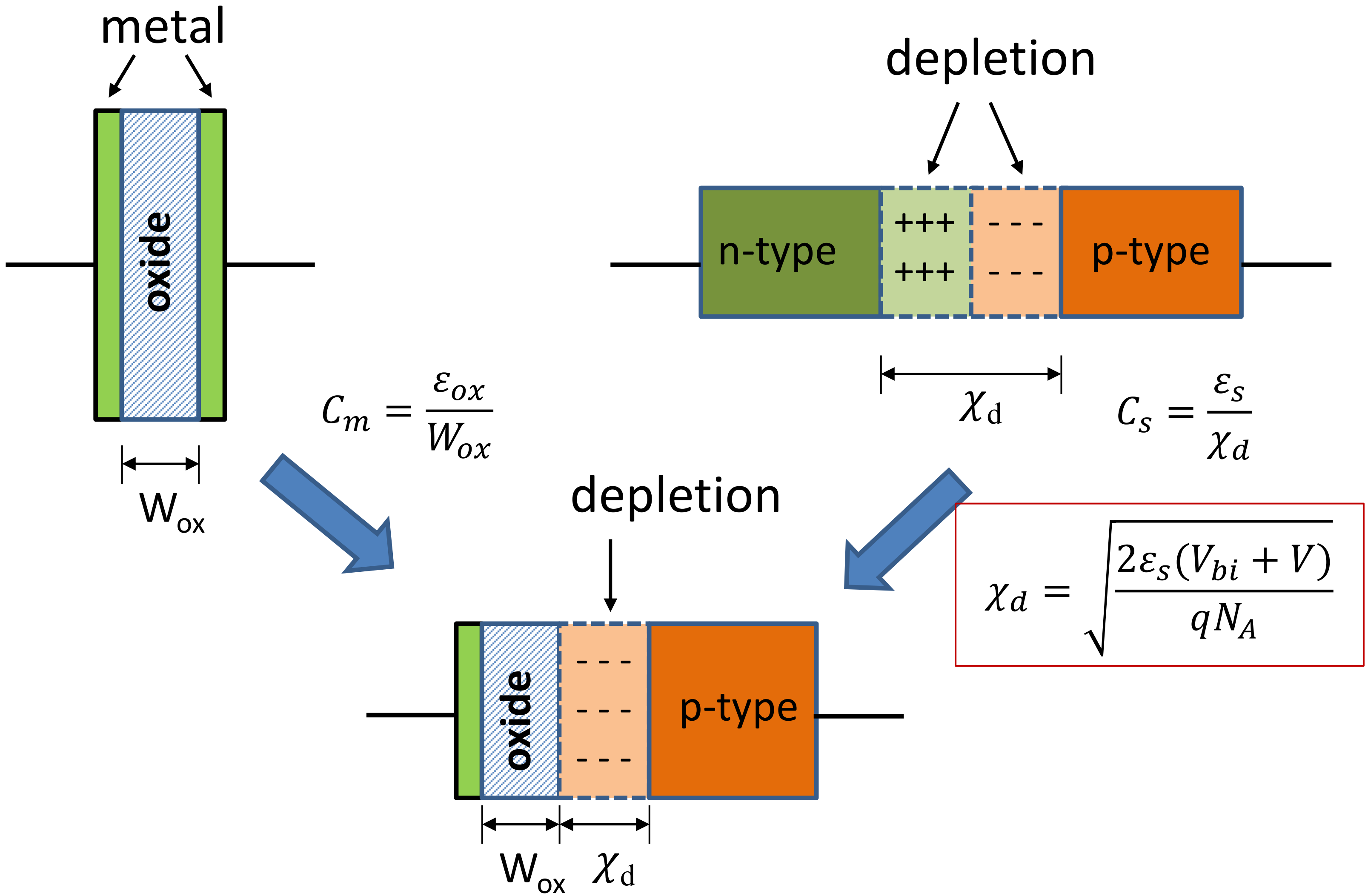
$$C_m = \frac{\varepsilon_{ox}}{W_{ox}}$$



$$C_s = \frac{\varepsilon_s}{\chi_d}$$

$$\boxed{\chi_d = \sqrt{\frac{2\varepsilon_s(V_{bi} + V)}{qN_A}}}$$

10.2 The capacitance-voltage characteristics



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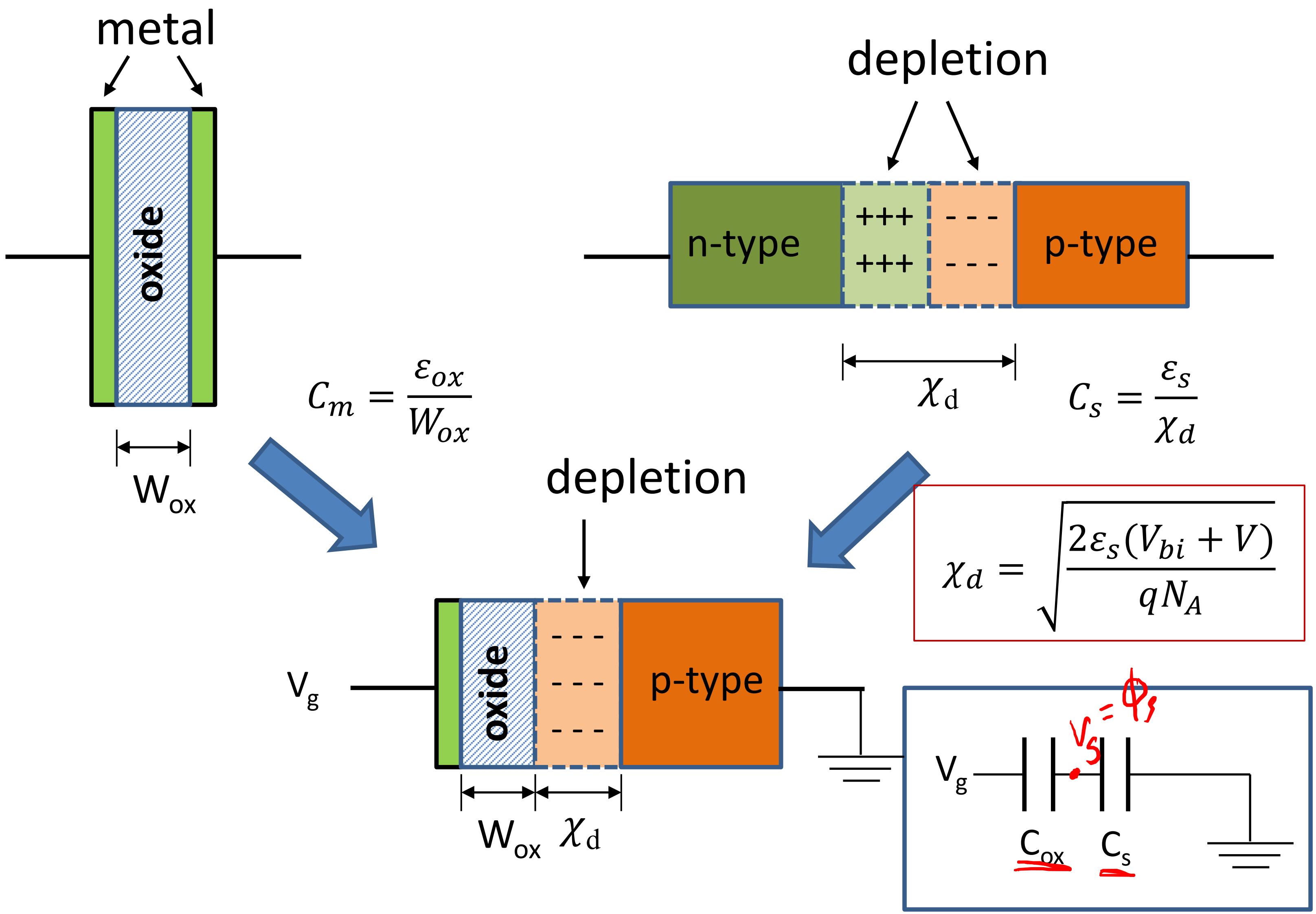

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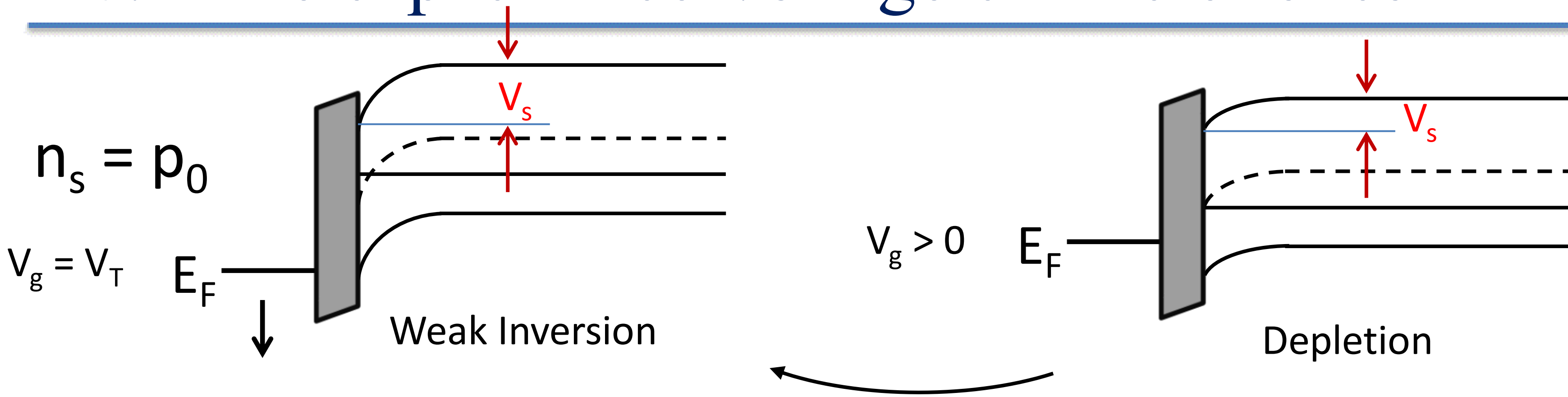

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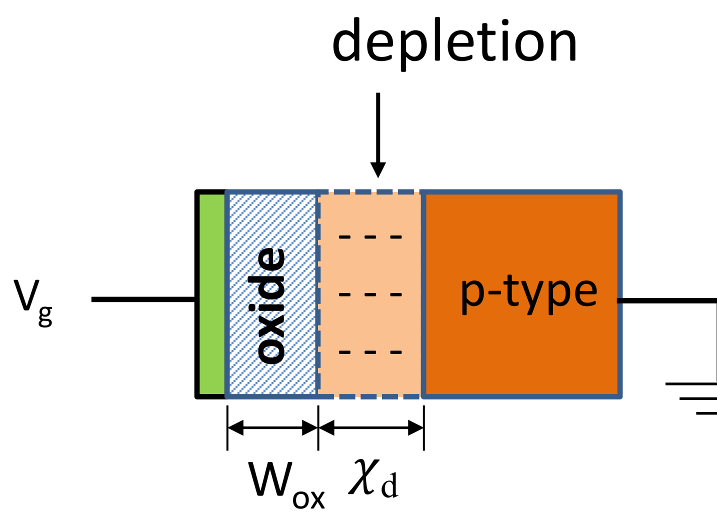
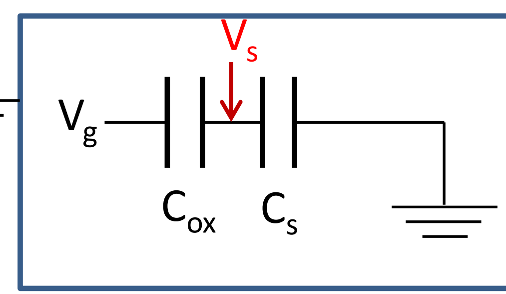
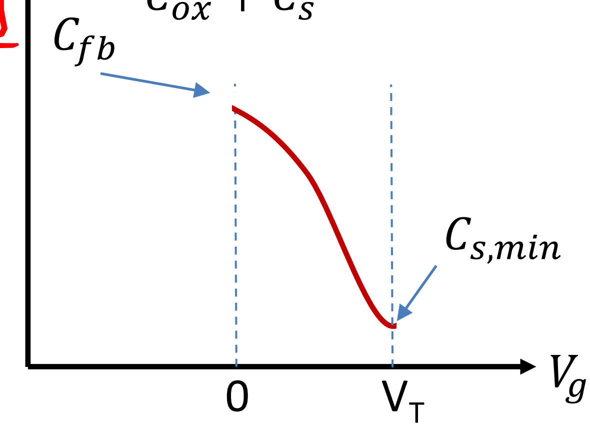




10.2 The capacitance-voltage characteristics

$$\boxed{A C_s^3 + B C_s^2 + C C_s + D = 0}$$

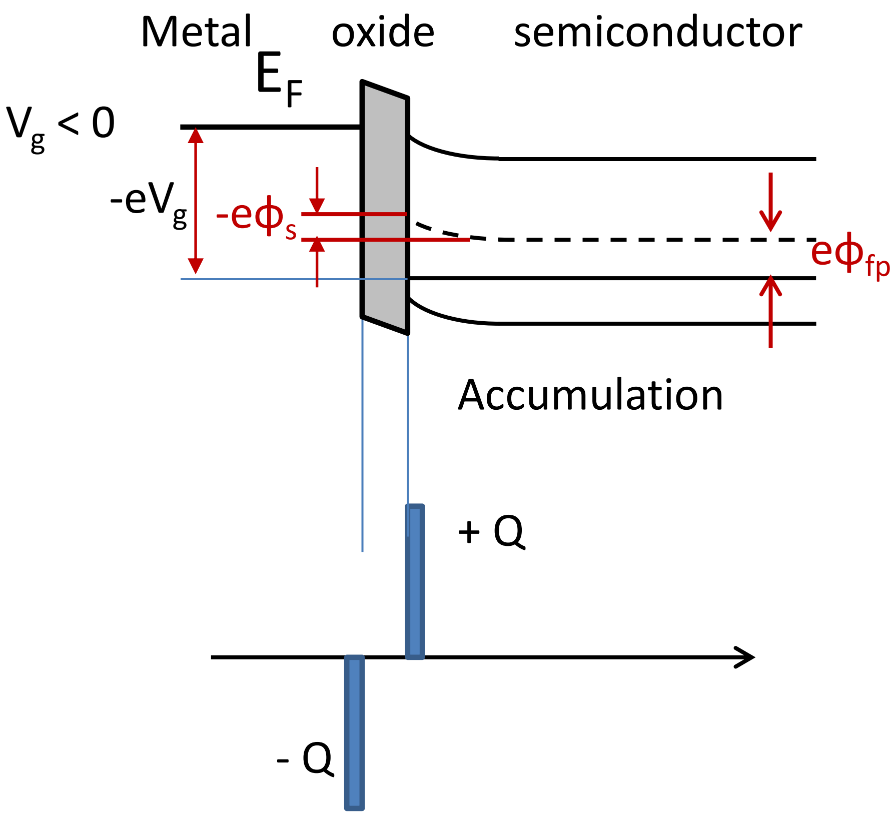
$$C = \frac{C_{ox} C_s}{C_{ox} + C_s}$$

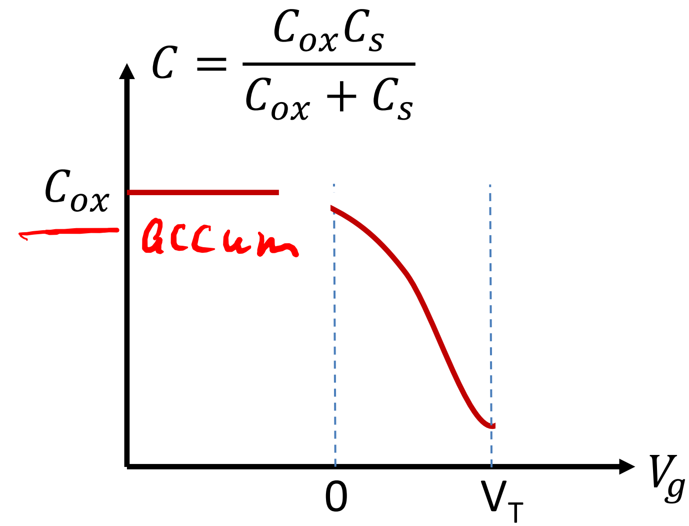


$$\begin{cases} V_s = \dfrac{C_g \cdot C_{ox}}{C_{ox} + C_s} \\ C_s = \dfrac{\varepsilon_s}{\sqrt{\dfrac{2 \varepsilon_s V_s}{q N_A}}} \end{cases}$$

10.2 The capacitance-voltage characteristics

Accumulation





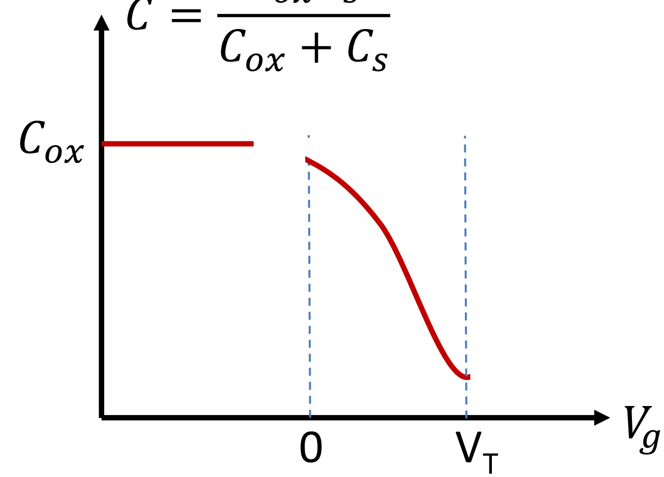
$C_s \rightarrow \infty$

$$C = \frac{C_s C_{ox}}{C_s + C_{ox}} \approx C_{ox}$$

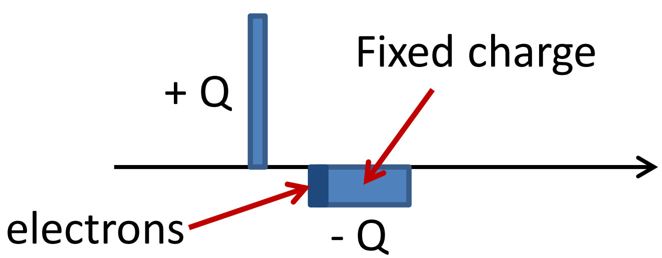
10.2 The capacitance-voltage characteristics

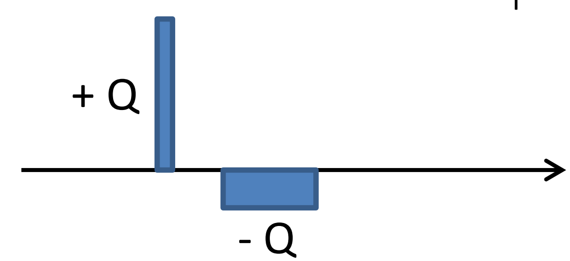
Depletion and weak inversion

$$C = \frac{C_{ox} C_s}{C_{ox} + C_s}$$

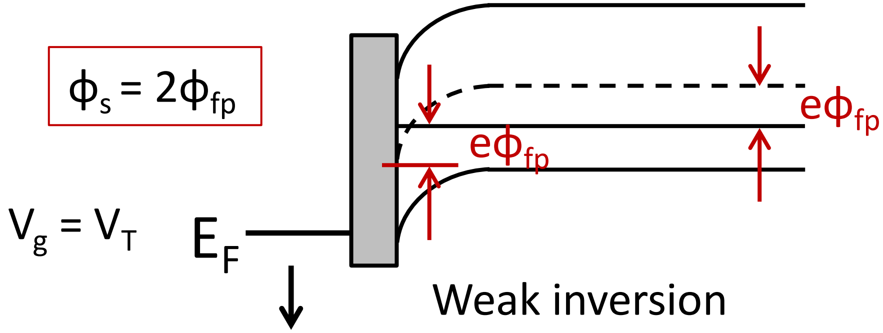


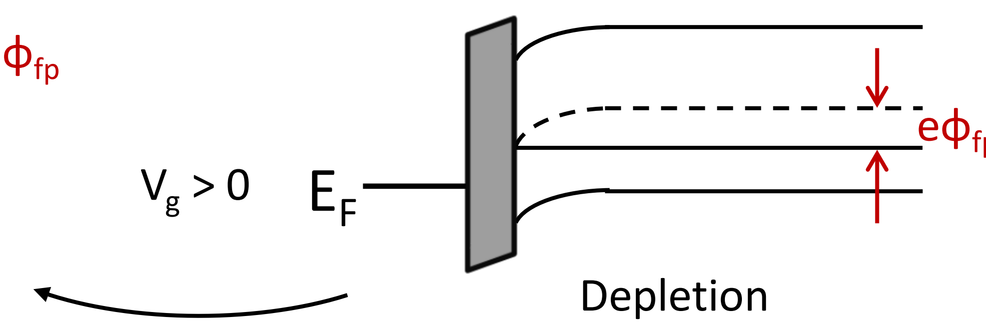
$$\boxed{C_s = \frac{\varepsilon_s}{\sqrt{\frac{2\varepsilon_s (V_s)}{qN_A}}}}$$





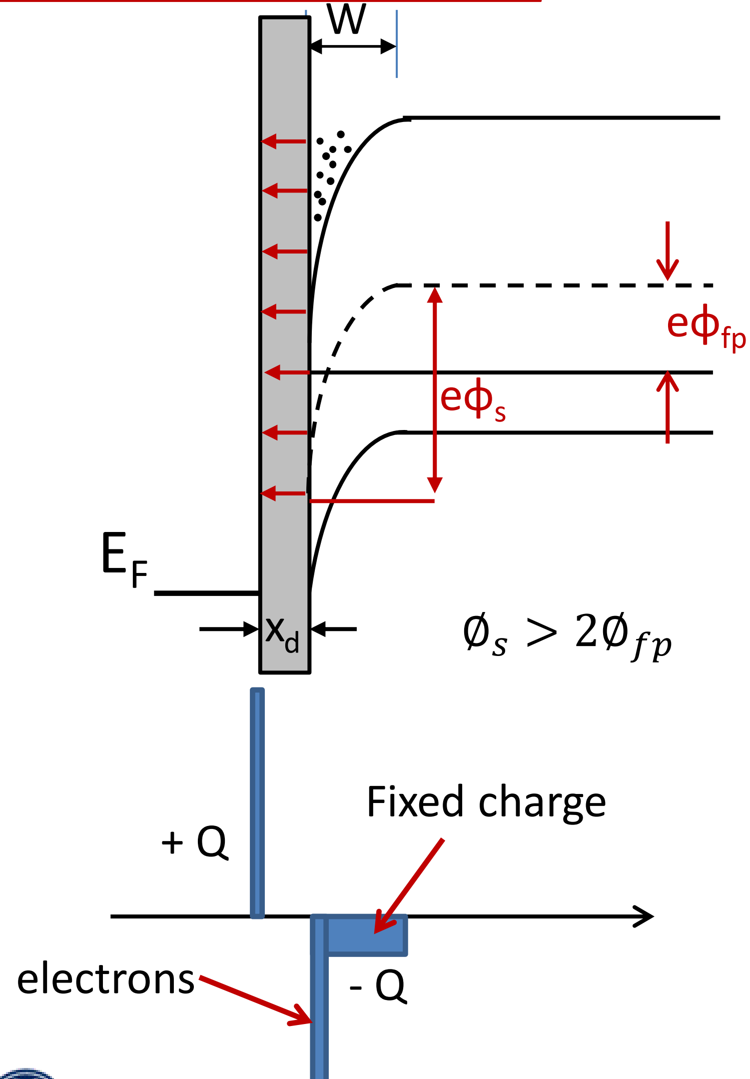
$\boxed{\phi_s = 2\phi_{fp}}$



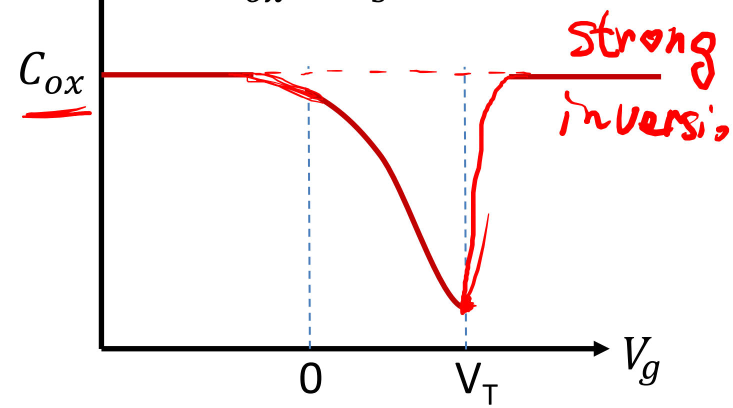


10.2 The capacitance-voltage characteristics

Strong inversion



$$C = \frac{C_{ox}C_s}{C_{ox} + C_s}$$

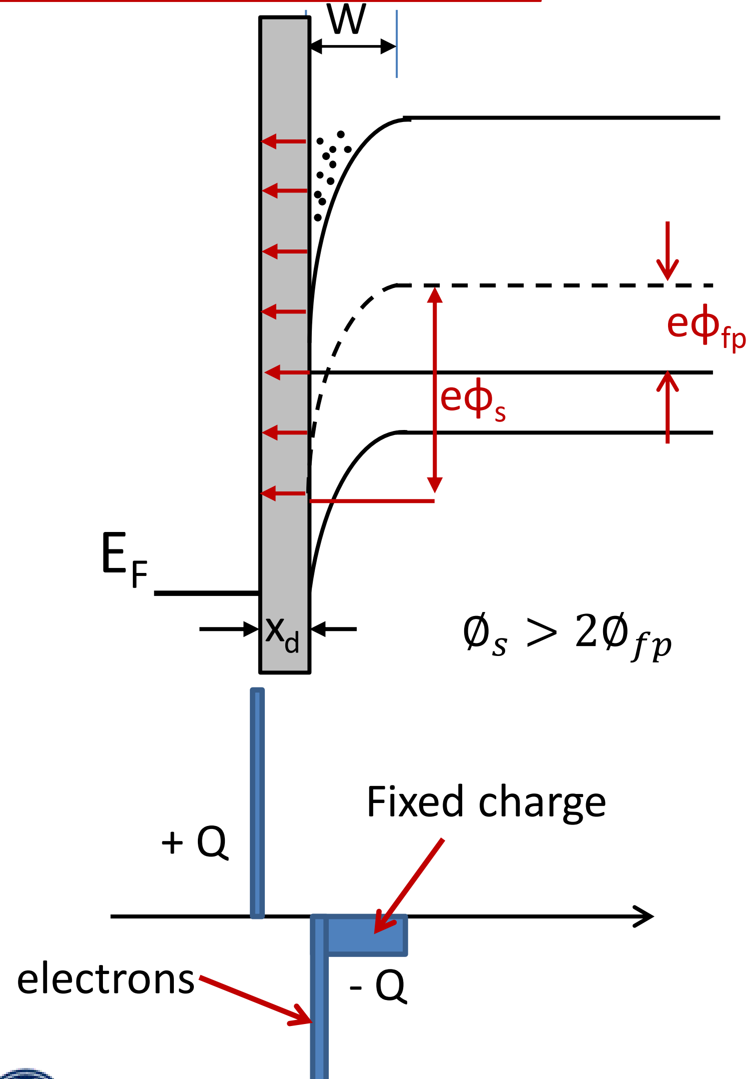


$C_s \rightarrow \infty$

$$C = \frac{C_s C_{ox}}{C_s + C_{ox}} \approx C_{ox}$$

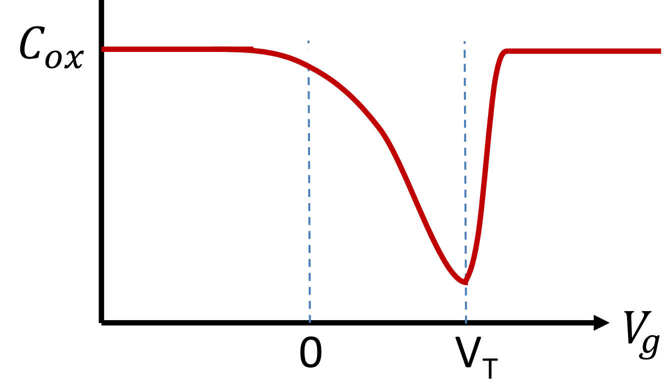
10.2 The capacitance-voltage characteristics

Strong inversion



$$\phi_s > 2\phi_{fp}$$

$$C = \frac{C_{ox}C_s}{C_{ox} + C_s}$$



$C_s \rightarrow \infty$

$$C = \frac{C_s C_{ox}}{C_s + C_{ox}} \approx C_{ox}$$

Check your understanding

Problem Example #2

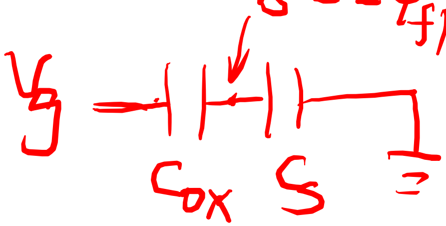
Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}. The oxide is silicon dioxide with a thickness of $t_{ox} = 18$ nm $= 180$ Å, and the gate is aluminum.

Calculate C_{ox}, C'_{min}, and C'_{FB} for a MOS capacitor.

$$C_{min} = \frac{\cancel{\varepsilon_{ox} t_{ox}}\; t_{ox} \cdot x_{dT}}{\varepsilon_{ox} x_{dT} + \varepsilon_s \cdot t_{ox}}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{18 \times 10^{-7}} = 1.92 \times 10^{-7}\ F/cm^2$$

$V_G = 2\phi_{fp}$



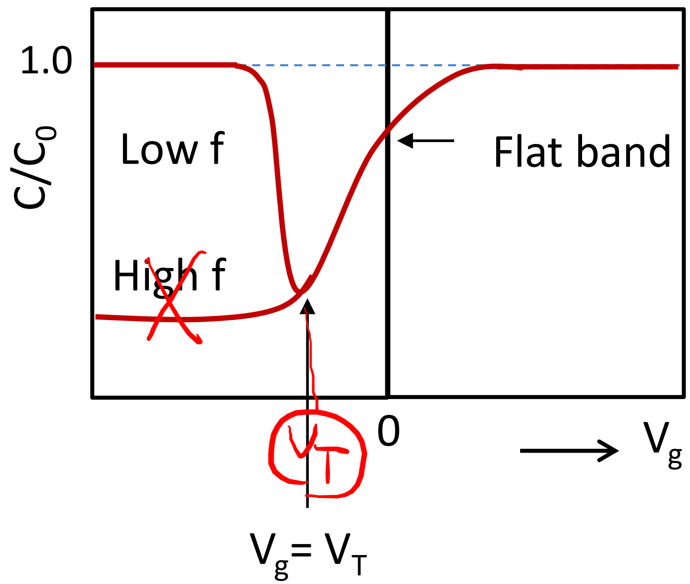
$$\frac{1}{C_t} = \frac{1}{C_{ox}} + \frac{1}{C_{s\,min}} = \frac{\varepsilon_{ox}}{t_{ox}} + \frac{\varepsilon_s}{x_{dT}}$$

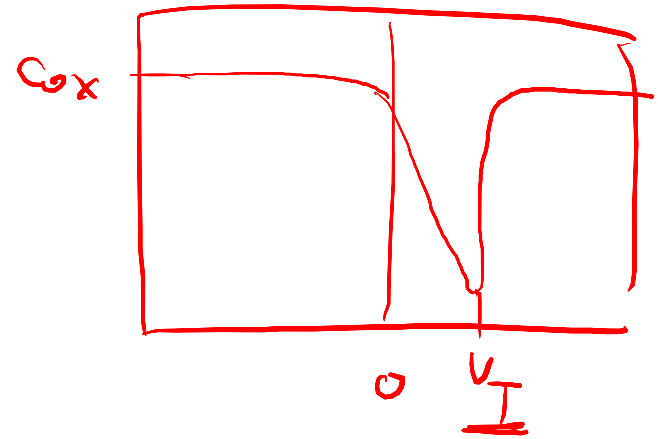
$$x_{dT} = \left(\frac{4\varepsilon_s \phi_{fp}}{eN_a}\right)^{1/2}$$

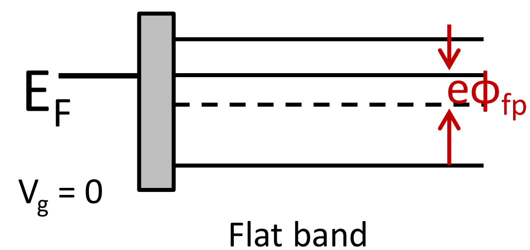
$$C_{s\,min} = \frac{\varepsilon_{si}}{x_{dT}}$$

10.2 The capacitance-voltage characteristics

n-type semiconductor







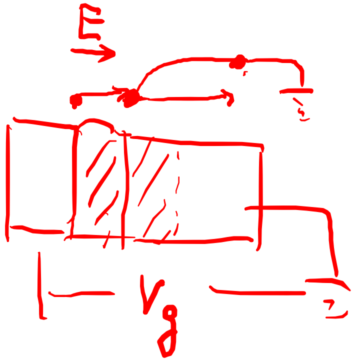
n-type substrate

10.2 The capacitance-voltage characteristics

Threshold voltage

$V_T = V_g = E \cdot t_{ox} + \phi_s$

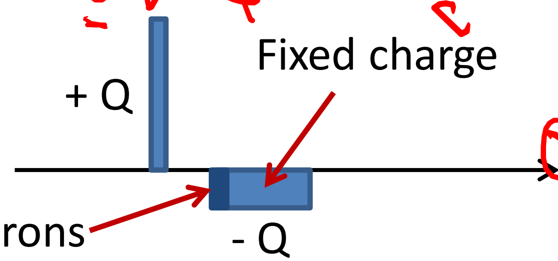
$V_{ox} = N_a \cdot x_{dT} / C_{ox}$



$$C_s = \frac{\varepsilon_s}{\sqrt{\frac{2\varepsilon_s(V_s)}{qN_A}}} = \frac{\varepsilon_s}{\sqrt{\frac{2\varepsilon_s(2\phi_{fp})}{qN_A}}}$$

$C \cdot V = Q \quad V = \frac{Q}{C}$

$$2\phi_{fp} = \frac{V_T C_{ox}}{C_{ox} + C_s} \Rightarrow V_T = 2\phi_{fp} + 2\phi_{fp}\frac{C_s}{C_{ox}}$$

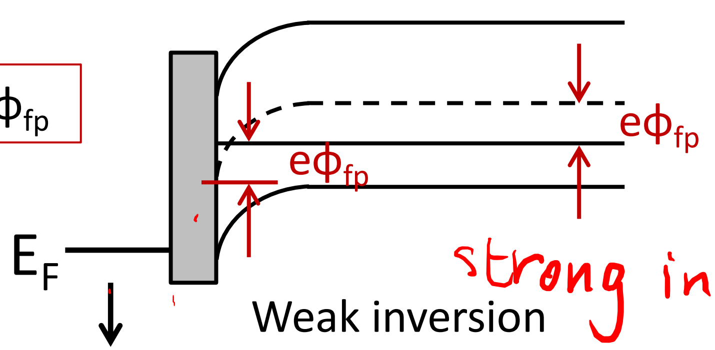


$Q = x_{dT} \cdot N_a$

$$V_T = 2\phi_{fp} + \frac{2\sqrt{e\varepsilon_s N_A \phi_{fp}}}{C_{ox}}$$

$\phi_s = V_s = 2\phi_{fp}$

$V_g = V_T$

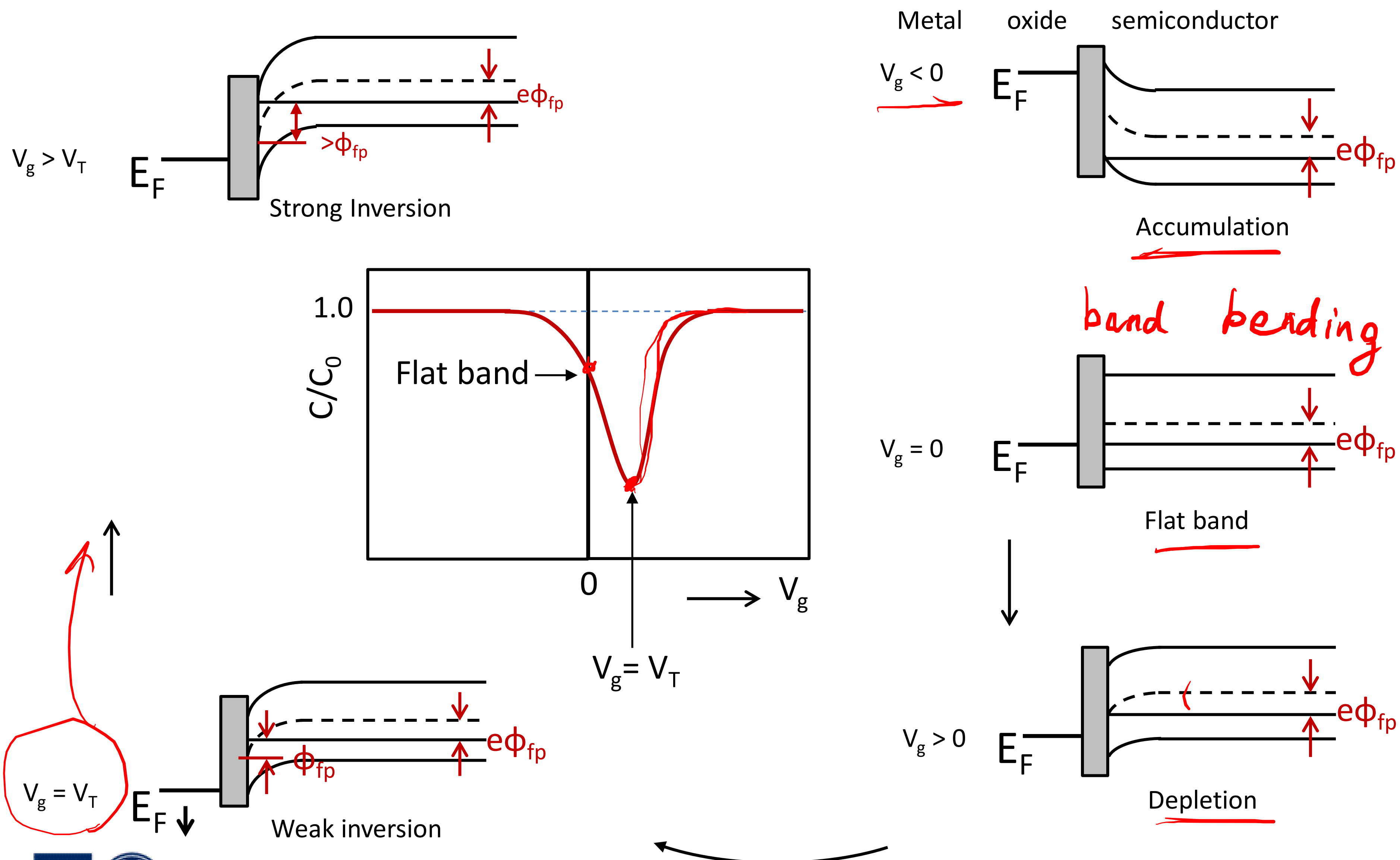


strong inversion

$$V_T = 2\phi_{fp} + \frac{N_a \cdot x_{dT}}{C_{ox}}$$

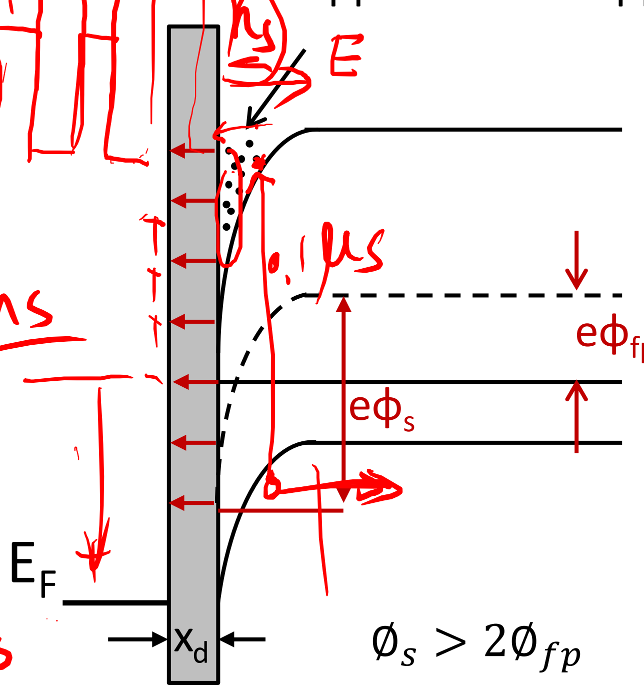
$$x_{dT} = \sqrt{\frac{4\varepsilon_s \cdot \phi_{fp}}{eN_a}}$$

10.2 The capacitance-voltage characteristics: summary



Question: W_{dep}

Appear and disappear



$\emptyset_s > 2\emptyset_{fp}$

Where are the electrons coming from and going to?

V_T W_{dep} $2V_T$ W_{dep}

10μs 10μs

1ns 5ns $2W_{dep}$ $2V_T$ $3V_T$ $3W_{dep}$ V_T 0

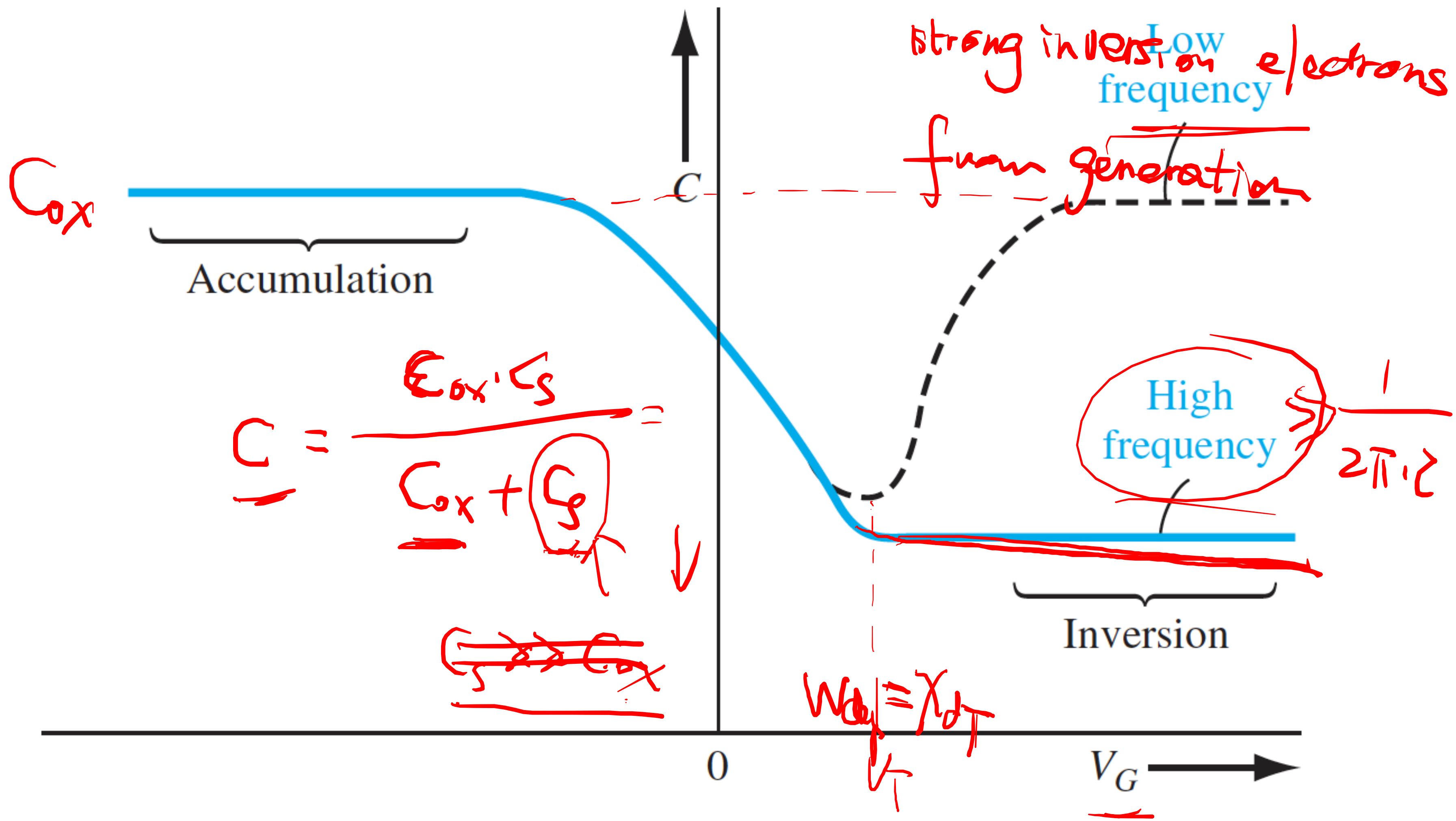
7ns 1ns

$$\frac{1}{2\pi T} = \frac{1}{2\pi \times 7\,\text{ns}} = \frac{1}{2\times 3.14\times 7 \times 10^{-9}} = \frac{1}{42\times 10^{-9}} = 2.4\times 10^{+7}\ \text{Hz} = 24\ \text{MHz}$$

$\boxed{2\ \text{GHz}}$

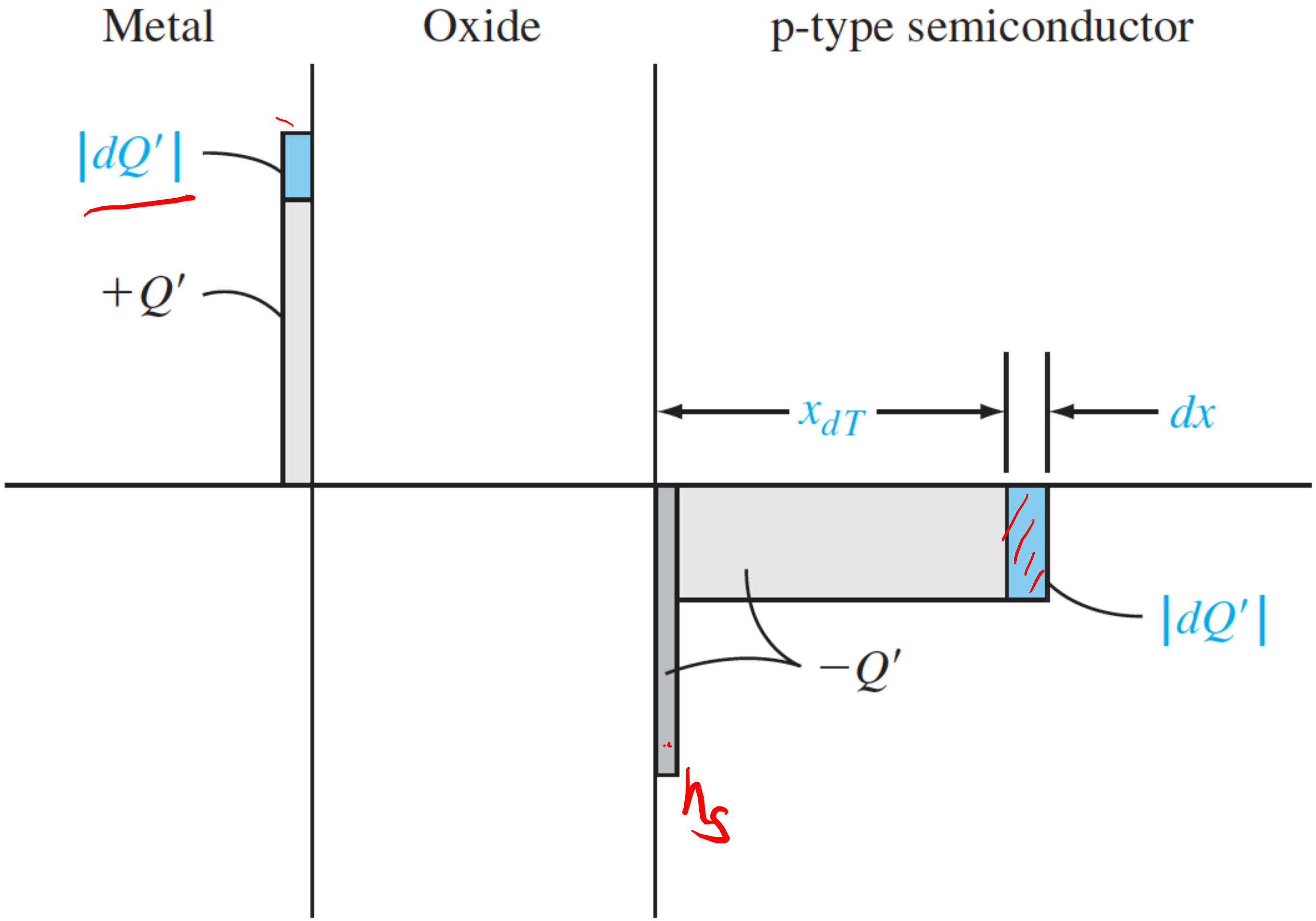
10.2 The capacitance-voltage characteristics

Frequency dependence



10.2 The capacitance-voltage characteristics

Frequency dependence



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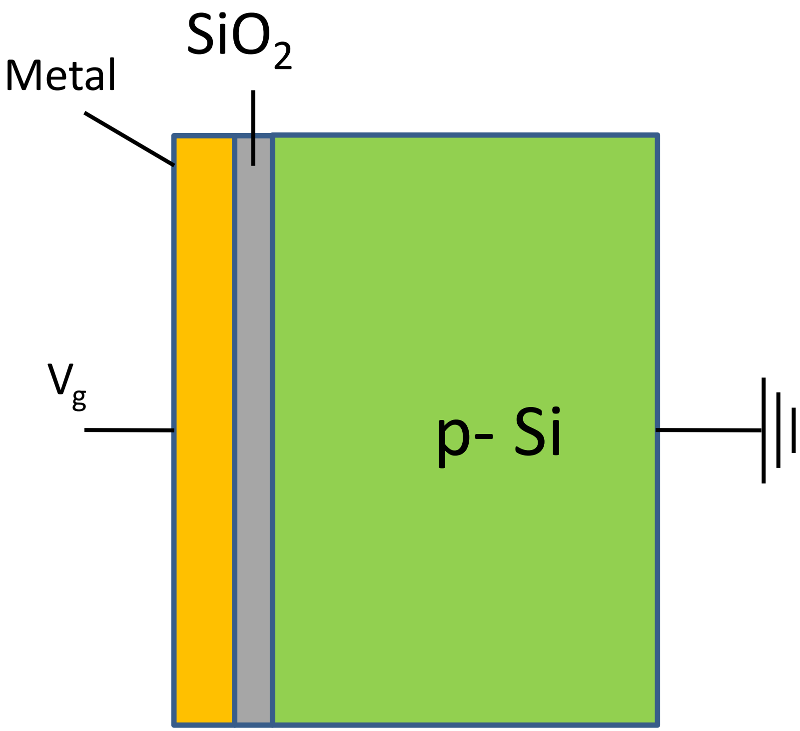
10.2 Capacitance-voltage characteristics

10.3 Non-ideal effects

10.4 The basic MOSFET operation

10.3 Non-ideal effects

Work function difference



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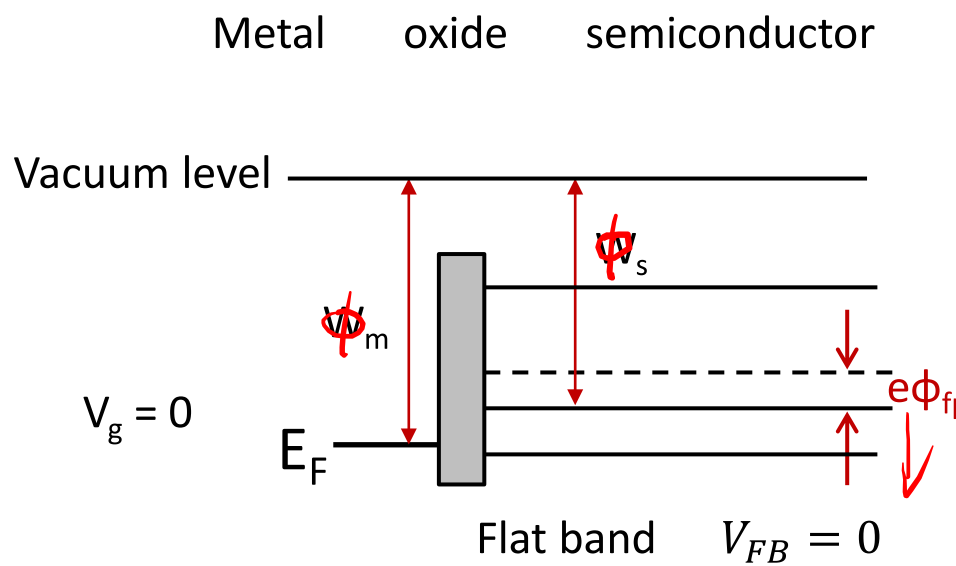

10.3 Non-ideal effects

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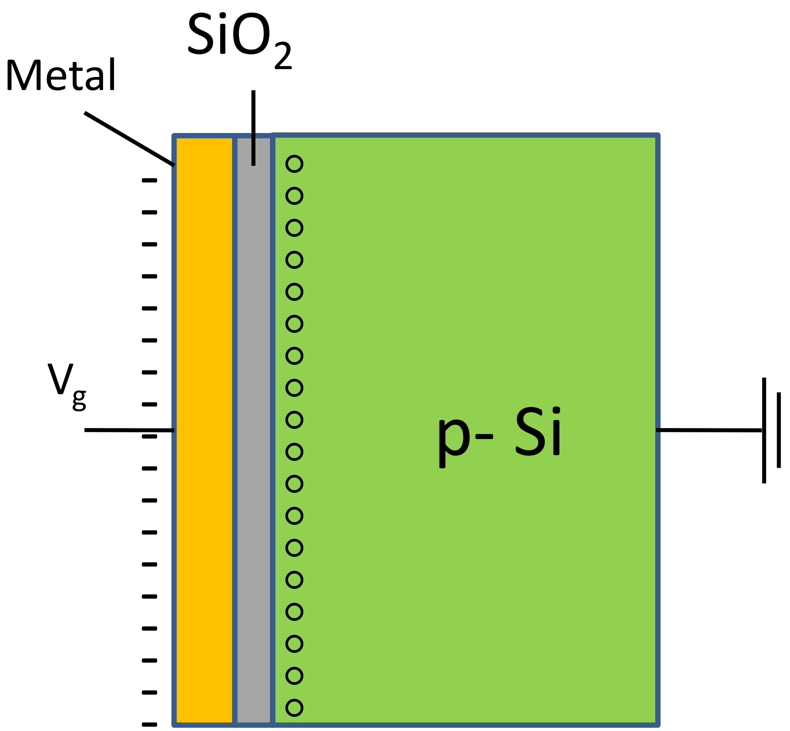

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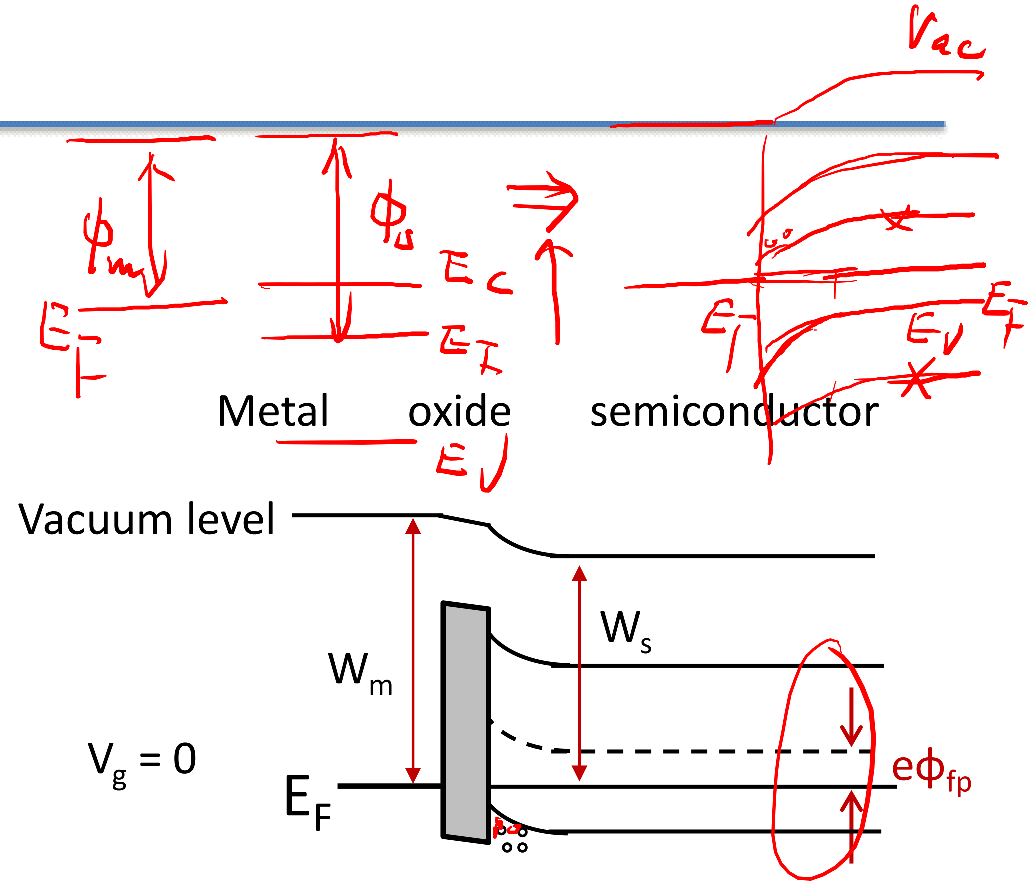

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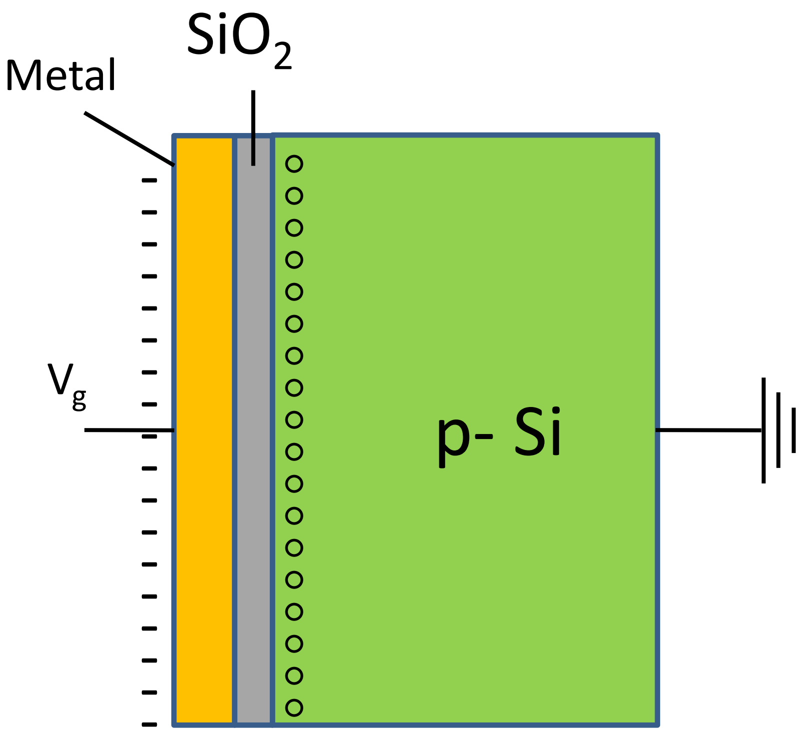

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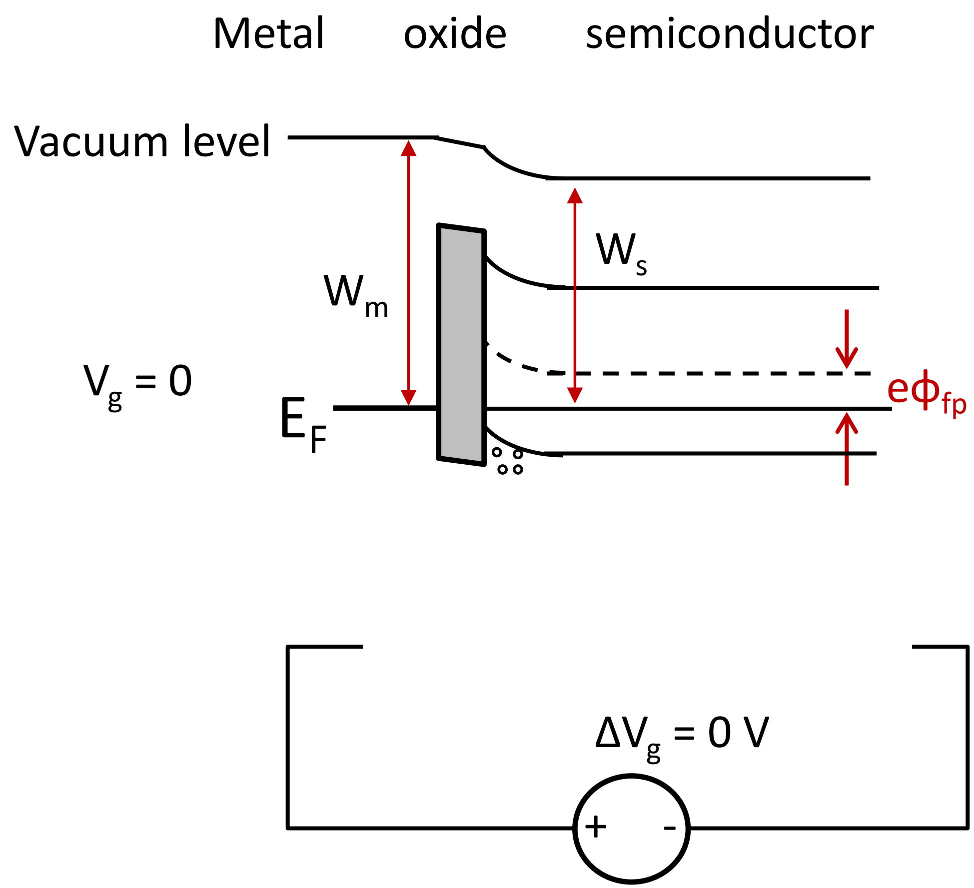
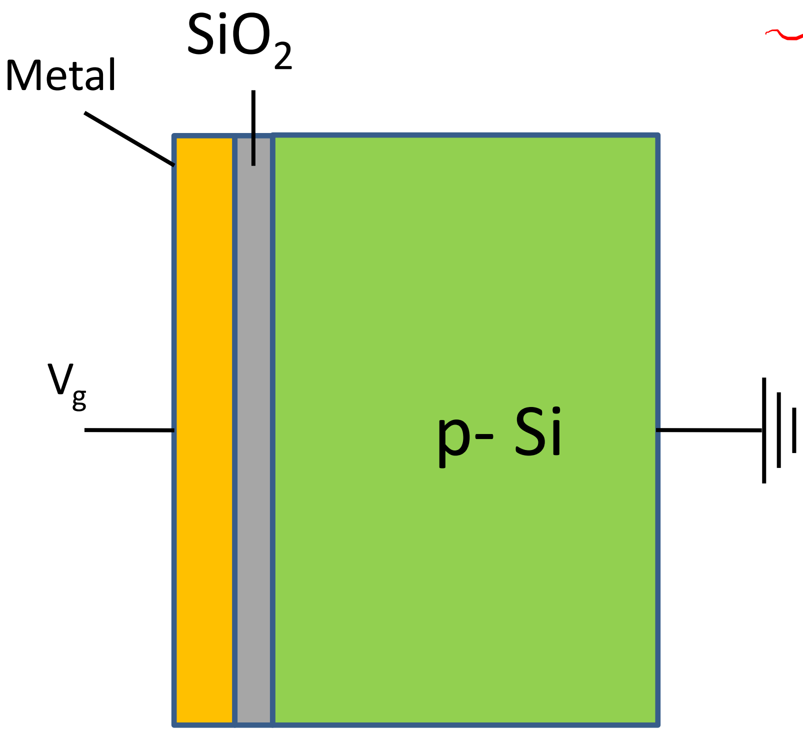


10.3 Non-ideal effects

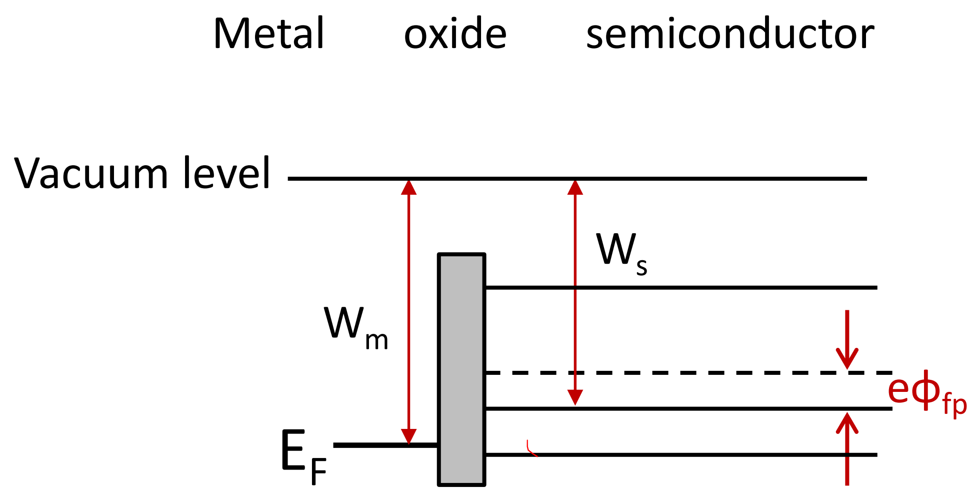
$$\sqrt{\frac{4\varepsilon\phi_{fI}}{2N_a}}$$

Work function difference

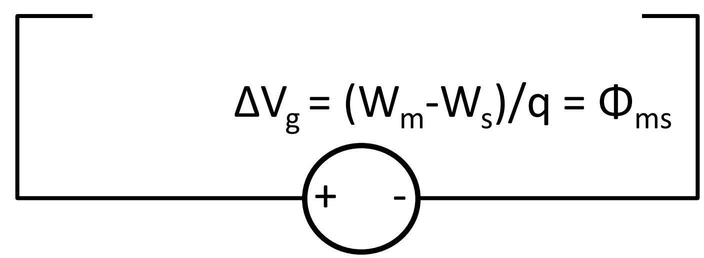
$$V_T = 2\phi_{fp} + \frac{N_a \cdot x_{dT}}{C_{ox}} + \frac{\phi_m - \phi_s}{q}$$



Metal-insulator-semiconductor (MIS)

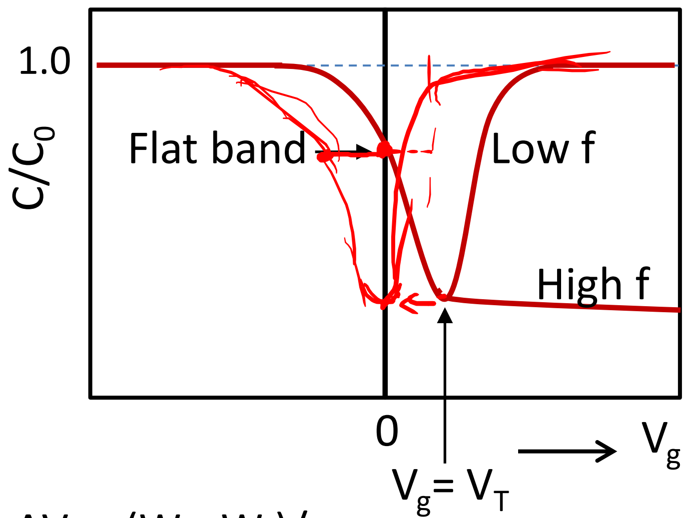


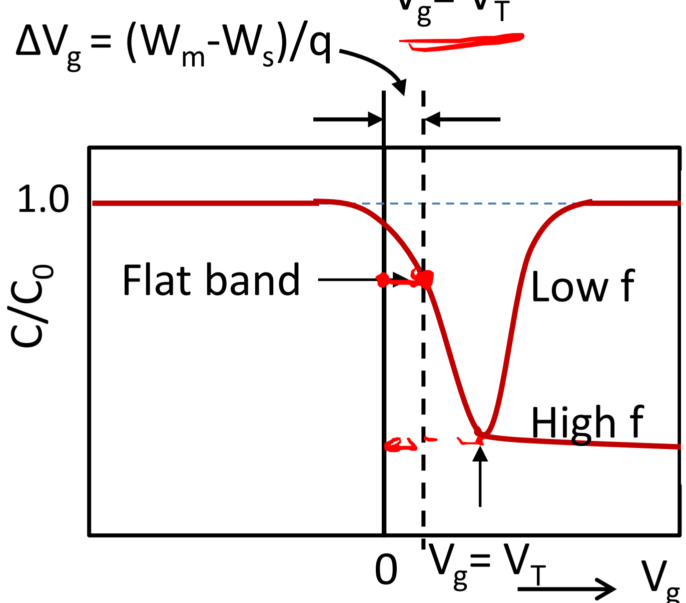
Flat band $V_{FB} = (W_m - W_s)/q$



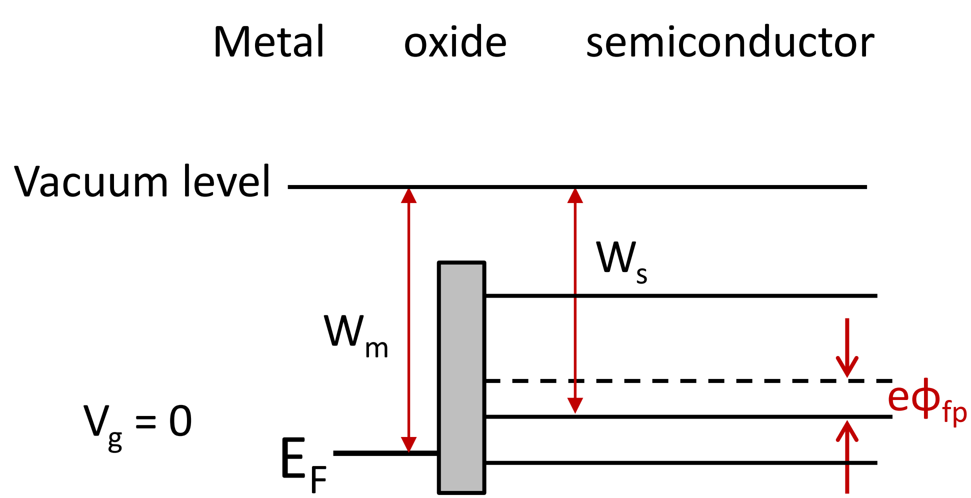
$\Delta V_g = (W_m - W_s)/q = \Phi_{ms}$

10.3 Non-ideal effects

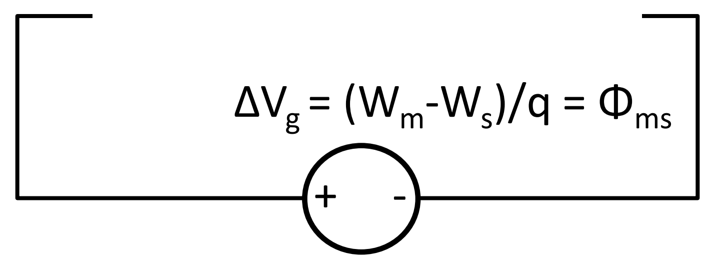




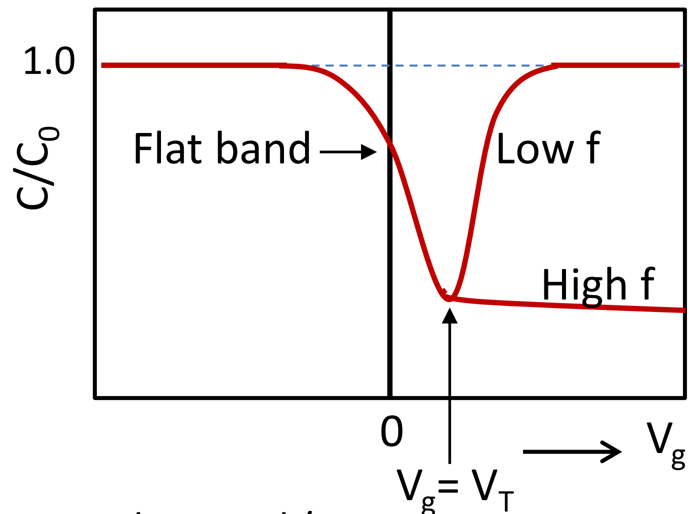
Work function difference



Flat band $V_{FB} = (W_m - W_s)/q$

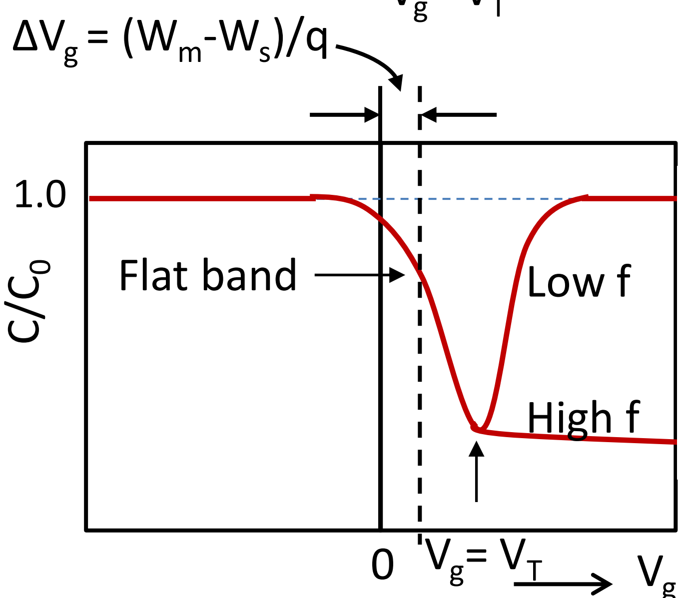


10.3 Non-ideal effects



Work function difference

$$V_T = 2\phi_{fp} + t_{ox}\sqrt{\frac{4eN_a\varepsilon_{Si}\phi_{fp}}{\varepsilon_{ox}^2}} = 2\phi_b + \frac{|Q_{SD}|}{C_{ox}}$$



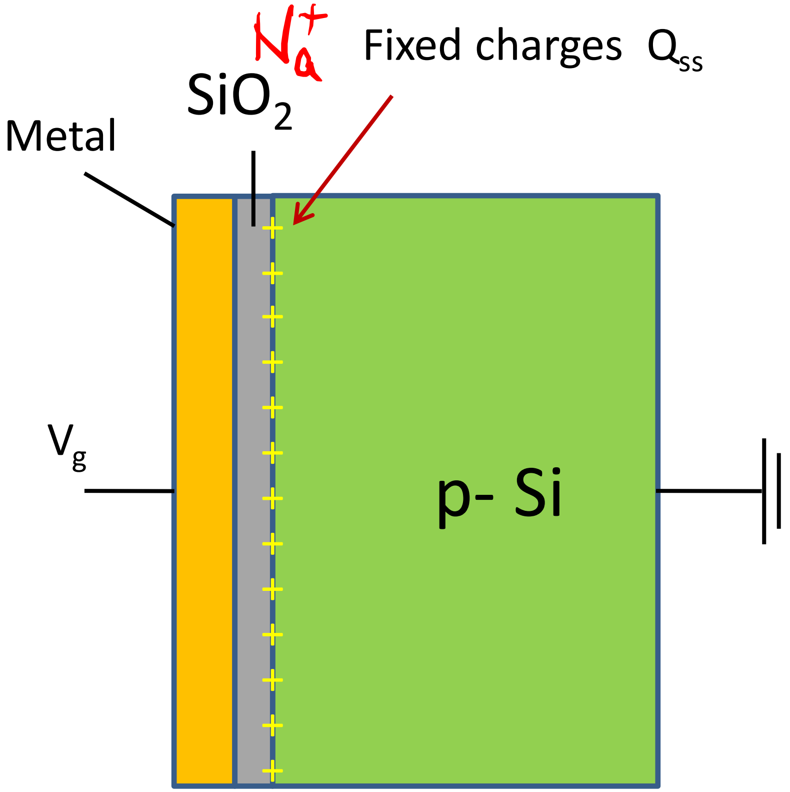
$$V_T = 2\phi_{fp} + t_{ox}\sqrt{\frac{4eN_a\varepsilon_{Si}\phi_{fp}}{\varepsilon_{ox}^2}} + V_{FB}$$

$$= 2\phi_{fp} + \frac{|Q_{SD}|}{C_{ox}} + \phi_{ms}$$

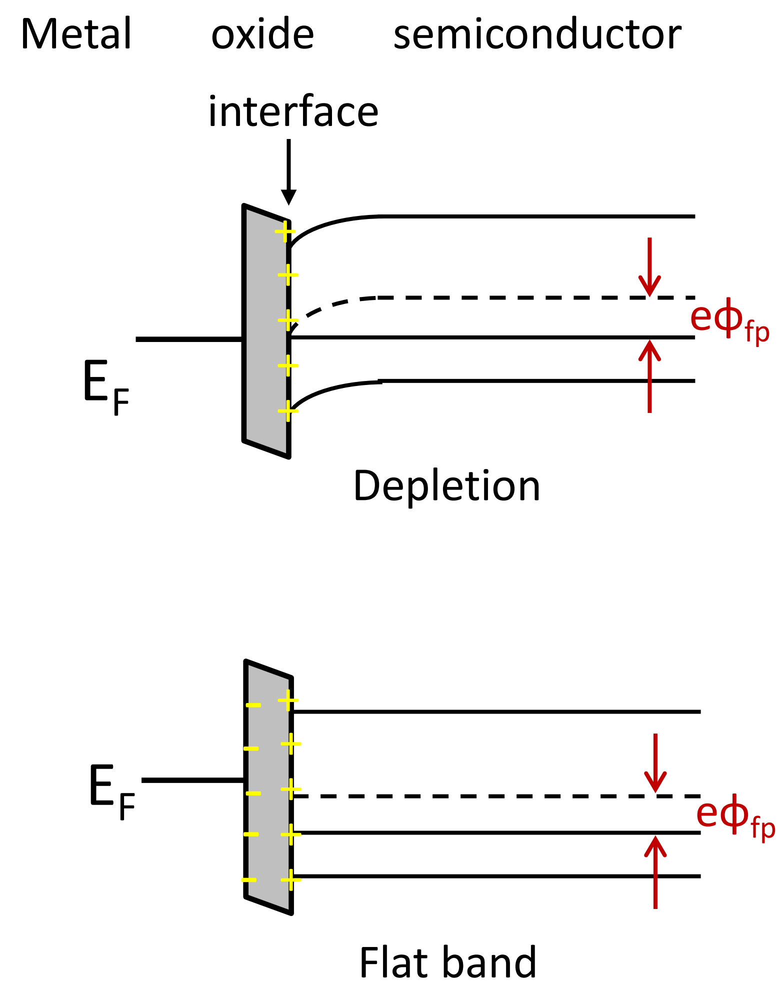
$$\frac{\phi_m - \phi_s}{e}$$

10.3 Non-ideal effects

Fixed charges



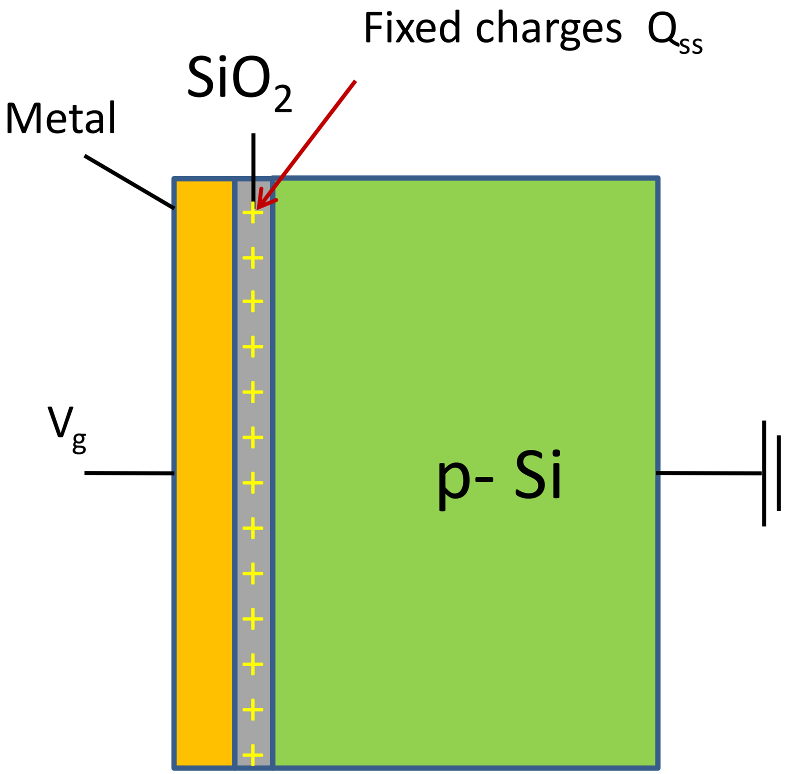
Metal-insulator-semiconductor (MIS)



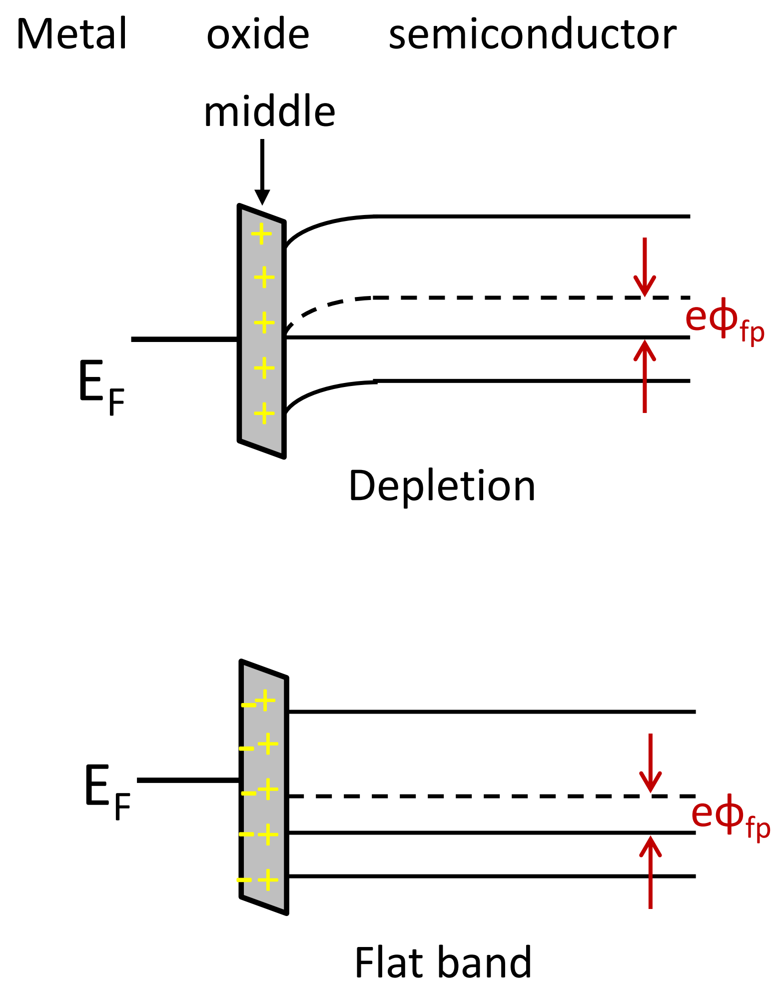
$$V_g = V_{FB} = -Q_{ss}/C$$

10.3 Non-ideal effects

Fixed charges



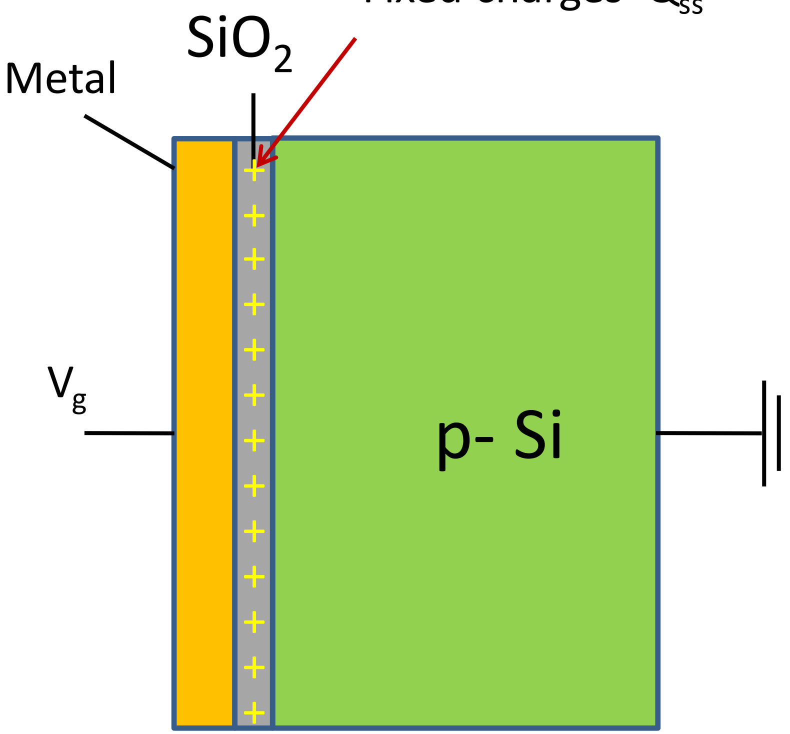
Metal-insulator-semiconductor (MIS)



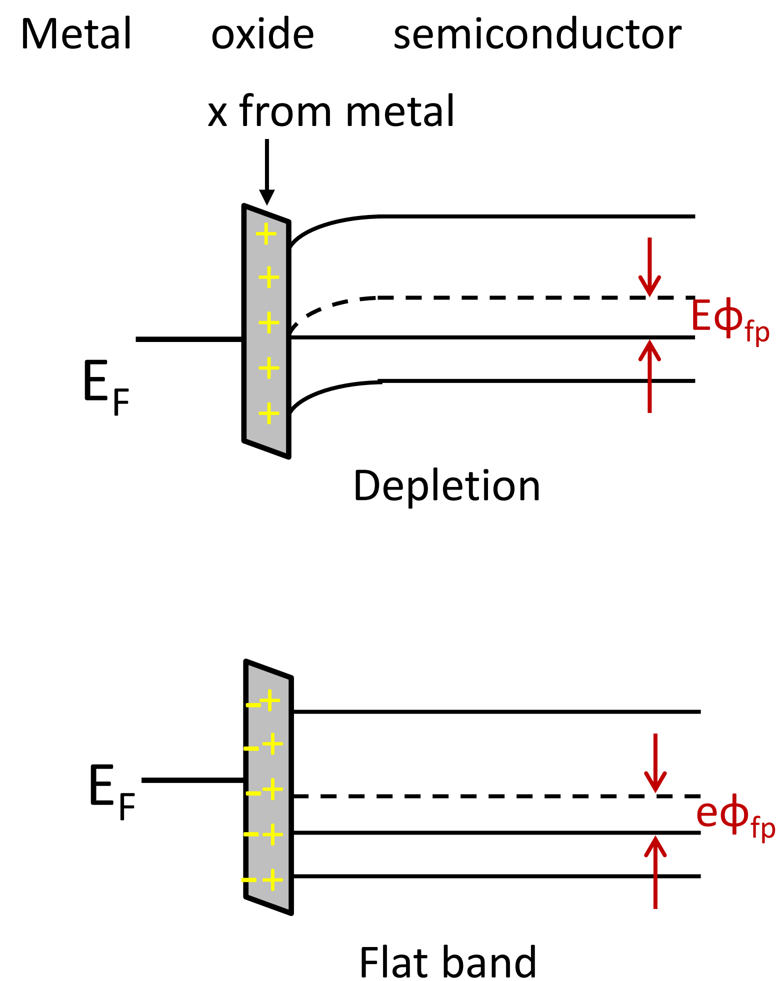
$$V_g = V_{FB} = -Q_{ss}/2C$$

10.3 Non-ideal effects

Fixed charges



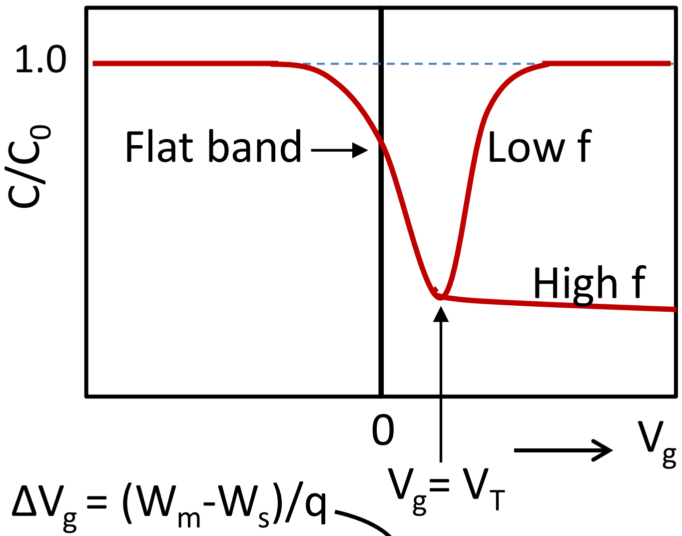
Metal-insulator-semiconductor (MIS)

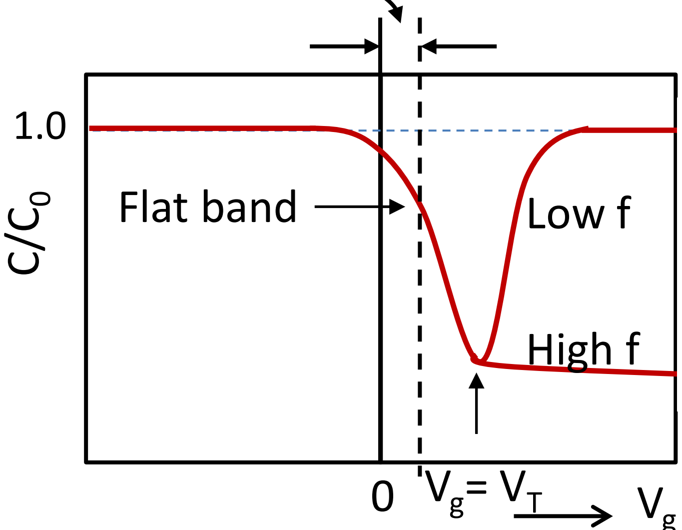


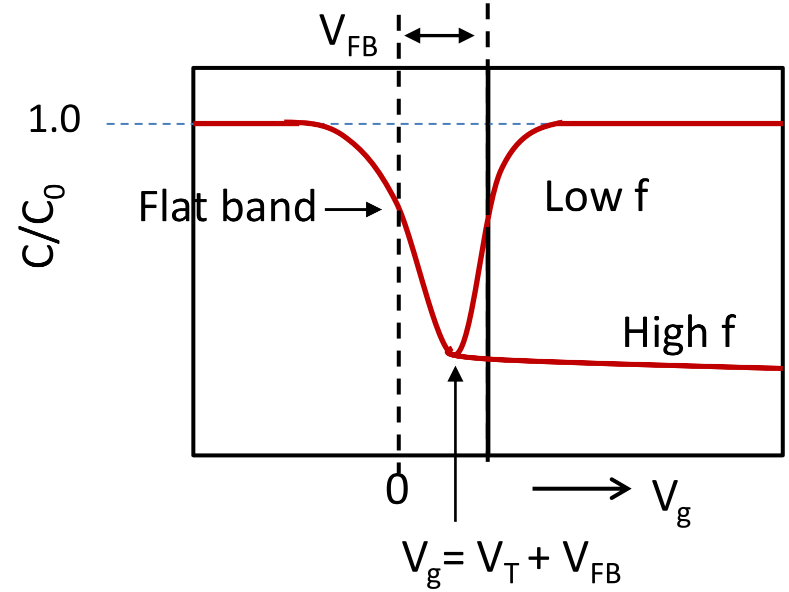
$$V_g = V_{FB} = -\frac{Q_{ss}}{C} \cdot \frac{x}{d}$$

10.3 Non-ideal effects

Fixed charges







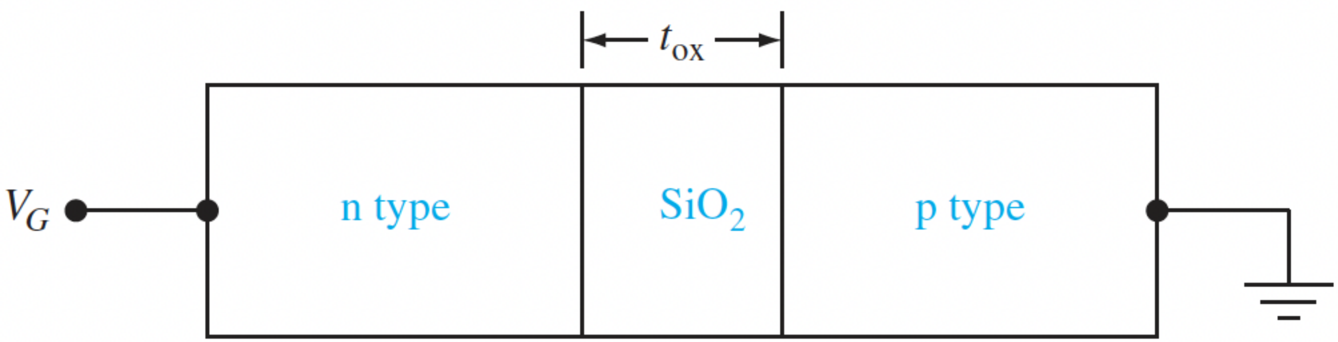
$$V_T = 2\phi_{fp} + t_{ox}\sqrt{\frac{4eN_a\varepsilon_{Si}\phi_{fp}}{\varepsilon_{ox}^2}} + V_{FB}$$

$$= 2\phi_{fp} + \frac{|Q_{SD}|}{C_{ox}} + \phi_{ms} - \frac{Q_{ss}}{C_{ox}}$$

Check your understanding

Problem Example #3

Consider an SOS capacitor as shown in Figure P10.29. Assume the SiO_2 is ideal (no trapped charge) and has a thickness of $t_{ox} = 500$ Å. The doping concentrations are $N_d = 10^{16}$ cm^{-3} and $N_a = 10^{16}$ cm^{-3}. (*a*) Sketch the energy-band diagram through the device for (*i*) flat band, (*ii*) $V_G = +3$ V, and (*iii*) $V_G = -3$ V. (*b*) Calculate the flat-band voltage. (*c*) Estimate the voltage across the oxide for (*i*) $V_G = +3$ V and (*ii*) $V_G = -3$ V. (*d*) Sketch the high-frequency *C–V* characteristic curve.



Check your understanding

Problem Example #3

Check your understanding

Problem Example #3

Check your understanding

Problem Example #3

Check your understanding

Problem Example #4

Objective: Calculate the threshold voltage of a MOS system using an aluminum gate.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{15}$ cm^{-3}. Let $Q'_{ss} = 10^{10}$ cm^{-2}, $t_{ox} = 12$ nm $= 120$ Å, and assume the oxide is silicon dioxide.

Check your understanding

Problem Example #4

Outline

10.1 The two-terminal MOS structure

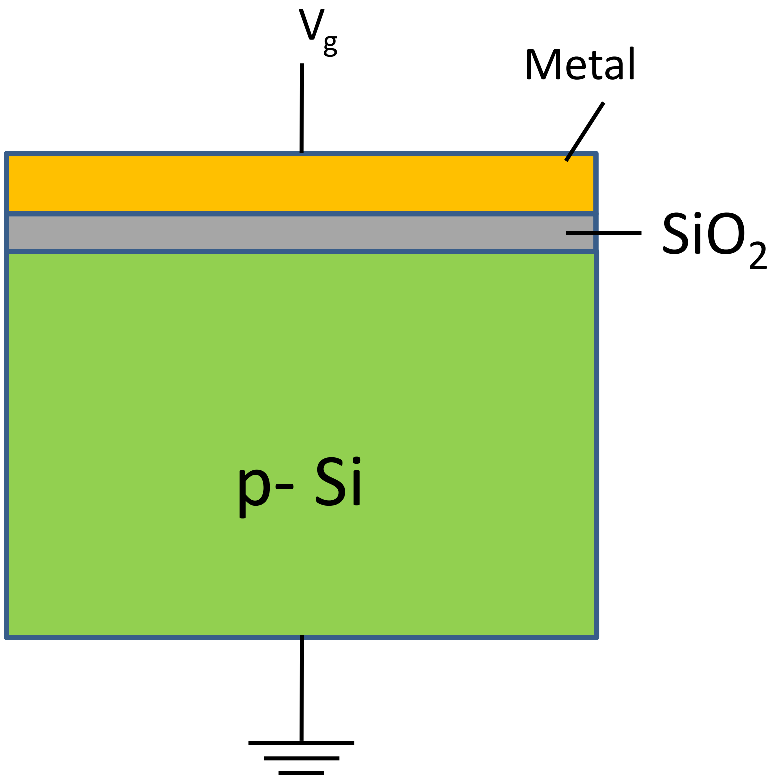
10.2 Capacitance-voltage characteristics

10.3 Non-ideal effects

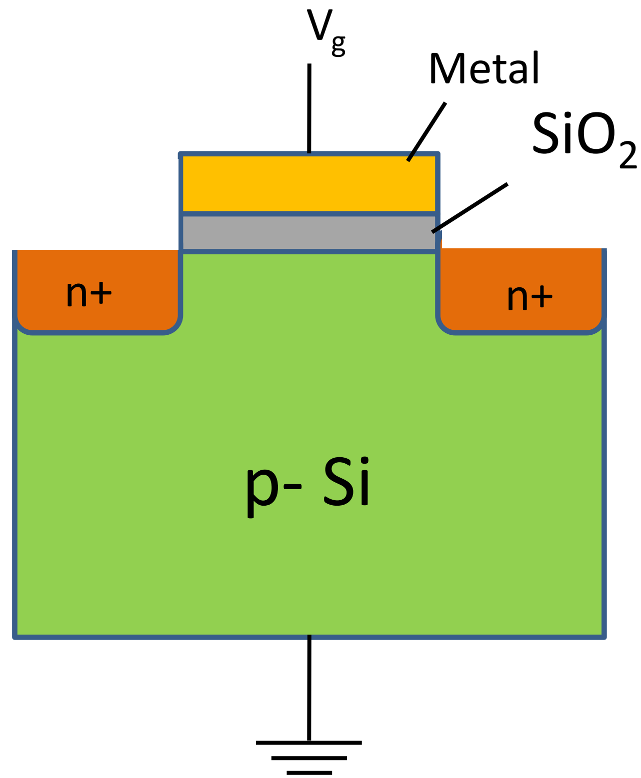
10.4 The basic MOSFET operation

10.4 The basic MOSFET operation

Metal-Oxide-Semiconductor field effect transistor: MOSFET



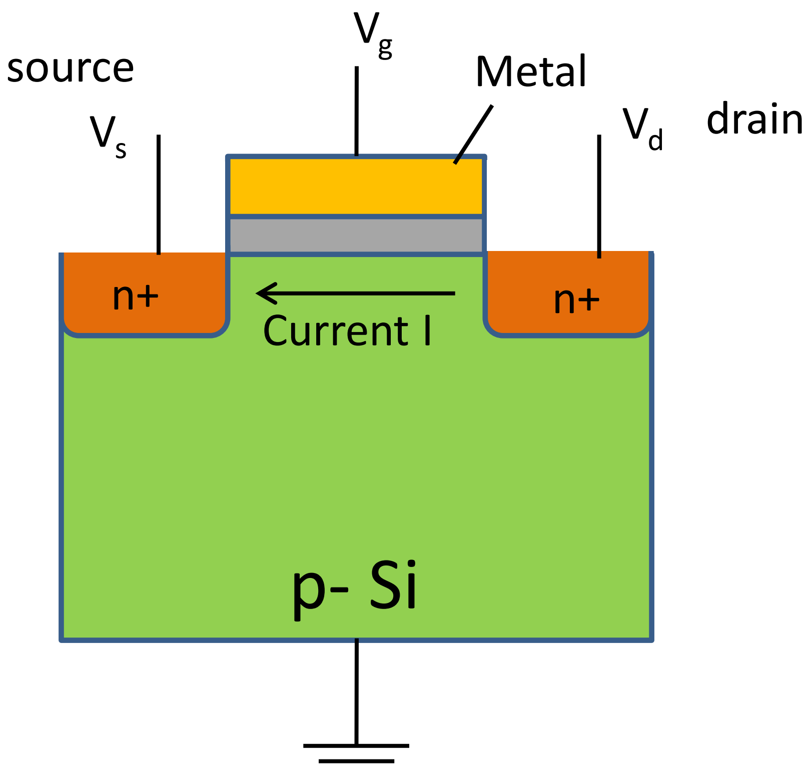
MOS capacitor

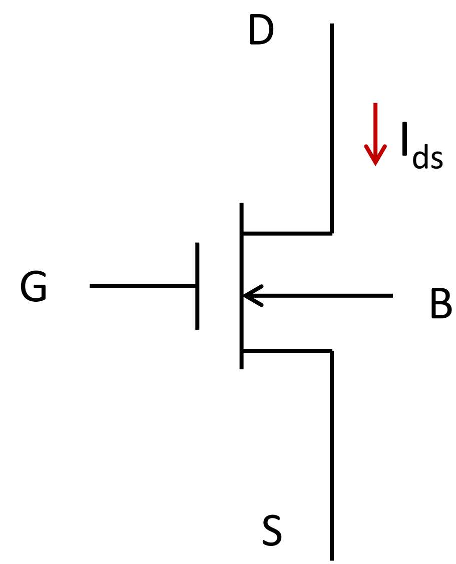


MOSFET

10.4 The basic MOSFET operation

Metal-Oxide-Semiconductor field effect transistor: MOSFET

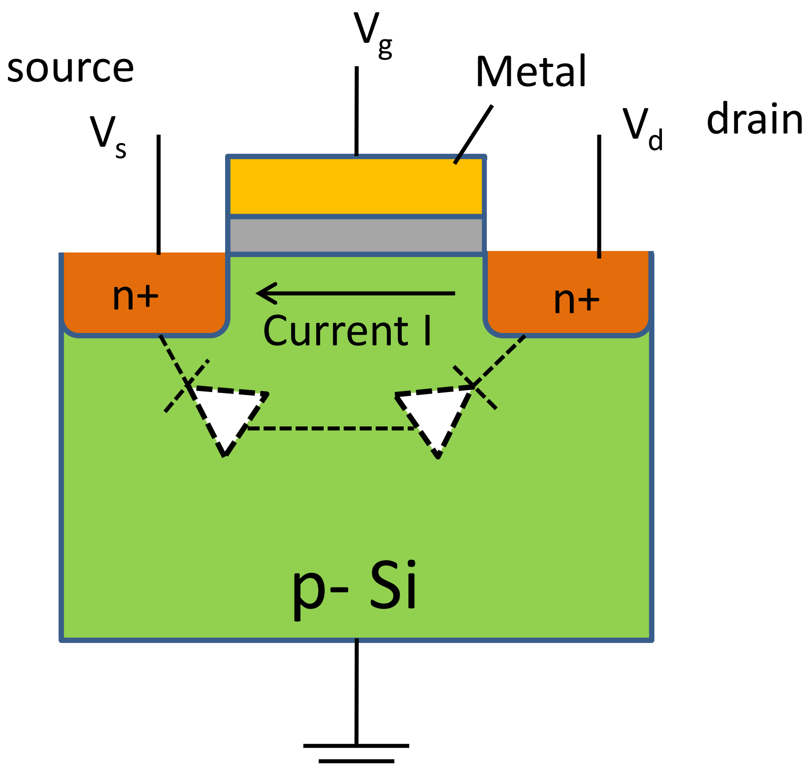




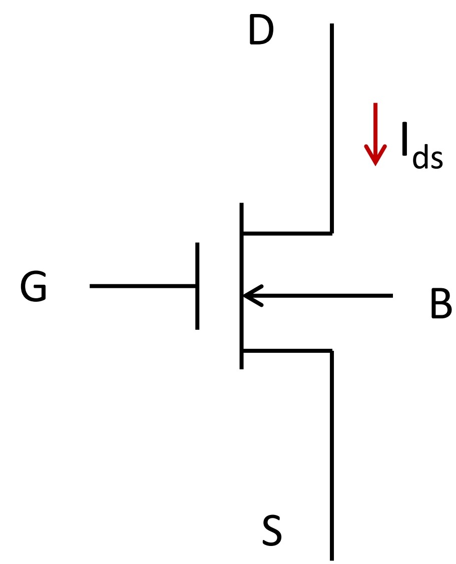
Metal-oxide-semiconductor (MOS)

10.4 The basic MOSFET operation

Metal-Oxide-Semiconductor field effect transistor: MOSFET

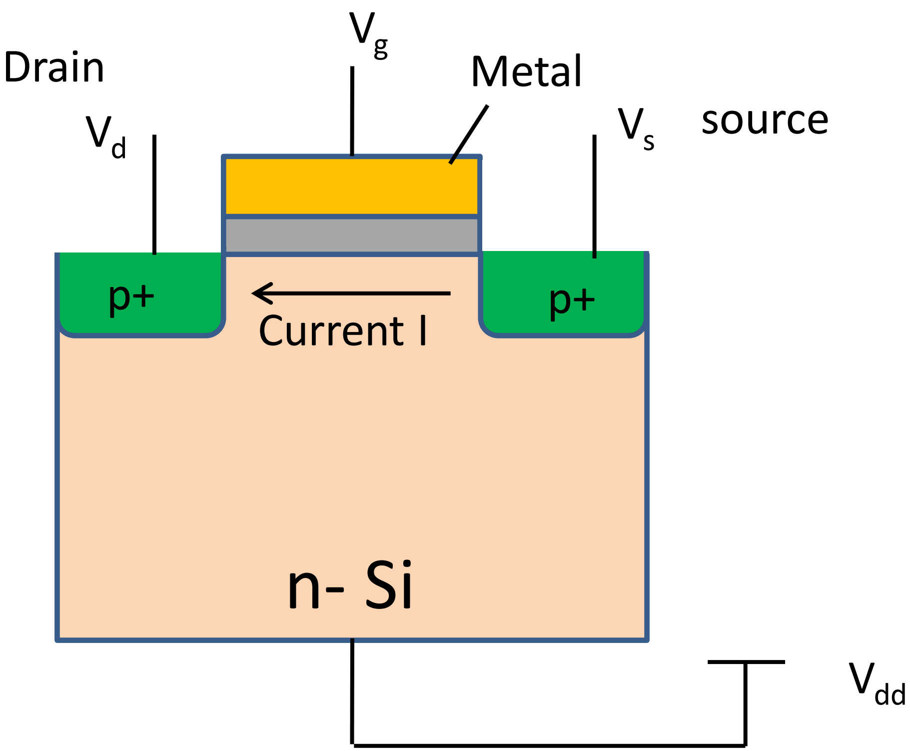


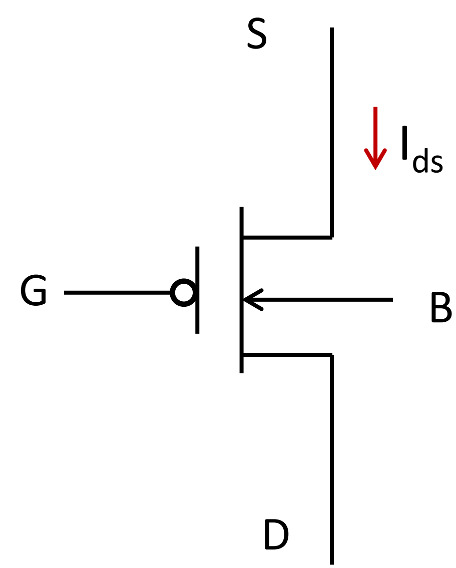
MOSFET



10.4 The basic MOSFET operation

Metal-Oxide-Semiconductor field effect transistor: p-type MOSFET

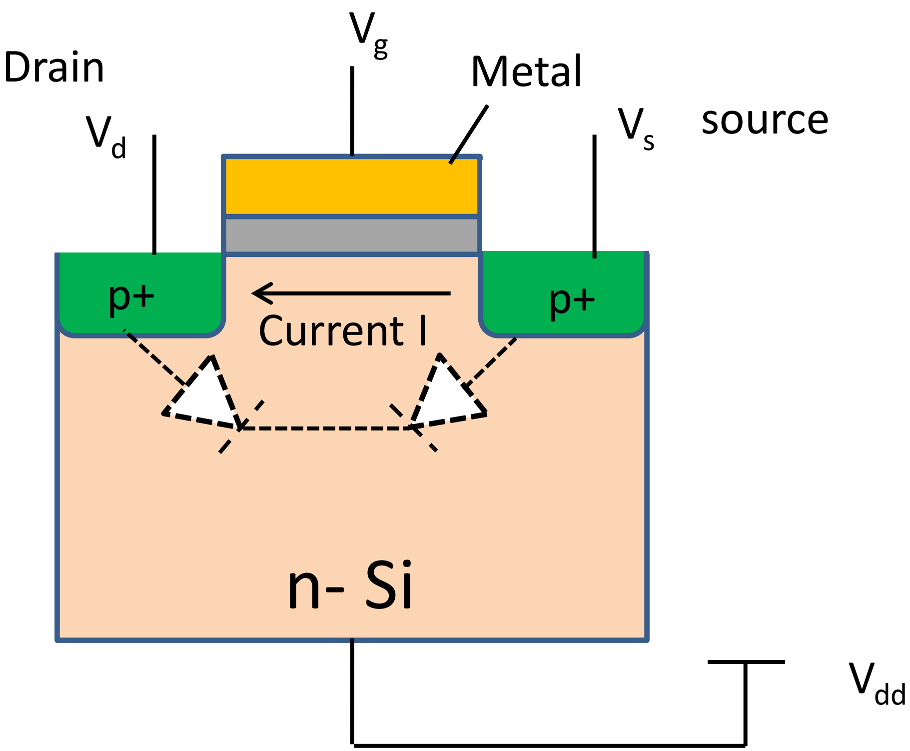




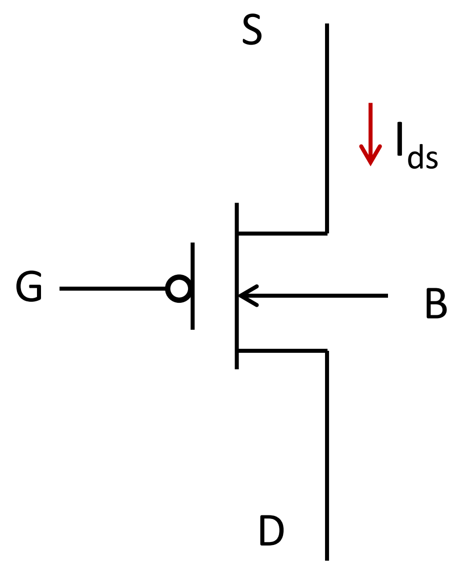
P-type MOSFET

10.4 The basic MOSFET operation

Metal-Oxide-Semiconductor field effect transistor: P MOSFET

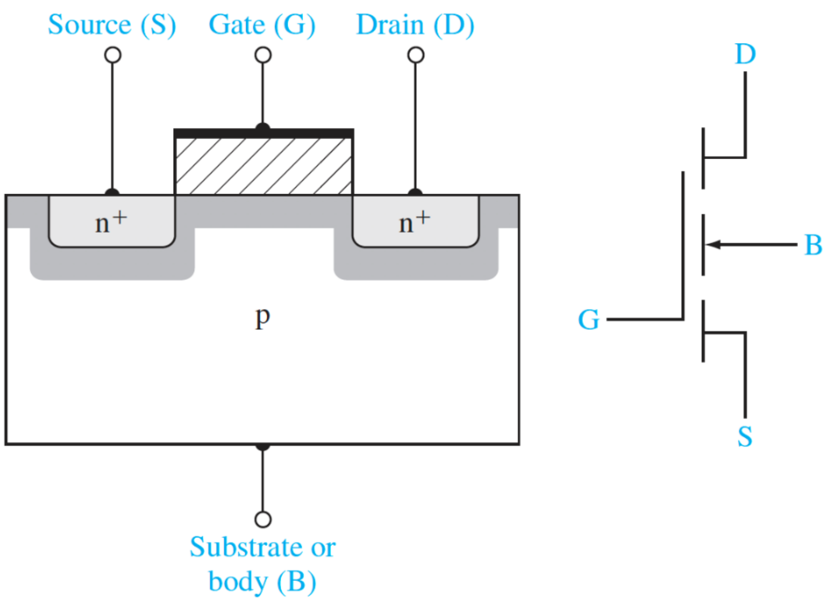


P-type MOSFET

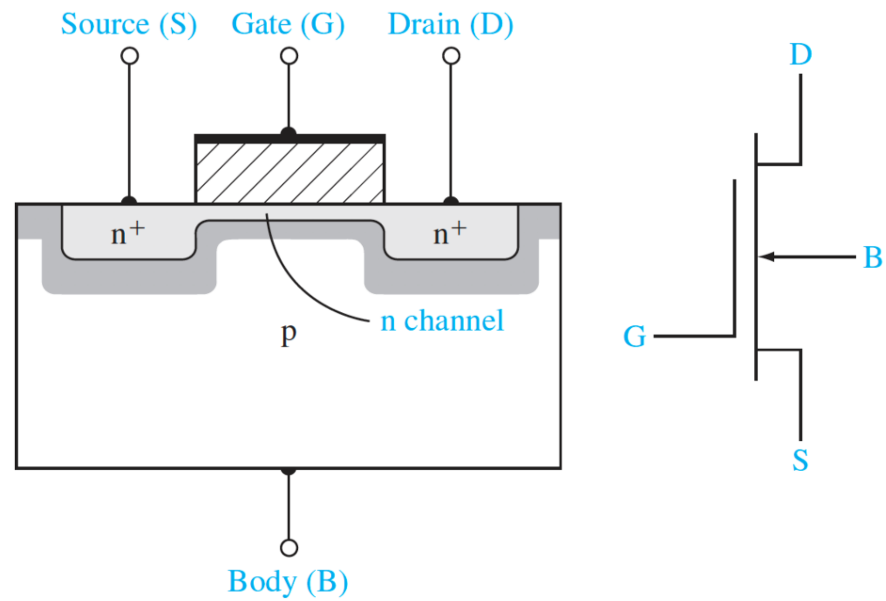


10.4 The basic MOSFET operation

MOSFET structures



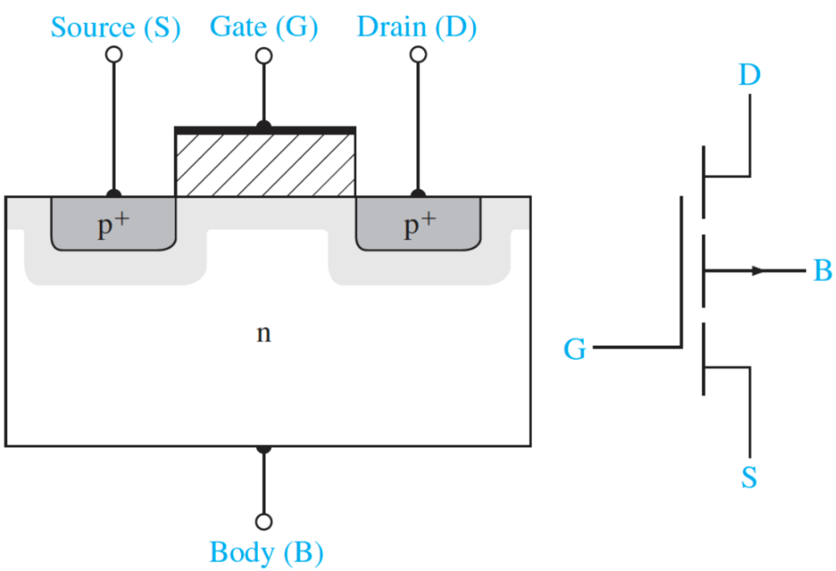
NMOS Enhancement mode



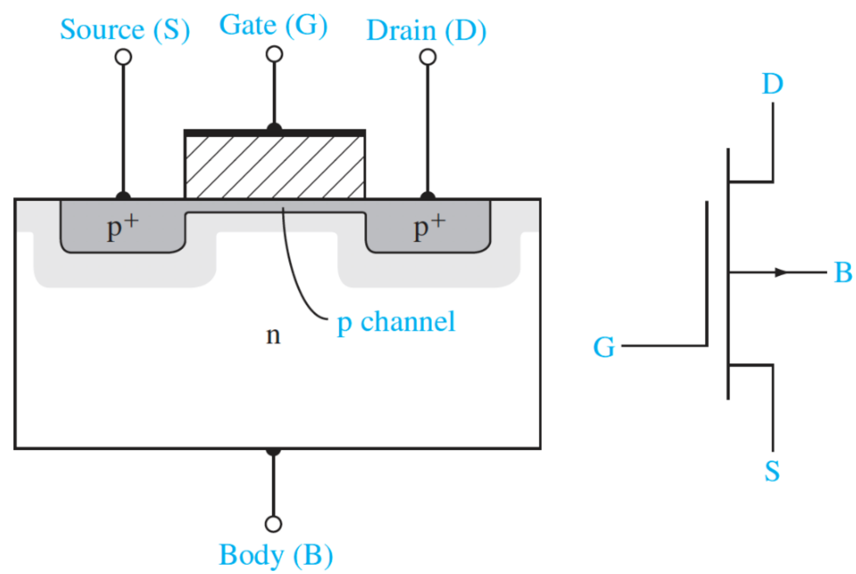
NMOS Depletion mode

10.4 The basic MOSFET operation

MOSFET structures



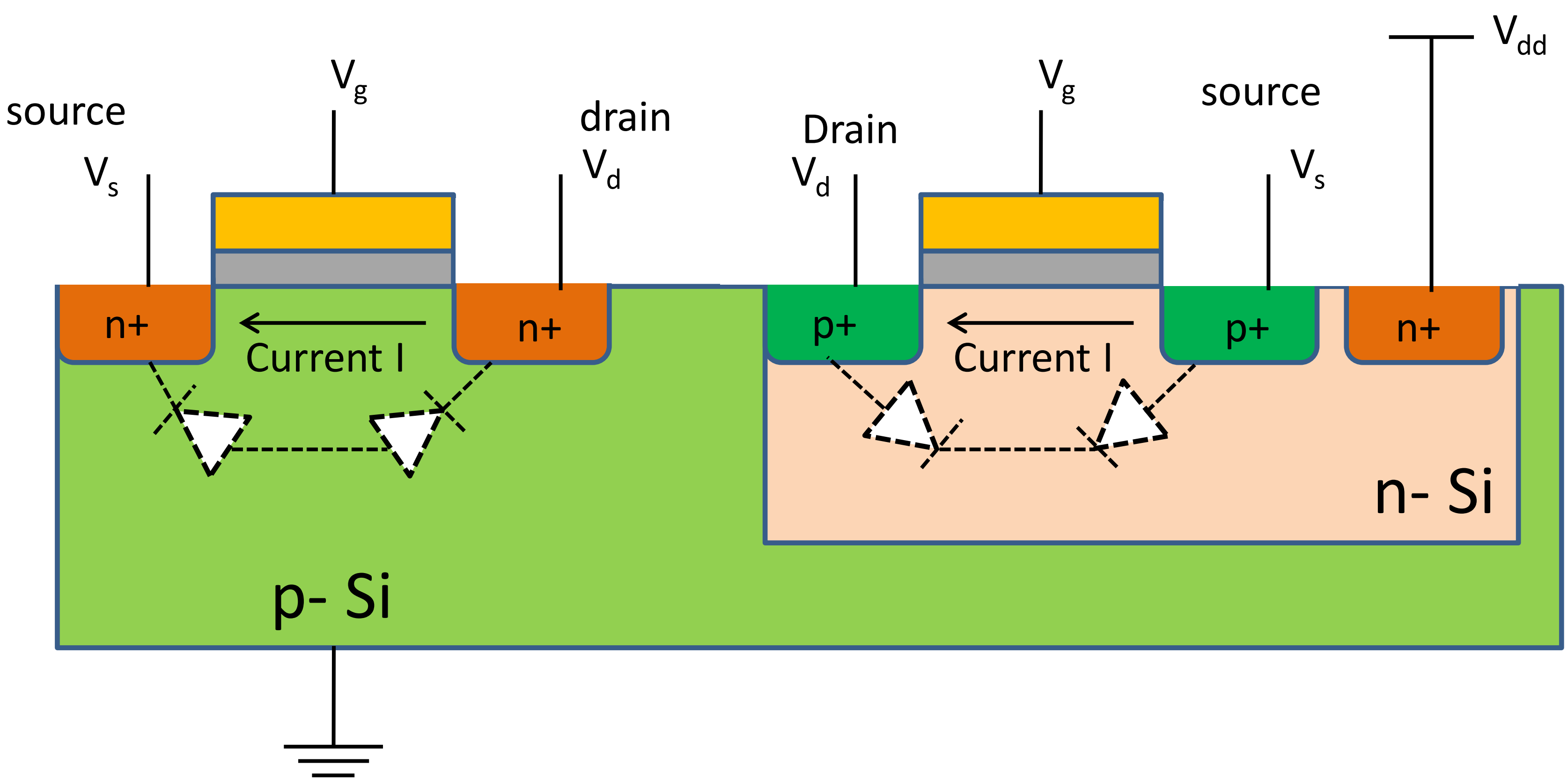
PMOS Enhancement mode



PMOS Depletion mode

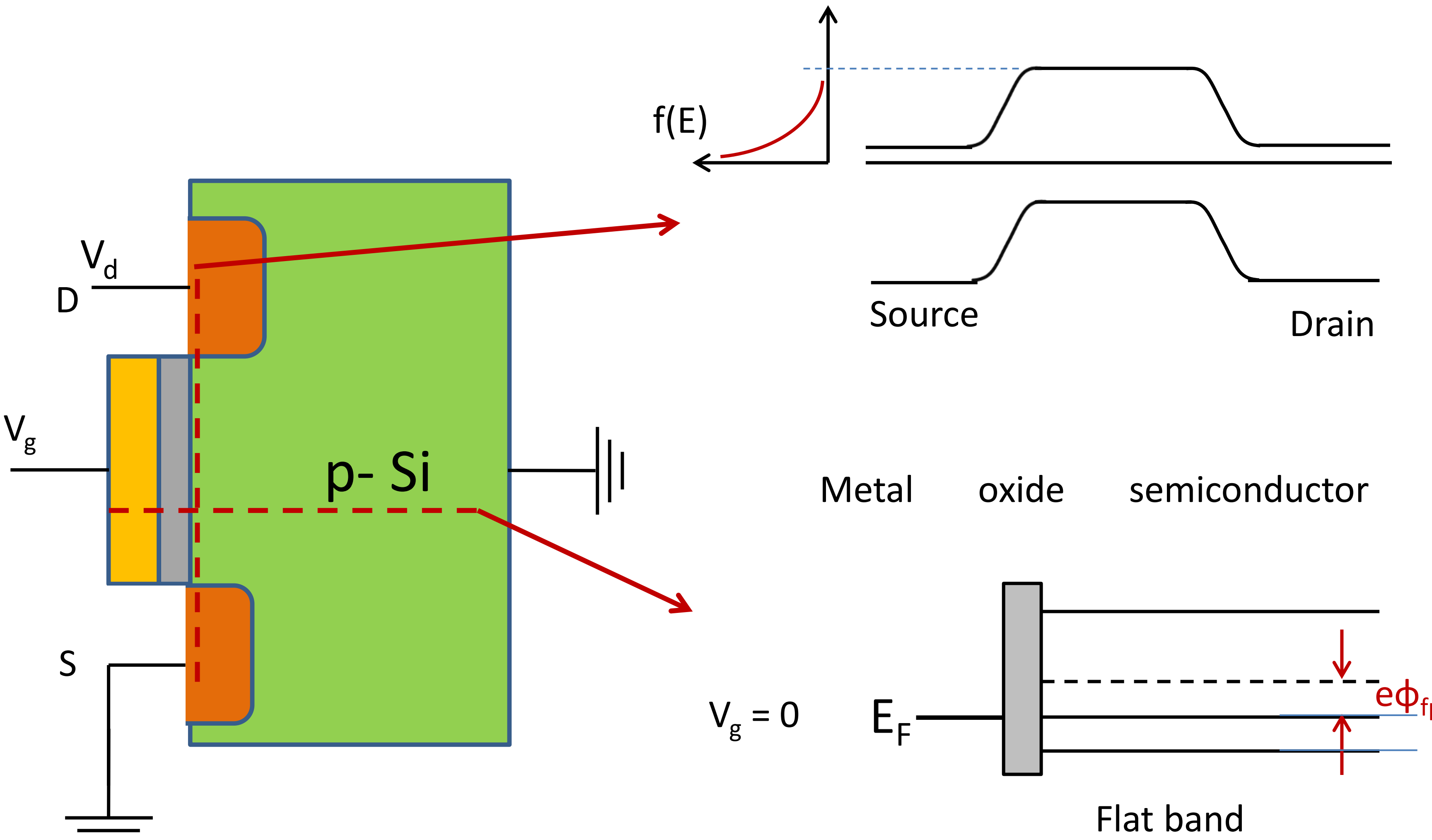
10.4 The basic MOSFET operation

Metal-Oxide-Semiconductor field effect transistor: CMOS

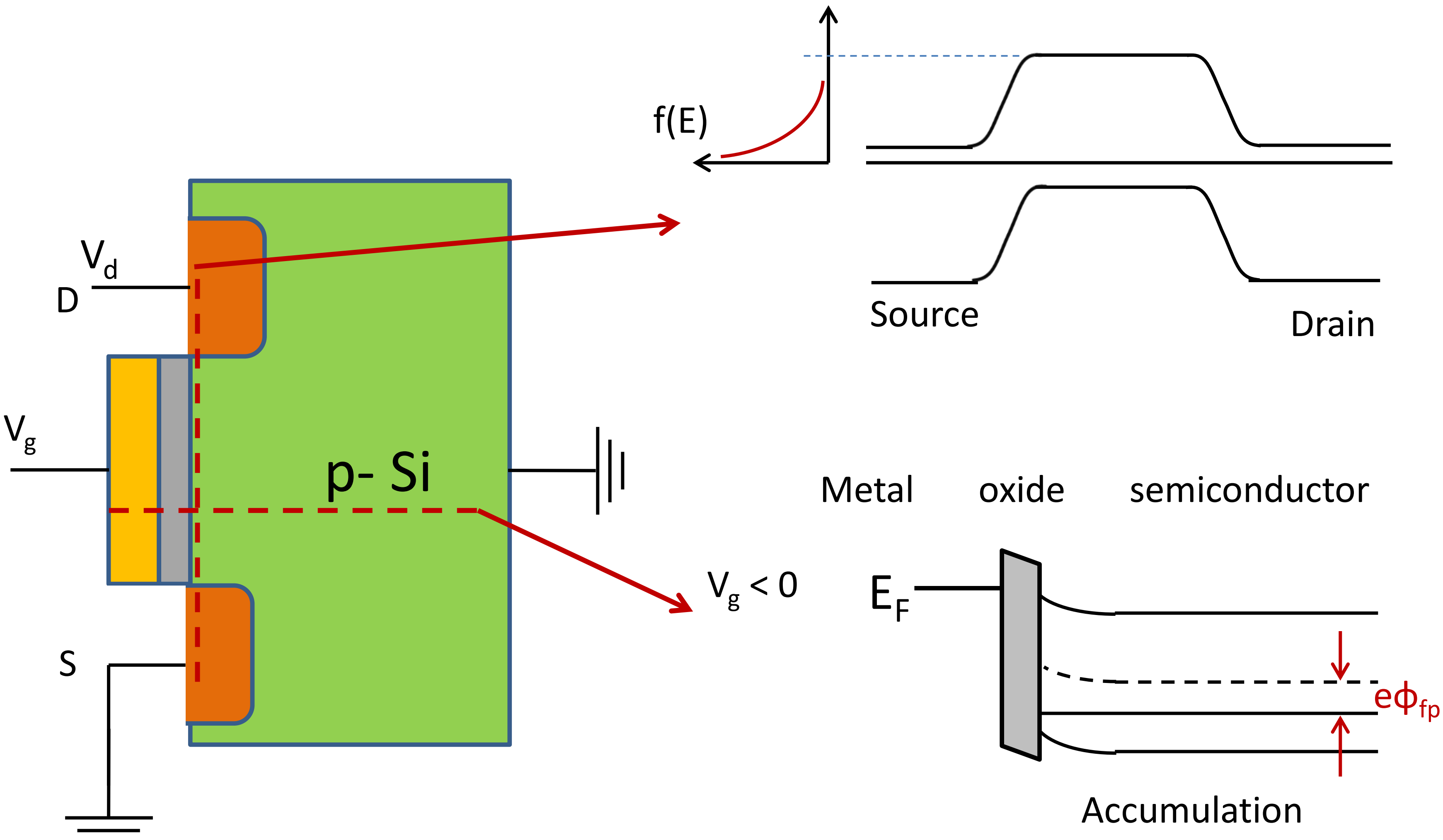


Complementary Metal-oxide-semiconductor (CMOS) field effect transistors

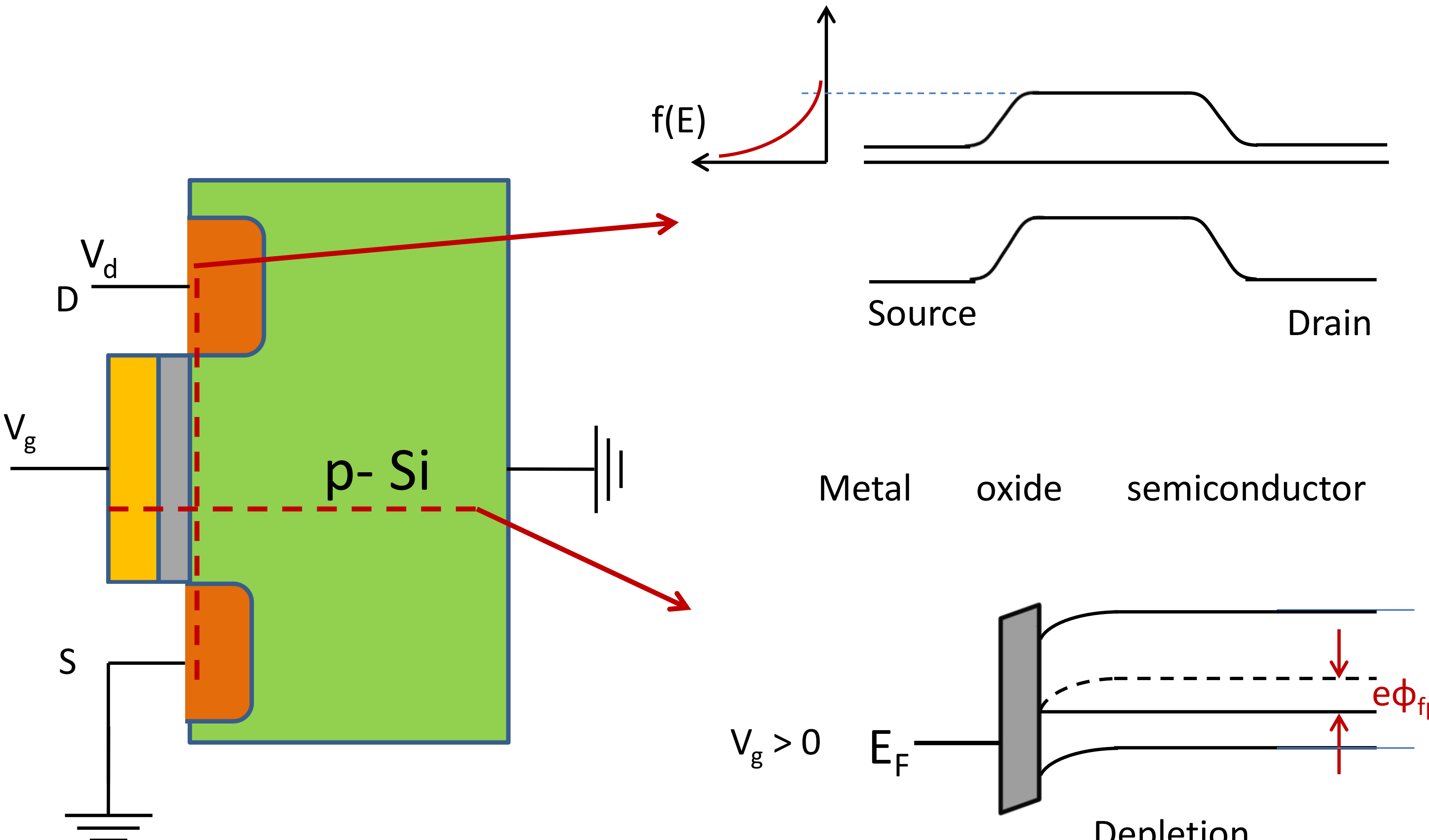
10.4 The basic MOSFET operation



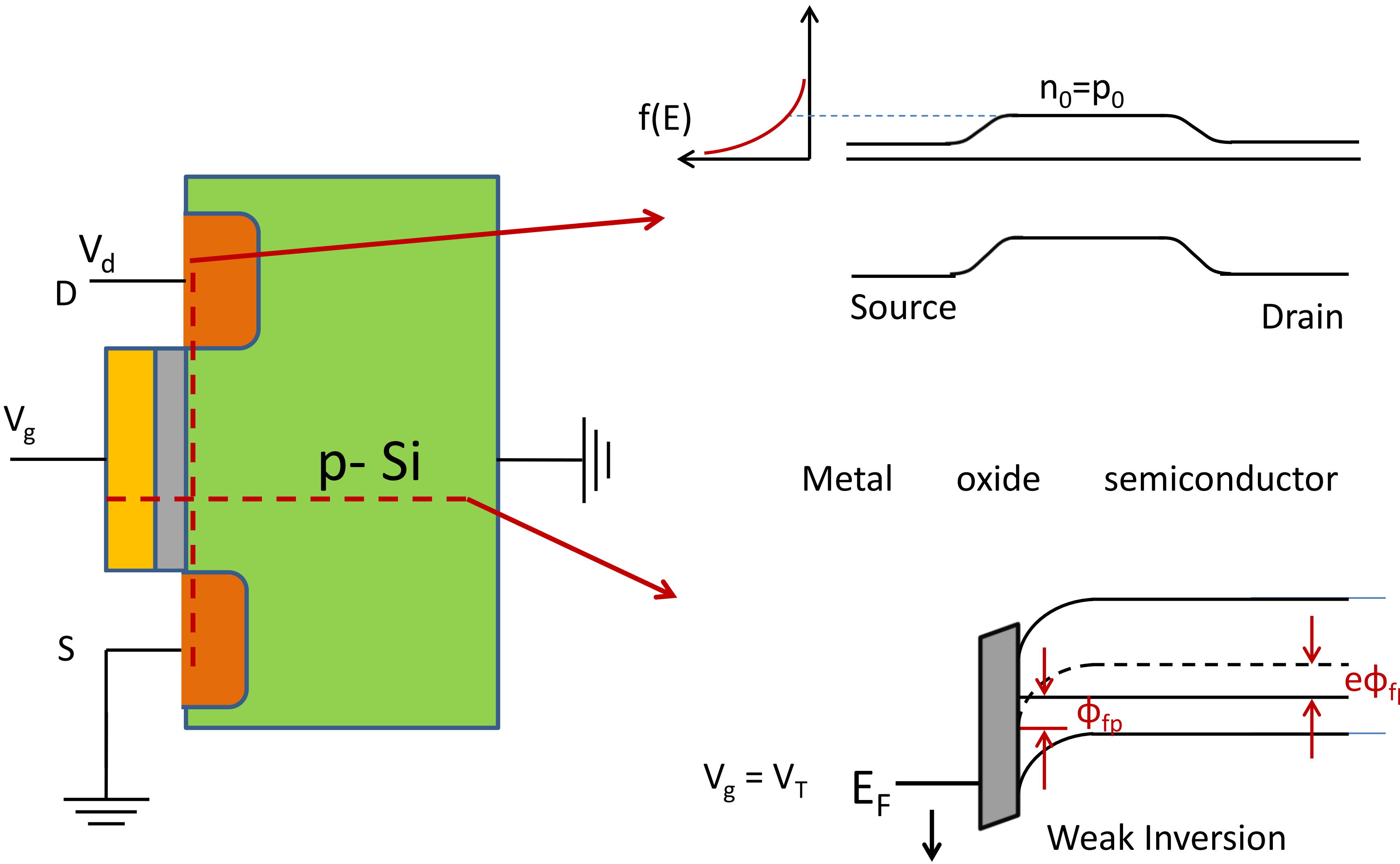
10.4 The basic MOSFET operation



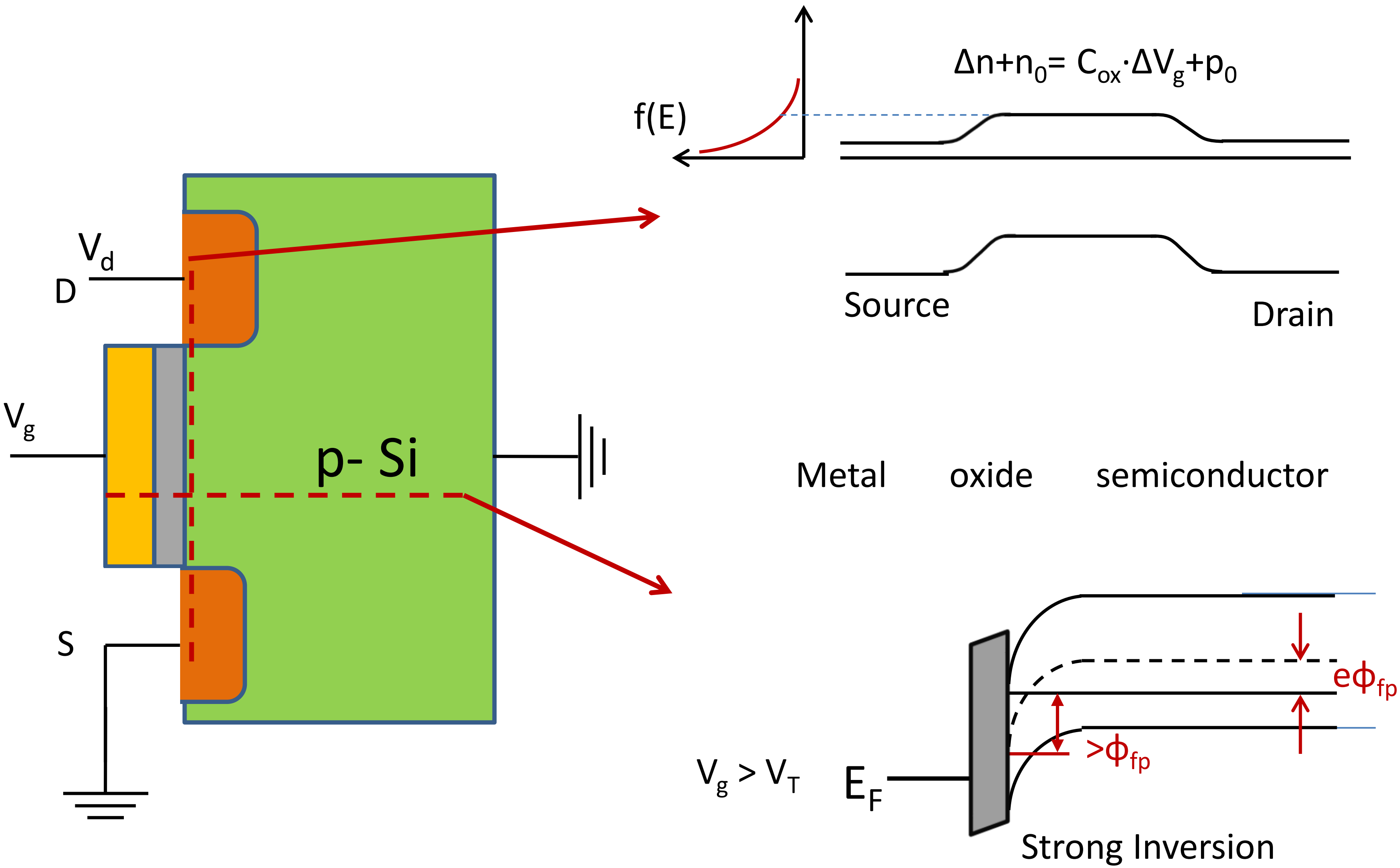
10.4 The basic MOSFET operation



10.4 The basic MOSFET operation

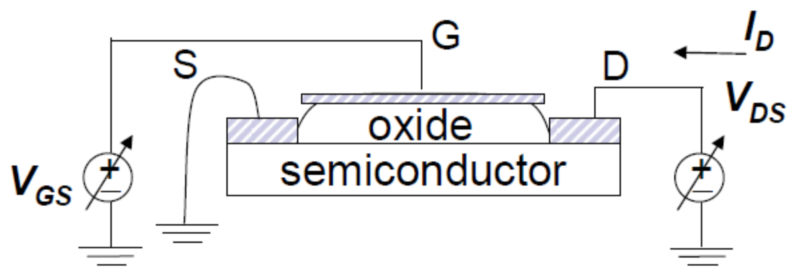


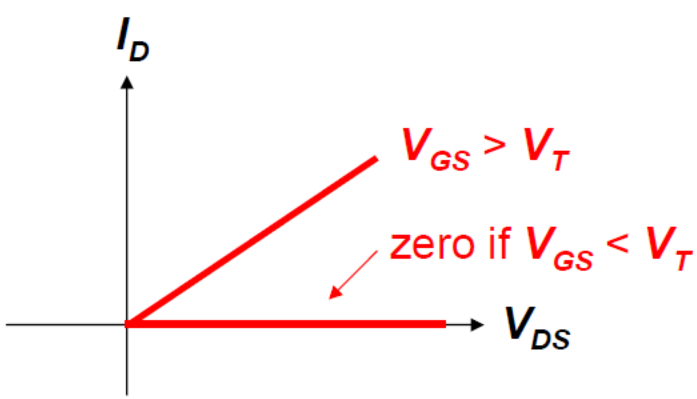
10.4 The basic MOSFET operation



NMOSFET I_D vs. V_{DS} Characteristics

Next consider I_D (flowing into **D**) versus V_{DS}, as V_{GS} is varied:





Above threshold ($V_{GS} > V_T$): "inversion layer" of electrons appears, so conduction between **S** and **D** is possible

Below "threshold" ($V_{GS} < V_T$): no charge → no conduction

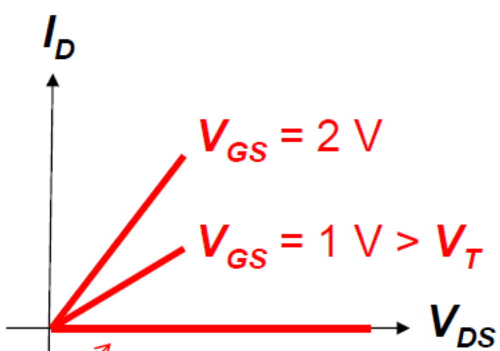
Current-voltage characteristics

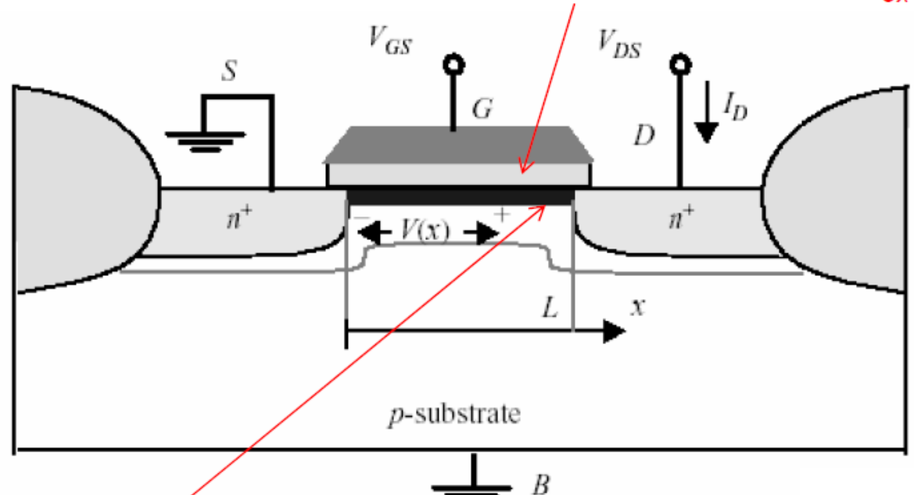
The MOSFET as a Controlled Resistor

- The MOSFET behaves as a resistor when V_{DS} is low:
  - Drain current I_D increases linearly with V_{DS}
  - Resistance R_{DS} between SOURCE & DRAIN depends on V_{GS}
    - R_{DS} is lowered as V_{GS} increases above V_T

oxide thickness $\equiv t_{ox}$

NMOSFET Example:





I_{DS} = 0 if $V_{GS} < V_T$

Inversion charge density $Q_i(x) = -C_{ox}[V_{GS}-V_T-V(x)]$
where $C_{ox} \equiv \varepsilon_{ox} / t_{ox}$

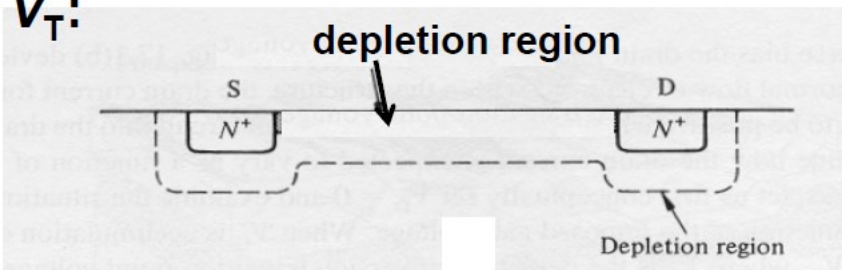
10.4 The basic MOSFET operation

Derivation of I_{ds} vs V_{ds} and V_{gs}

10.4 The basic MOSFET operation

Charge in an N-Channel MOSFET

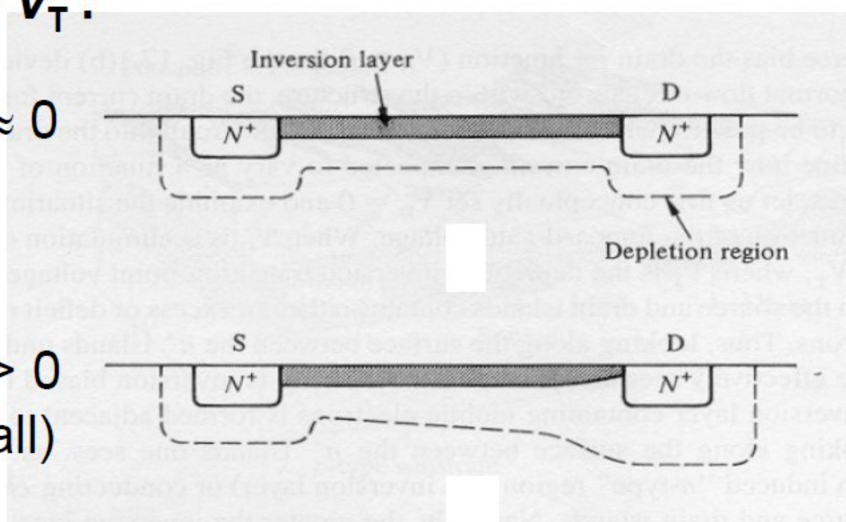
$V_{GS} < V_T$:



(no inversion layer at surface)

$V_{GS} > V_T$:

$V_{DS} \approx 0$



$V_{DS} > 0$ (small)

$$I_D = WQ_{inv}v$$
$$= WQ_{inv}\mu_n E$$
$$= WQ_{inv}\mu_n\left(\frac{V_{DS}}{L}\right)$$

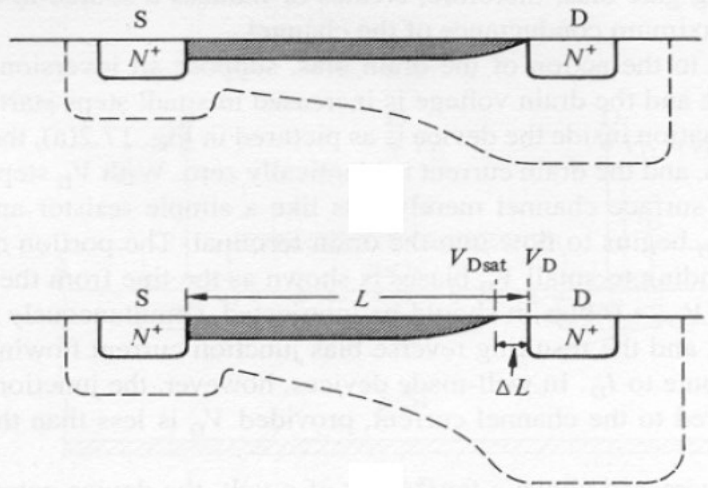
Average electron velocity ***v*** is proportional to lateral electric field ***E***

10.4 The basic MOSFET operation

What Happens at Larger V_{DS}?

$V_{GS} > V_T$:

$V_{DS} = V_{GS} - V_T$



$V_{DS} > V_{GS} - V_T$

Inversion-layer is "pinched-off" at the drain end

As V_{DS} increases above $V_{GS} - V_T \equiv V_{DSAT}$,

the length of the "pinch-off" region ΔL increases:

- "extra" voltage ($V_{DS} - V_{Dsat}$) is dropped across the distance ΔL
- the voltage dropped across the inversion-layer "resistor" remains V_{Dsat}

$\Rightarrow$ the drain current I_D saturates

Note: Electrons are swept into the drain by the E-field when they enter the pinch-off region.

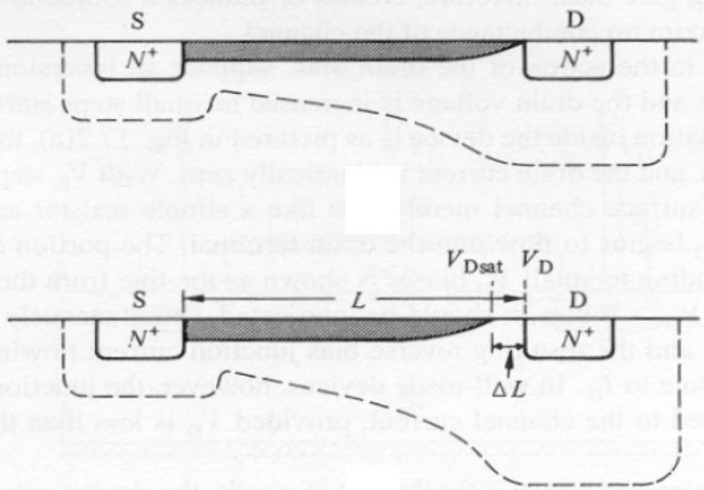
10.4 The basic MOSFET operation

What Happens at Larger V_{DS}?

$V_{GS} > V_T$:

$V_{DS} = V_{GS} - V_T$

$V_{DS} > V_{GS} - V_T$



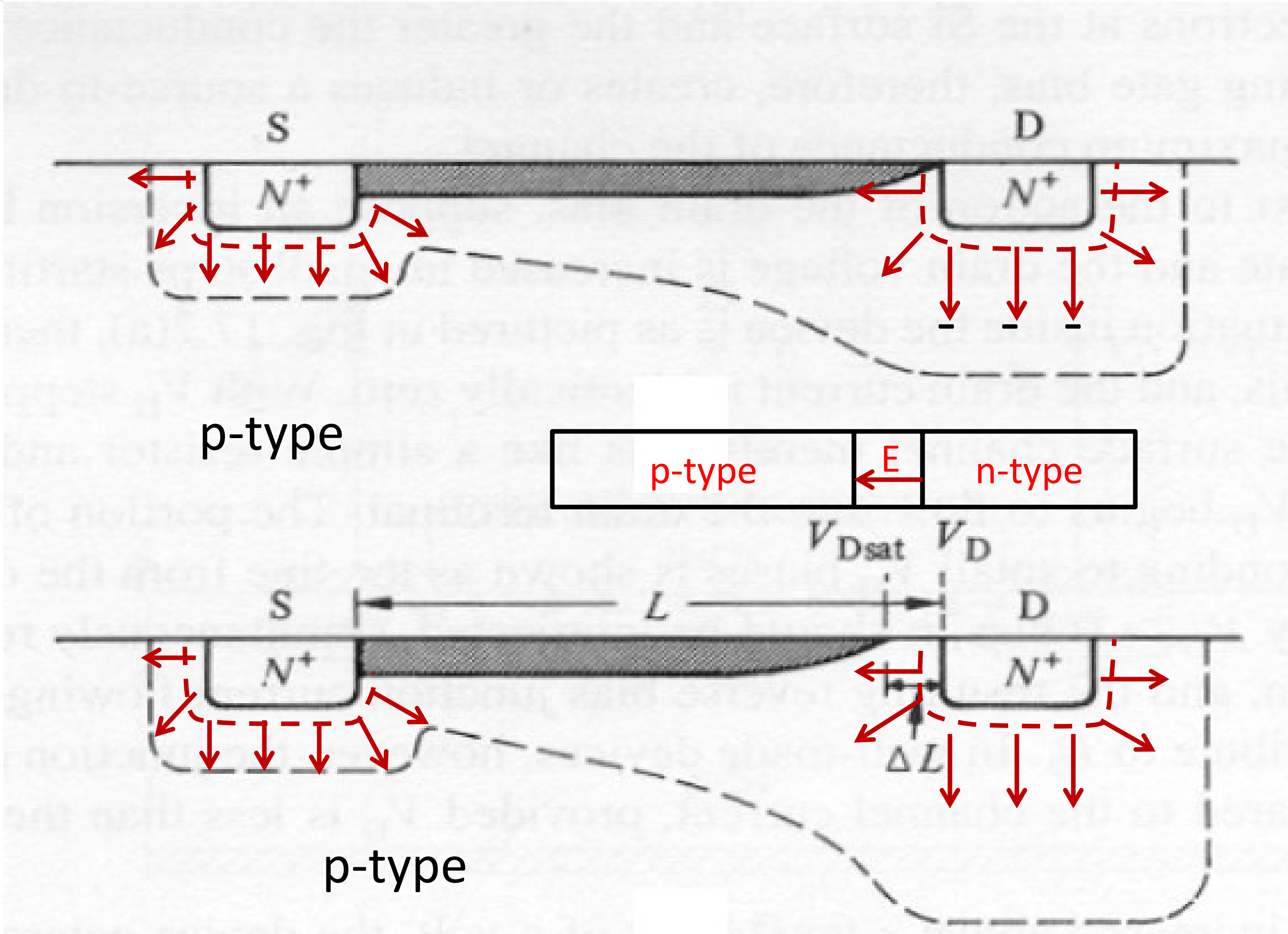
Inversion-layer is "pinched-off" at the drain end

As V_{DS} increases above $V_{GS} - V_T \equiv V_{DSAT}$,

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)V_{DS}$$

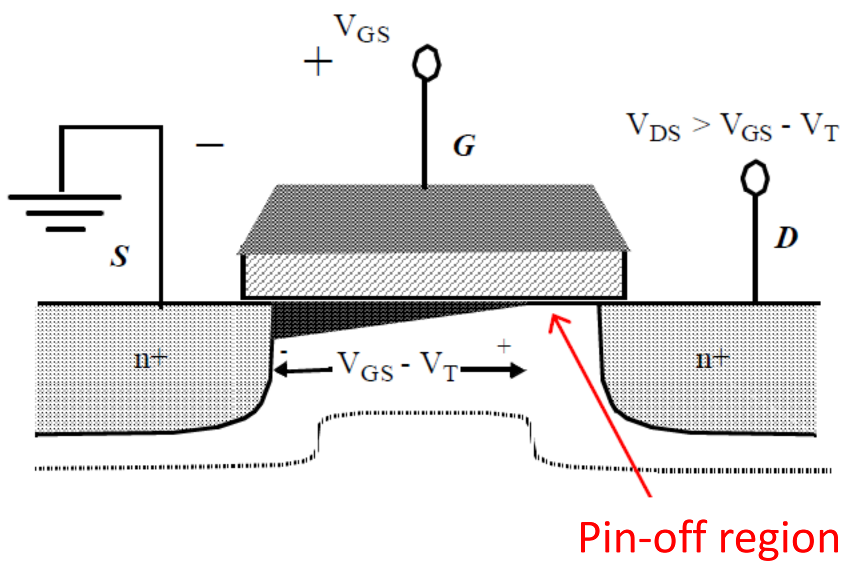
I_D will not increase after $V_{DS} \geq V_{GS} - V_T$

10.4 The basic MOSFET operation



Summary of I_D vs. V_{DS}

- As V_{DS} increases, the inversion-layer charge density at the drain end of the channel is reduced; therefore, I_D does not increase linearly with V_{DS}.
- When V_{DS} reaches $V_{GS} - V_T$, the channel is "pinched off" at the drain end, and I_D saturates (*i.e.* it does not increase with further increases in V_{DS}).



$$\boxed{I_{DSAT} = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2}$$

10.4 The basic MOSFET operation

I_D vs. V_{DS} Characteristics

The MOSFET I_D-V_{DS} curve consists of two regions:

1) Resistive or "Triode" Region: $0 < V_{DS} < V_{GS} - V_T$

$$I_D = k_n' \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

where $k_n' = \mu_n C_{ox}$

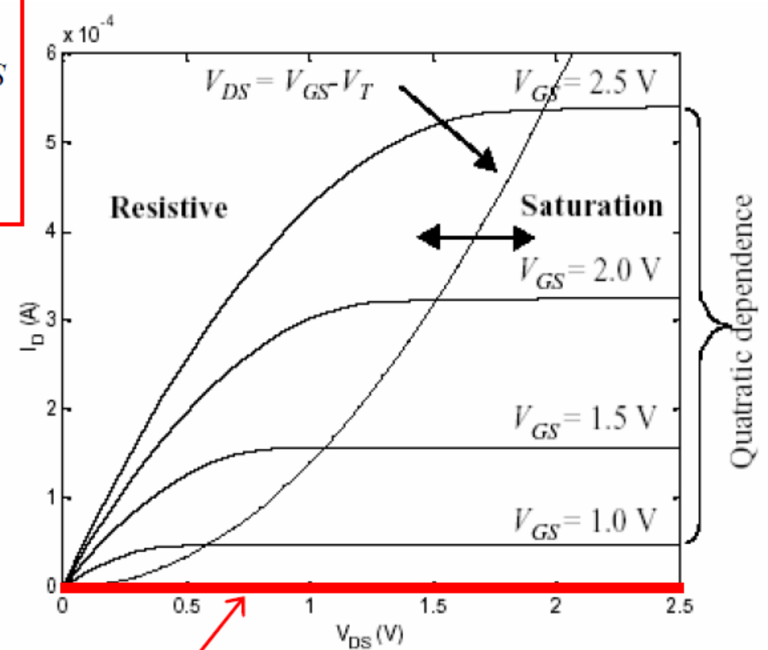
process transconductance parameter

2) Saturation Region:

$V_{DS} > V_{GS} - V_T$

$$I_{DSAT} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

where $k_n' = \mu_n C_{ox}$

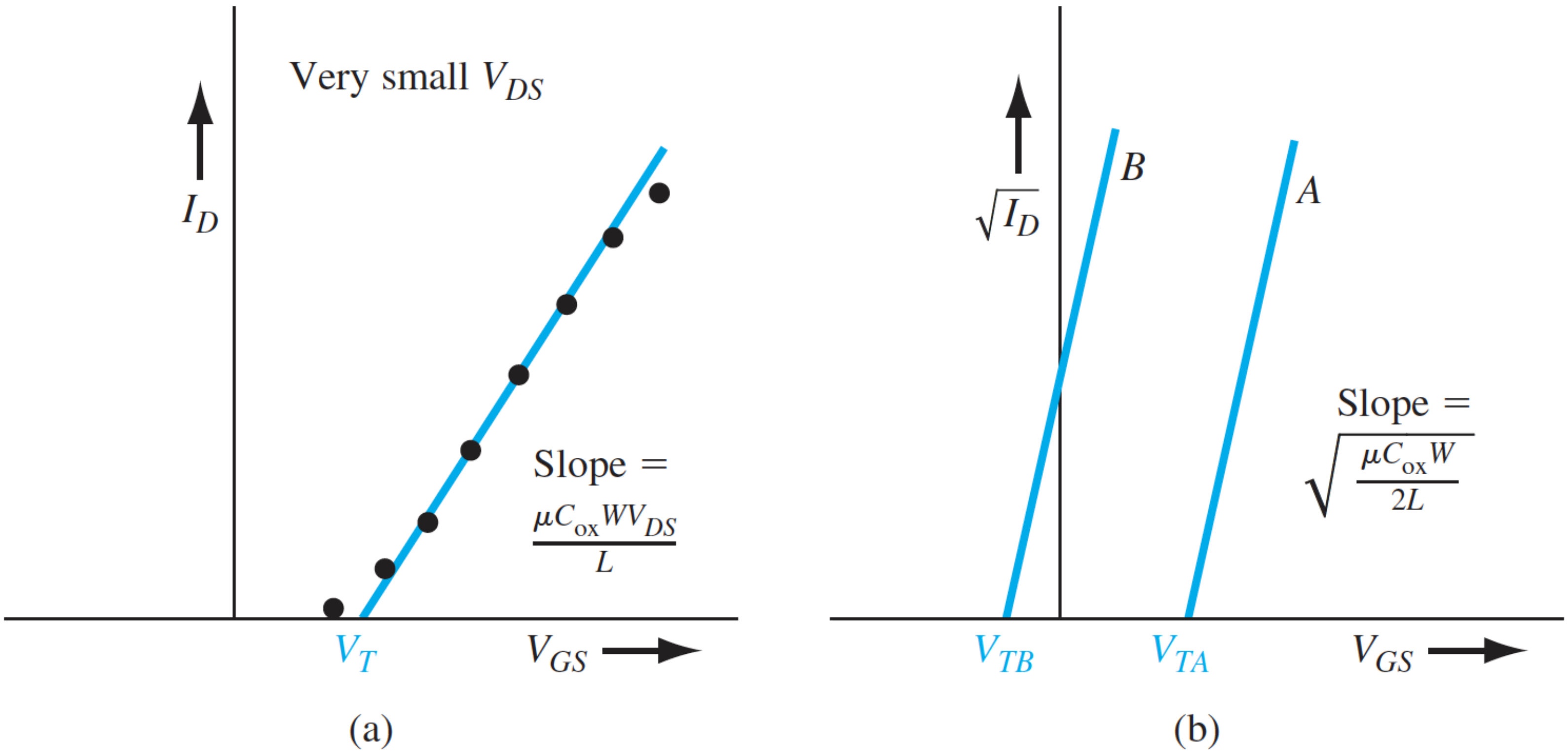


"CUTOFF" region: $V_G < V_T$

10.4 The basic MOSFET operation

$$I_D = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)V_{DS}$$

$$\sqrt{I_D(\text{sat})} = \sqrt{\frac{W\mu_n C_{ox}}{2L}}(V_{GS} - V_T)$$



Check your understanding

Problem example 5

Objective: Design the width of a MOSFET such that a specified current is induced for a given applied bias.

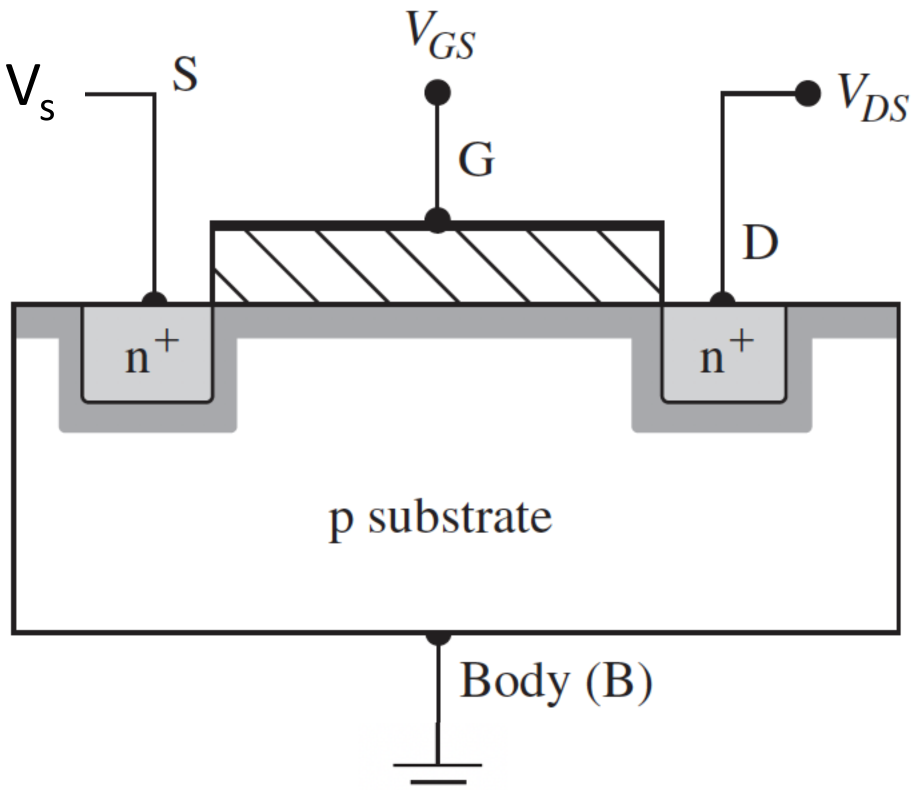
Consider an ideal n-channel MOSFET with parameters $L = 1.25\ \mu m$, $\mu_n = 650\ cm^2/V\text{-}s$, $C_{ox} = 6.9 \times 10^{-8}\ F/cm^2$, and $V_T = 0.65\ V$. Design the channel width W such that $I_D(sat) = 4\ mA$ for $V_{GS} = 5\ V$.

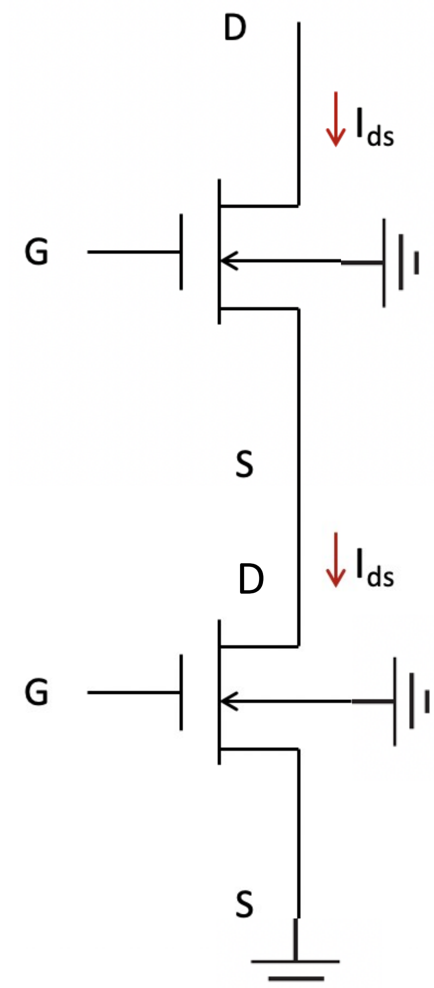
Check your understanding

Problem example 5

10.4 The basic MOSFET operation

Substrate bias effect





10.4 The basic MOSFET operation

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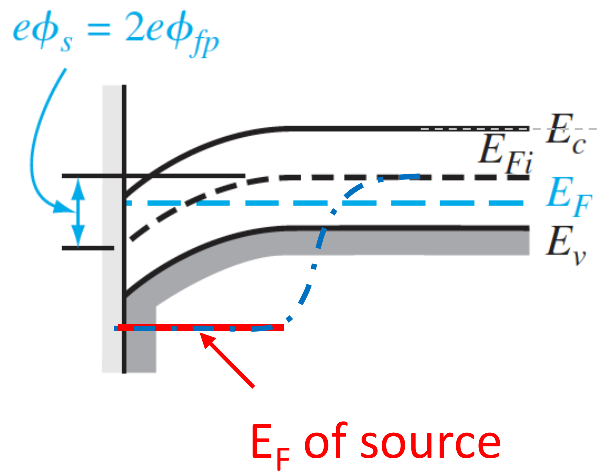

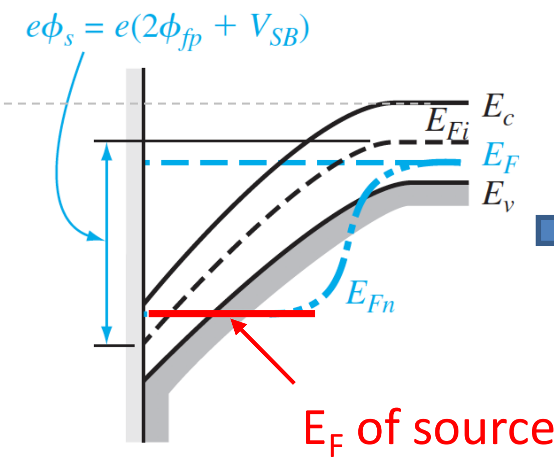

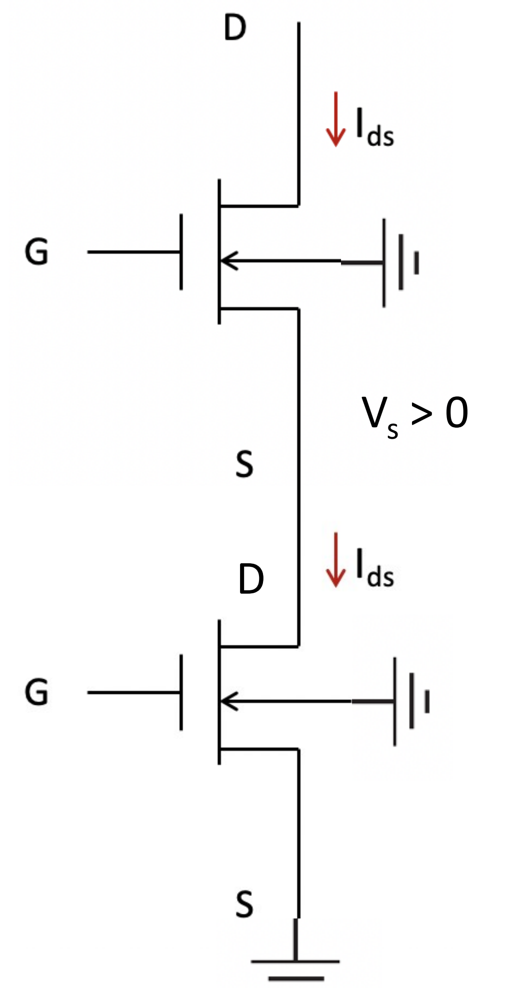

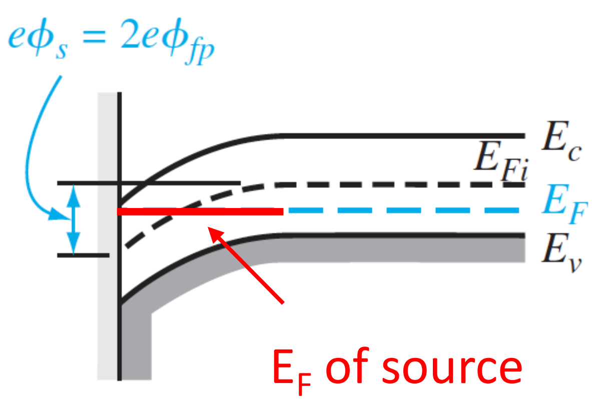

10.4 The basic MOSFET operation

Substrate bias effect

When $V_{SB} = 0$, we had

When $V_{SB} > 0$, the space charge width increases and we now have

The change in the space charge density is then

10.4 The basic MOSFET operation

Substrate bias effect

$$\boxed{\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{\mathrm{ox}}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{\mathrm{ox}}}\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]}$$

$$\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} \qquad \Delta V_T = \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

Check your understanding

Problem example 6

Objective: Calculate the body-effect coefficient and the change in the threshold voltage due to an applied source-to-body voltage.

Consider an n-channel silicon MOSFET at $T = 300$ K. Assume the substrate is doped to $N_a = 3 \times 10^{16}$ cm^{-3} and assume the oxide is silicon dioxide with a thickness of $t_{ox} = 20$ nm $= 200$ Å. Let $V_{SB} = 1$ V.

Check your understanding

Problem example 7