VE320 Introduction to Semiconductor Physics and Devices

Final Recitation Class: Chapter 11

VE320 Teaching Group SU2022

University of Michigan-Shanghai Jiaotong University
Joint Institute

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1. Chapter 11: MOSFET Non-ideal Effects
   Subthreshold Conduction
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Subthreshold Conduction

- For NMOS, ideally we assume $I_D = 0$ when $V_{GS} < V_T$.
- Experimentally, there is subthreshold current.

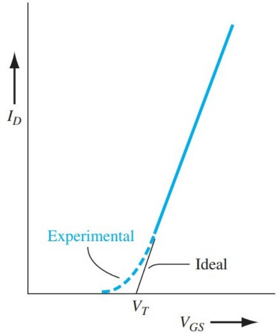


Figure: Comparison of ideal and experimental plots of $\sqrt{I_D}$ versus V_{GS}. Assume saturation region.

Subthreshold Conduction

- Under weak inversion ($\phi_{fp} < \phi_s < 2\phi_{fp}$), E_F is closer to E_C.
- The semiconductor surface develops a lightly doped n-type material.

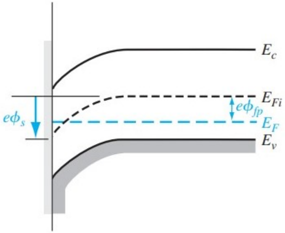


Figure: Energy-band diagram when $\phi_{fp} < \phi_s < 2\phi_{fp}$.

Subthreshold Conduction

- There is a potential barrier between the n source and channel region which the electrons must overcome to generate current.
- $I_D(\text{sub}) \propto \left[\exp\left(\frac{eV_{GS}}{kT}\right)\right] \cdot \left[1 - \exp\left(\frac{-eV_{DS}}{kT}\right)\right]$
- If V_{DS} is larger than a few (kT/e) volts, the subthreshold current is independent of V_{DS}.
- When $V_{GS} < V_T$, $I_D(\text{sub}) \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$, where n (an experimental factor) is ideally 1.

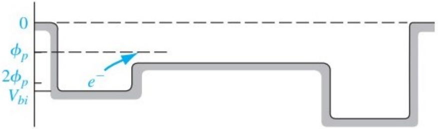
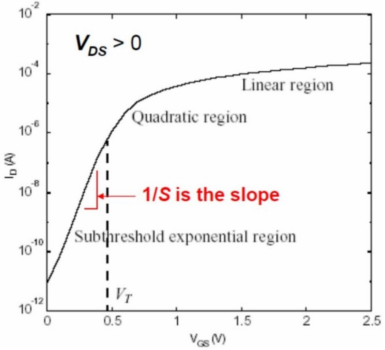


Figure: Energy-band diagrams along channel length at weak inversion.

Subthreshold Conduction

- Slope Factor (S): the inverse slope of the $\log(I_D)$ vs. V_{GS} characteristic in the subthreshold region.
- $S = n\left(\frac{kT}{q}\ln(10)\right)$ (volts per decade)
- At room temperature, $\frac{kT}{q}\ln(10) = 60\text{mV}$.

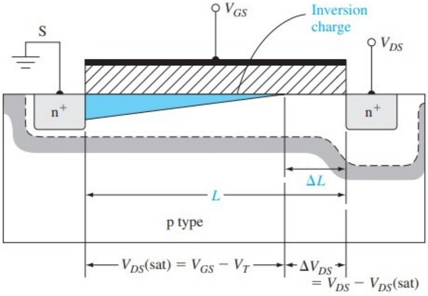


Subthreshold Conduction

- Design trade-offs
  - A larger subthreshold voltage results in larger power consumption in OFF state, and therefore larger consumption in the entire circuit.
  - We want to save the power and therefore we want higher threshold voltage for NMOS and lower threshold voltage for PMOS to save power.
  - On the other hand, we want larger ON current, and therefore we want lower threshold voltage for NMOS and higher for PMOS.

Channel Length Modulation

- We assume that the channel length L was a constant.
- However, in the saturation region, the depletion region at the drain (both NMOS and PMOS) extends into the channel.
- The effective channel length is reduced.



Channel Length Modulation

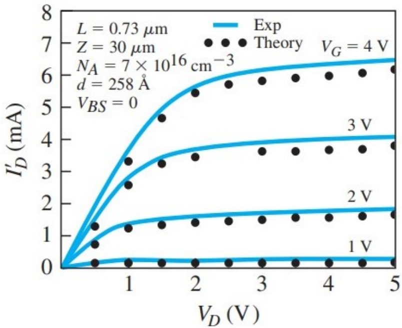
- The voltage across the effective channel length is constant: $V_{GS} - V_T$.
- The resistance across the effective channel is proportional to the length.
- I_D increases with decreasing L.
- $I'_D = \frac{L}{L-\Delta L} I_D$, where I'_D is the actual drain current and I_D is the ideal drain current.
- For saturation region, we have increasing current.

Question: why there is current across the depletion region?
- Electrons are injected into the depletion region and swept by the E-field to the drain.

Channel Length Modulation

- For NMOS: $I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$, λ is the channel length modulation parameter (given).
- For PMOS: the same, but with μ_p and I_{SD}, λ is negative (on the textbook).
- The derivation is done with approximations and not required. You don't need to calculate ΔL.

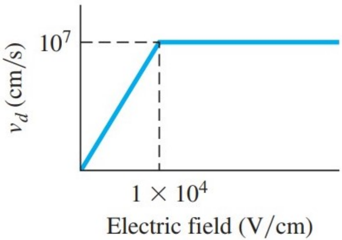
Channel Length Modulation



- $I'_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \right]$ where $k'_n = \mu_n C_{ox}$
- Output resistance: $r_o = \left(\frac{\partial I'_D}{\partial V_{DS}} \right)^{-1} = \left\{ \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot \lambda \right\}^{-1}$
- Since λ is normally small, $r_o \cong \frac{1}{\lambda I_D}$.

Velocity Saturation

- When electric field increases, carrier velocity will saturate, especially in short-channel devices.
- We assume that the velocity saturation is abrupt (see the graph).



Velocity Saturation

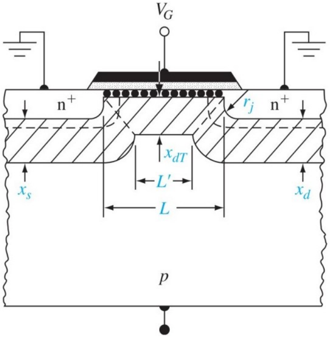
- After reaching the velocity saturation, the current will be roughly constant.
- With velocity saturation first, pinch-off can still happen if continuing increasing V_{DS}.
- With pinch-off happening with out velocity saturation, there will not be velocity saturation since the voltage across the effective channel length will be constant.
  - Though the channel length decreases, we assume the amount is small.
  - Therefore, the electric field intensity inside the effective channel remains almost the same.

$$I_{DSAT} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{1}{2} V_{DSAT} \right) V_{DSAT}$$

where V_{DSAT} is the velocity saturation voltage.

Short Channel Effect

- In long channel devices, the depletion regions of source and drain are very small parts of the entire channel.
- In short channel devices, the depletion region of the drain reduces the channel length effectively.



Short Channel Effect

- $V_{TN} = (|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{\rm ox}}{\epsilon_{\rm ox}}\right) + \phi_{ms} + 2\phi_{fp}$
- The amount of charge in the channel region $|Q'_{SD}(\max)|$ decreases and therefore V_{TN} decreases.
- For NMOS, as the channel length decreases, the threshold voltage shifts in the negative direction.
- For PMOS, as the channel length decreases, the threshold voltage shifts in the positive direction.
- The both move towards depletion mode.

NMOS

- Determine V_T, and sometimes consider substrate bias effects.
- When $V_{GS} < V_T$, $I_{DS} = 0$ or consider subthreshold current.
- Determine the minimum of velocity saturation voltage V_{DSAT} and pinch off voltage $V_{GS} - V_T$. Denote as V_{SAT}.
- If $V_{DS} < V_{SAT}$, $I_{DS} = \frac{W \mu_n C_{ox}}{2L} \left[2 \left(V_{GS} - V_T \right) V_{DS} - V_{DS}^2 \right]$.
- If $V_{DS} > V_{SAT}$, $I_{DS,\text{ideal}} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{1}{2} V_{SAT} \right) V_{SAT}$. If it is in pinch off region and we consider channel length modulation (remember even with velocity saturation, we can still reach pinch off), $I_{DS} = I_{DS,\text{ideal}}(1 + \lambda V_{DS})$.

PMOS

- Determine V_T, and sometimes consider substrate bias effects. Remember that for an enhancement mode PMOS, $V_T < 0$.
- When $V_{GS} > V_T$, $I_{SD} = 0$ or consider subthreshold current.
- Determine the minimum of velocity saturation voltage V_{DSAT} and pinch off voltage $V_{SG} + V_T$. Denote as V_{SAT}. The both are positive values.
- If $V_{SD} < V_{SAT}$, $I_{SD} = \frac{W\mu_p C_{ox}}{2L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right]$ or $I_{SD} = \frac{W\mu_p C_{ox}}{2L}[2(V_{SG} + V_T)V_{SD} - V_{SD}^2] > 0$.
- If $V_{SD} > V_{SAT}$, $I_{SD,\text{ideal}} = \mu_p C_{ox}\frac{W}{L}\left(V_{SG} + V_T - \frac{1}{2}V_{SAT}\right)V_{SAT}$. If it is in pinch off region and we consider channel length modulation (remember even with velocity saturation, we can still reach pinch off), $I_{SD} = I_{SD,\text{ideal}}(1 + |\lambda V_{SD}|)$.

Good luck for your final exam!