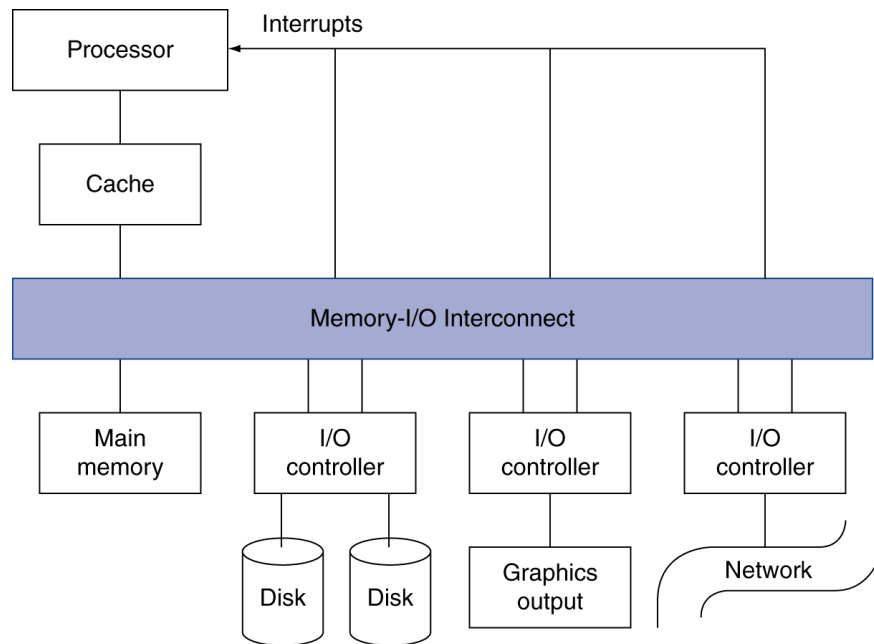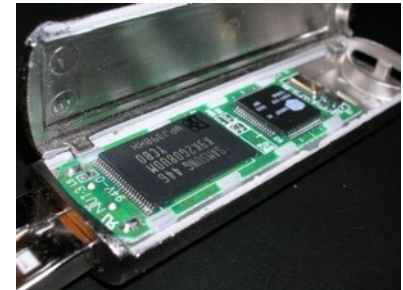# Topic 14

## I/Os and Their Interfaces

# Introduction

- I/O devices can be characterized by
  - Behavior: input, output, storage
  - Partner: human or machine
  - Data rate: bytes/sec, transfers/sec
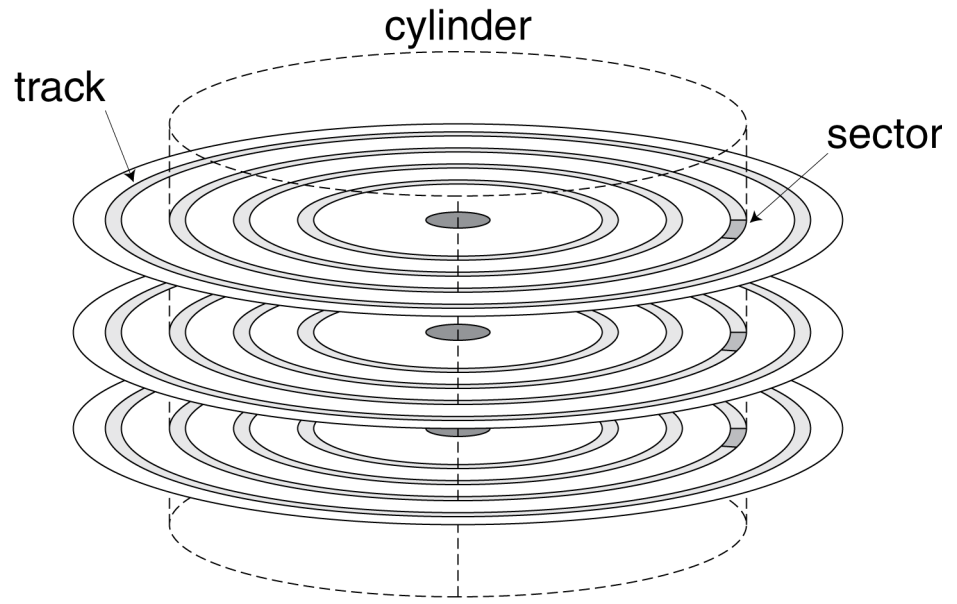- I/O bus connections

# Peripheral – Memory

- Volatile main memory
  - Loses instructions and data when power off
- Non-volatile secondary memory
  - Magnetic disk
  - Flash memory
  - Optical disk (CDROM, DVD)

3

# Disk Storage

- Nonvolatile, rotating magnetic storage

# Disk Sectors and Access

- Each sector records
  - Sector ID
  - Data (512 bytes)
  - Error correcting code (ECC)
    - Used to hide defects and recording errors
  - Synchronization fields and gaps
- Access to a sector involves
  - Queuing delay if other accesses are pending
  - Seek: move the heads
  - Rotational latency
  - Data transfer
  - Controller overhead

# Peripheral – Networks

- Communication and resource sharing
- Local area network (LAN): Ethernet
  - Within a building
- Wide area network (WAN): the Internet
- Wireless network: WiFi, Bluetooth
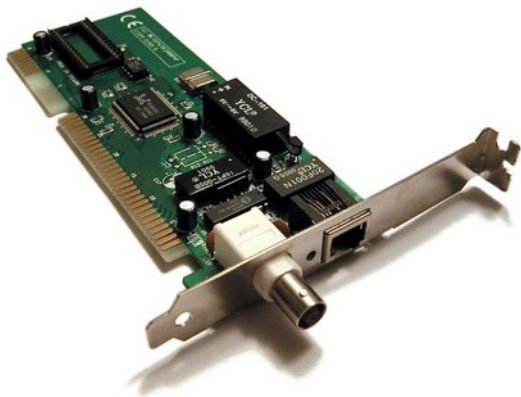
# **Peripheral – Many others**



(*Source: Wikipedia.org*)
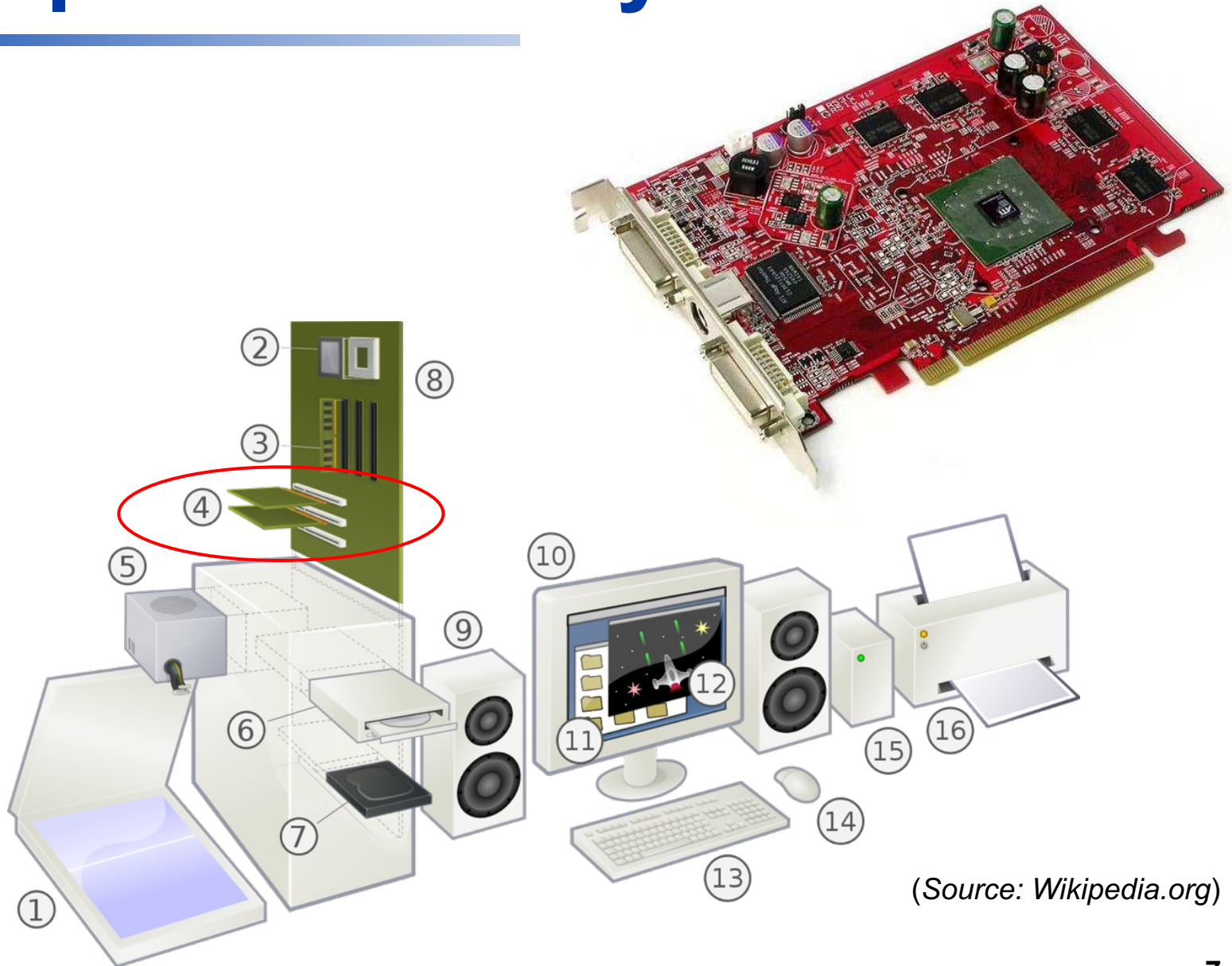
# I/O System Characteristics

- Dependability
  - Very important
  - Particularly for storage devices

- Performance measures
  - Latency (response time)
    - Desktops & embedded systems – mainly interested in response time & diversity of devices
  - Throughput (bandwidth)
    - Servers – mainly interested in throughput & expandability of devices

# I/O Management

- I/Os are managed by the Operating System (OS)
  - Multiple programs share I/O resources
    - Need protection and scheduling
    - Done by OS in supervisor mode
  - I/O causes asynchronous interrupts to communicate operation information with CPU
    - Same mechanism as exceptions
    - Interrupt service routine – part of OS
  - I/O programming is non-trivial and sophisticated
    - OS provides abstractions (interfaces) to programs
    - API – Application Programming Interface

# I/O Control Register

- I/O devices are controlled by a set of registers
  - Control registers
    - Cause device to do something
  - Status registers
    - Indicate what the device is doing or has done and occurrence of errors
  - Data registers
    - Write: transfer data to an I/O device
    - Read: transfer data from an I/O device

External World ⟷ I/O device [Control, Status, Data] ⟷ CPU
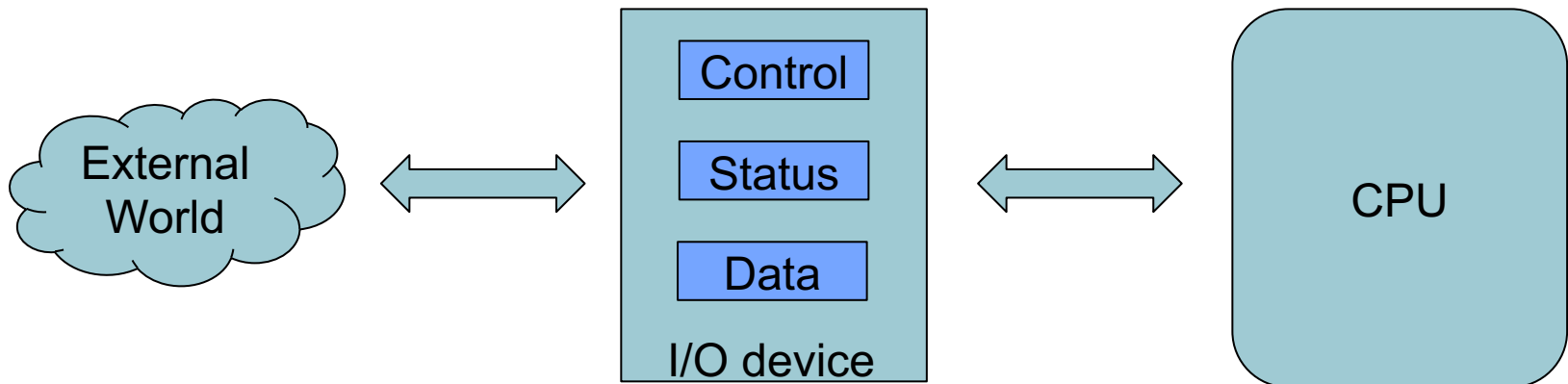
# OS (sw) & I/O (hw) Interface

- Memory mapped I/O
  - I/O registers are connected to memory locations
  - I/Os are accessed as regular memory locations
    - Accessible from software by virtual memory addresses
  - OS writes/reads memory to operate I/O devices
  - OS uses address translation mechanism to make them only accessible in kernel mode
    - Virtual address translation only accessible to OS

- I/O instructions
  - Separate instructions to access I/O registers
  - Can only be executed in kernel mode (by OS)

# Memory Mapped I/O
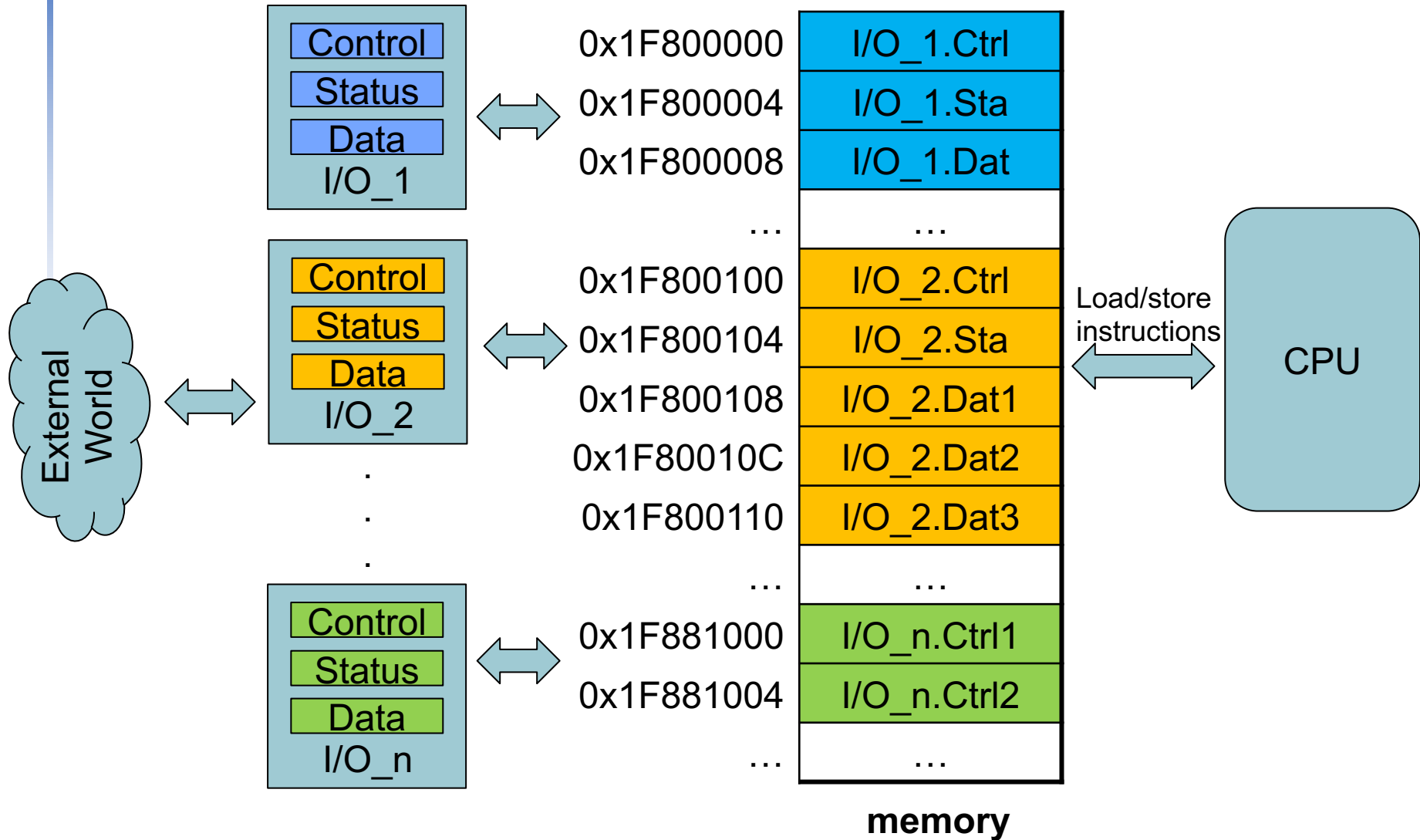
# I/O & Processor Communication – Polling

- Periodically check I/O status register
  - If device ready, do operation
  - If error, take action
- Common in small or low-performance real-time embedded systems
  - Predictable timing
  - Low hardware cost
- In other systems, wastes CPU time

# I/O & Processor Communication – Interrupt

- When a device is ready or error occurs
  - Controller interrupts CPU – by hardware
  - Will invoke handler between instructions
  - Not synchronized to instruction execution
- Interrupt Priority
  - Devices needing more urgent attention get higher priority
  - Higher priority interrupt can interrupt execution of a lower priority interrupt

# **Interconnecting Components**

- Need interconnections between
  - CPU, memory, and I/O controllers
  - Using buses
- Bus: shared communication channel
- Parallel set of wires for data and synchronization of data transfer
  - Advantages:
    - Versatility – various functions, easy to be added or removed
    - Low cost
  - Concerns: performance limited by physical factors
    - Bus speed – can become a communication bottleneck
    - Wire length, number of connections
- More recent alternative: high-speed serial connections

# Bus Types

- Processor-Memory buses (North connection)
  - Short, high speed
  - Designed to match memory organization
- I/O-Memory buses (South connection)
  - Longer, allowing multiple connections
  - Specified by standards for interoperability
  - Connected through a north bridge then to memory

# Typical x86 PC I/O System