Homework 6

VE370 - Intro to Computer Organization Summer 2022

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Exercise 1

The following code is written in C, where elements within the same row are stored contiguously. Assume each word is a 32-bit integer.

```
for (I=0; I<8; I++)
    for (J=0; J<8000; J++)
        A[I][J]=B[I][0]+A[J][I];
```

(1) Which variable references exhibit temporal locality?

(2) Which variable references exhibit spatial locality?

Answer:

(1) `B[I][0], I, J`

(2) `A[I][J]`

Exercise 2

Below is a list of 32-bit memory address references, given as word addresses:
`0x03, 0xB4, 0x2B, 0x02, 0xBF, 0x58, 0xBE, 0x0E, 0xB5, 0x2C, 0xBA, 0xFD`

(1) For each of these references, identify the tag and the cache index given a direct-mapped cache with 8 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

(2) For each of these references, identify the tag and the cache index given a direct-mapped cache with two-word blocks and a total size of 4 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

(3) You are asked to optimize a cache design for the given references. There are three direct-mapped cache designs possible, all with a total of 8 words of data: C1 has 1 -word blocks, C2 has 2-word blocks, and C3 has 4-word blocks. In terms of miss rate, which cache design is the best? If the miss stall time is 35 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design?

Answer:

(1)

	0x03	0xB4	0x2B	0x02	0xBF	0x58	0xBE	0x0E	0xB5	0x2C	0xBA	0xFD
tag	00000	10110	00101	00000	10111	10110	10111	00001	10110	00101	10111	11111
index	011	100	011	010	111	000	110	110	101	100	010	101
if hit	M	M	M	M	M	M	M	M	M	M	M	M

(2)

	0x03	0xB4	0x2B	0x02	0xBF	0x58	0xBE	0x0E	0xB5	0x2C	0xBA	0xFD
tag	00000	10110	00101	00000	10111	10110	10111	00001	10110	00101	10111	11111
index	01	10	01	01	11	00	11	11	10	10	01	10
if hit	M	M	M	M	M	M	H	M	H	M	M	M

(3)

	0x03	0xB4	0x2B	0x02	0xBF	0x58	0xBE	0x0E	0xB5	0x2C	0xBA	0xFD
tag	00000	10110	00101	00000	10111	10110	10111	00001	10110	00101	10111	11111
index	0	1	0	0	1	0	1	1	1	1	0	1
if hit	M	M	M	M	M	M	H	M	M	M	M	M

For C1, miss rate $= 12/12 = 100\%$

For C2, miss rate $= 10/12 = 83.3\%$

For C3, miss rate $= 11/12 = 91.7\%$

C2 design is the best.

C1 : $35 \times 12 + 2 \times 12 = 444$ cycles

C2: $35 \times 10 + 3 \times 12 = 386$ cycles

C3: $35 \times 11 + 5 \times 12 = 445$ cycles

Also, C2 design is the best.

Exercise 3

For a direct-mapped cache design with a 32-bit byte address, the following bits of the address are used to access the cache.

Tag	Index	0ffset
$31-10$	$9-5$	$4-0$

(1) What is the cache block size (in words)?

(2) How many blocks does the cache have?

(3) What is the ratio between total bits required for such a cache implementation over the data storage bits?

Beginning from power on, the following byte addresses for cache references are recorded.

Address											
0x00	0x04	0x10	0x84	0xE8	0xA0	0x400	0x1E	0x8C	0xC1C	0xB4	0x884

(4) For each reference, list

a) its tag, index, and offset

b) whether it is a hit or a miss, and

c) How many blocks were replaced (if any)?

(5) What is the hit ratio?

(6) Show the final state of the cache, with each valid line represented as <index, tag, data>.

Answer:

(1) 8 words

(2) 32 blocks

(3)

$$\frac{32 \times (1 + 22 + 32 \times 8)}{32 \times (32 \times 8)} = 1.09$$

(4)

	0x000	0x004	0x010	0x084	0x0B8	0x0B0	0x400	0x01E	0x08C	0xC1C	0x0B4	0x884
tag	00000	00000	00000	00000	00000	00000	00001	00000	00000	00011	00000	00010
index	00000	00000	00000	00100	00111	00101	00000	00000	00100	00000	00101	00100
offset	00000	00100	10000	00100	01000	00000	00000	11110	01100	11100	11010	00100
if hit	M	H	H	M	M	M	M	M	H	M	H	M
replace	F	F	F	F	F	F	T	T	F	T	F	T

(5)

$$\frac{4}{12} = 33.3\%$$

(6) `<00000 011 Mem[0xC00]-Mem[0xC1C]>`

`<00100 010 Mem[0x880]-Mem[0x89C]>`

`<00101 000 Mem[0x0A0]-Mem[0x0BC]>`

`<00111 000 Mem[0x0E0]-Mem[0x0FC]>`