Homework 3

VE370 - Intro to Computer Organization Summer 2022

* Name: Huang Yucheng ID: 519021910885

Exercise 1

Given RISC-V assembly instruction sequence:

```
bne x22, x23, Else
add x19, x20, x21
beq x0, x0, Exit
Else: lw x19, 0(x20)
Exit: ...
```

Assuming the memory location of the first instruction (bne) is `0x1000F400`, what are the values of the following control signals for each of the instructions?

Instruction	Branch	MemRead	MemtoReg	ALUOp	MemWrite	ALUSrc	RegWrite	Zero	Imm
add									
beq									
lw									

Answer:

Instruction	Branch	MemRead	MemtoReg	ALUOp	MemWrite	ALUSrc	RegWrite	Zero	Imm
add	0	0	0	10	0	0	1	0	1
beq	1	0	0	01	0	0	0	1	1
lw	0	1	1	00	0	1	1	0	0

Exercise 2

Given following assembly instruction:

```
and rd, rs1, rs2
```

(1) Which resources (blocks) perform a useful function for this instruction?

(2) Which resources (blocks) produce no output for this instruction? Which resources produce output that is not used?

Answer:

(1) We need: PC, ALU, Registers and mux for ALU/Memory.

(2) Every block has output, but output of Immgen is not used.

Exercise 3

Consider the following instruction mix:

R-type	I-type (non-lw)	Load	Store	Branch	Jump
24%	28%	25%	10%	11%	2%

(1) What fraction of all instructions use data memory?

(2) What fraction of all instructions use instruction memory?
(3) What fraction of all instructions use the sign extend?

Answer:

(1) $25\% + 10\% = 35\%$

(2) 100%

(3) $28\% + 25\% + 10\% + 11\% + 2\% = 76\%$

Exercise 4

When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get "broken" and always read a logical 0 . This is often called a "stuck-at- 0 " fault.
(1) Which instructions fail to operate correctly if the MemToReg wire is stuck at 0 ? (5 points)
(2) Which instructions fail to operate correctly if the ALUSrc wire is stuck at 0 ? (5 points)

Answer:

(1) Since MemToReg connects to the memory block and another mux, if it always reads a logical 0, the instructions need loading may not work, such as lw/lb.

(2) Since ALUSrc connects to the middle register which operates the instruction and it will only reads a 0. So all the I-type, S-type will not work now.

Exercise 5

Problems in this exercise assume that the logic blocks used to implement a processor's datapath have the following latencies:

I/D-Mem	RegiFile	Mux	ALU	Adder	Singate	RegiRead	RegiSetup	Sigtend	Control
250ps	150ps	25ps	200ps	150ps	5ps	30ps	20ps	50ps	50ps

In above table, "Register Read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register Setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

(1) What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)?
(2) What is the latency of lw?
(3) What is the latency of sw?
(4) What is the latency of beq?
(5) What is the latency of an arithmetic, logical, or shift I-type (non-load) instruction?
(6) What is the minimum clock period for this CPU?

Answer:

(1) 30+250+150+25+200+25+20 = 700 ps

(2) 30+250+150+25+200+250+25+20 = 950 ps

(3) 30+250+150+25+200+250 = 905 ps

(4) 30+250+150+25+200+5+25+20 = 705 ps

(5) 30+250+150+25+200+25+20 = 700 ps

(6) 30+250+150+25+200+250+25+20 = 950 ps

Exercise 6

Modify the single-cycle processor datapath to add a proposed new assembly instruction:

`ss rs1, rs2, immediate #Store Sum`

Operation: Mem[Reg[rs1]] = Reg[rs2]+ immediate

Answer:

First, we should place a new mux which connects Reg[rs1] and Reg[rs2], so that the control can choose the correct register. Second, we should place another mux which connects output and rs1, which can store the memory. Finally, other operation blocks are not necessarily modified.