VE370 Introduction to Computer Organization

Homework 7

Assigned: July 12, 2022

Due: 4:00pm on July 19, 2022

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1. (20 points) For a 2-way set associative cache with a 32-bit address and write back mechanism, the partition of the 32 bits are as follows:
    -   Offset: bit 6 to 0
    -   Index: bit 11-7

    (1) What is the size of the cache? (5 points)

    Starting from power on, the following byte addresses were used to access the cache memory: 0, 4, 20, 136, 232, 164, 1024, 30, 140, 3100, 176, 2180

    (2) What is the hit ratio? (5 points)

    (3) Show the final state of the cache, with each valid line represented as <index, tag, data>. (10 points)

2. (20 points) In general, cache access time is proportional to its capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for caches attached to each of two processors, P1 and P2.

	Size	Miss Rate	Hit Time
P1	16KB	4.3%	1.18 ns
P2	32KB	2.7%	2.22 ns

    (1) Assuming that the cache hit time determines the cycle times for P1 and P2, what are their respective clock rates? (5 points)

    (2) What is the AMAT for P1 and P2? AMAT (Average Memory Access Time) is defined as follows: AMAT = Hit time + Miss rate $\times$ Miss penalty (5 points).

    (3) Assuming a base CPI of 1.0 without any memory stalls, what is the actual CPI for P1 and P2? Which processor is faster? (10 points)

3. (60 points) Given the following byte addresses for memory access:

3, 180, 43, 3, 191, 89, 190, 14, 181, 44, 186, 252

(1) Show the final cache contents for a 3-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference identify the index bits, the tag bits, the offset bits, and if it is a hit or a miss. (20 points)

(2) Show the final cache contents for a fully associative cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference identify the index bits, the tag bits, and if it is a hit or a miss. (20 points)

(3) What is the miss rate for a fully associative cache with two-word blocks and a total size of 8 words, using LRU replacement? What is the miss rate using MRU (most recently used) replacement? Finally what is the best possible miss rate for this cache, given any replacement policy? (20 points)