Course Introduction

Instructional Support

- **Instructor:** Gang Zheng, Ph.D.
- **Office:** JI New Building 400E
- **Contact:** (021) 3420-6765 x4005, gzheng@sjtu.edu.cn
- **Teaching mode:** online (Feishu)
- **Office Hours:** W 2:00 – 6:00pm / Th 10:00am – noon, on Feishu, or by appointment
- **TAs:** Ms. WANG Runxi, wangrunxi@sjtu.edu.cn
- **Recitation:** recorded or on schedule
- **TA Office Hours:** TBD

What will be taught?

- Assembly language
- How computers execute programs?
- What's the correspondence between different levels of languages: C/C++, assembly, and machine language?
- How to design a processor as a digital system?
- What are the difficulties and tricks in the design of a CPU? How to resolve? How to improve?
- How memory works as part of a computer, and how is it organized?
- How processor, memory, and I/O devices work together as a computer?

What Are You Expected to Do?

- Write an assembly language program, translate the program into binary code, and trace execution of the program.
- Model a processor using hardware description languages (HDLs).
- Be able to identify and resolve potential data and control hazards in the Instruction Set Architecture (ISA)
- Understand memory hierarchy including cache, main memory, hard disk, and how data is stored, understand memory hits and misses
- Understand the memory mapped I/O concept and how I/O devices interface to the CPU
- Be able to use library and internet resources for literature search to learn contemporary issues, technologies, and future development trends in computing

Textbook

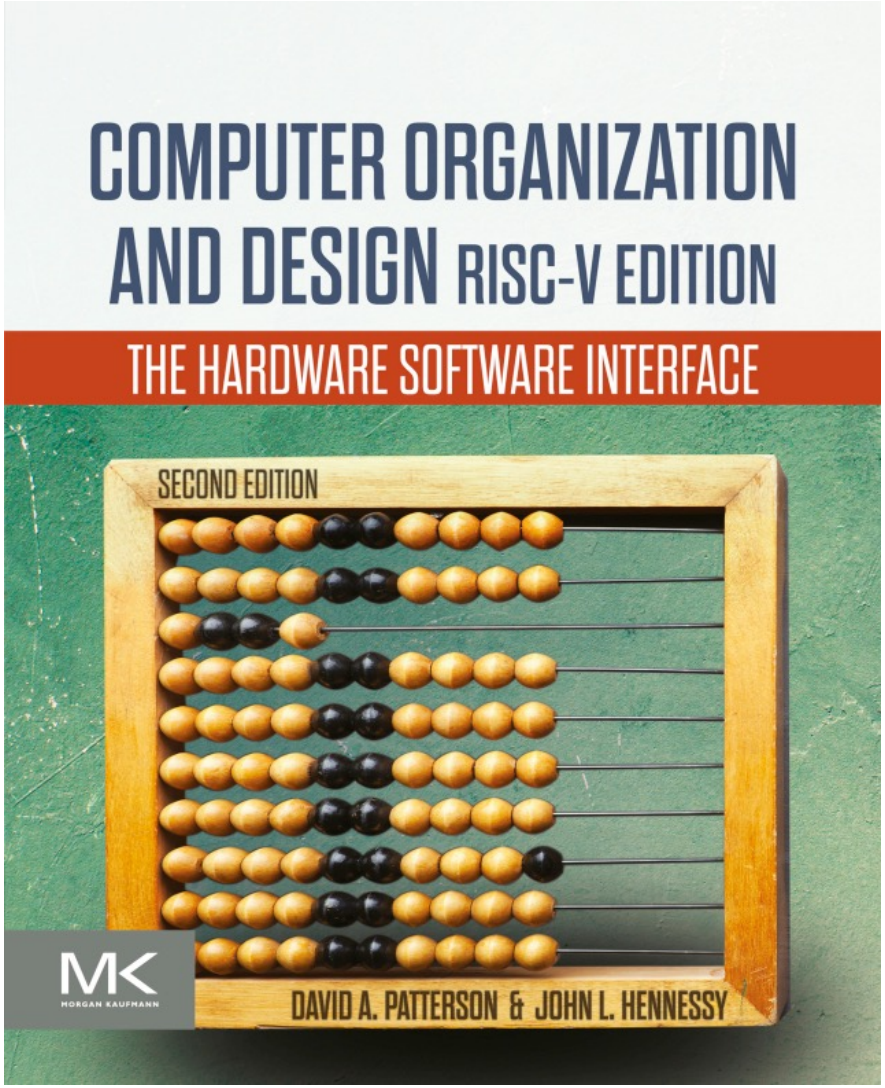
David Patterson and John Hennessy

Computer Organization and Design RISC-V Edition, 2nd edition

Morgan Kaufmann, 2020,

ISBN-10: 0128203315

ISBN-13: 978-0128203316



Tentative Schedule

Week	Date	Topics	Projects
1	5/10	Course Introduction, introduction to computer	
	5/12	RISC-V assembly: operations and operands	
	5/13	RISC-V assembly: operations and operands	
2	5/17	RISC-V assembly: function and function call	P1. RISC-V Assembly
	5/19	RISC-V assembly: function and function call	
3	5/24	RISC-V assembly: instruction encoding	P2. Assembly Programming
	5/26	Review & Discussion	
	5/27	CPU: single cycle processor	
4	5/31	CPU: single cycle processor	P3. Single Cycle Processor
	6/2	CPU: pipelined processor	
5	6/7	CPU: pipelined processor	
	6/9	Review & Discussion	
	6/10	CPU: data hazards	
6	6/14	CPU: data hazards	P4. Pipelined Processor
	6/16	CPU: data hazards	
7	6/21	Midterm Exam	
	6/23	Review & Discussion	
	6/24	CPU: control hazards	
8	6/28	CPU: control hazards	P5. Resolving Hazards
	6/30	Memory: cache	
9	7/5	Memory: cache	
	7/7	Memory: cache	
	7/8	Memory: cache	
10	7/12	Review & Discussion	P6. Cache Memory Start Literature Review
	7/14	Memory: virtual memory	
11	7/19	Memory: virtual memory	
	7/21	Memory: virtual memory	
	7/22	Review & Discussion	
12	7/26	I/Os and interfaces	P7. Virtual Memory Continue Literature Review
	7/28	I/Os and interfaces	
13	TBD	Final Exam	Literature Review Report

Course Policies

- **Honor Code:**
  - Honor Code of the Joint Institute
  - ***Addendum to the Honor Code for Online Teaching***.
- **Test:**
  - Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.
- **Attendance:**
  - Strongly encouraged for better understanding of difficult concepts and student engagement during class time
- **Participation:**
  - Active participation is highly expected for all students. This involves:
    - Participation in interactive activities during the lecture time
    - Active involvement in projects and office hours
    - Proper assistance to other students in group studying
    - Contributions to the Q&A on Piazza, etc.

Course Policies

- **Individual Assignments:**
  - Homework, some projects, literature review report
  - OK to discuss course topics and help each other understand the project/homework requirements better
  - NOT OK for duplicated submission
- **Group Assignments:**
  - Some projects are team efforts
  - Teams of 2 students, grouped randomly
- **Submission:**
  - Electronic submission on Canvas before deadline

Assessment Methods

- **Homework:**
  - About 8 homework assignments
- **Quiz:**
  - About 5 pop quizzes
- **Examination:**
  - Two online or paper-based examinations.
  - The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.
- **Projects:**
  - 7 projects
  - Project 1-3 are individual work, Projects 4-7 are team work

Assessment Methods

- **Literature Review:**
  - Choose an interesting area, search literatures to review, write a review report
- **Participation and Etiquette:**
  - Classroom interaction with the instructor and other students
  - effective contribution on Piazza
  - active participation in team-based projects.
  - Vandalism, spam messages, verbal and other forms of abuse, violation of English-only policies and disturbance of the learning experience of other students are not permitted

Grading Policy

Homework *	10%
Pop quiz	10%
Midterm Exam	15%
Final Exam	15%
Engineering Projects */**	40%
Literature Review Report *	5%
Participation & Etiquette	5%
Total	**100%**

*Individual assignments

**Group assignments

Note: final letter grades may be curved