Homework 7

VE370 - Intro to Computer Organization Summer 2022

* Name: Huang Yucheng ID: 519021910885

Exercise 1

For a 2-way set associative cache with a 32-bit address and write back mechanism, the partition of the 32 bits are as follows:

- Offset: bit 6 to 0
- Index: bit 11-7

(1) What is the size of the cache?

Starting from power on, the following byte addresses were used to access the cache memory: 0, 4, 20, 136, 232, 164, 1024, 30, 140, 3100, 176, 2180

(2) What is the hit ratio?

(3) Show the final state of the cache, with each valid line represented as <index, tag, data>

Answer:

(1) Since we have $2^5 \times 2 = 64$ blocks, and each block has $2^5 \times 4 = 128$ bytes. The size is $64 \times 128 = 8192$ bytes. Exactly, 65536 bits.

And also, we need to store tags. $20 \times 64 = 1280$ bits. So, the total bits are $65536 + 1280 = 66816$ bits.

(2)

	tag	index	H/M
0000 0000 0000	0(twenty zeros)	0	M
0000 0000 0100	0	0	H
0000 0001 0100	0	0	H
0000 1000 1000	0	1	M
0000 1110 1000	0	1	H
0000 1010 0100	0	1	H
0100 0000 0000	0	8	M
0000 0001 1110	0	0	H
0000 1000 1100	0	1	H
1100 0001 1100	0	24	M
0000 1011 0000	0	1	H
1000 1000 0100	0	17	M

The rate is $7/12 = 0.5833$

(3)

$$< 00000, 0, \text{Mem}[0 \sim 31] >$$
$$< 00001, 0, \text{Mem}[32 \sim 63] >$$
$$< 01000, 0, \text{Mem}[256 \sim 287] >$$
$$< 10001, 0, \text{Mem}[544 \sim 575] >$$
$$< 11000, 0, \text{Mem}[768 \sim 799] >$$

Exercise 2

In general, cache access time is proportional to its capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for caches attached to each of two processors, P1 and P2.

	Size	Miss Rate	Hit Time
P1	16 KB	4.3%	1.18 ns
P2	32 KB	2.7%	2.22 ns

(1) Assuming that the cache hit time determines the cycle times for P1 and P2, what are their respective clock rates?

(2) What is the AMAT for P1 and P2? AMAT (Average Memory Access Time) is defined as follows: AMAT = Hit time + Miss rate × Miss penalty.

(3) Assuming a base CPI of 1.0 without any memory stalls, what is the actual CPI for P1 and P2? Which processor is faster?

Answer:

(1)

$$\text{P1} = 1/1.18 \text{ ns} = 0.847\text{GHz}$$
$$\text{P2} = 1/2.22 \text{ ns} = 0.450\text{GHz}$$

(2)

$$\text{P1} = 1.18 \text{ ns} + 4.3\% \times 70 \text{ ns} = 4.19 \text{ ns}$$
$$\text{P2} = 2.22 \text{ ns} + 2.7\% \times 70 \text{ ns} = 4.11 \text{ ns}$$

(3) P1 Miss penalty = $70/1.18 = 59$ cycles

Effective CPI = $1 + 136\% \times 4.3\% \times 59 = 4.45$

P2 Miss penalty = $70/2.22 = 32$ cycles

Effective CPI = $1 + 136\% \times 2.7\% \times 32 = 2.17$

So, P2 is better.

Exercise 3

Given the following byte addresses for memory access: 3, 180, 43, 3, 191, 89, 190, 14, 181, 44, 186, 252

(1) Show the final cache contents for a 3-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference identify the index bits, the tag bits, the offset bits, and if it is a hit or a miss.

(2) Show the final cache contents for a fully associative cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference identify the index bits, the tag bits, and if it is a hit or a miss.

(3) What is the miss rate for a fully associative cache with two-word blocks and a total size of 8 words, using LRU replacement? What is the miss rate using MRU (most recently used) replacement? Finally what is the best possible miss rate for this cache, given any replacement policy?

Answer:

(1)

	3	180	43	3	191	89	190	14	181	44	186	252
tag	000	101	001	000	101	010	101	000	101	001	101	111
set	00	10	01	00	11	11	11	01	10	01	11	11
offset	0|11	1|00	0|11	0|11	1|11	0|01	1|10	1|10	1|01	1|00	0|10	1|00
H/M	M	M	M	H	M	M	H	M	H	H	H	M

index	tag	data1	data2
00	000	Mem[0]	Mem[1]
01	001	Mem[10]	Mem[11]
	000	Mem[2]	Mem[3]
10	101	Mem[44]	Mem[45]
11	101	Mem[46]	Mem[47]
	010	Mem[22]	Mem[23]
	111	Mem[62]	Mem[63]

(2)

	3	180	43	3	191	89	190	14	181	44	186	252
tag	0	101101	001010	0	101111	010110	101111	000011	101101	001011	101110	111111
set	–	–	–	–	–	–	–	–	–	–	–	–
offset	11	00	11	11	11	01	10	10	01	00	10	00
H/M	M	M	M	H	M	M	H	M	H	M	M	M

tag	data
000000	Mem[0]
101101	Mem[45]
111111	Mem[63]
101111	Mem[47]
010110	Mem[22]
000011	Mem[3]
001011	Mem[11]
101110	Mem[21]

(3)

	3	180	43	3	191	89	190	14	181	44	186	252
tag	00000	10110	00101	00000	10111	01011	10111	00001	10110	00101	10111	11111
set	–	–	–	–	–	–	–	–	–	–	–	–
offset	0|11	1|00	0|11	0|11	1|11	0|01	1|10	1|10	1|01	1|00	0|10	1|00
LRU	M	M	M	H	M	M	H	M	M	M	H	M
MRU	M	M	M	H	M	M	M	M	H	H	M	M

For LRU:

tag	data1	data2
10110	Mem[44]	Mem[45]
00101	Mem[10]	Mem[11]
11111	Mem[62]	Mem[63]
10111	Mem[46]	Mem[47]

For MRU:

tag	data1	data2
00000	Mem[0]	Mem[1]
10110	Mem[44]	Mem[45]
11111	Mem[62]	Mem[63]
00001	Mem[2]	Mem[3]

As is shown in the table, both of the two methods has miss rate $9/12 = 0.75$