# VE370  Introduction to Computer Organization

# Homework 4

**Assigned: June 7, 2022**

**Due: 4:00pm on June 16, 2022**

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1.  (15 points) Given this instruction:
    ```
    lw x5, -4(x2)
    ```

    As the instruction goes through the pipeline, what will be stored in the pipeline registers:
    IF: what's in PC
    ID: what's in IF/ID
    EX: what's in ID/EX?
    MEM: what's in EX/MEM
    WB: what's in MEM/WB?

2.  (20 points) Assume that individual stages of the RISC-V pipelined datapath have the following latencies:

    | IF | ID | EX | MEM | WB |
    |--------|--------|--------|--------|--------|
    | 250 ps | 350 ps | 150 ps | 300 ps | 200 ps |

    Also, assume that instructions executed by the processor are broken down as follows:

    | ALU/Logic | Jump/Branch | Load | Store |
    |-----------|-------------|------|-------|
    | 45% | 20% | 20% | 15% |

    (1) What is the clock cycle time? (2 points)

    (2) What is the execution time of a sw instruction in the pipelined processor? (3 points)

    (3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor? (5 points)

    (4) Using the processor to run a program of 1,000 instructions, what is the total execution time? What is the CPI? (10 points)

3.  (10 points) Assume that x11 is initialized to 11 and x12 is initialized to 22. Suppose you executed the code below on a pipelined processor that does not handle data hazards at all.
    ```
    L1: addi x11, x12, 5
    L2: add x13, x12, x11
    L3: addi x14, x11, 15
    ```

    (1) Indicate data dependencies, if any, in above instruction sequence. (which register between which instructions) (5 points)

(2) What would the final values of registers x13 and x14 be? (5 points)

4. (30 points) Given the following instructions:
```
L1: sw  x18,-12(x8)
L2: lw  x3,8(x18)
L3: add x6,x3,x3
L4: or  x8,x9,x6
```
   a) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)
   b) Assume there is ALU-ALU forwarding. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)
   c) Assume there is full forwarding. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)

5. (25 points) Given this assembly instruction sequence executed by the pipelined processor:
```
sub x6, x2, x1
lw  x3, 8(x6)
lw  x2, 0(x6)
or  x3, x5, x3
sw  x3, 0(x5)
```
   a) If the processor has forwarding, but we forgot to implement the hazard detection unit, what happens when this code executes? (5 points)
   b) If there is forwarding, for the first five cycles during the execution of this code, specify which signals are asserted in each cycle by hazard detection and forwarding units. (10 points)
   c) If there is no forwarding, what new inputs and output signals do we need for the hazard detection unit? Using this instruction sequence as an example, explain why each signal is needed. (10 points)