CS264A: Homework #2

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Problem 1

1. **Solution:** One minimal unsat core is:
$\{\{X \vee Y\}, \{X \vee Z\}, \{\neg Y \vee W\}, \{\neg Z \vee \neg W\}, \{\neg X \vee W\}, \{\neg X \vee \neg W \vee V\}, \{\neg X \vee \neg W \vee \neg V\}, \{Z \vee \neg X\}, \{\neg Z \vee W\}\}$

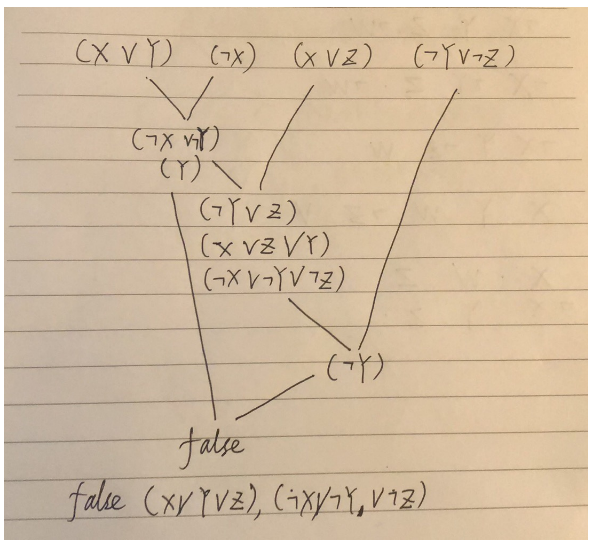
Problem 2

1. **Solution:**

X	Y	Z	$Cost$
T	T	T	2
T	T	F	1
T	F	T	1
T	F	F	1
F	T	T	1
F	T	F	1
F	F	T	1
F	F	F	2

So there are multiple optimal solutions with cost 1 listed above except $\{X, Y, Z\}$ and $\{\neg X, \neg Y, \neg Z\}$

2. **Solution:** The resolution graph is below and the compensation clause are $\{X \vee Y \vee Z\}, \{\neg X \vee \neg Y \vee \neg Z\}$



Problem 3

1. **Solution:** In this case, the resolvent will be: $\{(B \vee C) \vee (D \vee E)\}$
   And the compensation clauses will be
   $A \vee B \vee C \vee \neg D$
   $A \vee B \vee C \vee D \vee \neg E$
   $\neg A \vee D \vee E \vee \neg B$
   $\neg A \vee D \vee E \vee B \vee \neg E$

Problem 4

Solution:

A	B	C	D	E	SAT
T	T	T	T	T	yes
T	T	T	T	F	no
T	T	T	F	T	yes
T	T	T	F	F	no
T	T	F	T	T	no
T	T	F	T	F	no
T	T	F	F	T	yes
T	T	F	F	F	no
T	F	T	T	T	no
T	F	T	T	F	yes
T	F	T	F	T	yes
T	F	T	F	F	yes
T	F	F	T	T	no
T	F	F	T	F	yes
T	F	F	F	T	yes
T	F	F	F	F	yes
F	T	T	T	T	yes
F	T	T	T	F	yes
F	T	T	F	T	yes
F	T	T	F	F	yes
F	T	F	T	T	no
F	T	F	T	F	no
F	T	F	F	T	yes
F	T	F	F	F	no
F	F	T	T	T	no
F	F	T	T	F	yes
F	F	T	F	T	yes
F	F	T	F	F	yes
F	F	F	T	T	no
F	F	F	T	F	yes
F	F	F	F	T	yes
F	F	F	F	F	yes

1. The MajSAT problem is yes according to the truth table we have above. the 32 results have 12 un-sat worlds but 20 sat worlds.

2. **Solution:** Is there an X = {A,B,C} instantiation under which the majority of {D,E} are sat? yes

   When X = T which means A = T, B = T, C = T. The majority of Y is not sat since it's half and half.

   When X = F which has 7 scenarios. Specifically, when A =F , B =F , C =F. The majority of Y is sat with 3 out of 4 in total.

Problem 4 continued on next page. . .

Solution: Is the majority of X = {A,B,C} instantiation under which the majority of {D,E} are sat? yes

When X = T which means A = T, B = T, C = T. The majority of Y is not sat since it's half and half.

When X = F which has 7 scenarios:

A = T, B = T, C = F : majority not sat

A = T, B = F, C = T : majority sat

A = T, B = F, C = F : majority sat

A = F, B = T, C = T : majority sat

A = F, B = T, C = F : majority not sat

A = F, B = F, C = T : majority sat

A = F, B = F, C = F : majority sat

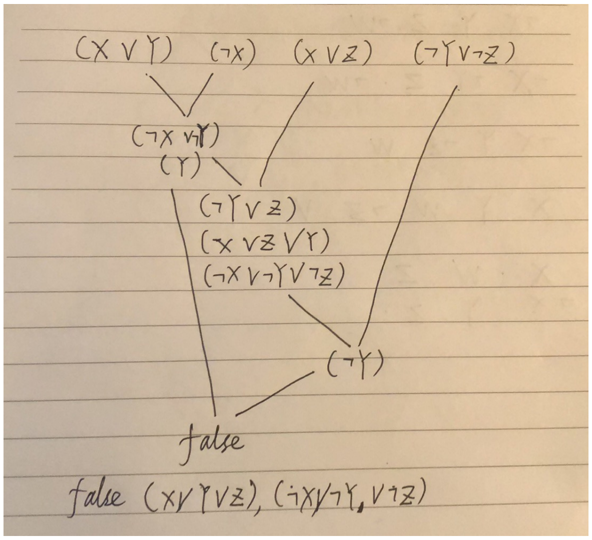
5 out of 8 instantiation of X are sat under which the majority of Y are sat.

3. So the answer is yes.

Problem 5

Solution:

The boolean formula is shown below:



To calculate the weighted model count, A = T, C = F, B = T/F

The results are

$\theta_A \theta_{A|B} \theta_{B|\neg C} = 0.6 * 0.8 * 0.75 = 0.36$

$\theta_A \theta_{A|\neg B} \theta_{\neg B|\neg C} = 0.6 * 0.2 * 0.7 = 0.084$

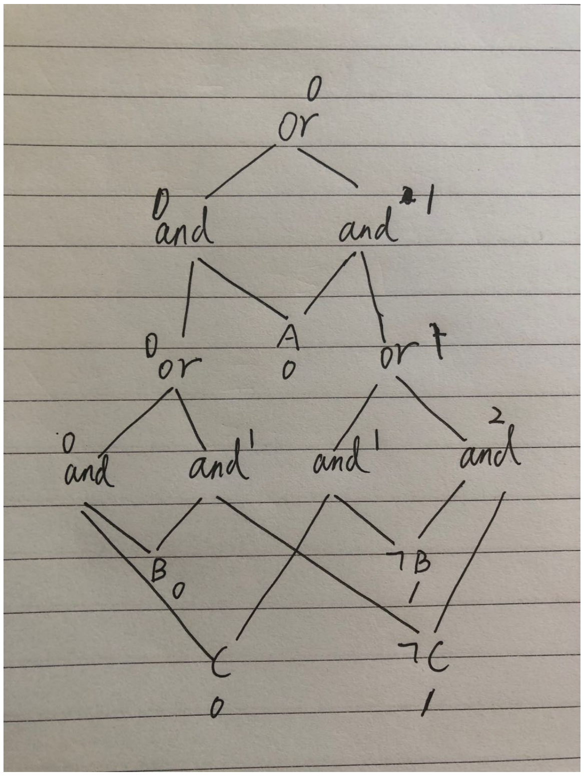
1. In total: 0.444

Problem 6

1. **Solution:**
   The subcircuits under gate AND3 overlap : A,C and C so it is not decomposable.
   The subcircuits under gate OR are mutually exclusive
   $A \vee B \wedge \neg C$
   $(\neg C \vee \neg A) \wedge C$
   Cannot happend together, so they are deterministic.

Problem 7

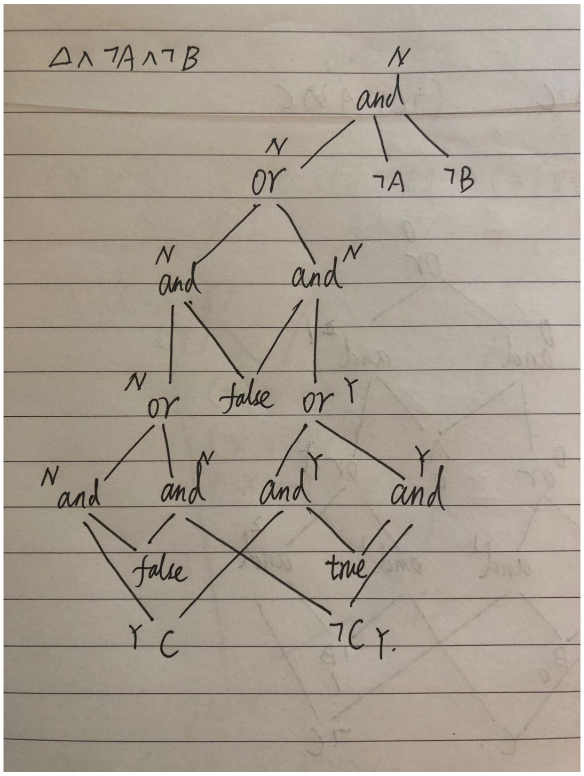
1. **Solution:** The minimum cardinality of each literal and gate is shown below.



Problem 7 continued on next page. . .

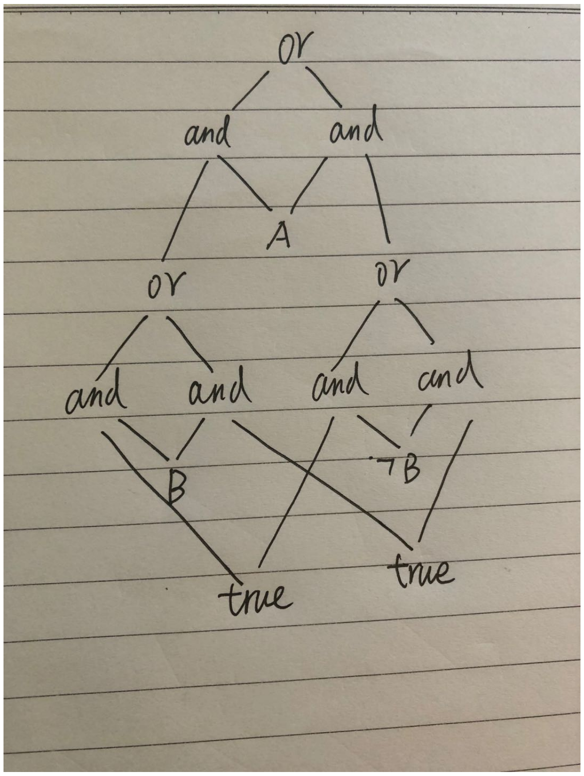
2. **Solution:**

When to check if a clause $(A \vee B)$is entailed, we need to check if $(\Delta \wedge \neg A \wedge \neg B)$ is inconsistent. Then we replace the literal in circuit with corresponding boolean and check if the circuit is inconsistent.



3. **Solution:**

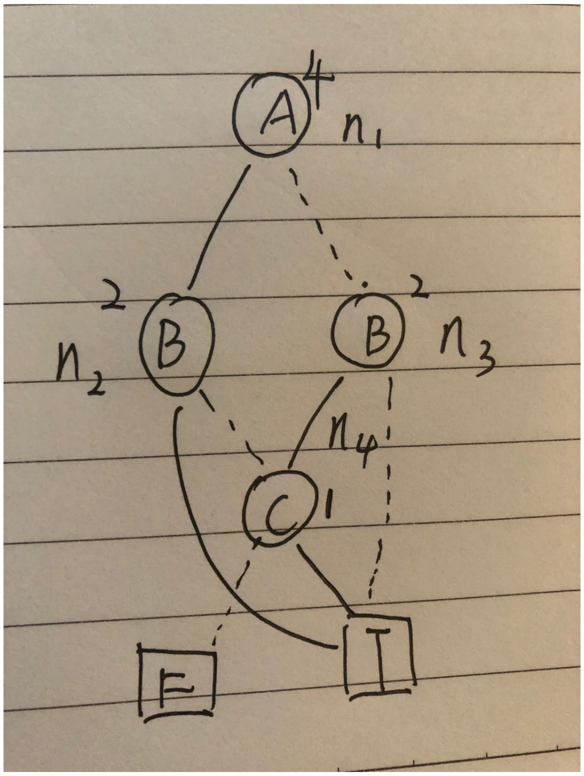
Existential quantify is to remove the literal from the knowledge base but still representing the same logic. So we want if there exists an C then the knowledge base works. To do this we need to replace all C with true.



Problem 8

1. **Solution:**

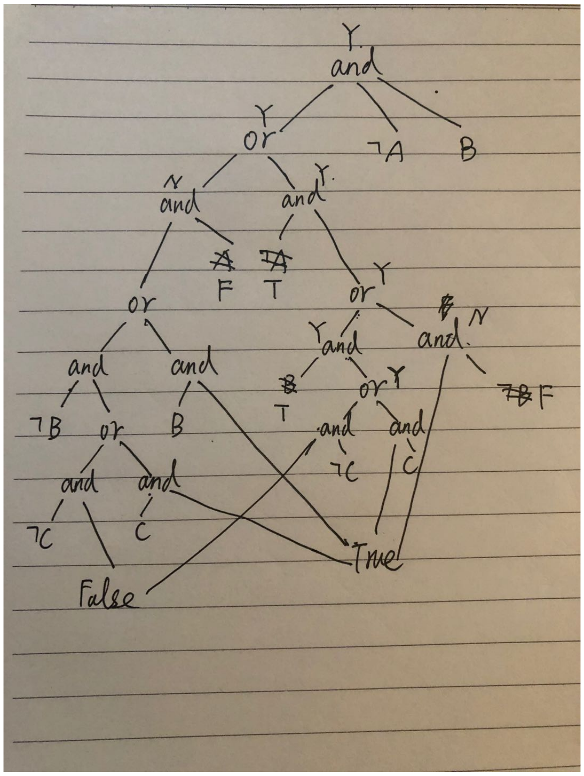
The model count for each node is shown below:



Solution:

First we convert the OBDD to cicuits form. And to check the entailment of $(A \vee \neg B)$, we need to check that $\Delta \neg A \wedge B$ is inconsistent.

The cicuits is shown below and by replacing literal with corresponding true/false we are able to see the final answer is consistent so $(A \vee \neg B)$ is not entailed.

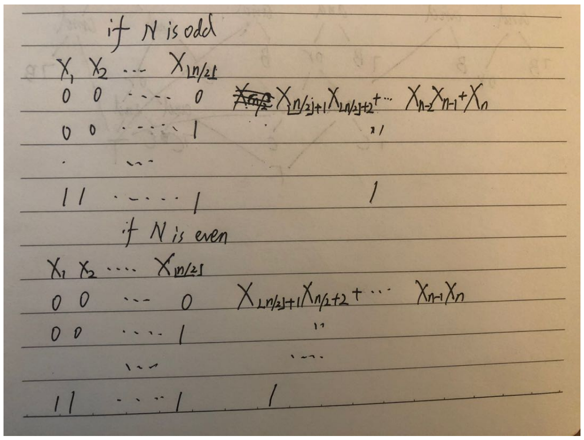
2. 

Problem 9

1. **Solution:**

   There are two scenarios:1. N is odd. 2. N is even.

   If there is any pair in X_1 to $X_{\lfloor N/2-1 \rfloor}$ are both 1, then the subfunction is 1. Otherwise the subfunction is shown in the first row of the table. Similar to N is even.

   if N is odd

$X_1\ X_2 \cdots X_{\lfloor n/2 \rfloor}$	
$0\ 0 \cdots 0$	$\cancel{X_{n/2}}\ X_{\lfloor n/2 \rfloor+1}X_{\lfloor n/2 \rfloor+2}+\cdots X_{n-2}X_{n-1}+X_n$
$0\ 0 \cdots 1$	"
$\cdots$	
$1\ 1 \cdots 1$	1

   if N is even

$X_1\ X_2 \cdots X_{\lfloor n/2 \rfloor}$	
$0\ 0 \cdots 0$	$X_{\lfloor n/2 \rfloor+1}X_{n/2+2}+\cdots X_{n-1}X_n$
$0\ 0 \cdots 1$	"
$\cdots$	$\cdots$
$1\ 1 \cdots 1$	1

   Therefore, there are two sub-functions.

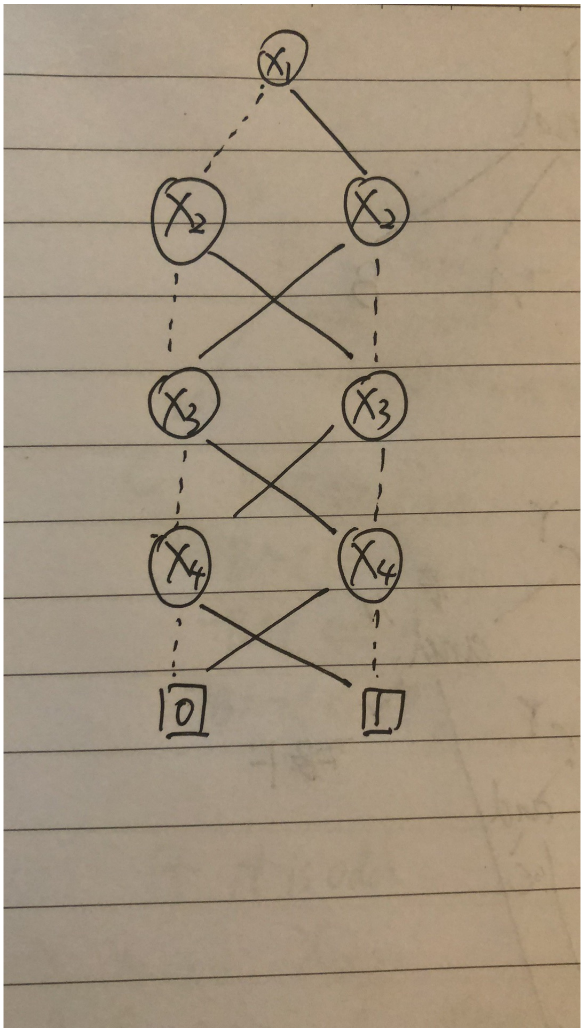
2. **Solution:**

   After apply the reducing rules on the OBDD.

   Finally it will have one X_1 node and two node for X_2 .... X_N and two sink nodes. The total are 2N+1.

3. **Solution:**

The OBDD is shown below:



Problem 10

1. **Solution:** Universal quantifying a variable is to check if all literals in Δ is this variable.

   In order to check the variables in linear time, one property of the NNF is that all variables are in the leaf of the NNF circuits. Going over the leaves of circuits takes linear time.

   Below is the algorithm:

   Check if the given node is null. If null, then return from the function. Check if it is a leaf node. If the node is a leaf node, then check if the node is the specified variable. If in the above step, the node is not a leaf node then check if the left and right children of node exist. If yes then call the function for left and right child of the node recursively.

   The time complexity will be O(n) where n is the number of nodes in the circuits. Moreover, according to the definition the number of nodes is the size of the circuits. So it is in time linear in the circuit size.