REF Schematic for RK3568

Main Functions Introduction

1) PMIC: RK809-5+DiscretePower
2) RAM: DDR4 2x16Bit------------------Default
   Option:LPDDR4/4x 1X32bit(200ball)
   Option:DDR3 4x16bit
   Option:DDR3 4x16bit+2x16bit ECC
   Option:DDR4 2x16bit+1x16bit ECC
   Option:LPDDR3 1x32bit(178ball)
   Option:DDR4 4x16bit
3) ROM: eMMC--------------------------Default
   Option:Nand Flash
   Option:SPI Falsh
4) Support:1 x Micro SD Card3.0
5) Support:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1 + 1 x SATA3.0 Port2 ----------Default
   Option:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1 + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB3.0 OTG0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x SATA3.0 Port2
   Option:1 x USB3.0 OTG0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB3.0 HOST1 + 1 x SATA3.0 Port2
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB3.0 HOST1 + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x SATA3.0 Port2
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x 1Lane PCIe2.0(RC Mode)
6) Support:1 x USB2.0 HOST2+ 1 x USB2.0 HOST3 -- ------Default
7) Support:4G module Via MiniPCIe2.0 Slot With PCIE2.0 and USB2.0 HOST3 function ------Option
8) Support:2 x 1Lane PCIe3.0 Connector (RC Mode) ------Default
   Option:1 x 2Lanes PCIe3.0 Connector (RC Mode)
   Option:1 x 2Lanes PCIe3.0 Connector (EP Mode)
9) Support:1 x HDMI2.0 TX
10) Support:1 x LCM MIPI DSI TX0 ----------Default
   Option:1 x LCM MIPI DSI TX1
   Option:1 x LCM LVDS TX
   Option:1 x LCM Dual MIPI DSI TX
   Option:1 x LCM eDP TX
11) Support:1 x VGA OUT ----------Default
12) Support:1 x 4Lanes Camera MIPI CSI RX ----------Default
   Option:2 x 2Lanes Camera MIPI CSI RX
   Option:1 x HDMI1.4 RX(HDMI to MIPI CSI)
13) Support:a/b/g/n/ac 2X2 SDIO WIFI5+BT5.0+PCM --------Default
   Option:a/b/g/n/ac 1X1 SDIO WIFI+BT+PCM
   Option:a/b/g/n/ac/ax 2X2 PCIe WIFI6+BT5.0+PCM
14) Support:1 x 10/100/1000 Ethernet(RGMII1_M1) -------Default
   Option:1 x 10/100/1000 Ethernet(RGMII0)
   Option:1 x 10/100/1000 PCIe Ethernet Card
15) Support:1 x Headphone output ----------Default
16) Support:1 x ECM MIC + 1 x Speaker out ----------Default
   Option:4 x MEMS MIC + 1 x Speaker out + Loopback or 2 x MEMS MIC + 1 x Speaker out + Loopback
   Option:4 x MEMS MIC + 2 x Speaker out + Loopback
17) Support:1 x IR Receiver ----------Default
18) Support:Array Key(MENU,VOL+,VOL-,ESC),Reset,Power on/off Key
19) Support:3 x UART + 1 x RS485 + 1 x CAN FD(Option)
20) Support:Debug UART and ARM JTAG

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	00.Cover Page				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	1 of 69

Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

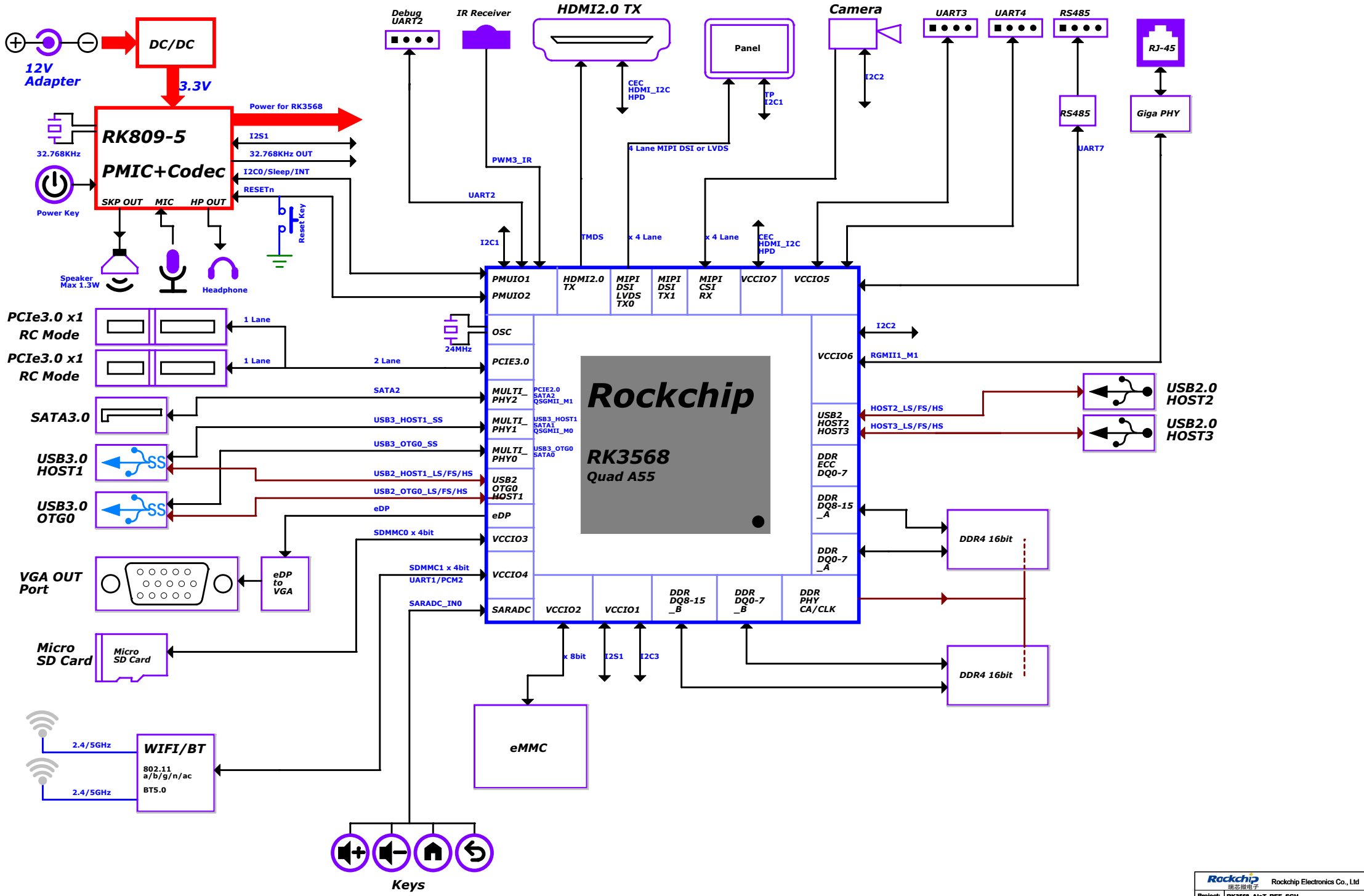
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	01.Index and Notes				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	2 of 69

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-02-04	Zhangdz	1:Revision preliminary version	

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	02.Revision History				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	3 of 69

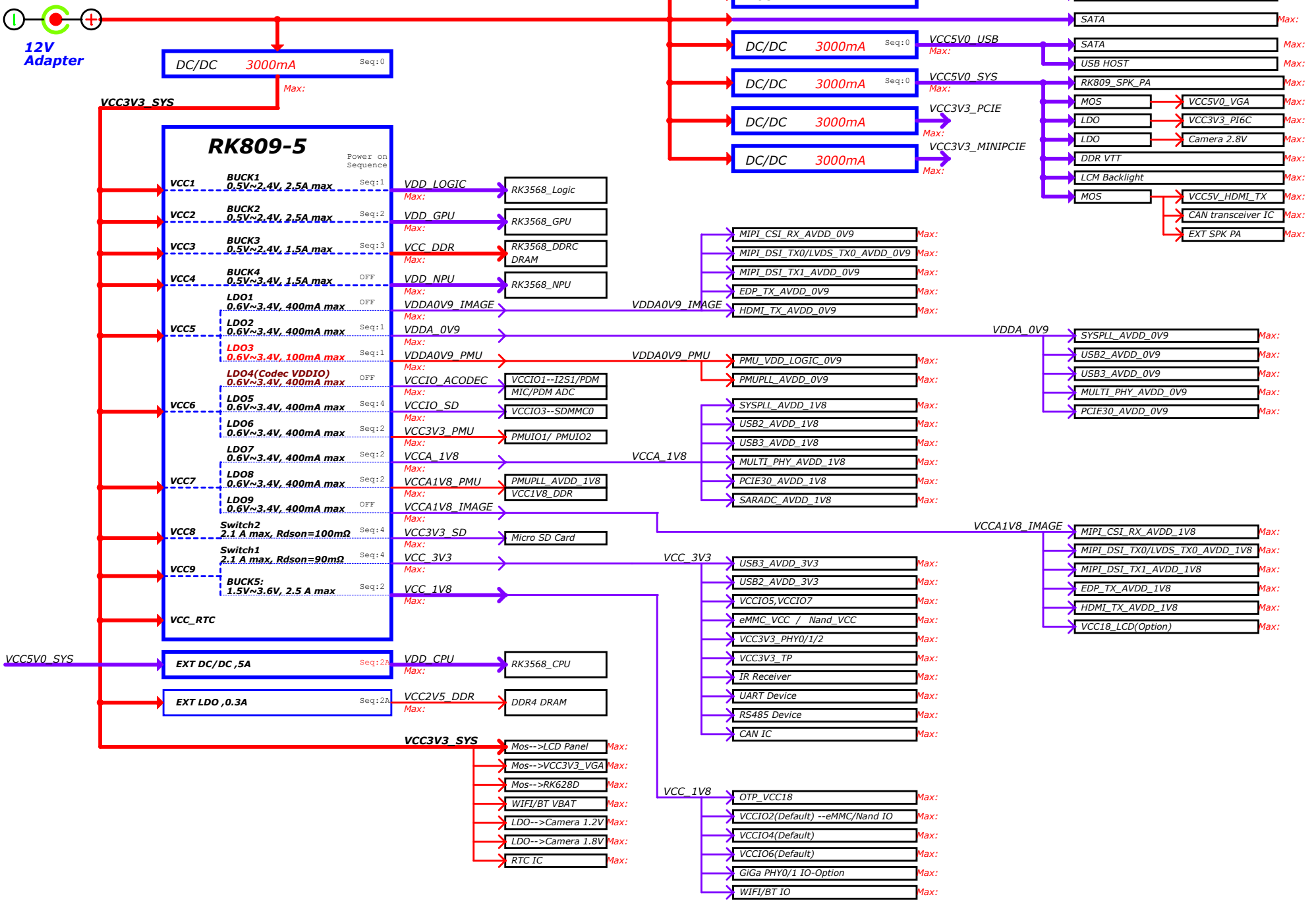
RK3568 Ref Block Diagram(Default configuration)



Rockchip Confidential

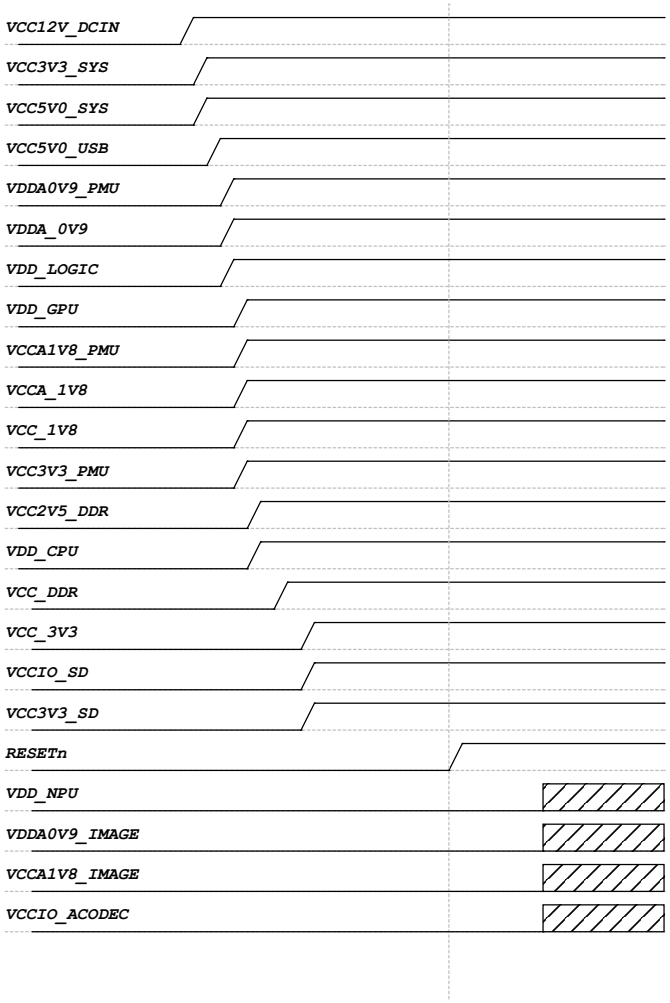
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	03.Block Diagram
Date:	Thursday, February 04, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	4 of 69

Default Power Diagram



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	04.Power Diagram
Date:	Thursday, February 04, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	5 of 69

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

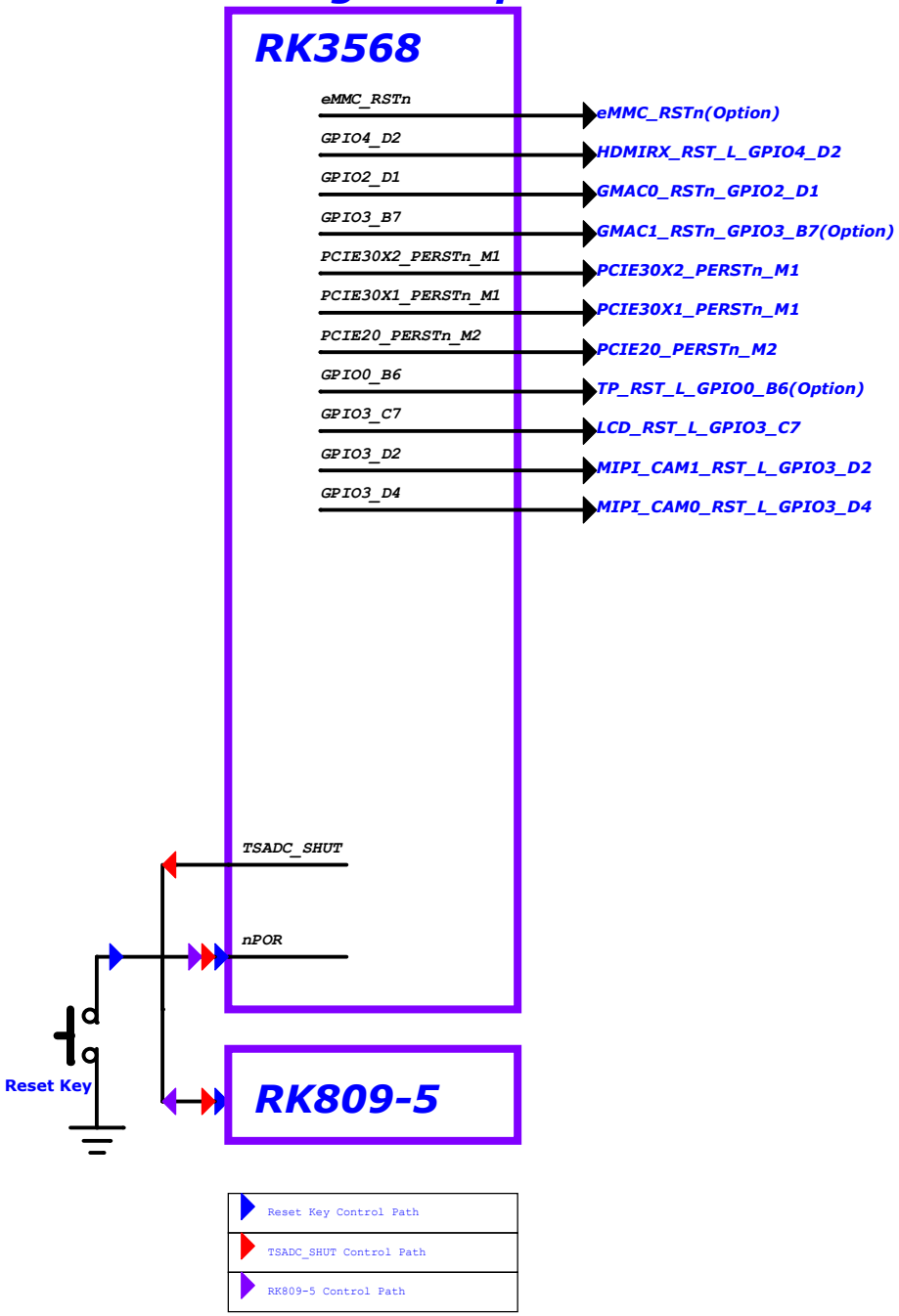
Default IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

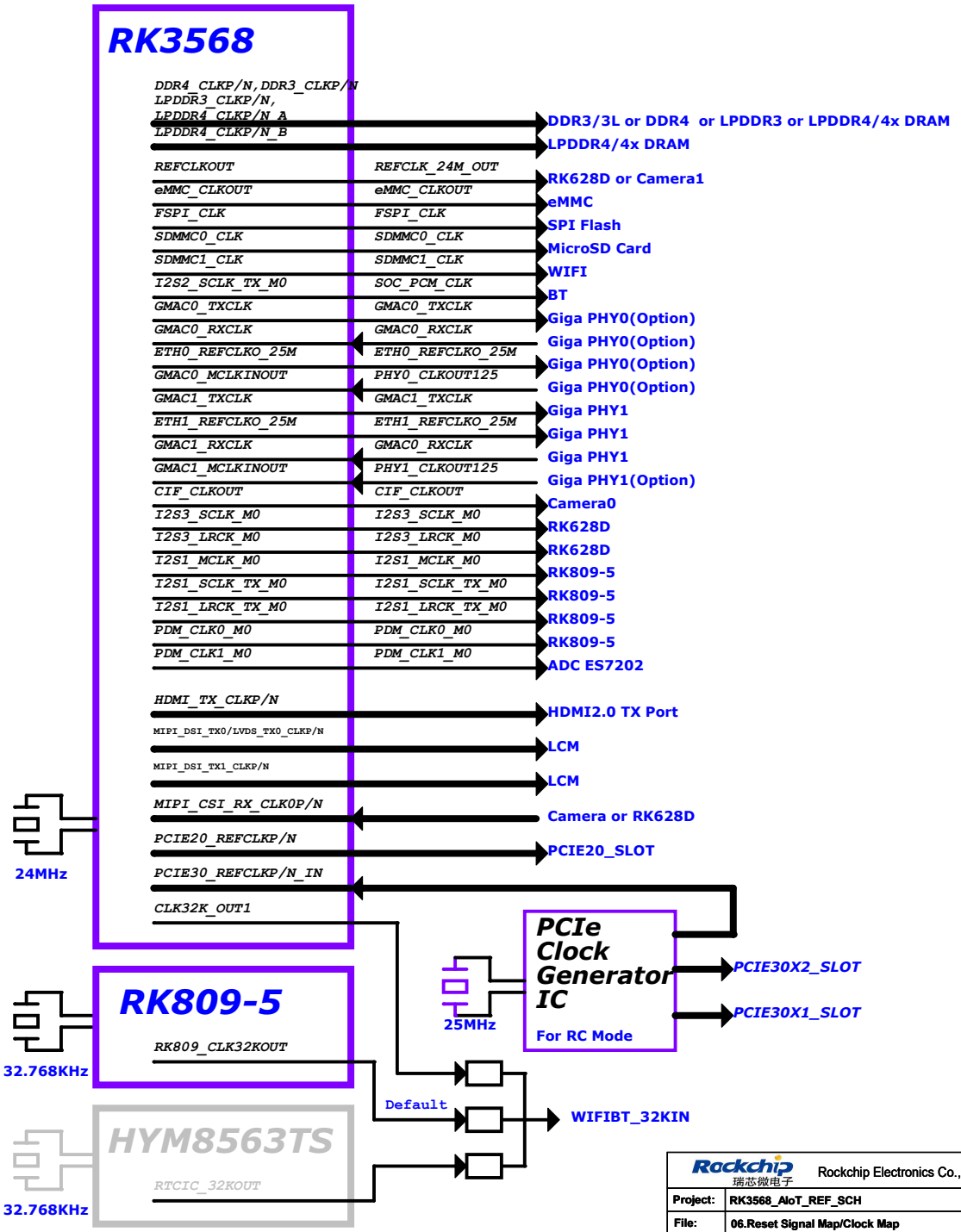
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	05.Power Sequence/IO Domain Map				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	6 of 69

Default Reset Signal Map



Default Clock Map



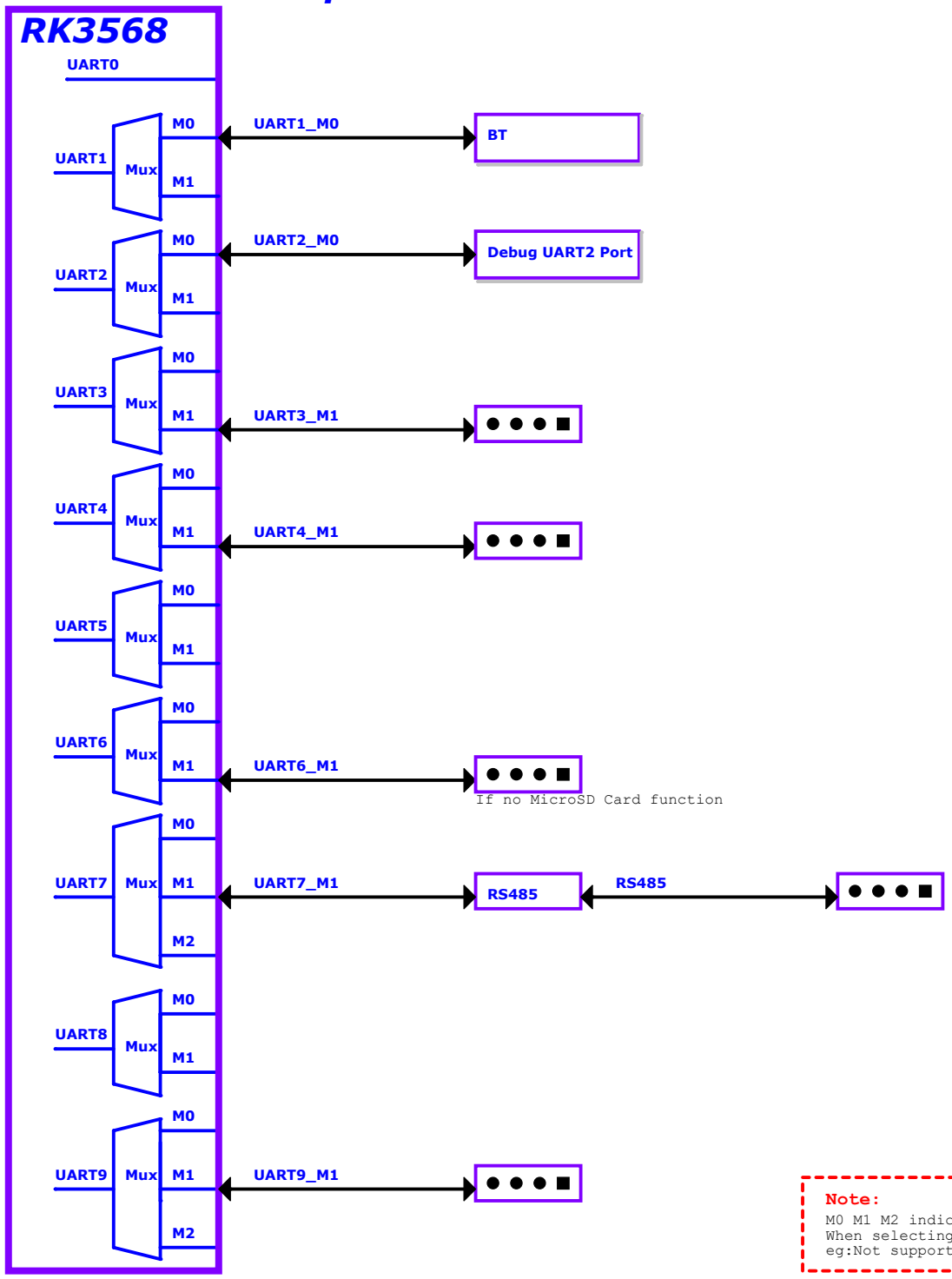
Note:
The power off hold time scheme is required,
It is recommended to use external RTC IC

Rockchip Confidential

Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd					
Project:	RK3568_AIoT_REF_SCH				
File:	06.Reset Signal Map/Clock Map				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	7 of 69

Default UART Map

Rockchip Confidential



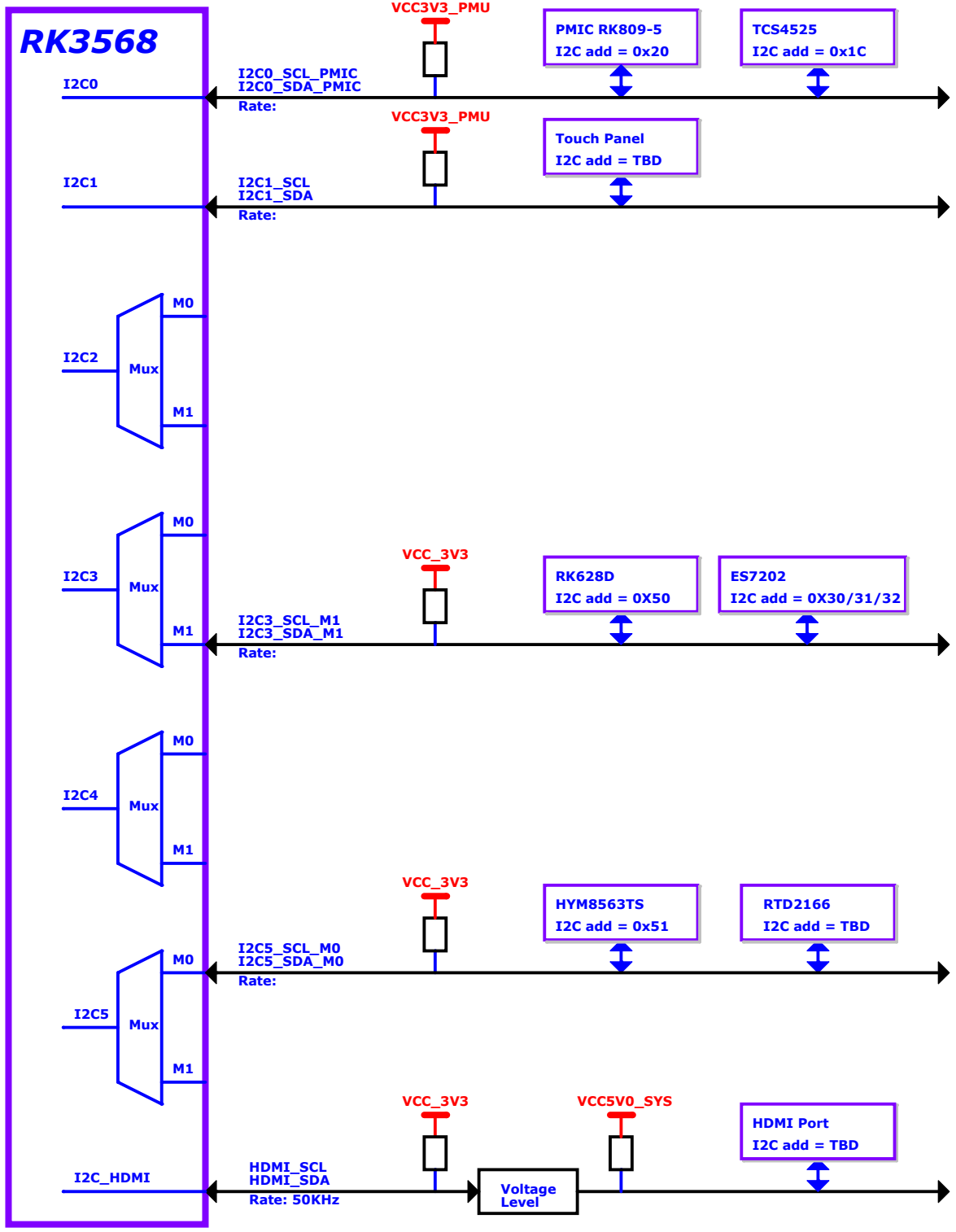
Note:

M0 M1 M2 indicates that the same function is multiplexed to different IO
When selecting, only M0 or M1 or M2 can be selected
eg:Not supported UART1_TX_M0 and UART1_RX_M1 combination

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	07.UART Map				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	8 of 69

Default I2C Map

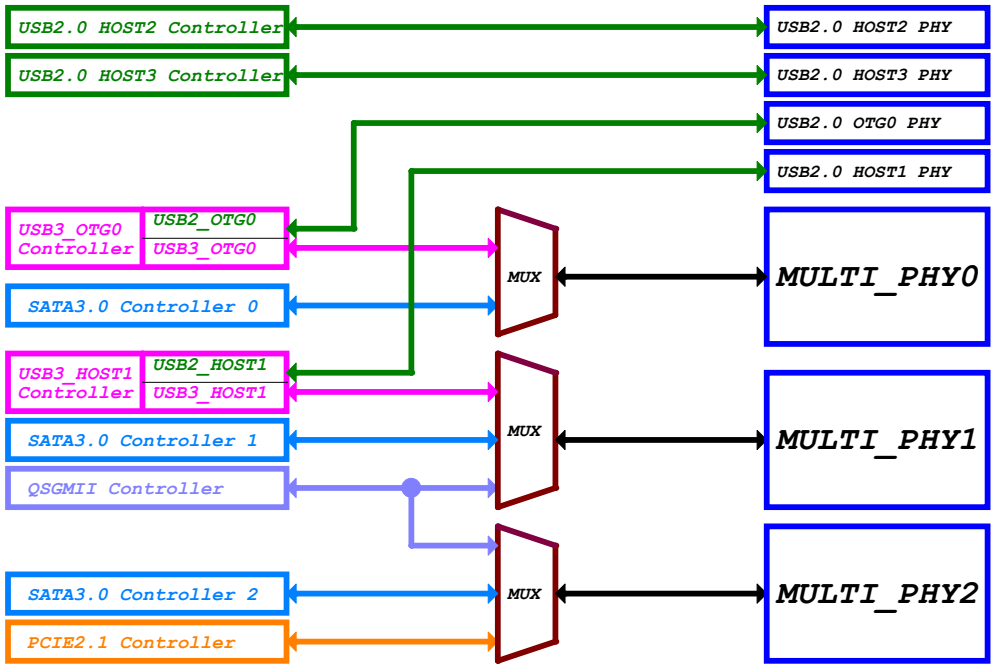
Note:
M0 M1 M2 indicates that the same function is multiplexed to different IO. When selecting, only M0 or M1 or M2 can be selected
eg:
Not supported I2C1_SCL_M0 and I2C1_SDA_M1 combination



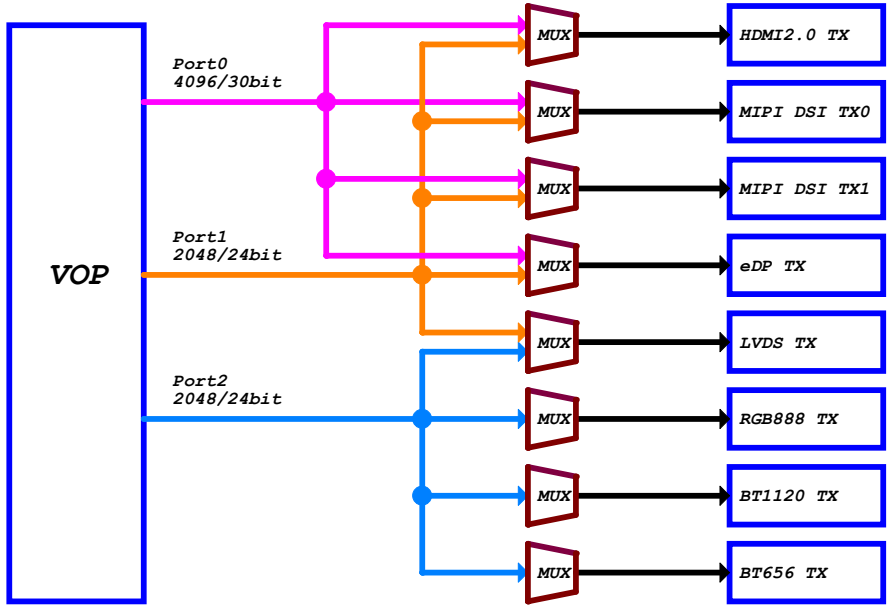
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	08.I2C Bus Map				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	9 of 69

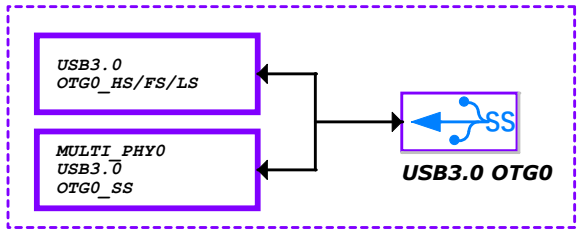
MULTI_PHY0/1/2 Path Map



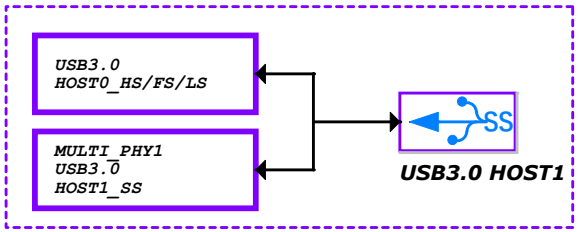
VOP Path Map



USB3.0 OTG0



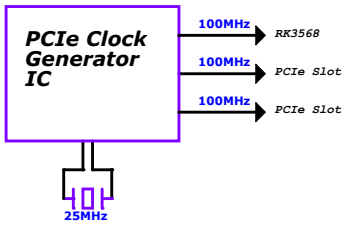
USB3.0 HOST1



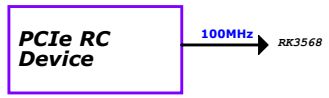
PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIE30_REFCLK (RC:input)	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
			PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

PCIe3.0 REFCLK-RC Mode



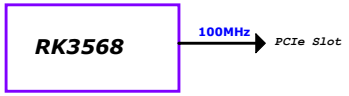
PCIe3.0 REFCLK-EP Mode



PCIe2.1 PHY

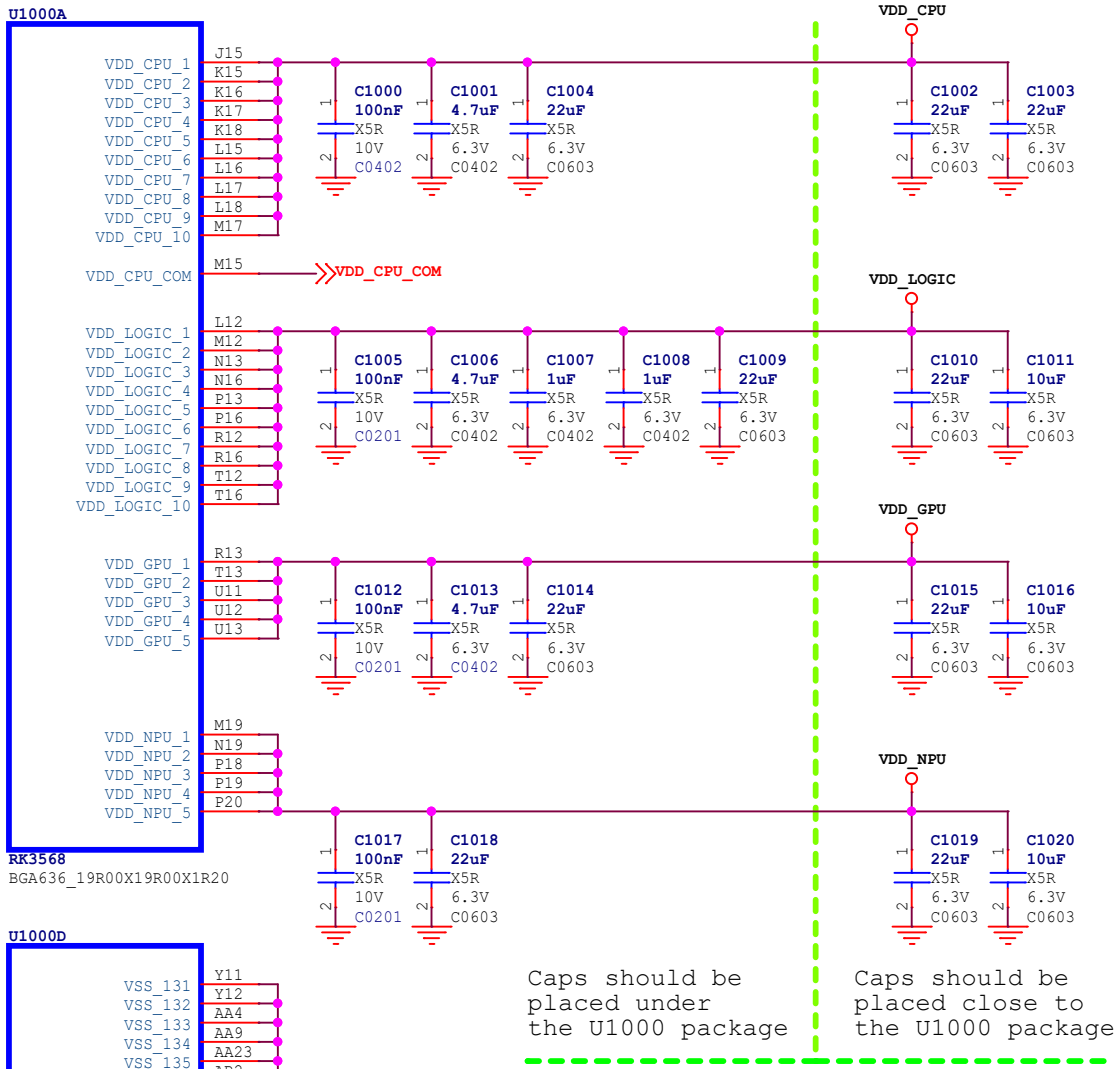
MULTI_PHY2	PCIe2.1 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

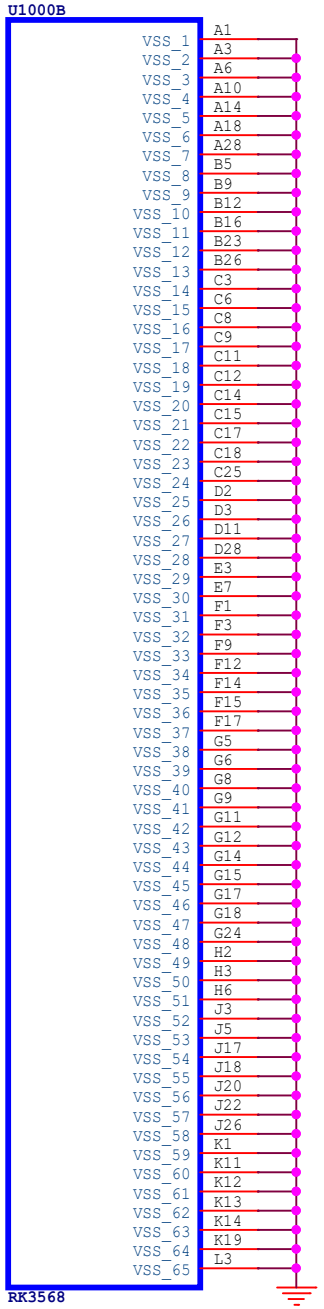
PCIe2.1 REFCLK-RC Mode

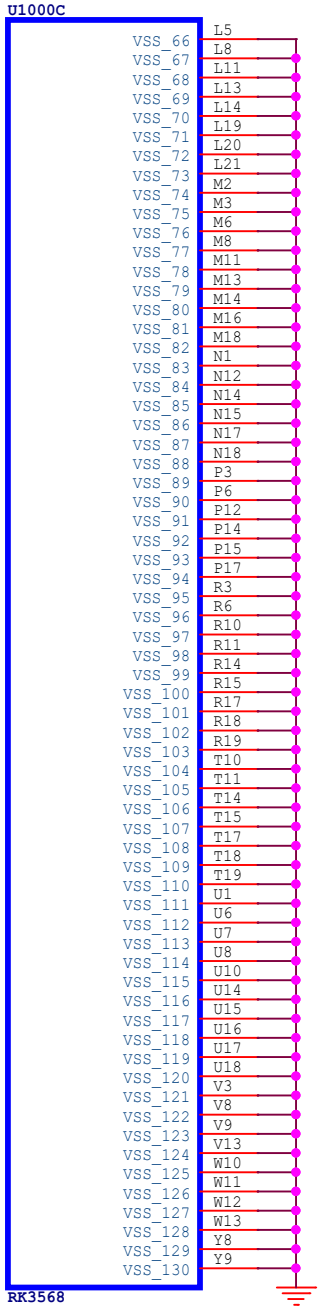


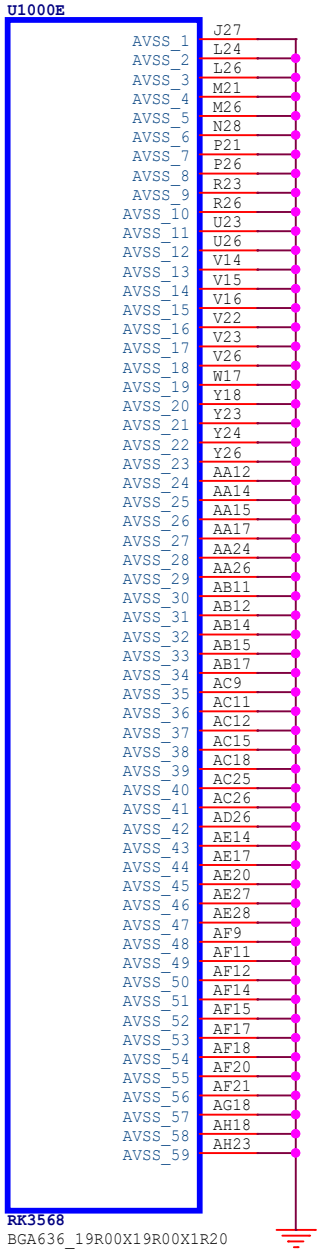
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	09.PCIE30/MULTI_PHY/VOP Fun Map
Date:	Thursday, February 04, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	10 of 69

RK3568_ABCDE (Power&Gnd)



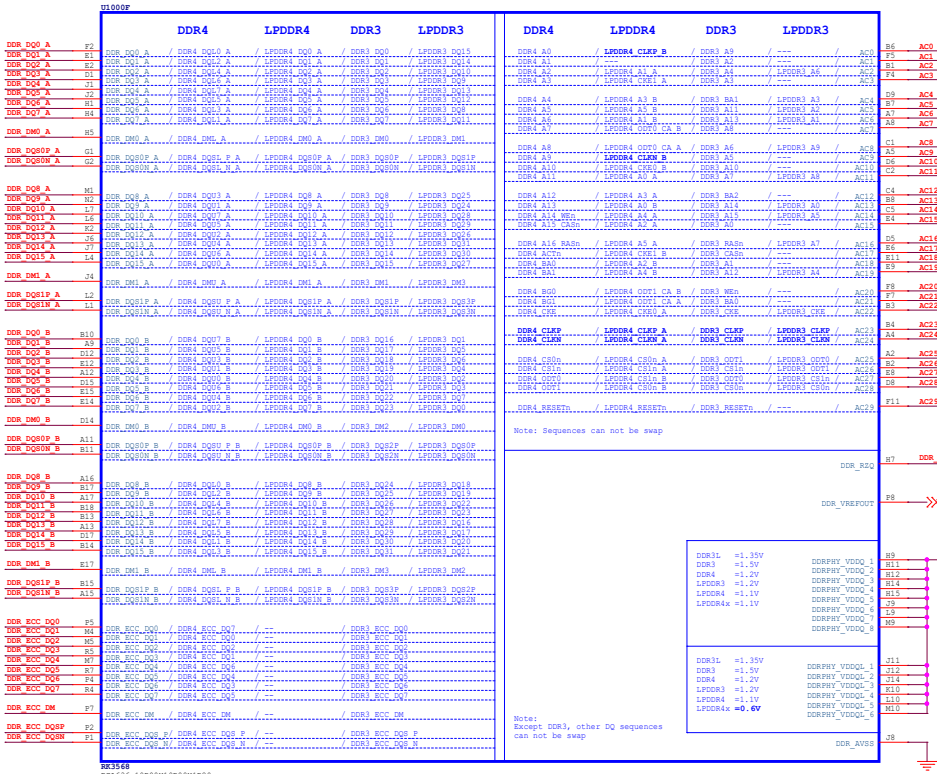




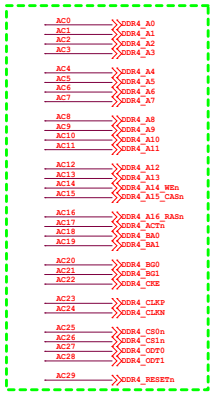


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	10.RK3568_Power/GND				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	11 of 69

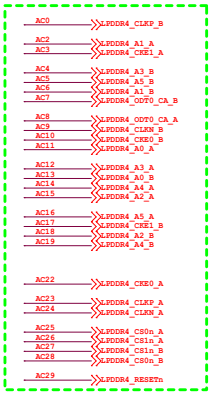
RK3568_F (DDR PHY)



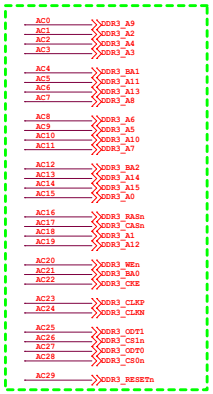
Default DDR4 AC



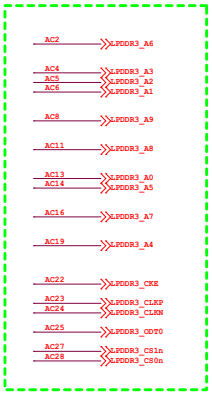
LPDDR4/4x AC



DDR3 AC



LPDDR3 AC

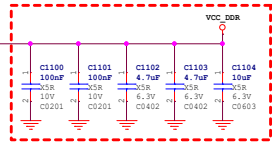


R1100 1 2 120R 1% R0201 — For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

R1101 1 2 120R 1% R0201 VCC_DDR — For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

DDR_RZQ

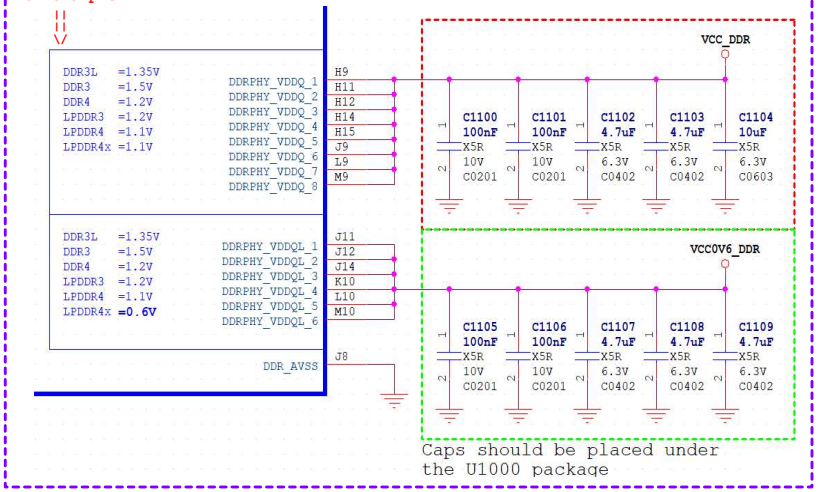
DDRPHY_VREFOUT



Default DDR4

Note:
Caps should be placed under the U1000 package

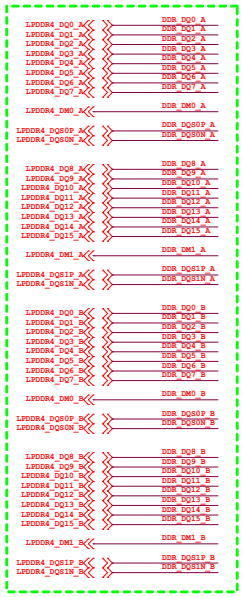
Note:
LPDDR4x mode:
Pin J11,J12,J14,K10,L10,M10 connected to VCC0V6_DDR power supply
For example



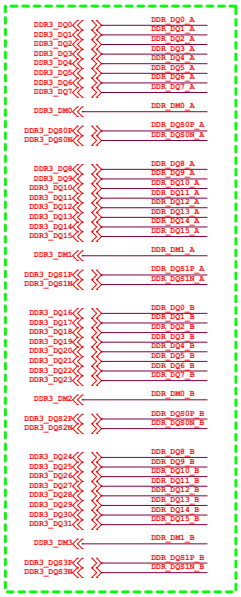
Caps should be placed under the U1000 package

Default DDR4 DQ

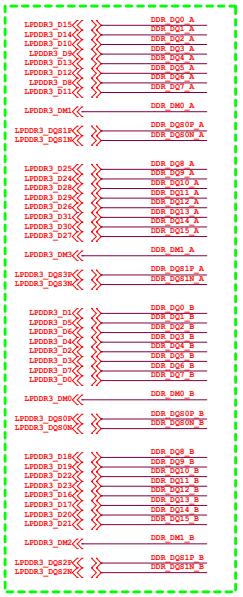
LPDDR4/4x DQ



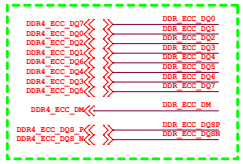
DDR3 DQ



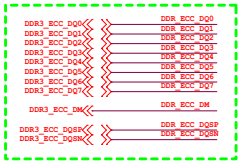
LPDDR3 DQ



DDR4 ECC DQ



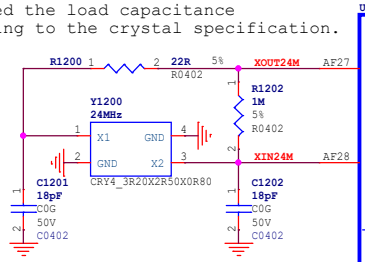
DDR3 ECC DQ

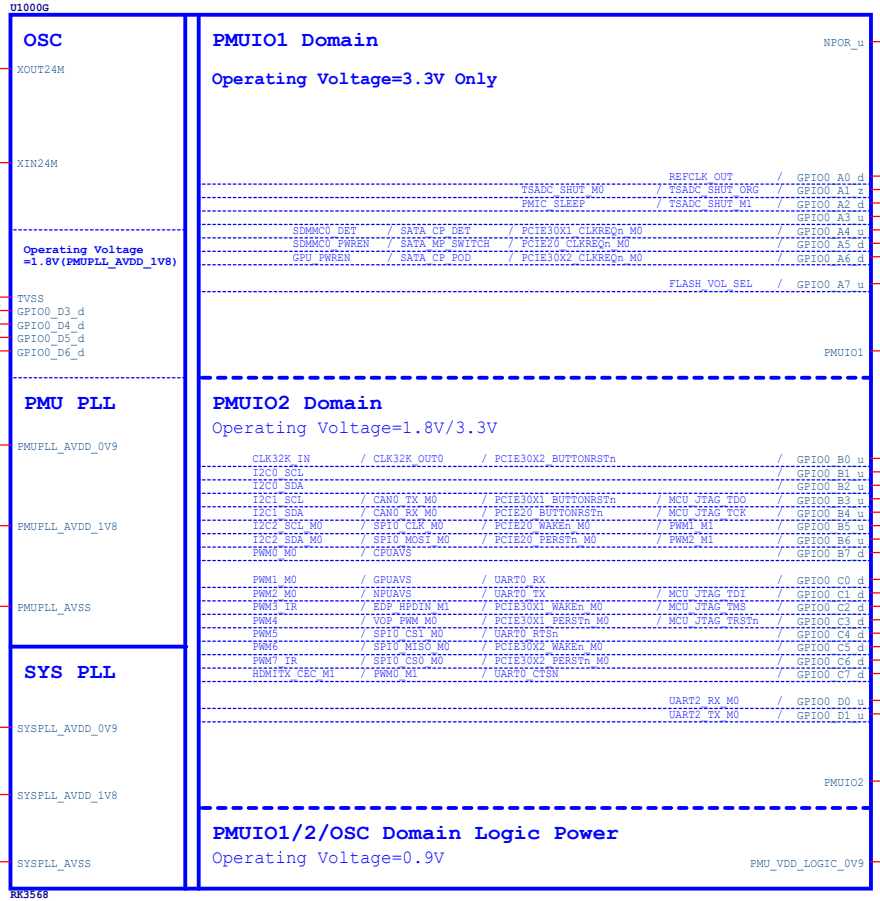


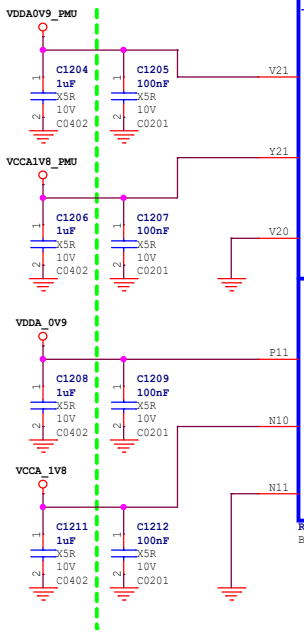
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	11.RK3568_DDR PHY		
Date:	Thursday, February 04, 2021	Rev:	V1.0
Designed by: Zhangtz	Reviewed by: Default	Sheet:	12 of 69

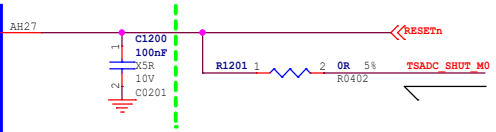
RK3568_G(OSC/PLL/PMUIO1/2)

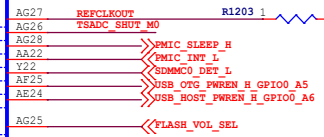
Note:
Adjusted the load capacitance according to the crystal specification.

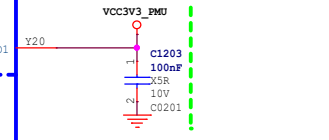


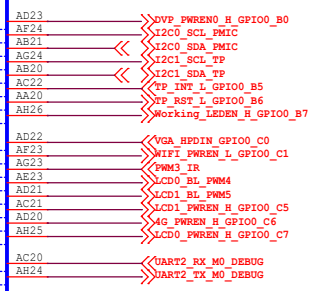


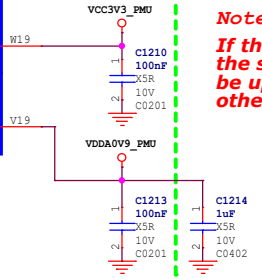


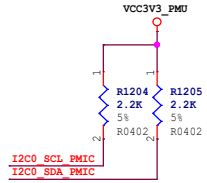


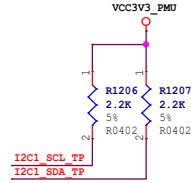


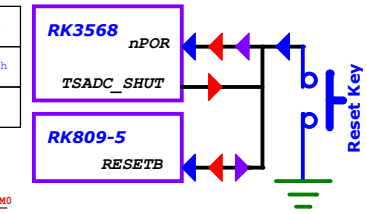












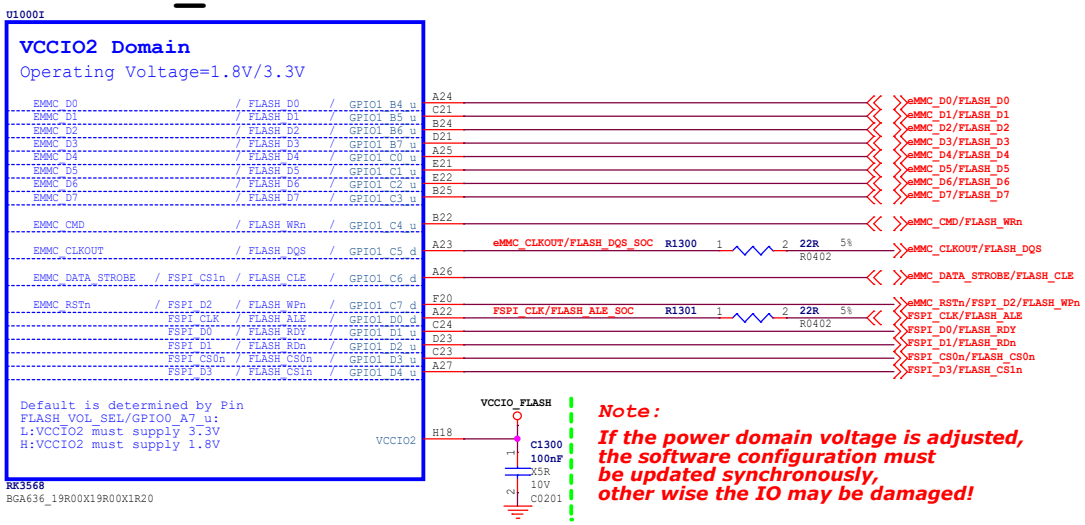
Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

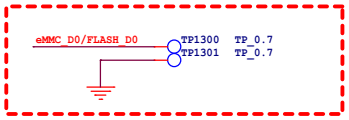
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	12.RK3568_OSC/PLL/PMUIO				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	13 of 69

RK3568_I(VCCIO2 Domain)



Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

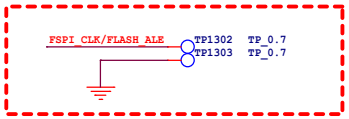


Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added



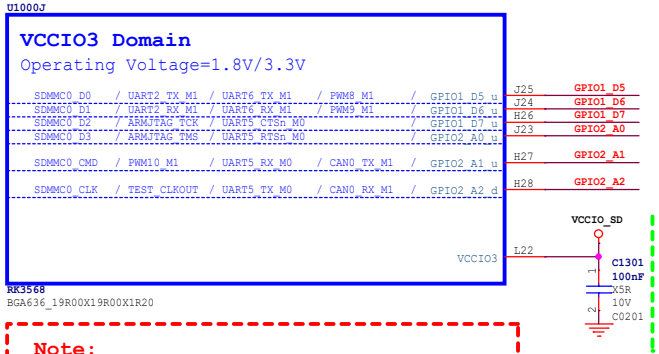
Note:

For SPI Flash:
If FSPI_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware
When writing mismatched firmware or other conditions result in boot failure, use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)

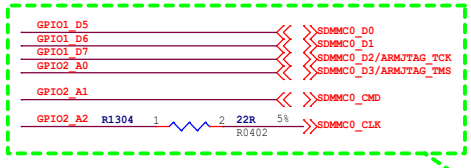


Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

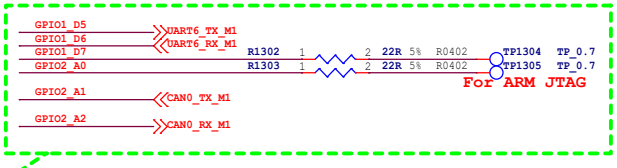
Default

SDMMC0&JTAG



If no MicroSD Card function:

UART&CAN&JTAG



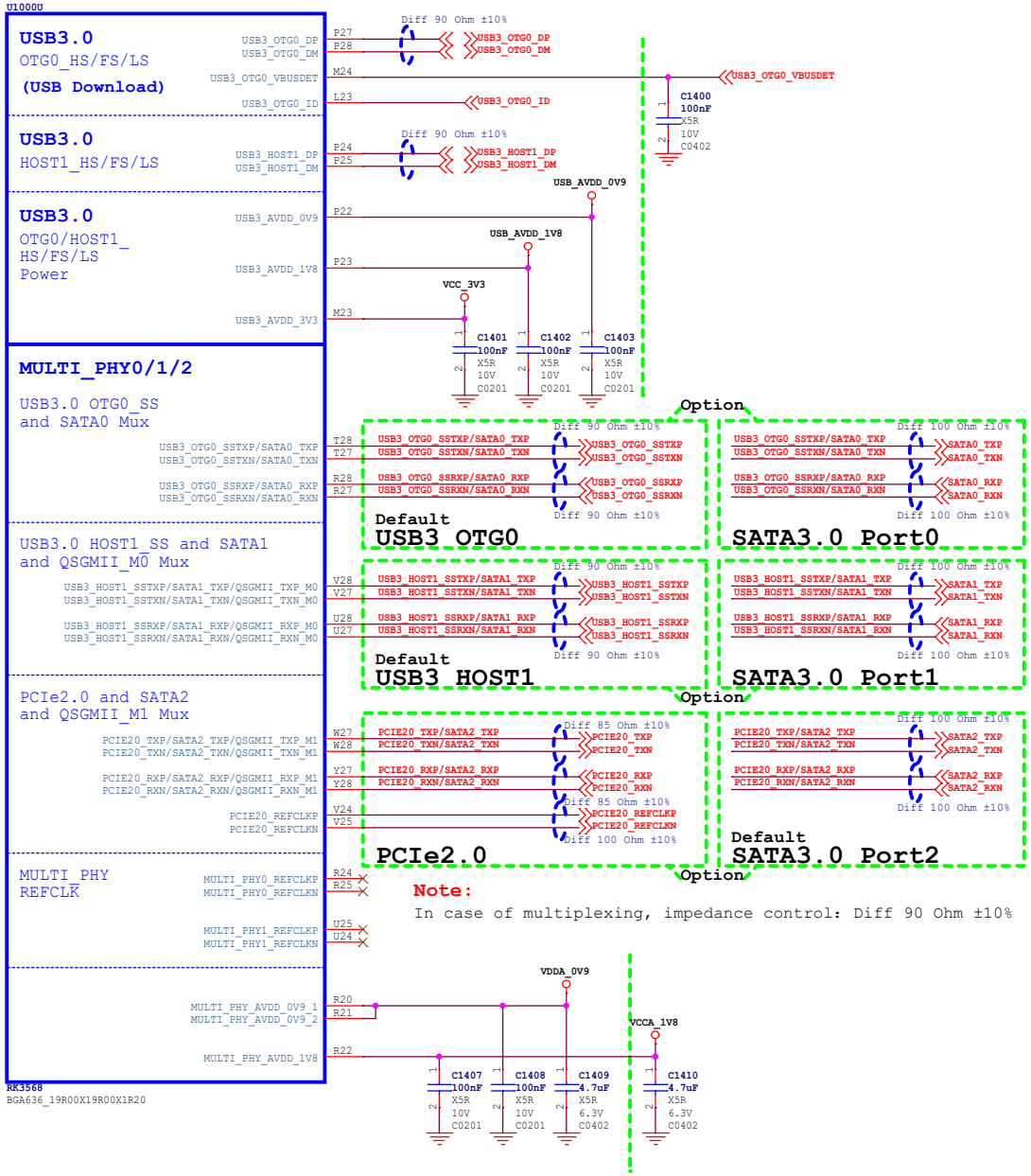
Option

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	13.RK3568_Flash/SD Controller				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	14 of 69

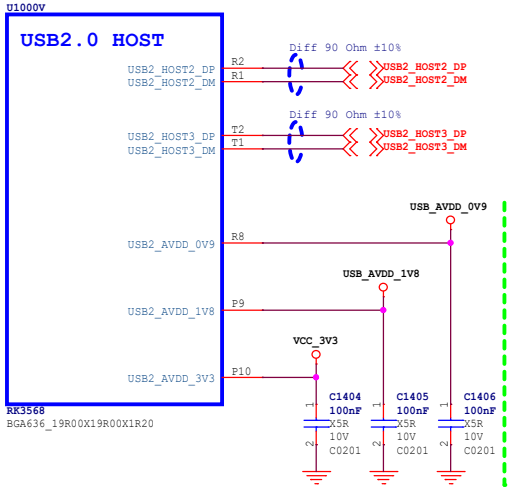
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



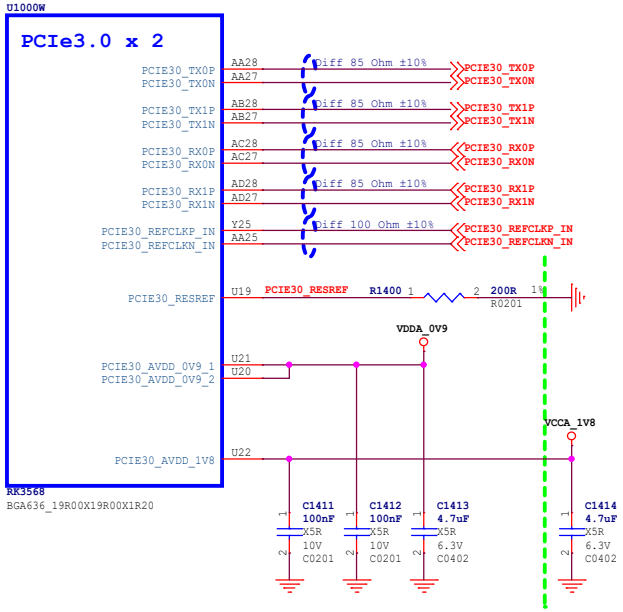
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_V(USB2.0 HOST)

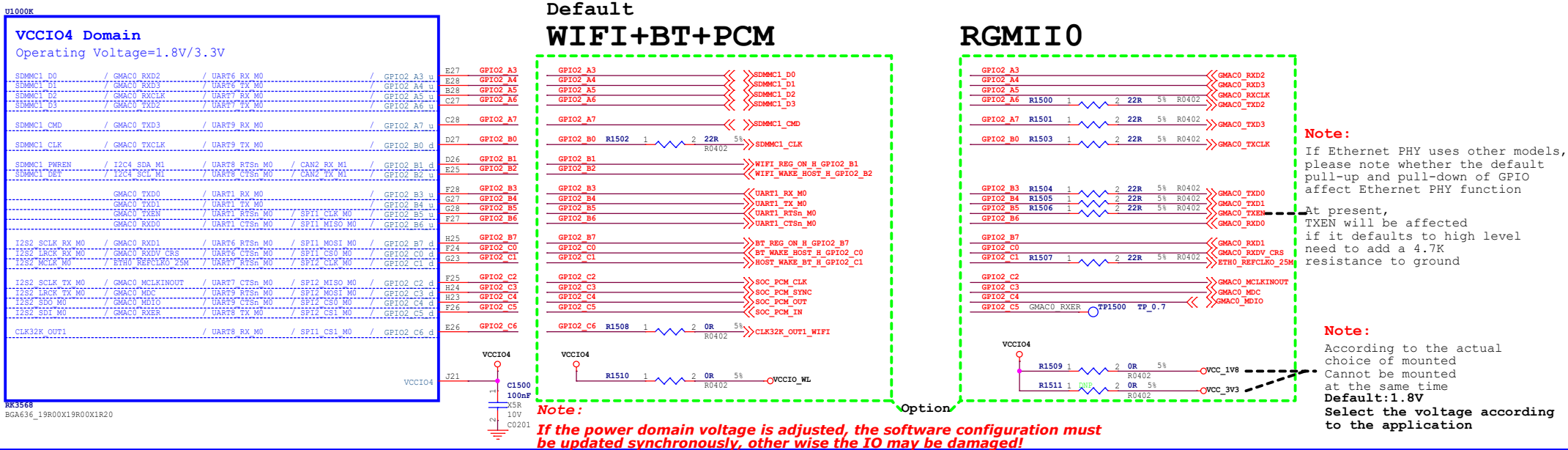


RK3568_W(PCIe3.0 x2)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	14.RK3568_USB/PCIe/SATA PHY				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	15 of 69

RK3568_K(VCCIO4 Domain)



Default

WIFI+BT+PCM

Option

RGMII0

Note:

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

Note:

According to the actual choice of mounted Cannot be mounted at the same time

Default:1.8V

Select the voltage according to the application

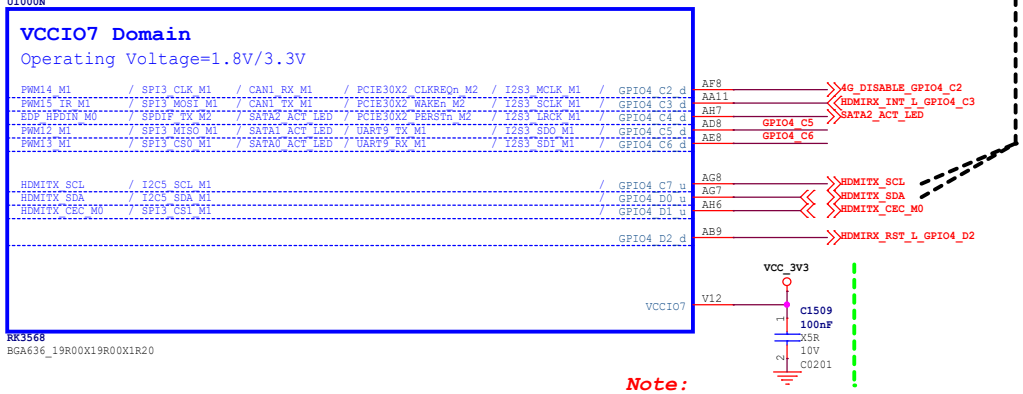
Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_N(VCCIO7 Domain)

Note:

When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices



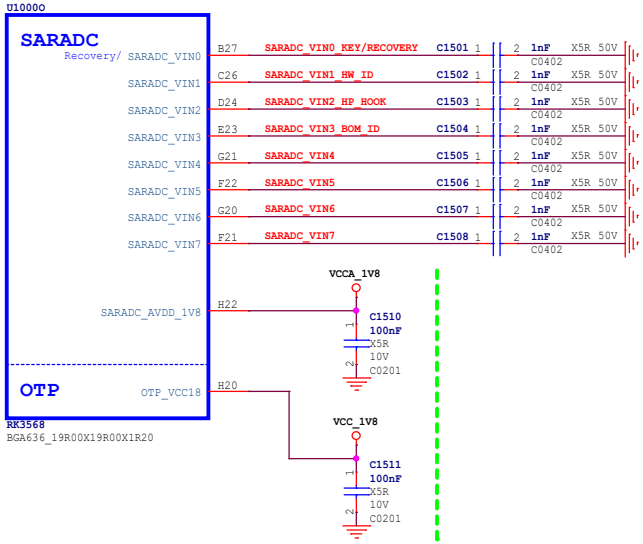
Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Default

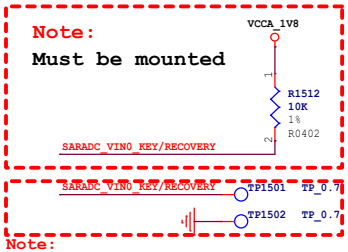
Option

RK3568_O(SARADC/OTP)



Note:

Must be mounted

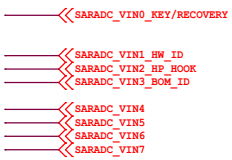


Note:

If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

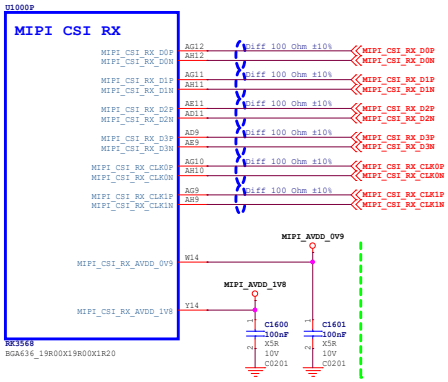


Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

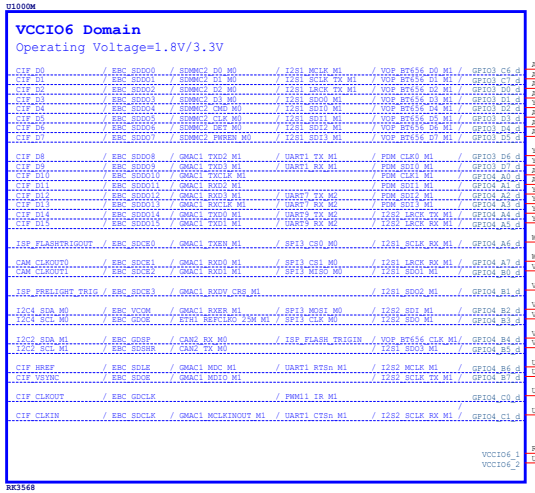
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	15.RK3568_SARADC/GPIO				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	16 of 69

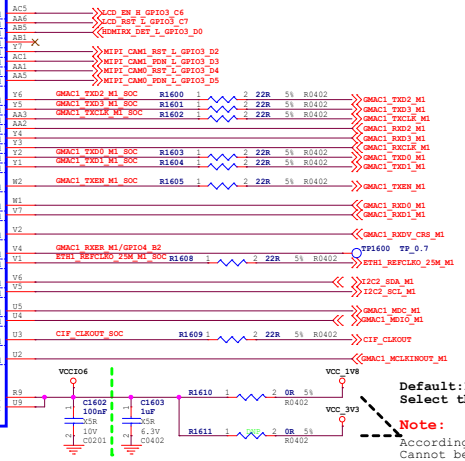
RK3568_P(MIPI_CSI_RX)

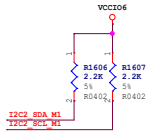


Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)







Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

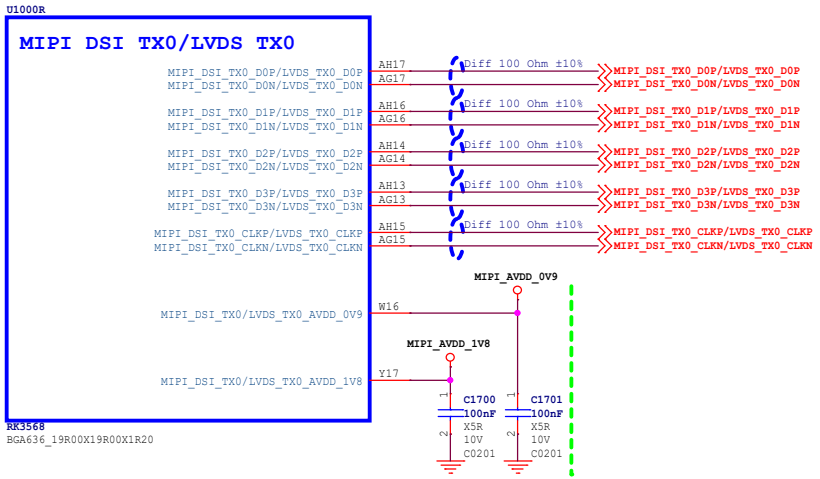
Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

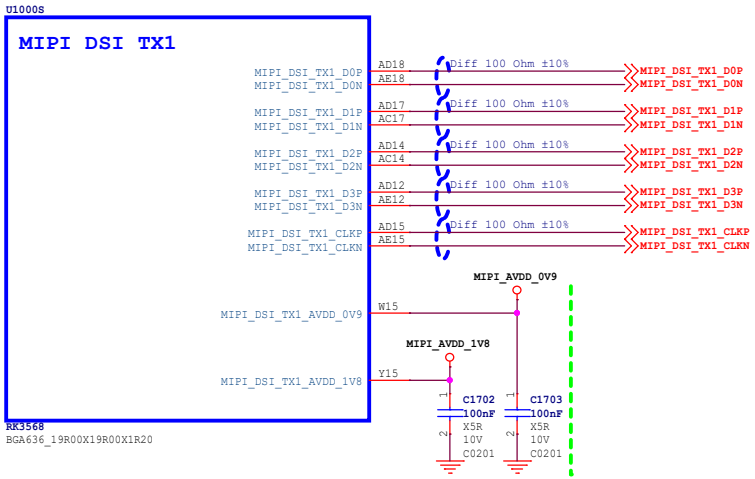
GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_RXDV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx_XTALIN PHYx_CLKOUT125(Option)			
GMACx_MCLKINOUT	<-------		GMACx_MCLKINOUT	------->	PHYx_XTALIN/REFCLK
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	16.RK3568_VI Interface
Date:	Thursday, February 04, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	17 of 69

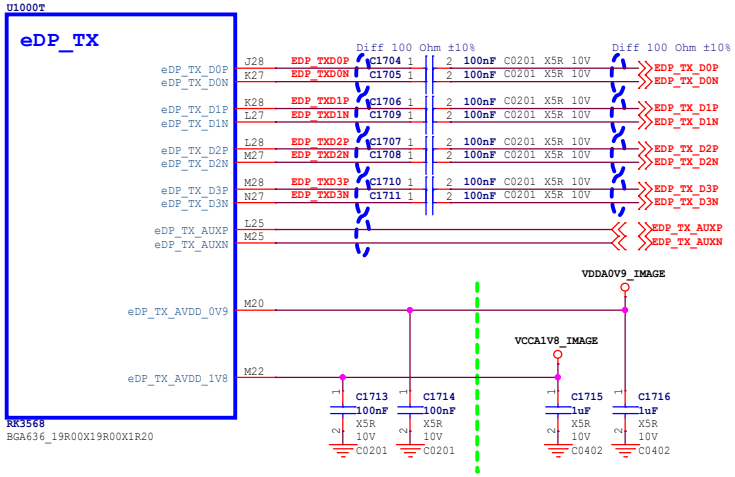
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



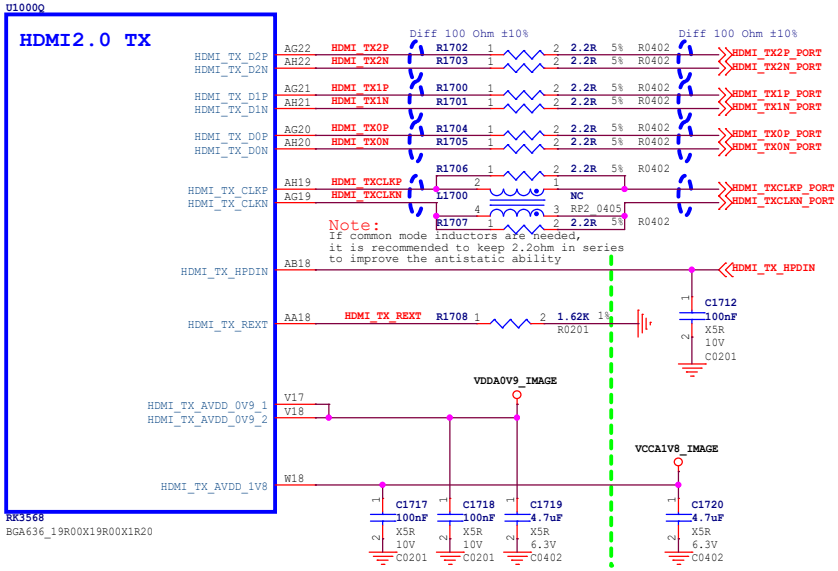
RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_Q(HDMI2.0 TX)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	17.RK3568_VO Interface_1				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	18 of 69

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3568
BGA636_19R00X19R00X1R20

AG6 PCIE20_CLKREQn_M1
AD7 PCIE20_WAKEn_M1
AC8 PCIE30X1_CLKREQn_M1
AC7 PCIE30X1_WAKEn_M1
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 PCIE30X2_PRSNT_L_GPIO2_D7

AH4 PCIE30X1_PRSNT_L_GPIO3_A0

AB8 PCIE30X1_PERSTn_M1

AE5 I2S3_MCLK_M0
AG4 I2S3_SCLK_M0_SOC — R1802 1 2 22R 5% R0402 — TP1800 TP_0.7 — I2S3_SCLK_M0
AF4 I2S3_LRCK_M0_SOC — R1803 1 2 22R 5% R0402 — I2S3_LRCK_M0
AH3 I2S3_SDO_M0 — TP1801 TP_0.7

AG3 I2S3_SDI_M0
AH2 GMAC1_INT/PMEB_GPIO3_A7
AG2 GMAC1_RSTn_GPIO3_B0

AG1 UART4_RX_M1
AF2 UART4_TX_M1
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 RS485_DIR_GPIO3_B5

AE3 GPIO3_B6
AD4 GPIO3_B7
AD2 GPIO3_C0

AD1 PCIE20_PERSTn_M1
AA7 HP_DET_L_GPIO3_C2
AC4 SPK_CTL_H_GPIO3_C3

AC3 UART7_TX_M1
AC2 UART7_RX_M1

V10
V11

VCC_3V3
C1800 100nF X5R 10V C0201

VCC_3V3
R1800 10K 5% R0402 — GMAC0_INT/PMEB_GPIO3_C0
R1801 10K 5% R0402 — GMAC1_INT/PMEB_GPIO3_A7
od

VCC_3V3
R1804 2.2K 5% R0402 — I2C5_SCL_M0
R1805 2.2K 5% R0402 — I2C5_SDA_M0

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Default
PCIe slot
GPIO3_B6 — PCIE20_PRSNT_L_GPIO3_B6

PCIe Ethernet
GPIO3_B6 — PCIE_ETH_ISOLATE_L_GPIO3_B6

Option

Default
GPIO3_B7 — UART3_TX_M1
GPIO3_C0 — UART3_RX_M1

GPIO3_B7 — GMAC0_RSTn_GPIO3_B7
GPIO3_C0 — GMAC0_INT/PMEB_GPIO3_C0

Option

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd			
Project:	RK3568_AIoT_REF_SCH			
File:	18.RK3568_VO Interface_2			
Date:	Thursday, February 04, 2021		Rev:	V1.0
Designed by:	Zhangdz	Reviewed by: Default	Sheet:	19 of 69

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

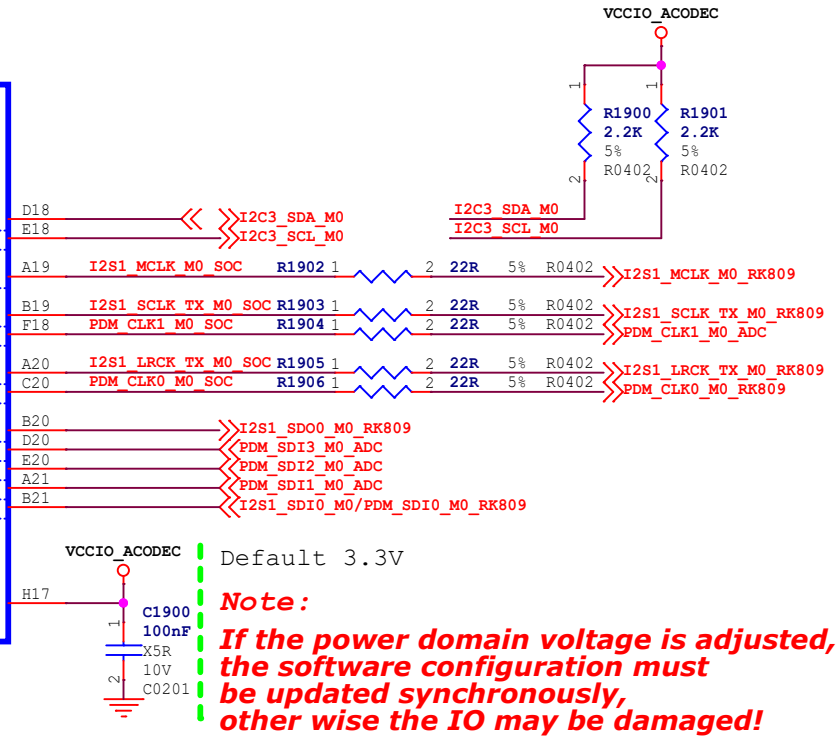
Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20



Note:

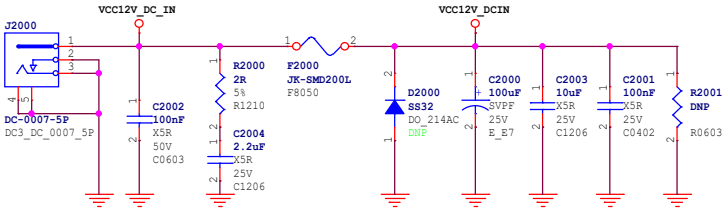
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

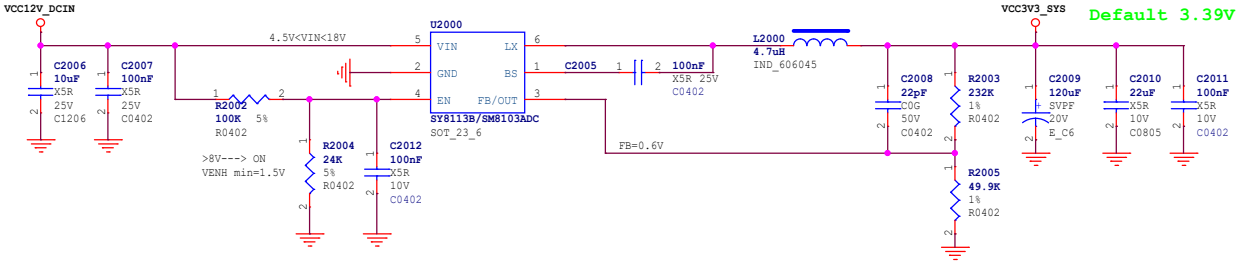
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	19.RK3568_Audio Interface				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	20 of 69

12V/3A DCIN

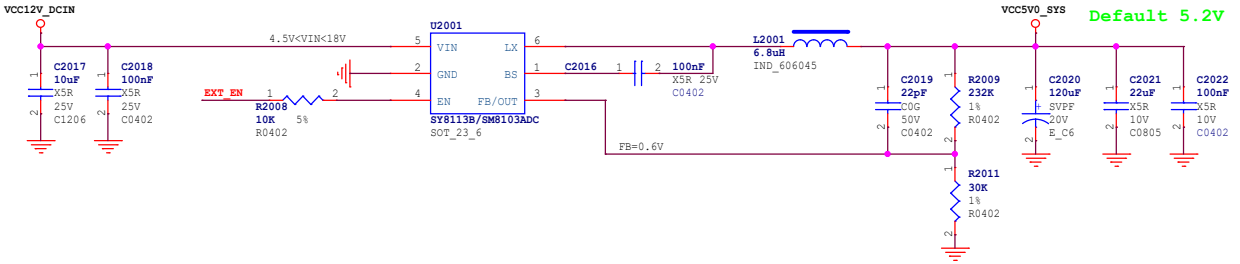
Note:
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe

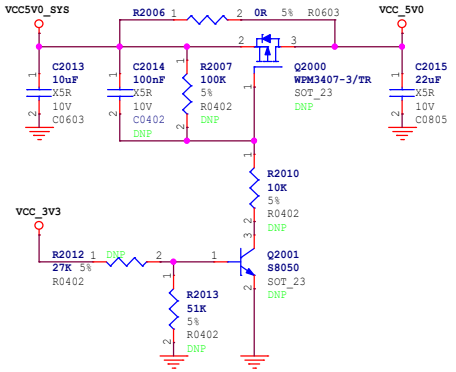


VCC3V3_SYS

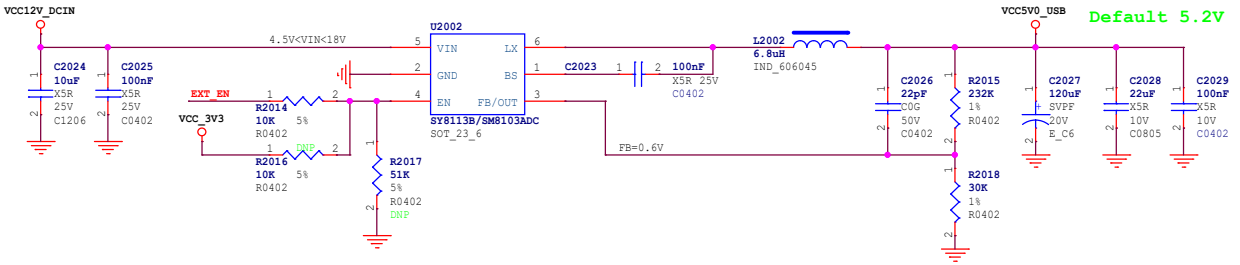


VCC5V0_SYS



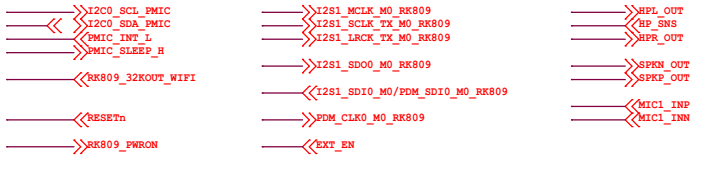


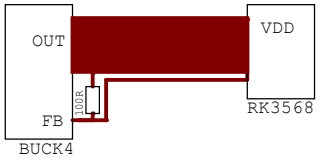
VCC5V0_USB



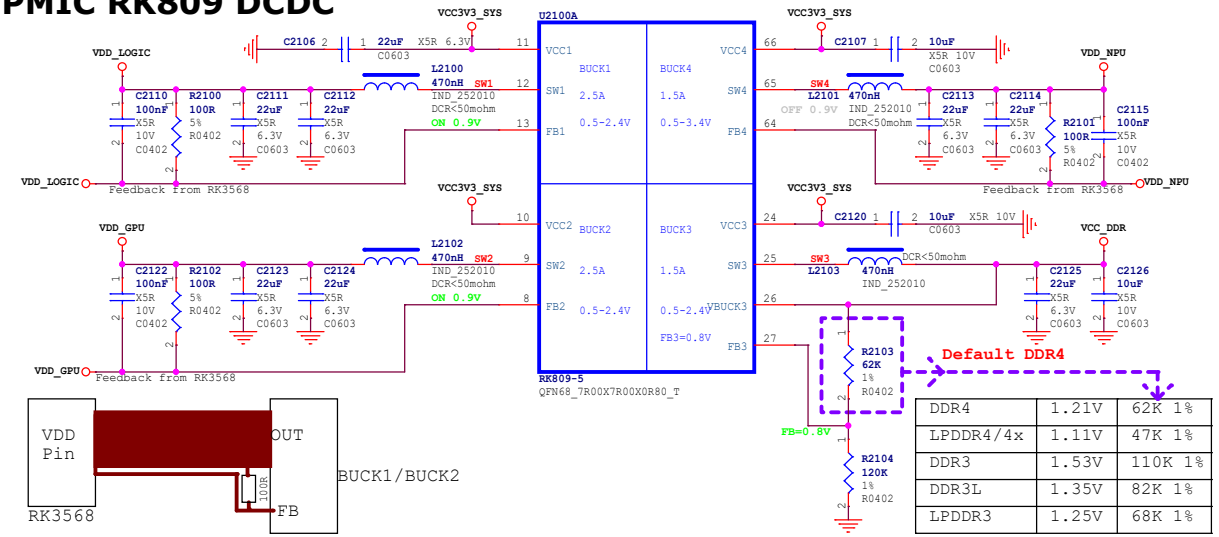
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	20.Power_DC IN				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	21 of 69



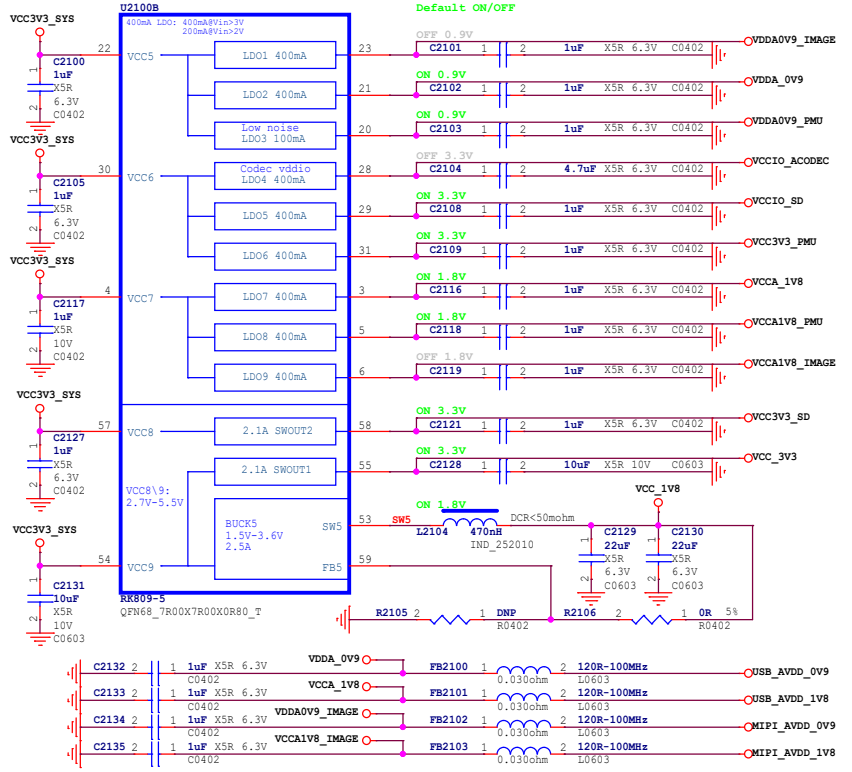


PMIC RK809 DCDC

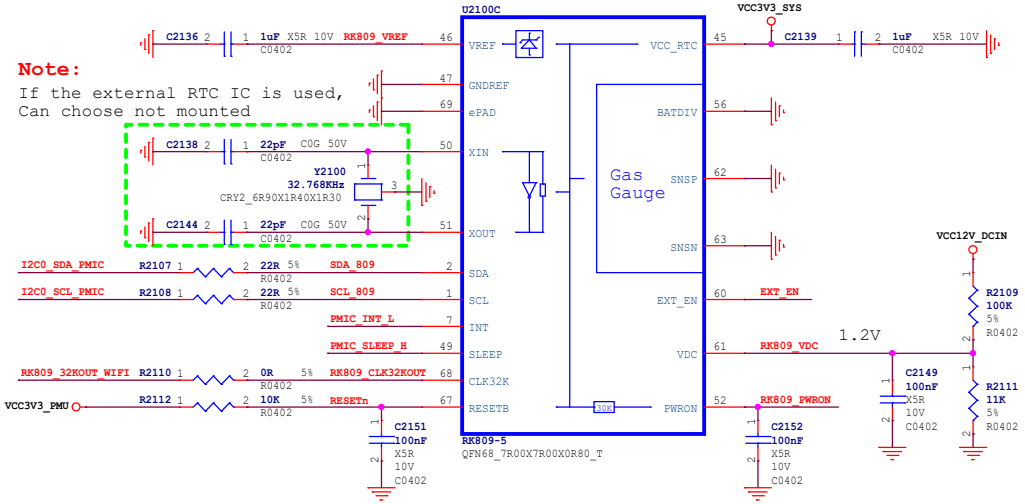


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

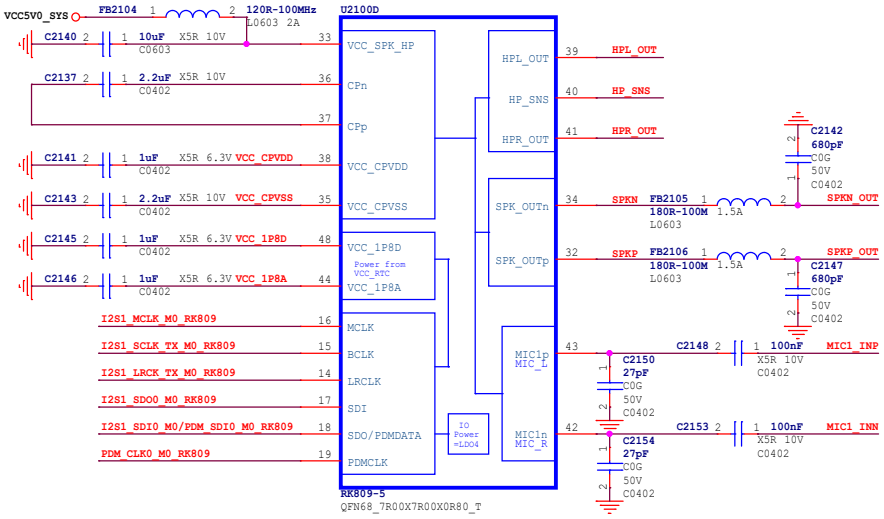
PMIC RK809 LDO



PMIC RK809 Managerment



PMIC RK809 CODEC



Note:

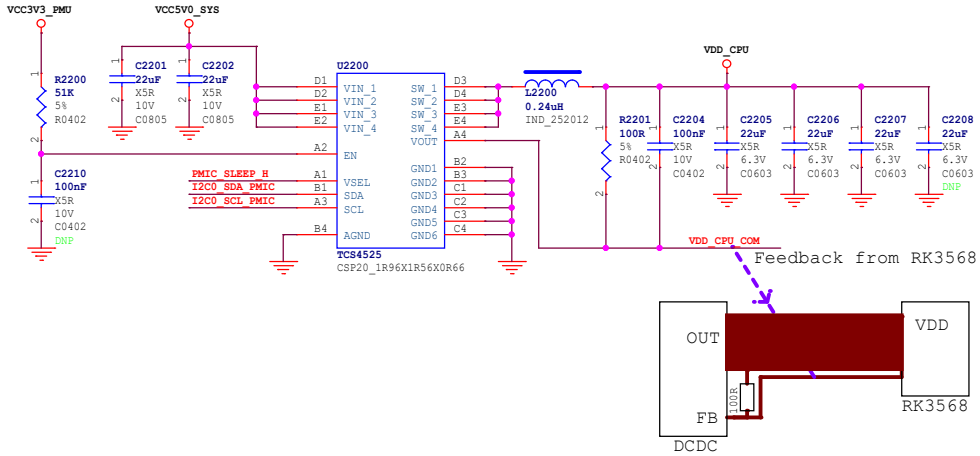
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	21.Power_PMIC				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	22 of 69

I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_SLEEP_H
VDD_CPU_COM
RTCIC_INT_L_GPIO0_D3
RTCIC_32KOUT
I2C5_SCL_M0
I2C5_SDA_M0
LCD0_PWREN_H_GPIO0_C7
LCD1_PWREN_H_GPIO0_C5

VDD_CPU

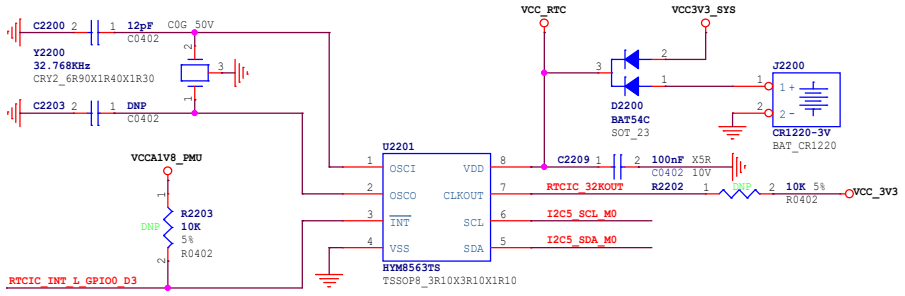


RTC IC --Option

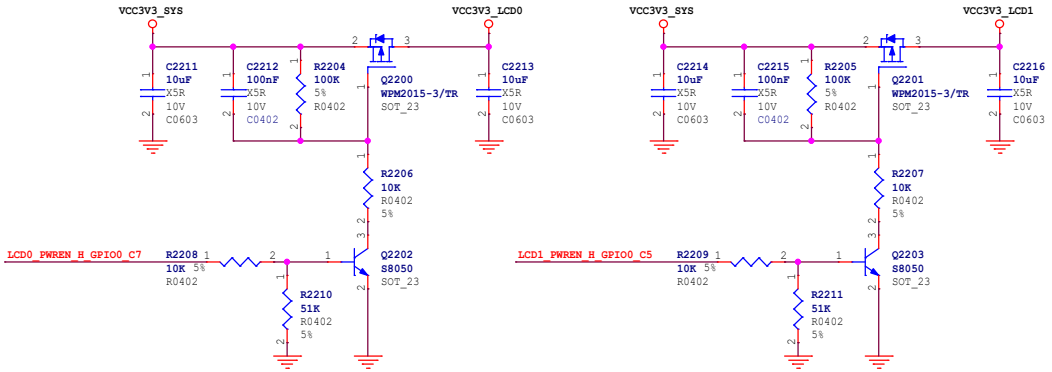
Note:

The power off hold time scheme is required,
It is recommended to use external RTC IC

But, it will not support the timing poweron function



Address:Read A3H,Write A2H



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	22.Power_Ext Discrete/RTC IC				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	23 of 69

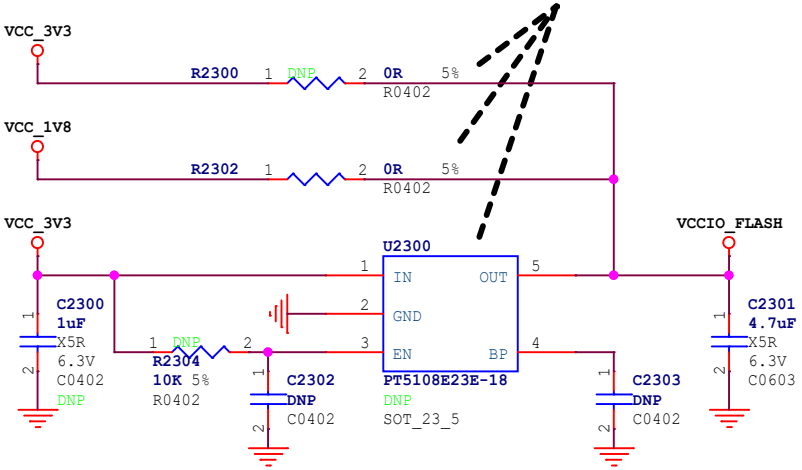
FLASH_VOL_SEL

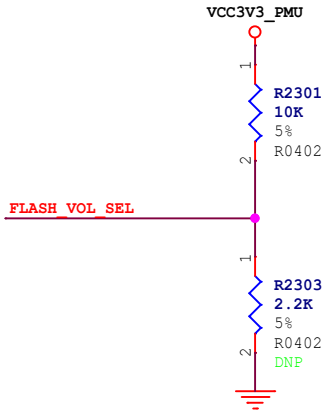
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

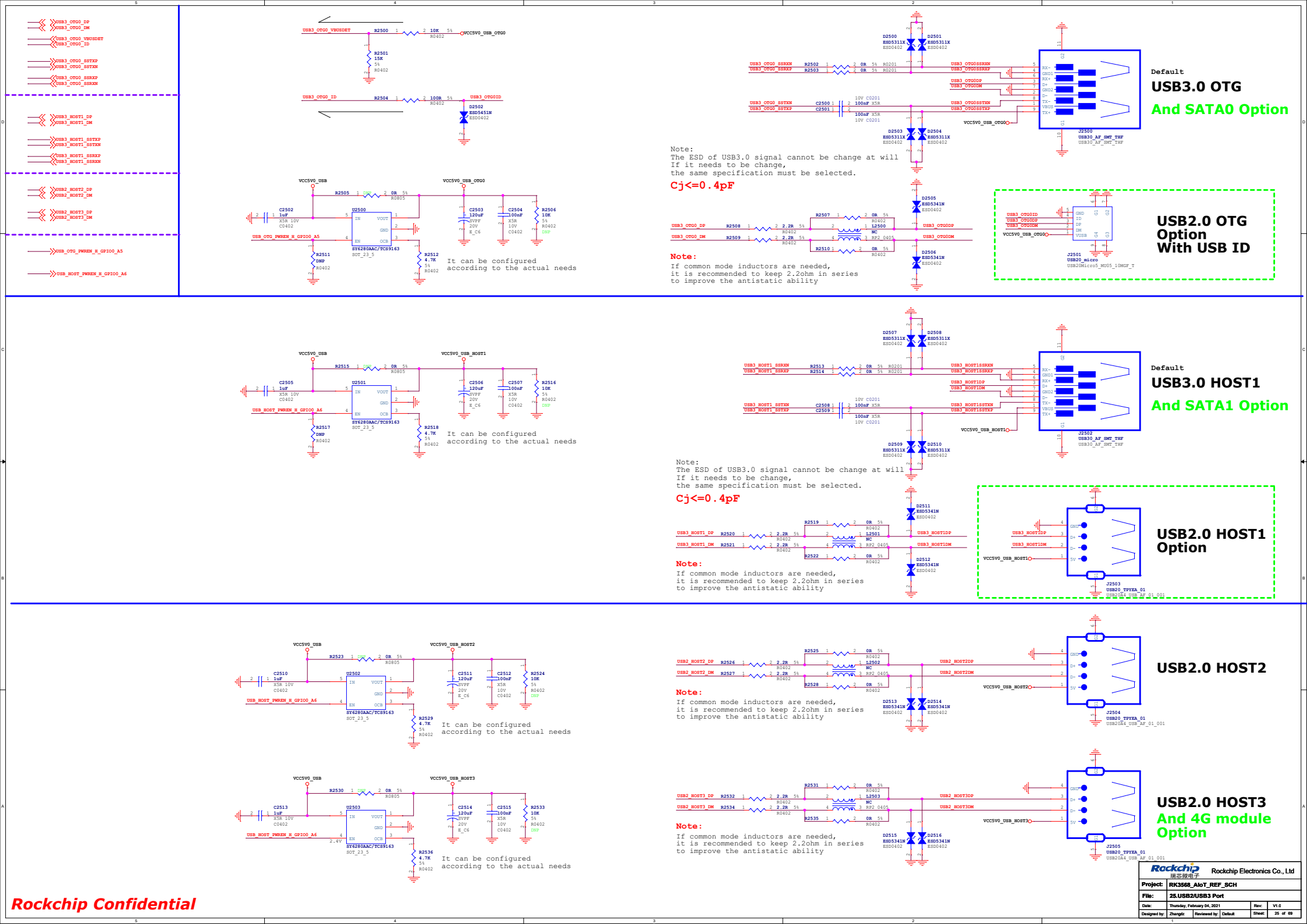
According to the actual choice of mounted
Cannot be mounted at the same time

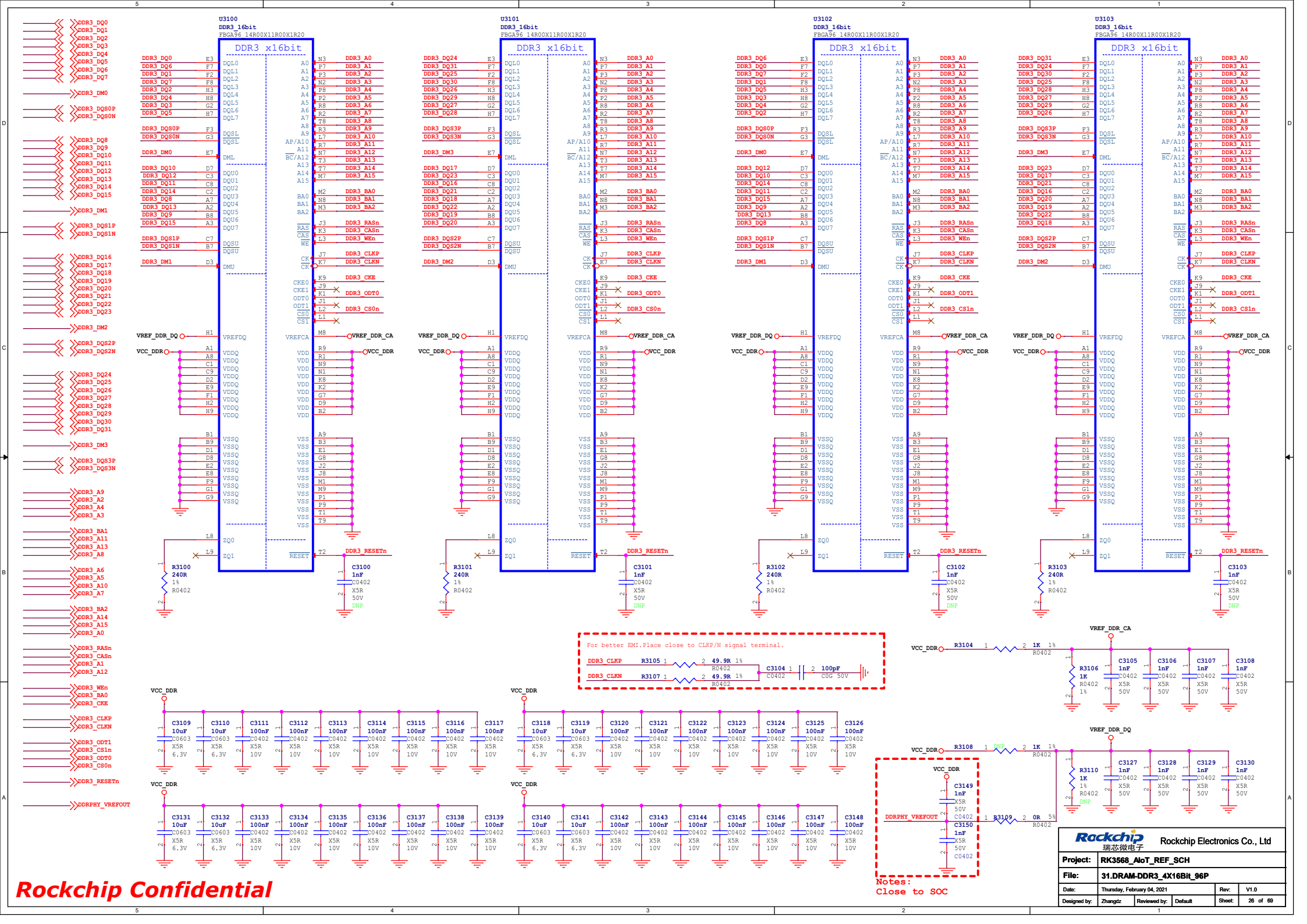


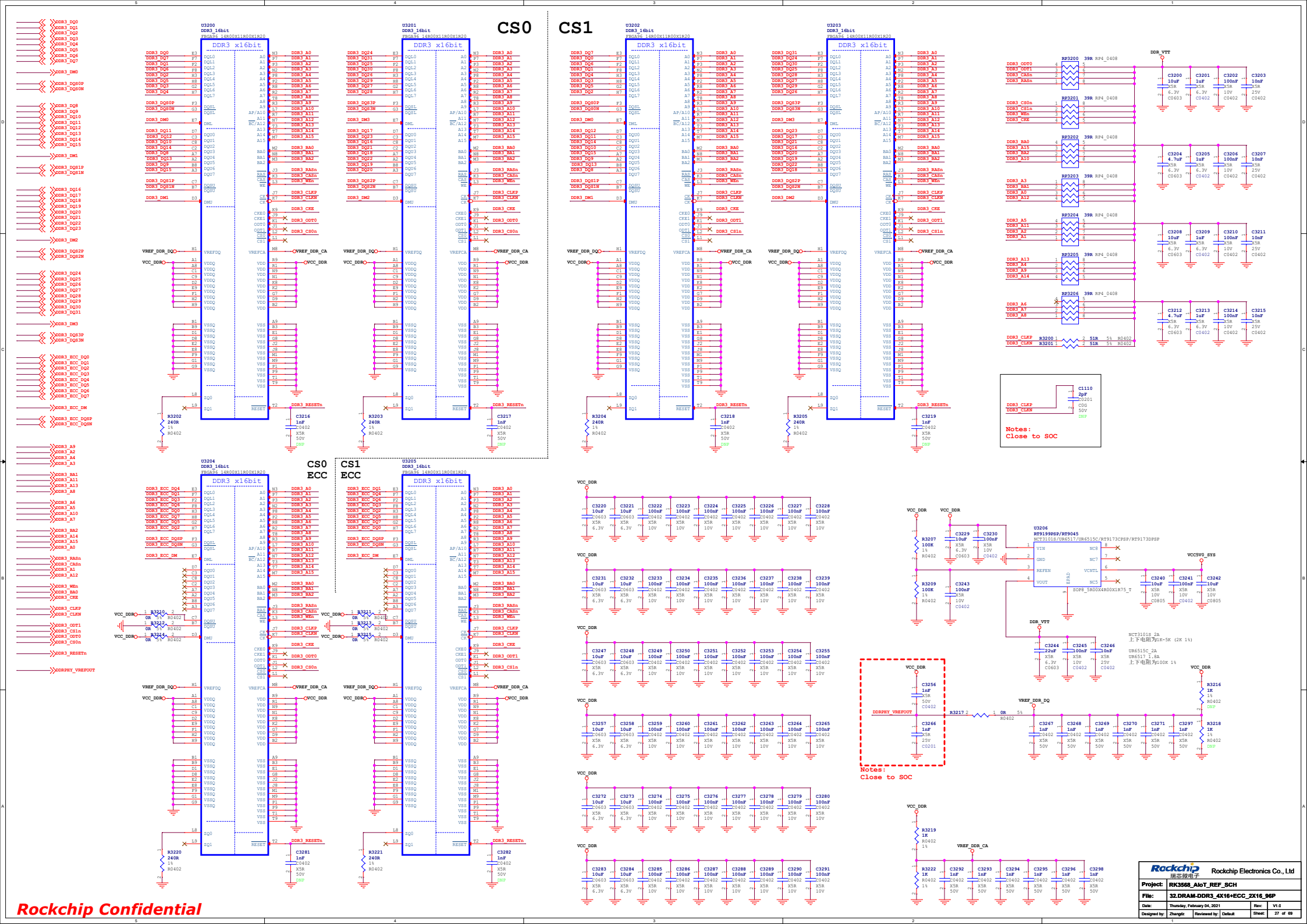


Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

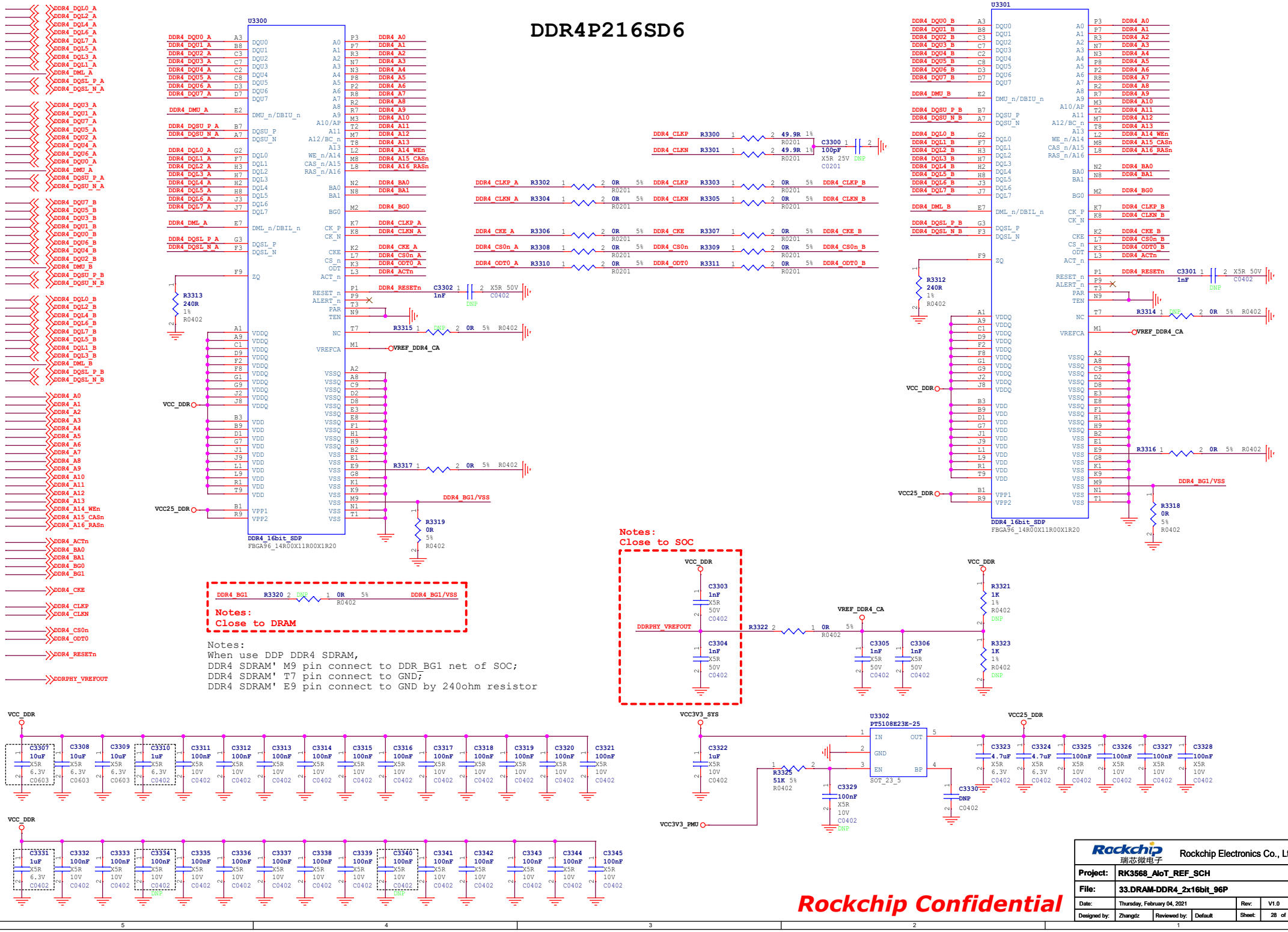
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	23.Power_Flash Power Manage				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	24 of 69


USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_VBUSDET
USB3_OTG0_ID
USB3_OTG0_SSTXP
USB3_OTG0_SSTXN
USB3_OTG0_SSRXP
USB3_OTG0_SSRXN
USB3_HOST1_DP
USB3_HOST1_DM
USB3_HOST1_SSTXP
USB3_HOST1_SSTXN
USB3_HOST1_SSRXP
USB3_HOST1_SSRXN
USB2_HOST2_DP
USB2_HOST2_DM
USB2_HOST3_DP
USB2_HOST3_DM
USB_OTG_PWREN_H_GPIO0_A5
USB_HOST_PWREN_H_GPIO0_A6
USB3_OTG0_VBUSDET
R2500 10K 5% R0402
VCC5V0_USB_OTG0
R2501 15K 5% R0402
USB3_OTG0_ID
R2504 100R 5% R0402
USB3_OTG0ID
D2502 ESD5451N ESD0402
VCC5V0_USB
VCC5V0_USB_OTG0
R2505 0R 5% R0805 DNP
C2502 1uF X5R 10V C0402
U2500 SY6280AAC/TCS9163 SOT_23_5
C2503 120uF SVPF 20V E_C6
C2504 100nF X5R 10V C0402
R2506 10K 5% R0402 DNP
R2511 DNP R0402
R2512 4.7K 5% R0402
It can be configured according to the actual needs
D2500 D2501 ESD5311X ESD0402
USB3_OTG0_SSRXN USB3_OTG0_SSRXP
R2502 R2503 0R 5% R0201
USB3_OTG0SSRXN USB3_OTG0SSRXP
USB3_OTG0DP USB3_OTG0DM
USB3_OTG0_SSTXN USB3_OTG0_SSTXP
C2500 C2501 100nF X5R 10V C0201
USB3_OTG0SSTXN USB3_OTG0SSTXP
D2503 D2504 ESD5311X ESD0402
J2500 USB30_AF_SMT_THF
Note:
The ESD of USB3.0 signal cannot be change at will
If it needs to be change,
the same specification must be selected.
Cj<=0.4pF
D2505 ESD5341N ESD0402
R2507 0R 5% R0402
R2508 R2509 2.2R 5% R0402
L2500 NC RP2_0405
R2510 0R 5% R0402
D2506 ESD5341N ESD0402
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
J2501 USB20_micro USB20Micro5_MU05_10MGF_T
Default
USB3.0 OTG
And SATA0 Option
USB2.0 OTG Option With USB ID
VCC5V0_USB
VCC5V0_USB_HOST1
R2515 0R 5% R0805 DNP
C2505 1uF X5R 10V C0402
U2501 SY6280AAC/TCS9163 SOT_23_5
C2506 120uF SVPF 20V E_C6
C2507 100nF X5R 10V C0402
R2516 10K 5% R0402 DNP
R2517 DNP R0402
R2518 4.7K 5% R0402
It can be configured according to the actual needs
D2507 D2508 ESD5311X ESD0402
USB3_HOST1_SSRXN USB3_HOST1_SSRXP
R2513 R2514 0R 5% R0201
USB3_HOST1SSRXN USB3_HOST1SSRXP
USB3_HOST1DP USB3_HOST1DM
USB3_HOST1_SSTXN USB3_HOST1_SSTXP
C2508 C2509 100nF X5R 10V C0201
USB3_HOST1SSTXN USB3_HOST1SSTXP
VCC5V0_USB_HOST1
D2509 D2510 ESD5311X ESD0402
J2502 USB30_AF_SMT_THF
Note:
The ESD of USB3.0 signal cannot be change at will
If it needs to be change,
the same specification must be selected.
Cj<=0.4pF
D2511 ESD5341N ESD0402
R2519 0R 5% R0402
USB3_HOST1_DP USB3_HOST1_DM
R2520 R2521 2.2R 5% R0402
L2501 NC RP2_0405
R2522 0R 5% R0402
D2512 ESD5341N ESD0402
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
J2503 USB20_TPYEA_01 USB20A4_USB_AF_01_001
Default
USB3.0 HOST1
And SATA1 Option
USB2.0 HOST1 Option
VCC5V0_USB
VCC5V0_USB_HOST2
R2523 0R 5% R0805 DNP
C2510 1uF X5R 10V C0402
U2502 SY6280AAC/TCS9163 SOT_23_5
C2511 120uF SVPF 20V E_C6
C2512 100nF X5R 10V C0402
R2524 10K 5% R0402 DNP
R2529 4.7K 5% R0402
It can be configured according to the actual needs
USB2_HOST2_DP USB2_HOST2_DM
R2525 0R 5% R0402
R2526 R2527 2.2R 5% R0402
L2502 NC RP2_0405
R2528 0R 5% R0402
D2513 D2514 ESD5341N ESD0402
J2504 USB20_TPYEA_01 USB20A4_USB_AF_01_001
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
USB2.0 HOST2
VCC5V0_USB
VCC5V0_USB_HOST3
R2530 0R 5% R0805 DNP
C2513 1uF X5R 10V C0402
U2503 SY6280AAC/TCS9163 SOT_23_5
C2514 120uF SVPF 20V E_C6
C2515 100nF X5R 10V C0402
R2533 10K 5% R0402 DNP
R2536 4.7K 5% R0402
It can be configured according to the actual needs
USB2_HOST3_DP USB2_HOST3_DM
R2531 0R 5% R0402
R2532 R2534 2.2R 5% R0402
L2503 NC RP2_0405
R2535 0R 5% R0402
D2515 D2516 ESD5341N ESD0402
J2505 USB20_TPYEA_01 USB20A4_USB_AF_01_001
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
USB2.0 HOST3
And 4G module Option
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 25.USB2/USB3 Port
Date: Thursday, February 04, 2021
Rev: V1.0
Designed by: Zhangtz
Reviewed by: Default
Sheet: 25 of 69




CS0
CS1
CS0 ECC
CS1 ECC
DDR3 x16bit
Notes:
Close to SOC
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 32.DRAM-DDR3_4X16+ECC_2X16_96P
Date: Thursday, February 04, 2021
Rev: V1.0
Designed by: Zhangtz
Reviewed by: Default
Sheet: 27 of 69

DDR4P216SD6

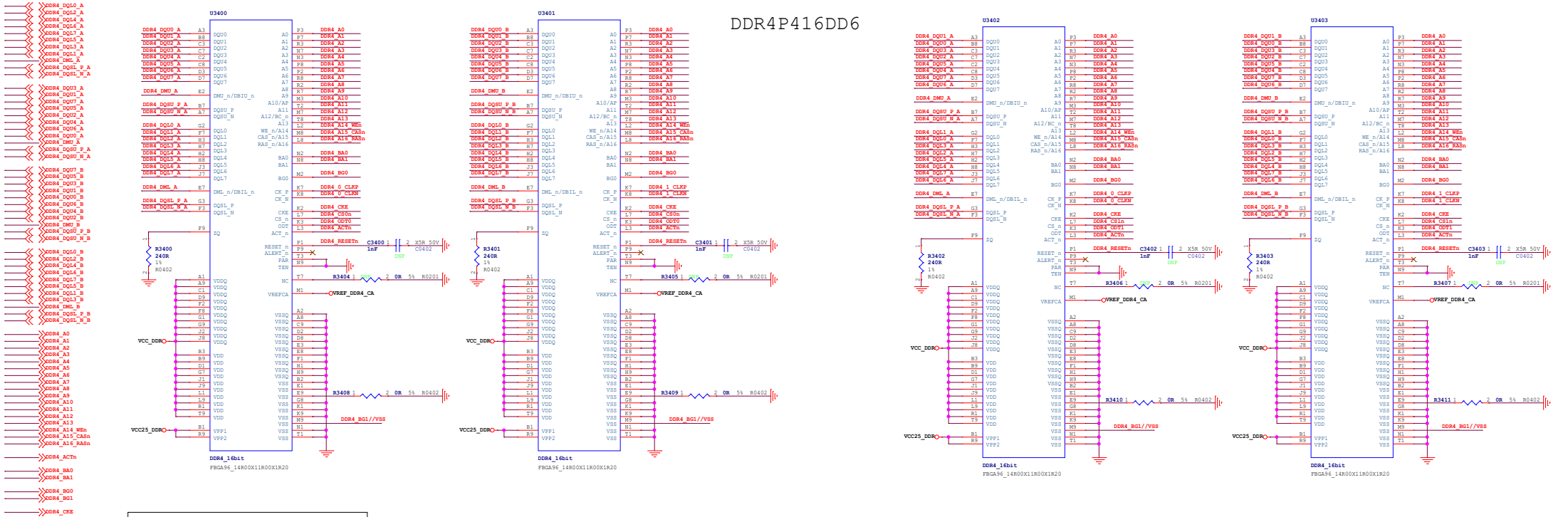


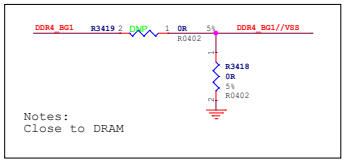
Notes:
When use DDP DDR4 SDRAM,
DDR4 SDRAM' M9 pin connect to DDR_BG1 net of SOC;
DDR4 SDRAM' T7 pin connect to GND;
DDR4 SDRAM' E9 pin connect to GND by 240ohm resistor

Rockchip Confidential

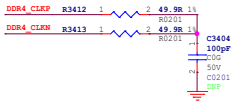
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	33.DRAM-DDR4_2x16bit_96P				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	28 of 69

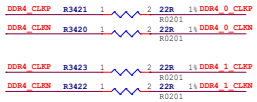
DDR4P416DD6

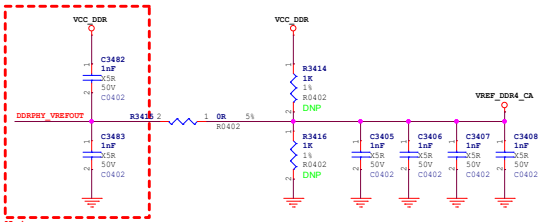


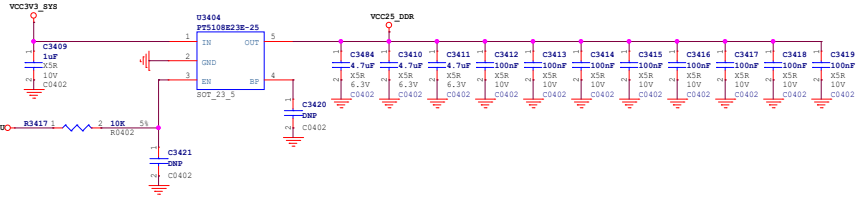


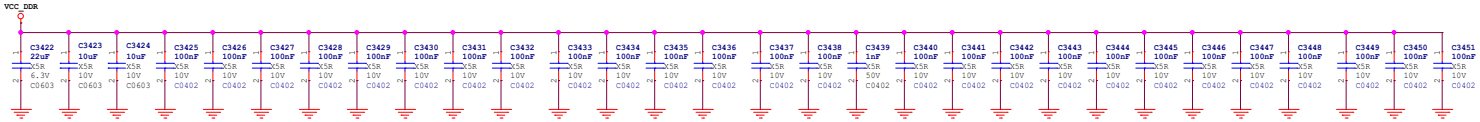
Notes:
When use 16Gbit/32Gbit DDR4 SDRAM,
DDR4 SDRAM' M9 pin connect to DDR_BG1 net of SOC;
DDR4 SDRAM' T7 pin connect to GND;
DDR4 SDRAM' E9 pin connect to GND by 240ohm resistor

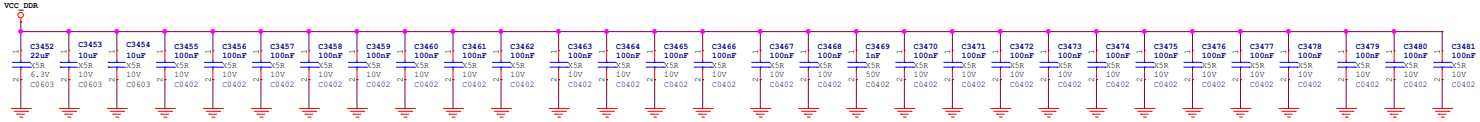




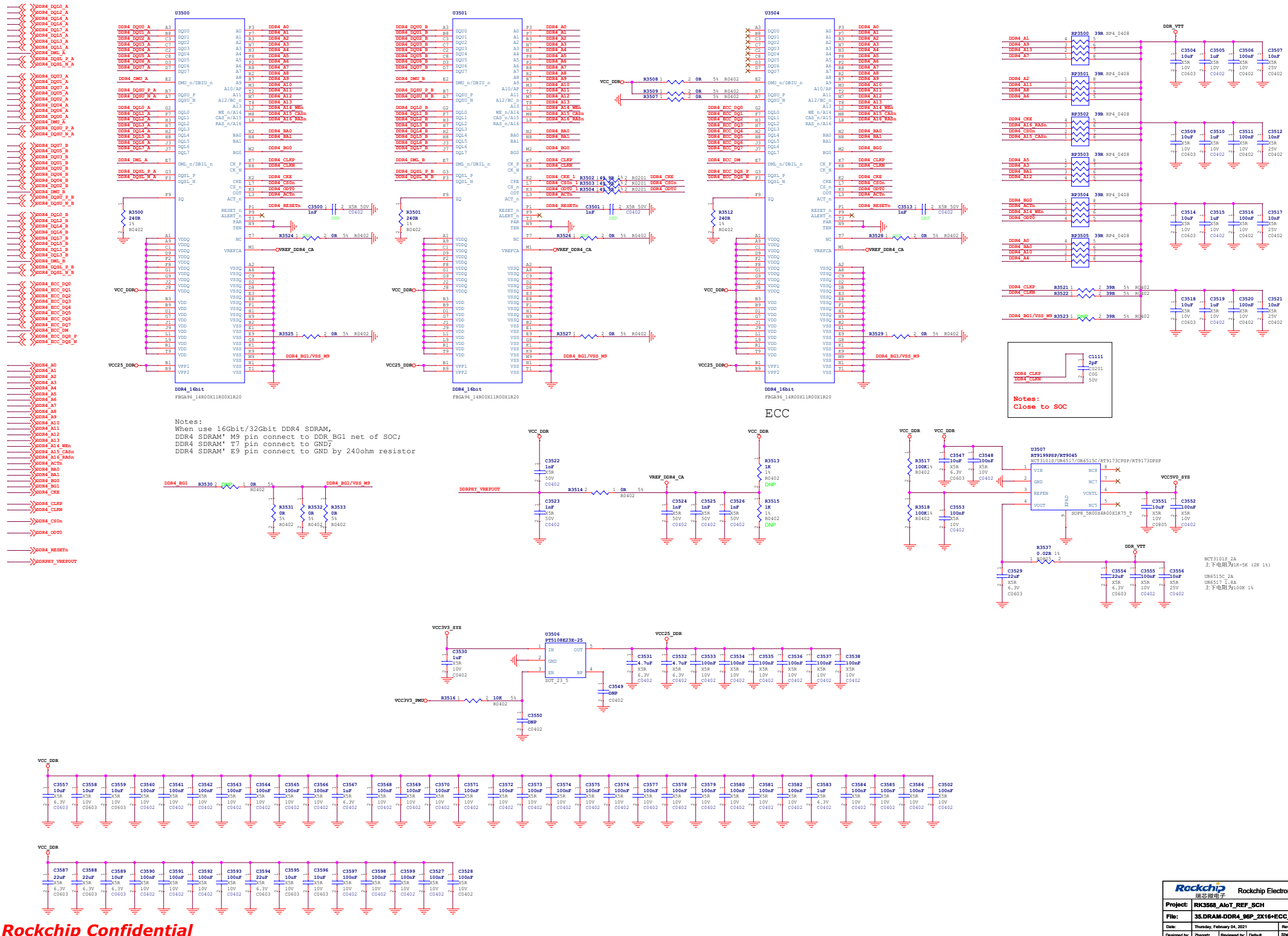


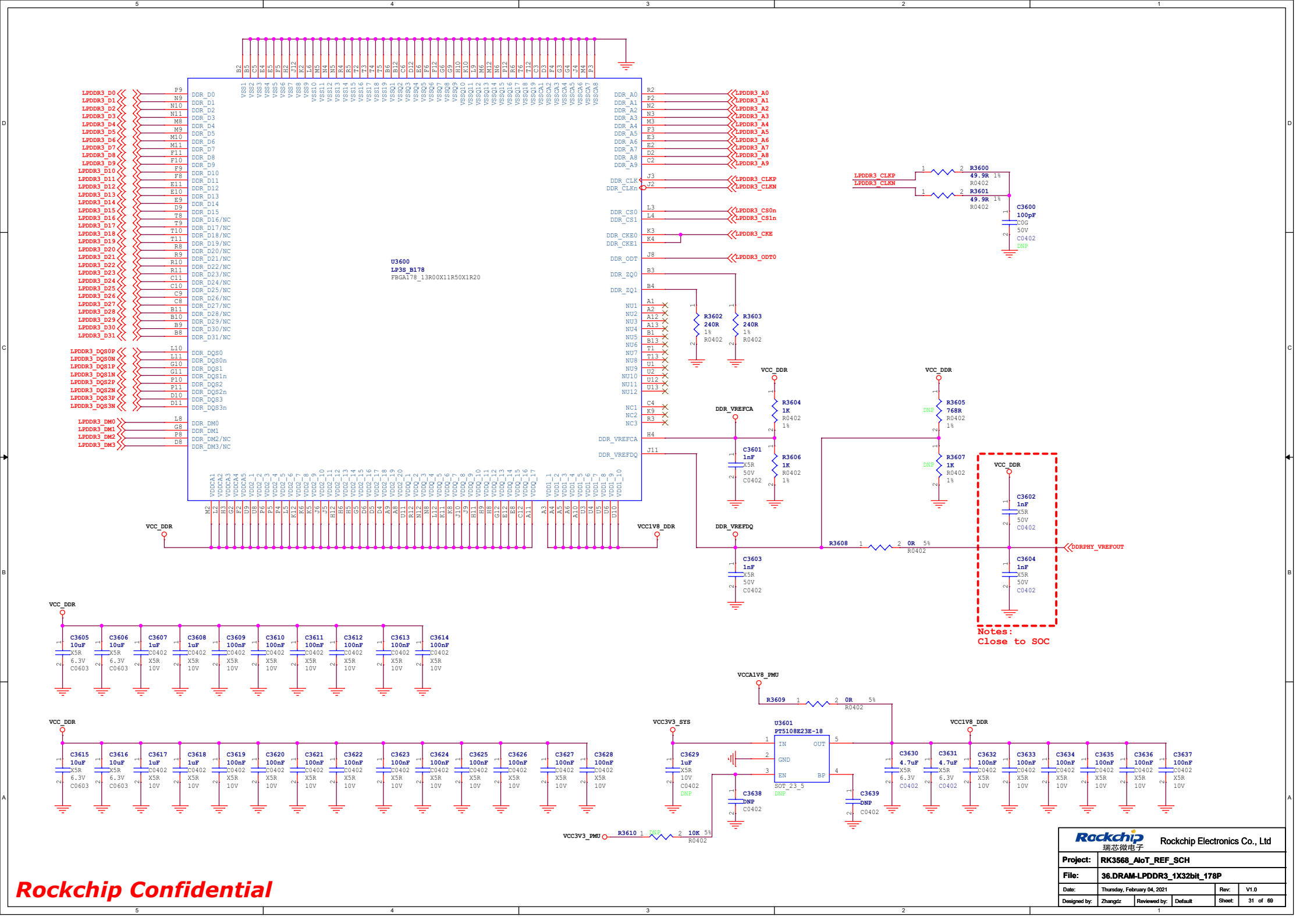






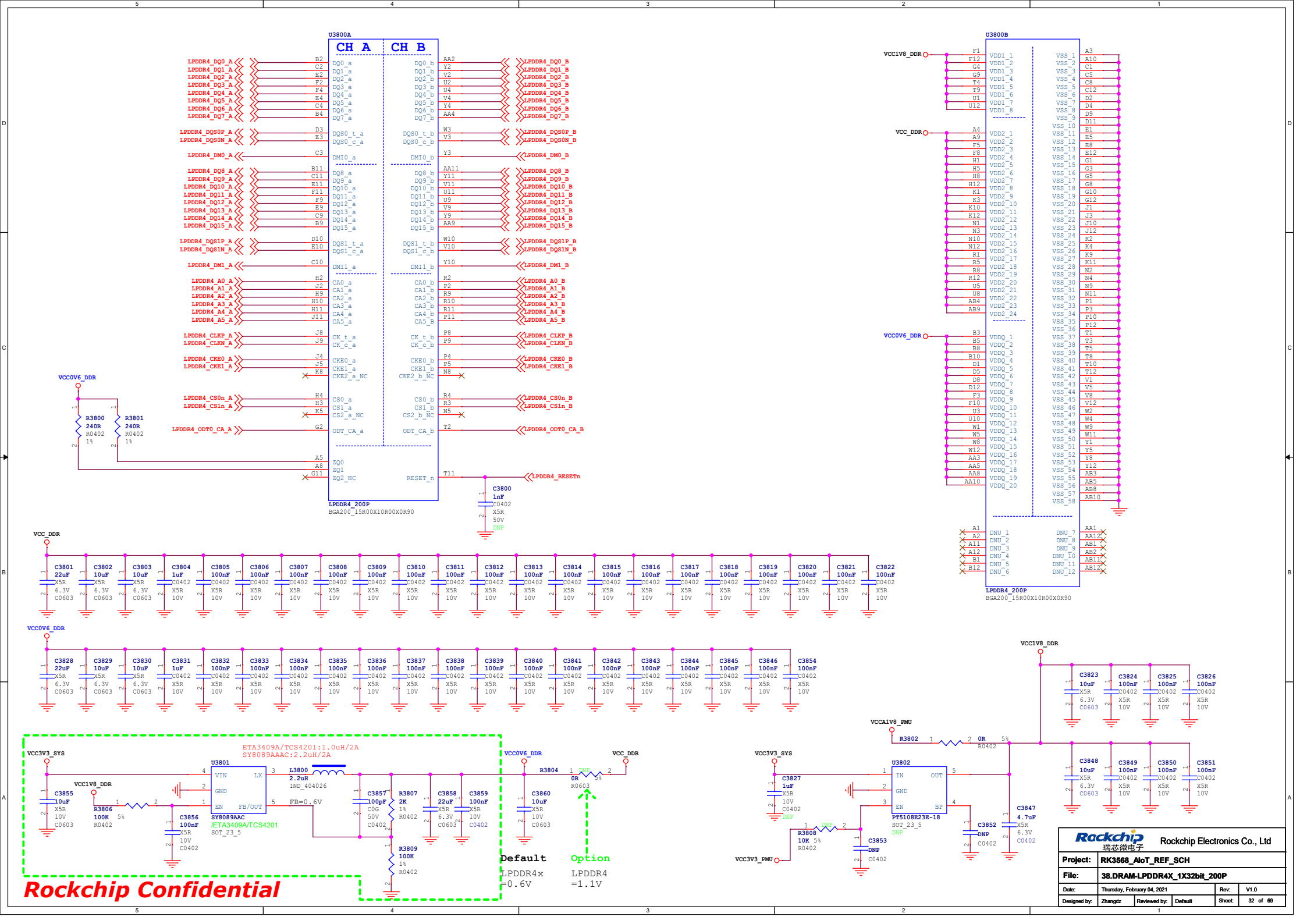
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	34.DRAM-DDR4_4x16Bit_96P		
Date:	Thursday, February 04, 2021	Rev:	V1.0
Designed by: Zhangtz	Reviewed by: Default	Sheet:	29 of 69


U3500
U3501
U3504
DDR4_16bit
FBGA96_14R00X11R00X1R20
ECC
Notes:
When use 16Gbit/32Gbit DDR4 SDRAM,
DDR4 SDRAM' M9 pin connect to DDR_BG1 net of SOC;
DDR4 SDRAM' T7 pin connect to GND;
DDR4 SDRAM' E9 pin connect to GND by 240ohm resistor
Notes:
Close to SOC
U3507
RT9199PSP/RT9045
NCT3101S/UR6517/UR6515C/RT9173CPSP/RT9173DPSP
SOP8_5R00X4R00X1R75_T
U3506
PT5108E23E-25
SOT_23_5
DDR_VTT
VCC_DDR
VCC25_DDR
VCC3V3_SYS
VCC5V0_SYS
VREF_DDR4_CA
DDR4_BG1/VSS_M9
Rockchip Confidential
Rockchip Electronics Co., Ltd
瑞芯微电子
Project: RK3568_AIoT_REF_SCH
File: 35.DRAM-DDR4_96P_2X16+ECC_1X16
Date: Thursday, February 04, 2021
Rev: V1.0
Designed by: Zhangtz
Reviewed by: Default
Sheet: 30 of 69

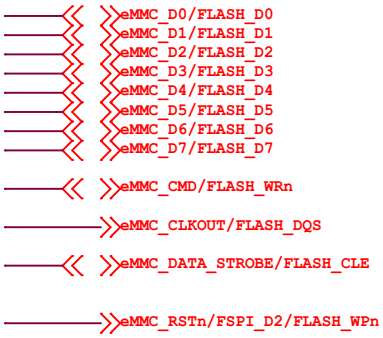


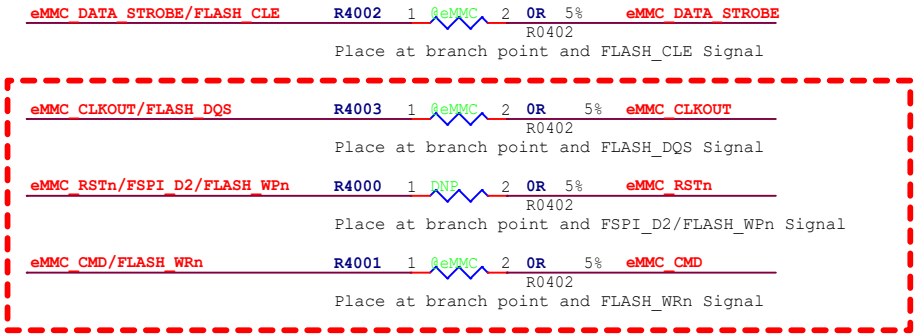
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	36.DRAM-LPDDR3_1X32bit_178P				
Date:	Thursday, February 04, 2021		Rev:	V1.0	
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	31 of 69


U3800A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U3800B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC_DDR
VCC0V6_DDR
VCC1V8_DDR
R3800 240R R0402 1%
R3801 240R R0402 1%
C3800 1nF C0402 X5R 50V DNP
C3801 22uF X5R 6.3V C0603
C3802 10uF X5R 6.3V C0603
C3803 10uF X5R 6.3V C0603
C3804 1uF C0402 X5R 10V
C3805 100nF C0402 X5R 10V
C3806 100nF C0402 X5R 10V
C3807 100nF C0402 X5R 10V
C3808 100nF C0402 X5R 10V
C3809 100nF C0402 X5R 10V
C3810 100nF C0402 X5R 10V
C3811 100nF C0402 X5R 10V
C3812 100nF C0402 X5R 10V
C3813 100nF C0402 X5R 10V
C3814 100nF C0402 X5R 10V
C3815 100nF C0402 X5R 10V
C3816 100nF C0402 X5R 10V
C3817 100nF C0402 X5R 10V
C3818 100nF C0402 X5R 10V
C3819 100nF C0402 X5R 10V
C3820 100nF C0402 X5R 10V
C3821 100nF C0402 X5R 10V
C3822 100nF C0402 X5R 10V
C3828 22uF X5R 6.3V C0603
C3829 10uF X5R 6.3V C0603
C3830 10uF X5R 6.3V C0603
C3831 1uF C0402 X5R 10V
C3832 100nF C0402 X5R 10V
C3833 100nF C0402 X5R 10V
C3834 100nF C0402 X5R 10V
C3835 100nF C0402 X5R 10V
C3836 100nF C0402 X5R 10V
C3837 100nF C0402 X5R 10V
C3838 100nF C0402 X5R 10V
C3839 100nF C0402 X5R 10V
C3840 100nF C0402 X5R 10V
C3841 100nF C0402 X5R 10V
C3842 100nF C0402 X5R 10V
C3843 100nF C0402 X5R 10V
C3844 100nF C0402 X5R 10V
C3845 100nF C0402 X5R 10V
C3846 100nF C0402 X5R 10V
C3854 100nF C0402 X5R 10V
C3823 10uF X5R 6.3V C0603
C3824 100nF C0402 X5R 10V
C3825 100nF C0402 X5R 10V
C3826 100nF C0402 X5R 10V
C3848 10uF X5R 6.3V C0603
C3849 100nF C0402 X5R 10V
C3850 100nF C0402 X5R 10V
C3851 100nF C0402 X5R 10V
VCC3V3_SYS
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
U3801
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
L3800 2.2uH IND_404026
FB=0.6V
C3855 10uF X5R 10V C0603
R3806 100K 5% R0402
C3856 100nF X5R 10V C0402
C3857 100pF C0G 50V C0402
R3807 2K 1% R0402
C3858 22uF X5R 6.3V C0603
C3859 100nF X5R 10V C0402
R3809 100K 1% R0402
R3804 0R R0603
C3860 10uF X5R 10V C0603
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
VCCA1V8_PMU
R3802 0R R0402
VCC3V3_PMU
U3802
PT5108E23E-18
SOT_23_5
C3827 1uF X5R 10V C0402
R3808 10K 5% R0402
C3853 DNP C0402
C3852 DNP C0402
C3847 4.7uF X5R 6.3V C0402
Rockchip Confidential
Rockchip 瑞芯微电子
Rockchip Electronics Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 38.DRAM-LPDDR4X_1X32bit_200P
Date: Thursday, February 04, 2021
Rev: V1.0
Designed by: Zhangdz
Reviewed by: Default
Sheet: 32 of 69

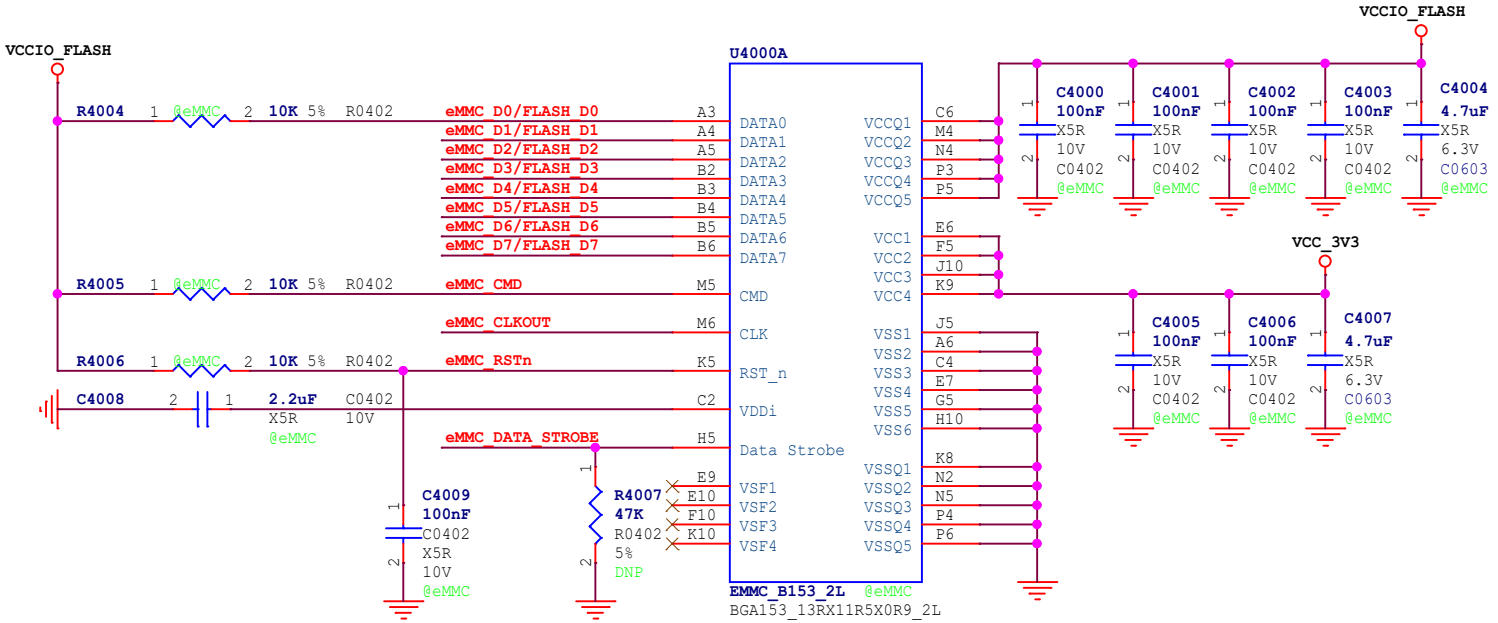
eMMC Flash

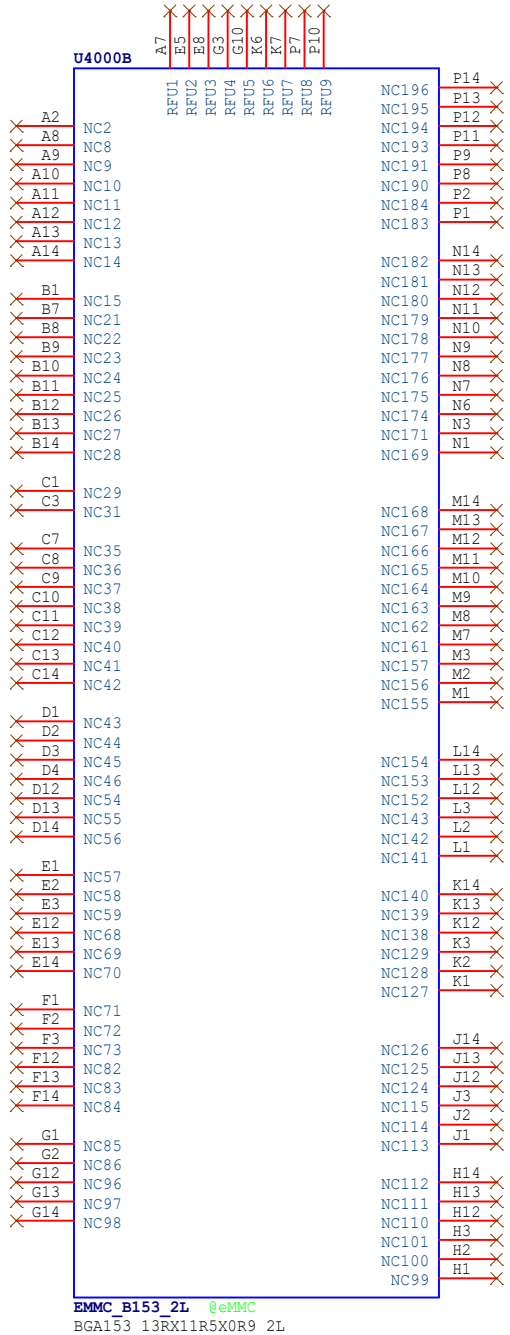




Note:

No need to double layout with Nand Flash, 0R resistor can be omitted



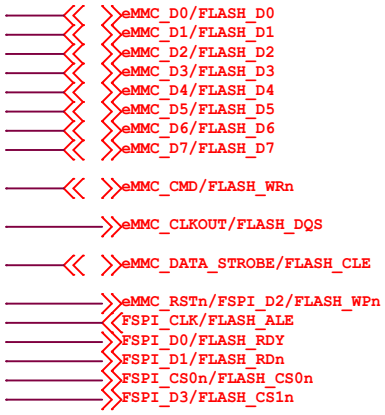


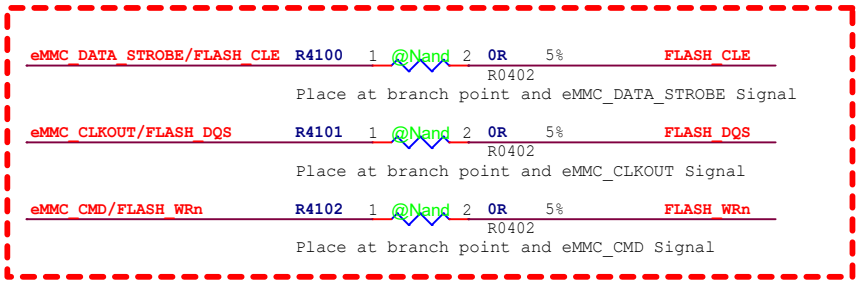
Note:

If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	40.Flash-eMMC Flash				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	33 of 69

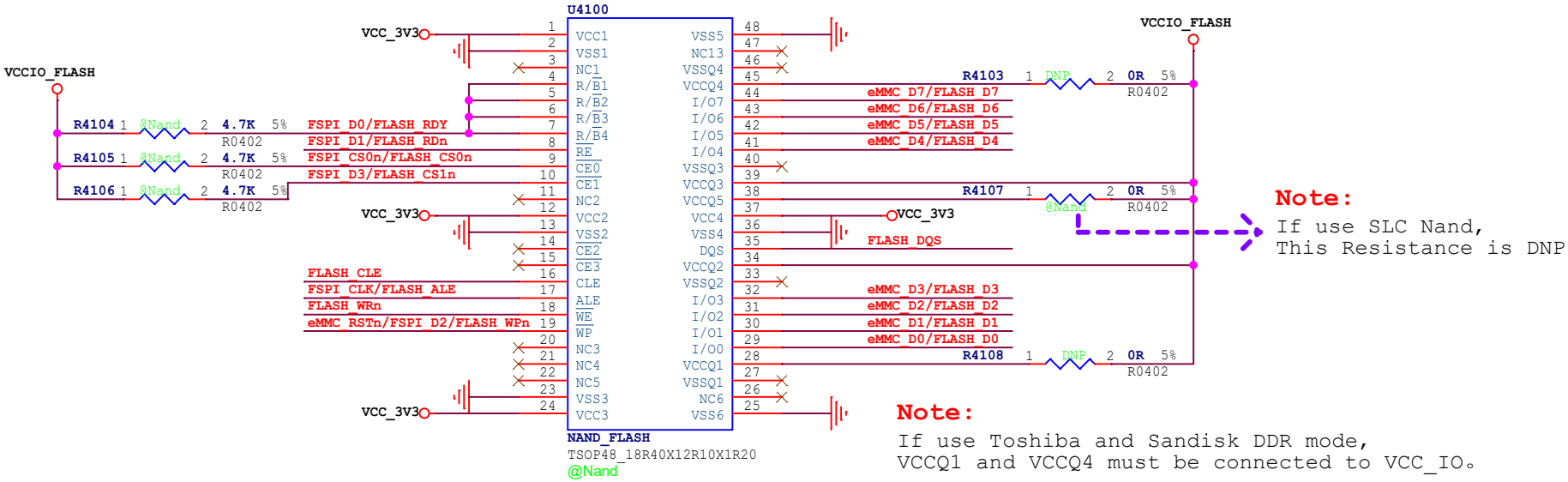
Nand Flash





Note:

No need to double layout with eMMC, 0R resistor can be omitted

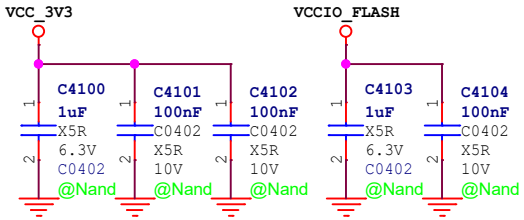


Note:

If use SLC Nand,
This Resistance is DNP

Note:

If use Toshiba and Sandisk DDR mode,
VCCQ1 and VCCQ4 must be connected to VCC_IO。

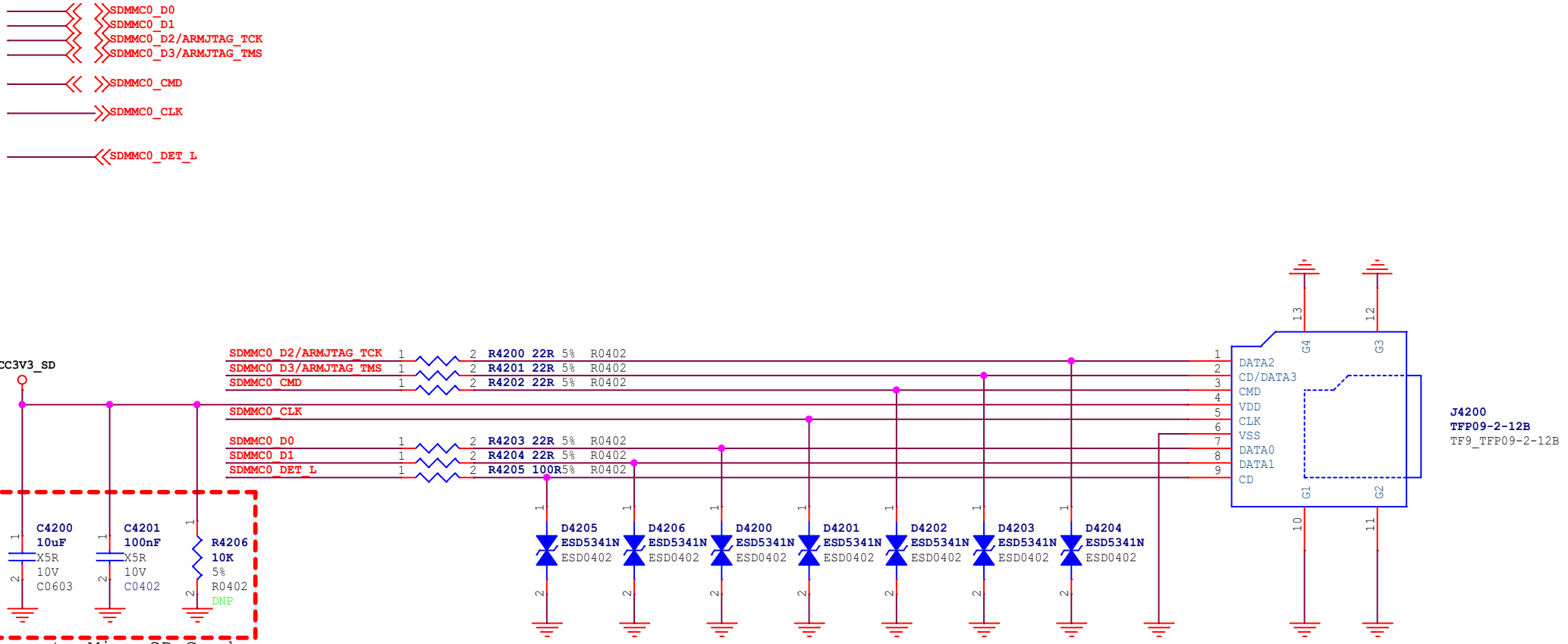


Note:

If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	41.Flash-Nand Flash(Option)				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	34 of 69

MicroSD Card



MicroSD Card

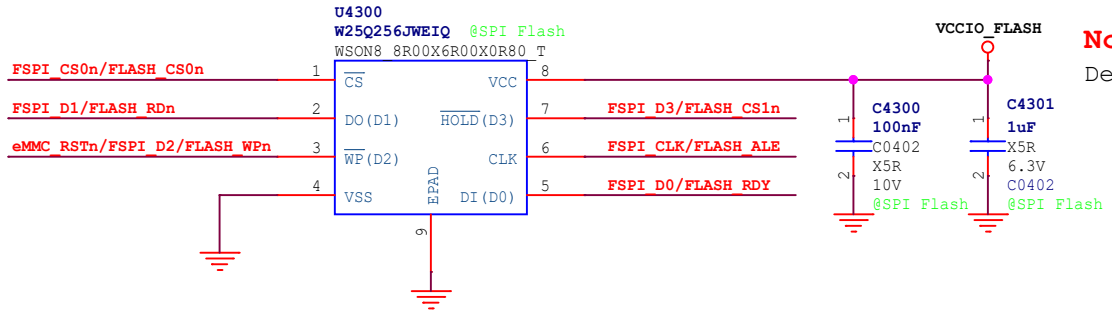
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	42.Flash-MicroSD Card				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	35 of 69

SPI Flash

FSPI_CLK/FLASH_ALE

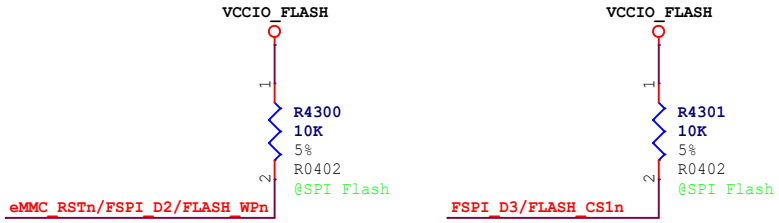
FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_D3/FLASH_CS1n

FSPI_CS0n/FLASH_CS0n



Note:
Default: 1.8V

Support:
1bit SPI NOR or SPI NAND
4bit SPI NOR or SPI NAND

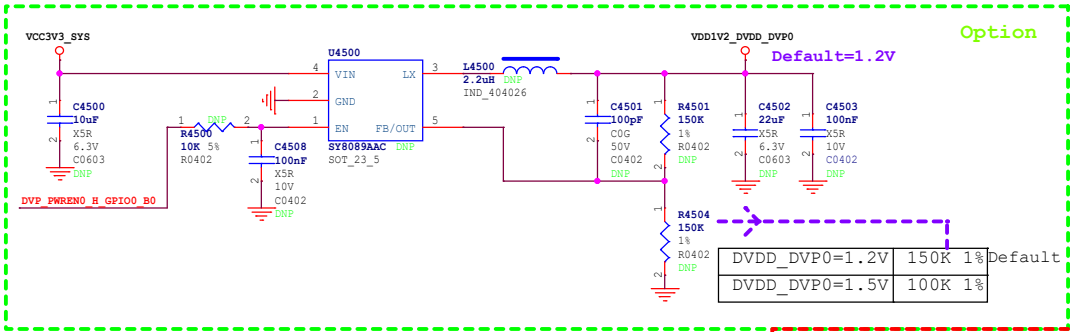


Note:
If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

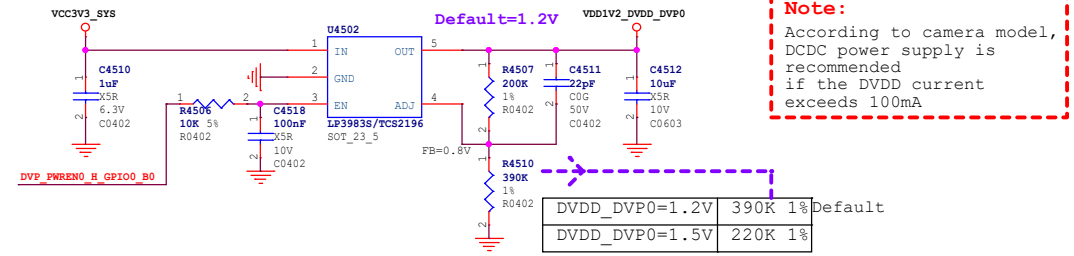
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	43.Flash-SPI FLASH(Option)				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	36 of 69

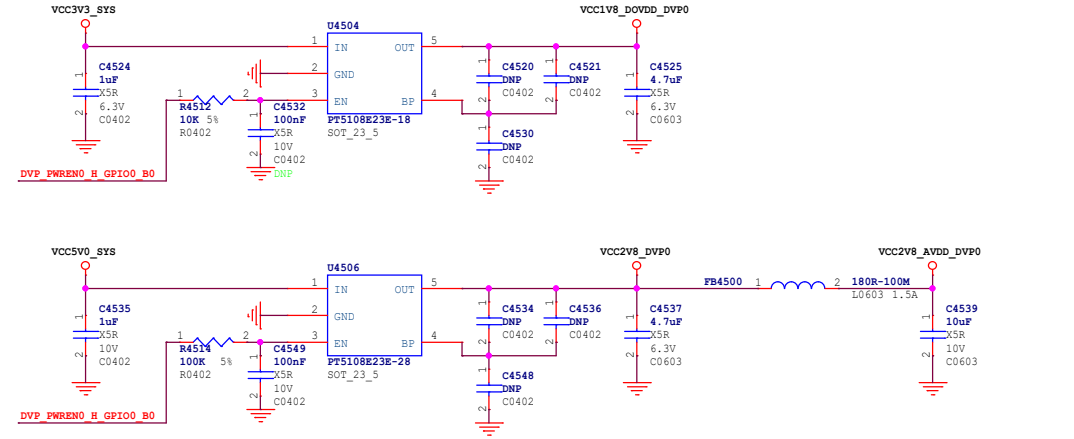
DVP_PWREN0_H_GPIO0_B0
HDMIRX_PWREN_H_GPIO0_D6

Camera0 Power supply



Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA

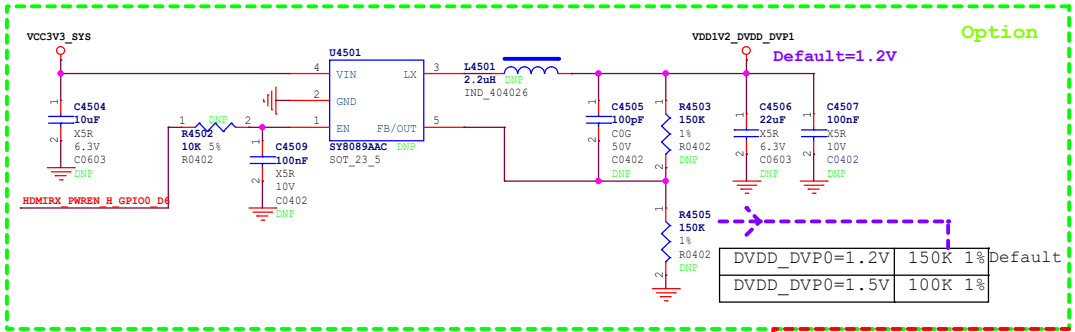




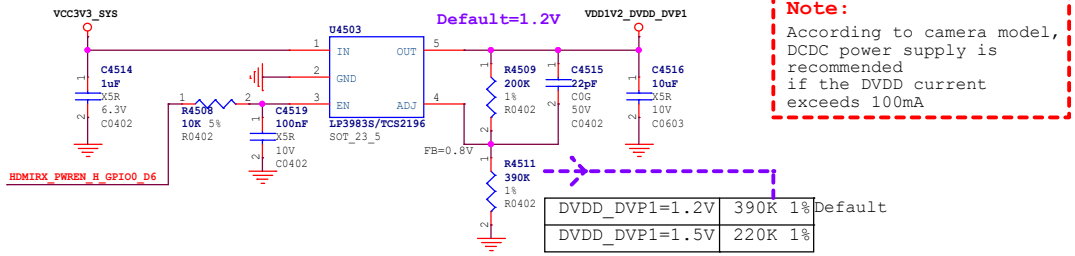
Note:
Adjust the power on sequence according to the camera model
eg:GC8034
Power on Sequence
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

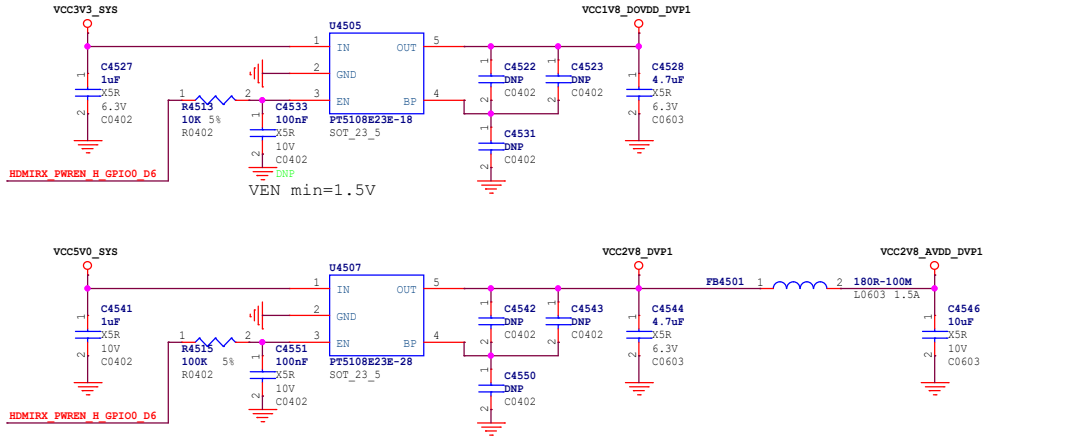
Camera1 Power supply

Note:
When the binocular camera is used,
If separate control is required,
separate power supply is recommended



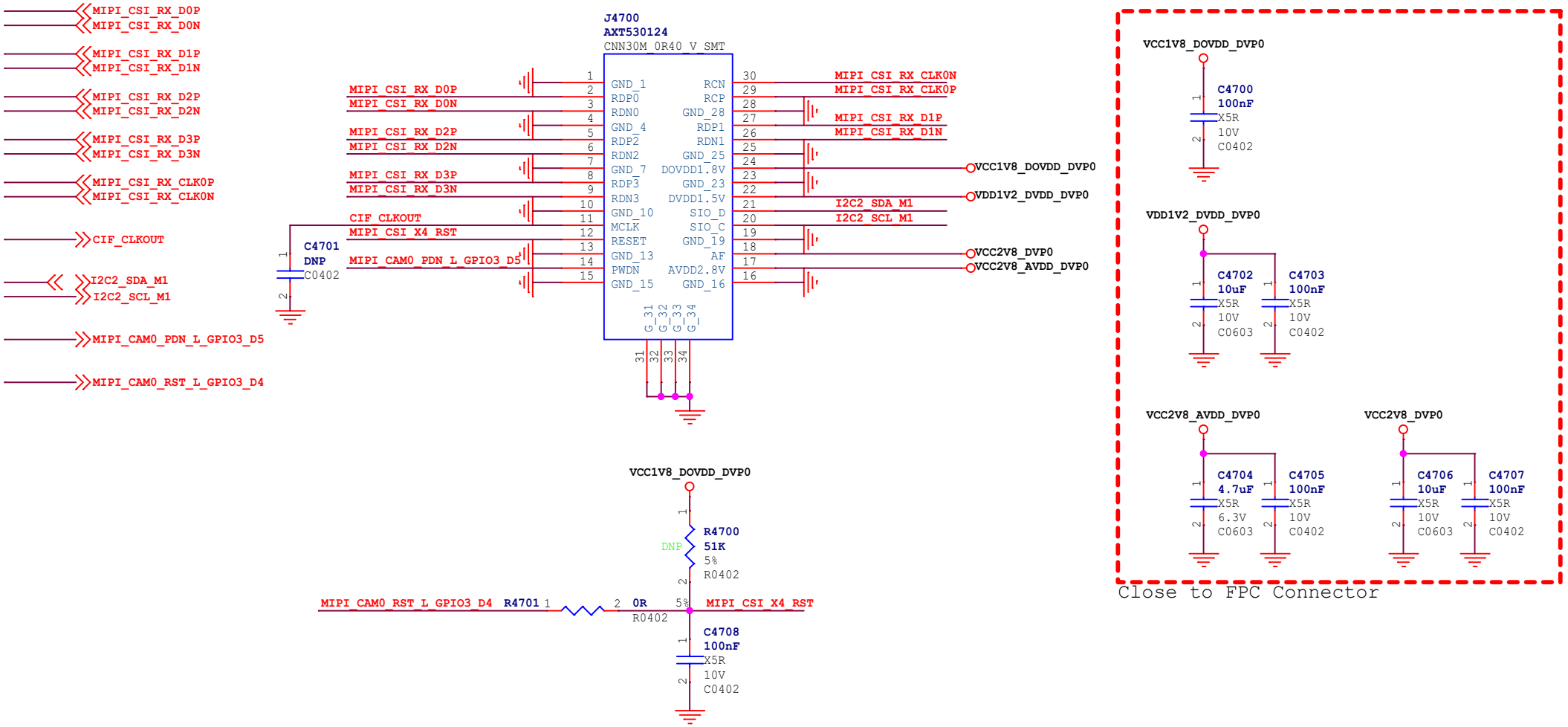
Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA





Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	45.VI-Camera_Power				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	37 of 69

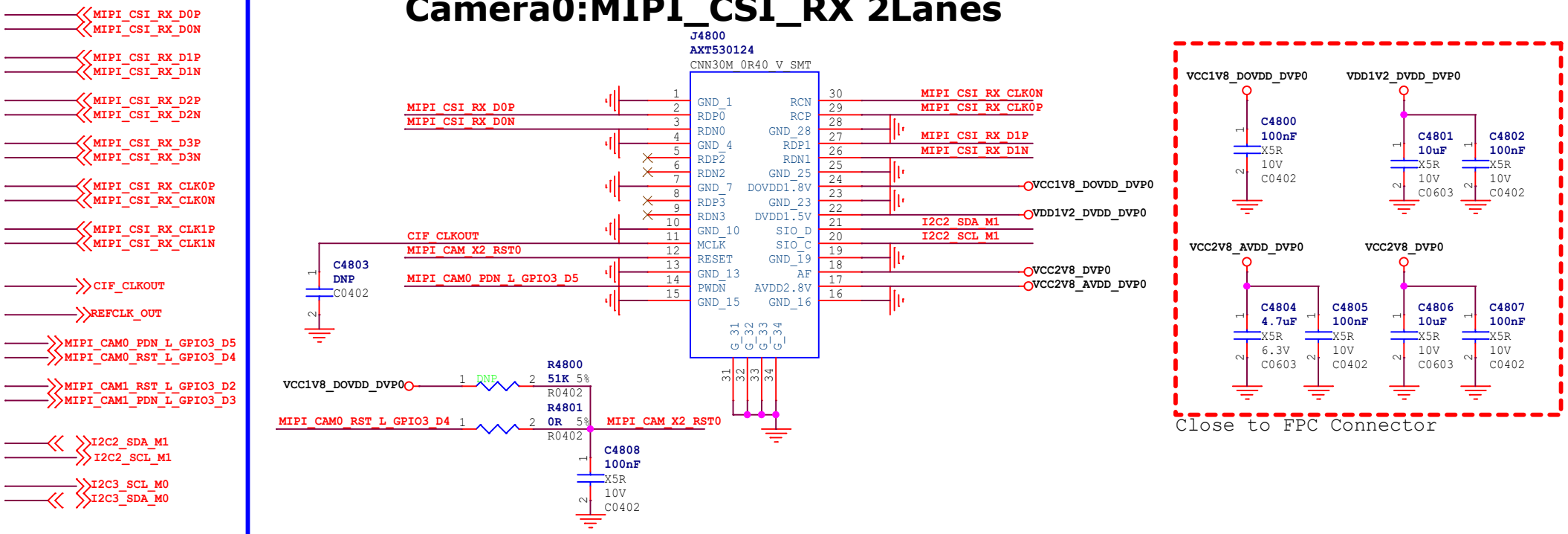
Camera0:MIPI_CSI_RX 4Lanes



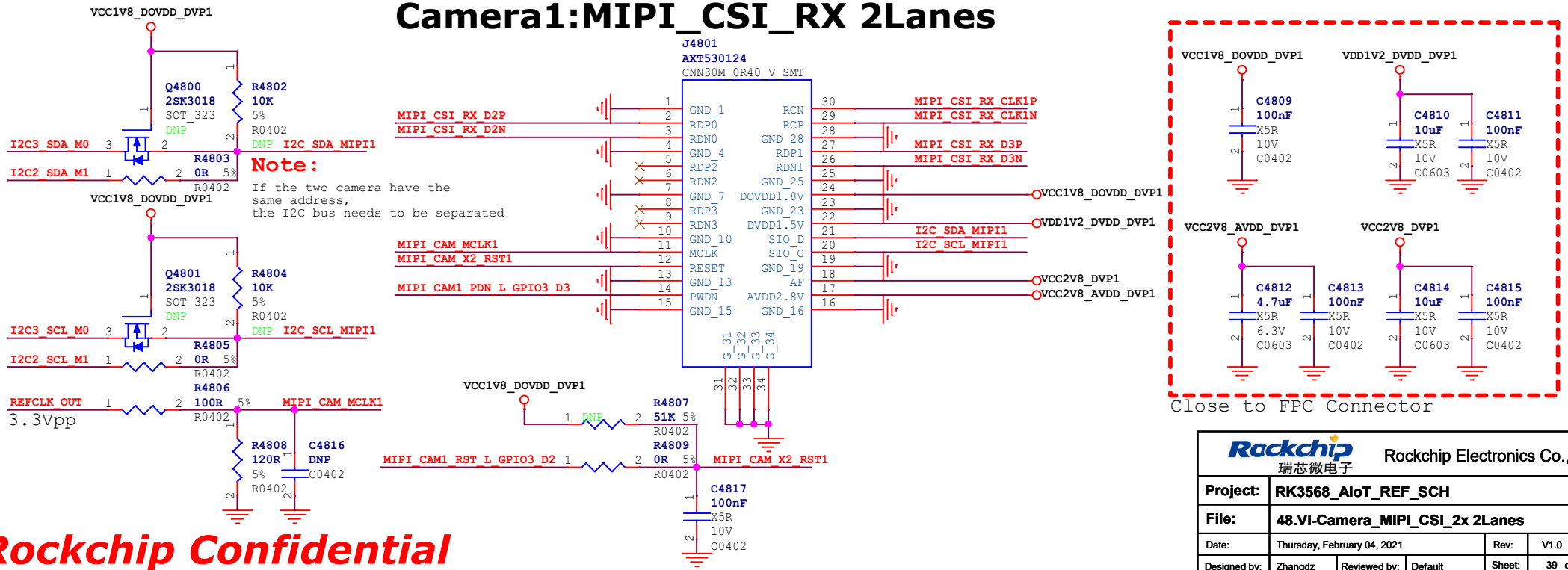
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	47.VI-Camera_MIPI_CSI_1x 4Lanes				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	38 of 69

Camera0:MIPI_CSI_RX 2Lanes



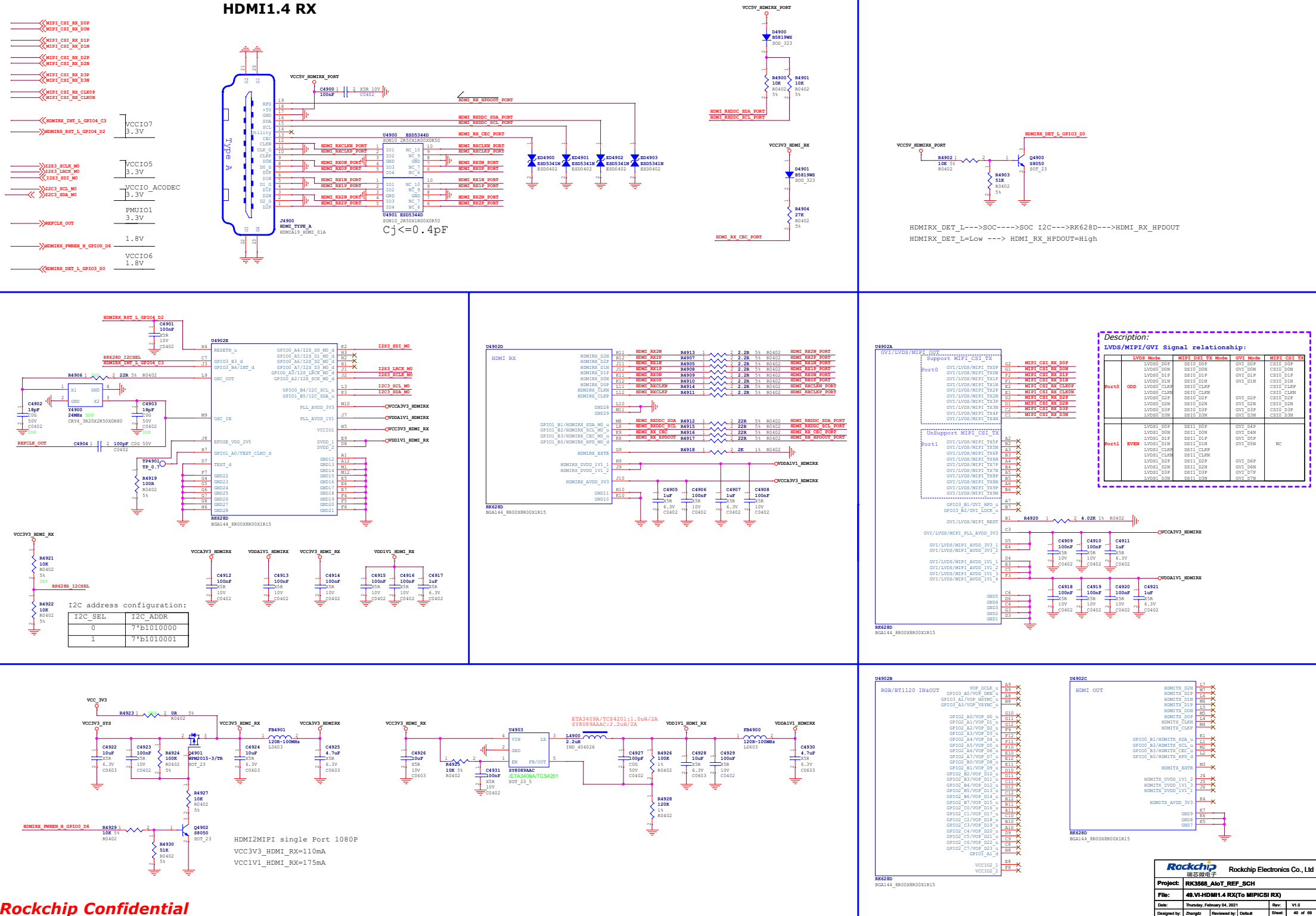
Camera1:MIPI_CSI_RX 2Lanes



Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	48.VI-Camera_MIPI_CSI_2x 2Lanes				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	39 of 69

HDMI1.4 RX



HDMIRX_DET_L--->SOC---->SOC I2C--->RK628D--->HDMI_RX_HPDOUT
HDMIRX_DET_L=Low ---> HDMI_RX_HPDOUT=High

I2C address configuration:

I2C_SEL	I2C_ADDR
0	7'b1010000
1	7'b1010001

Description:

LVDS/MIPI/GVI Signal relationship:

		LVDS Mode	MIPI_DSI_TX Mode	GVI Mode	MIPI_CSI_TX
Port0	ODD	LVDS0_D0P	DSI0_D0P	GVI_D0P	CSI0_D0P
		LVDS0_D0N	DSI0_D0N	GVI_D0N	CSI0_D0N
		LVDS0_D1P	DSI0_D1P	GVI_D1P	CSI0_D1P
		LVDS0_D1N	DSI0_D1N	GVI_D1N	CSI0_D1N
		LVDS0_CLKP	DSI0_CLKP		CSI0_CLKP
		LVDS0_CLKN	DSI0_CLKN		CSI0_CLKN
		LVDS0_D2P	DSI0_D2P	GVI_D2P	CSI0_D2P
		LVDS0_D2N	DSI0_D2N	GVI_D2N	CSI0_D2N
		LVDS0_D3P	DSI0_D3P	GVI_D3P	CSI0_D3P
		LVDS0_D3N	DSI0_D3N	GVI_D3N	CSI0_D3N
Port1	EVEN	LVDS1_D0P	DSI1_D0P	GVI_D4P	
		LVDS1_D0N	DSI1_D0N	GVI_D4N	
		LVDS1_D1P	DSI1_D1P	GVI_D5P	
		LVDS1_D1N	DSI1_D1N	GVI_D5N	NC
		LVDS1_CLKP	DSI1_CLKP		
		LVDS1_CLKN	DSI1_CLKN		
		LVDS1_D2P	DSI1_D2P	GVI_D6P	
		LVDS1_D2N	DSI1_D2N	GVI_D6N	
		LVDS1_D3P	DSI1_D3P	GVI_D7P	
		LVDS1_D3N	DSI1_D3N	GVI_D7N	

HDMI2MIPI single Port 1080P
VCC3V3_HDMI_RX=110mA
VCC1V1_HDMI_RX=175mA

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	49.V1-HDMI1.4 RX(To MIPICSI RX)
Date:	Thursday, February 04, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	40 of 69

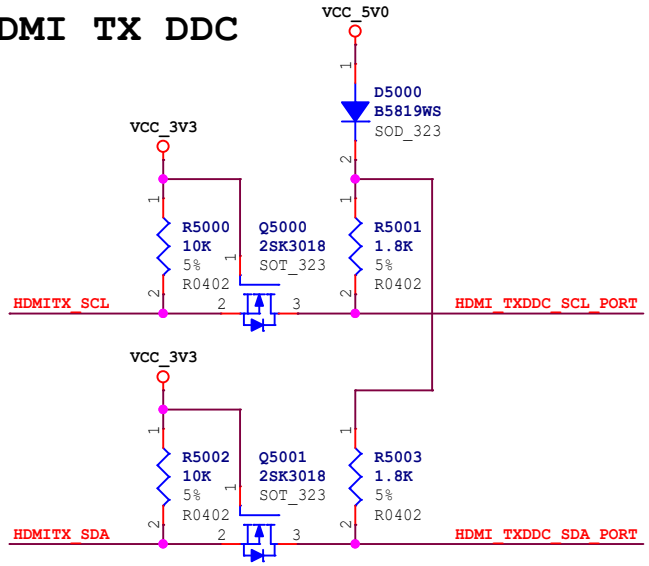
HDMI2.0 TX

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT

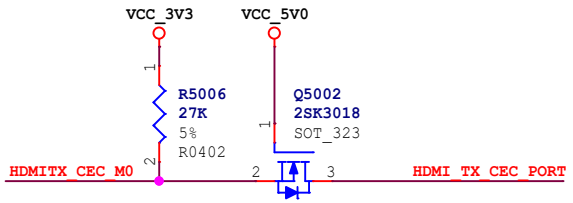
HDMITX_SCL
HDMITX_SDA

HDMITX_CEC_M0
HDMI_TX_HPDIN

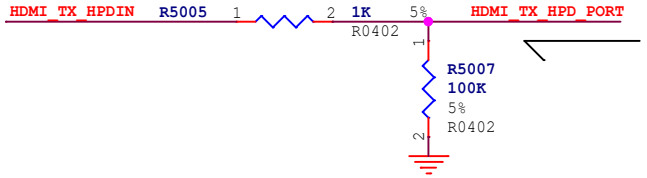
HDMI TX DDC

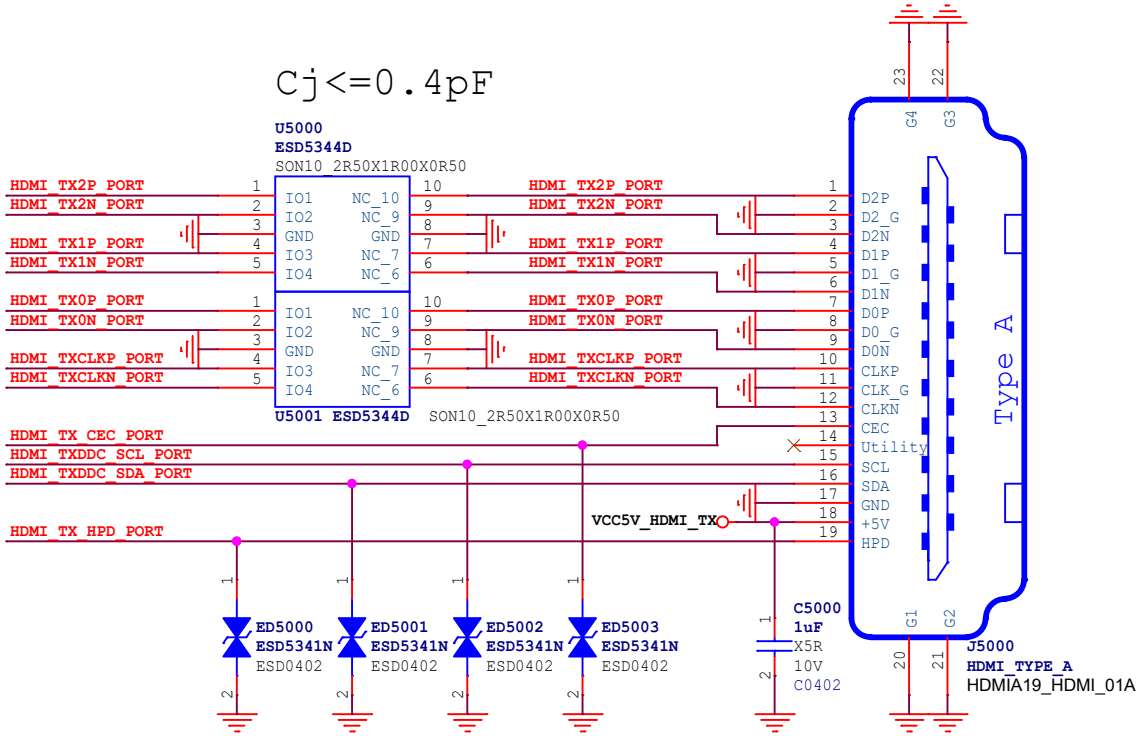


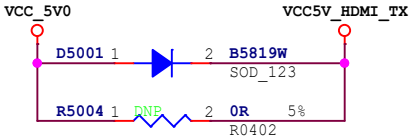
HDMI TX CEC



HDMI TX HPD



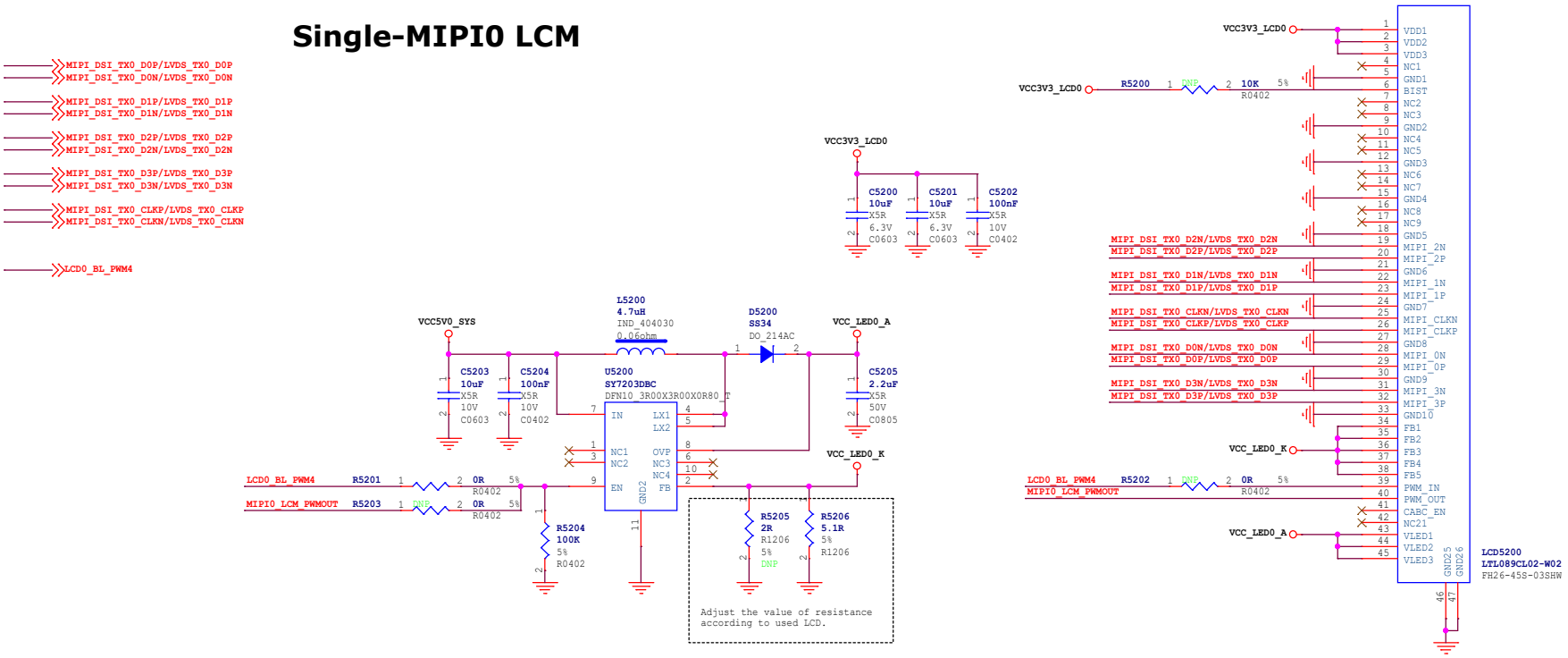




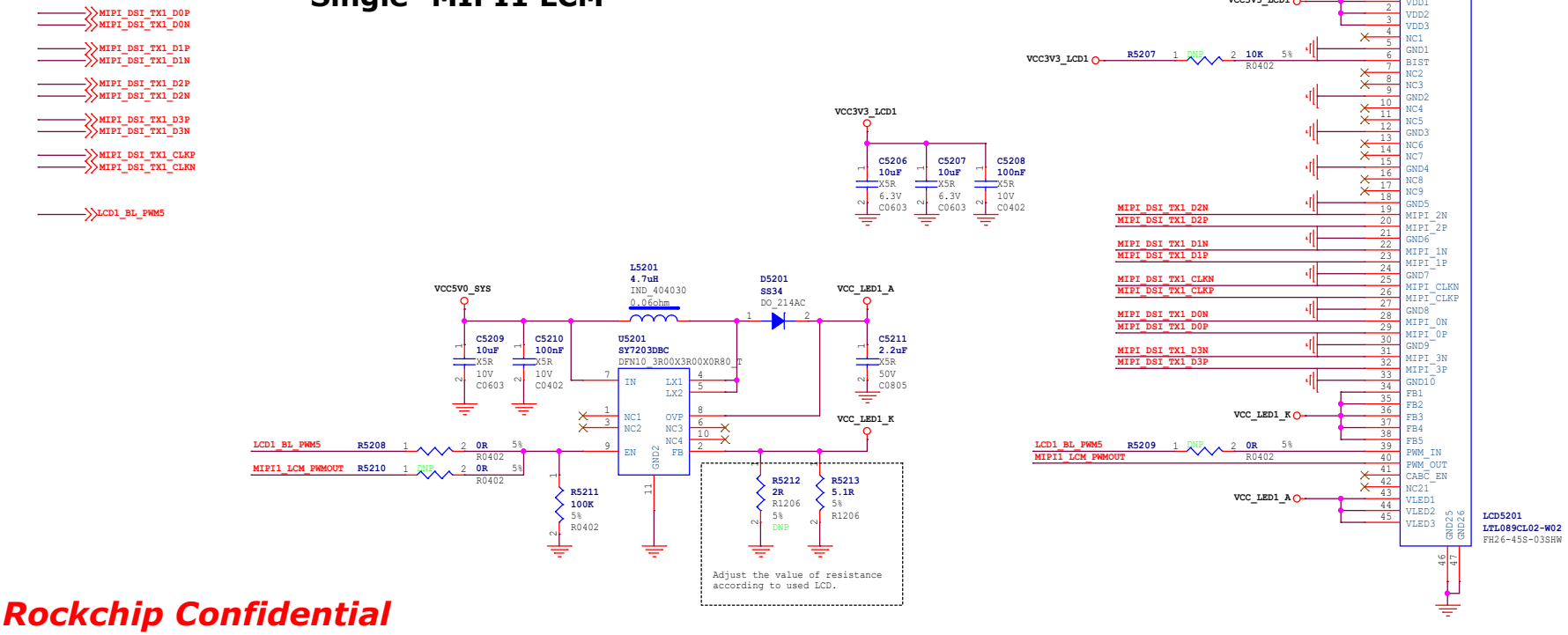
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	50.VO-HDMI2.0 TX				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	41 of 69

Single-MIPI0 LCM



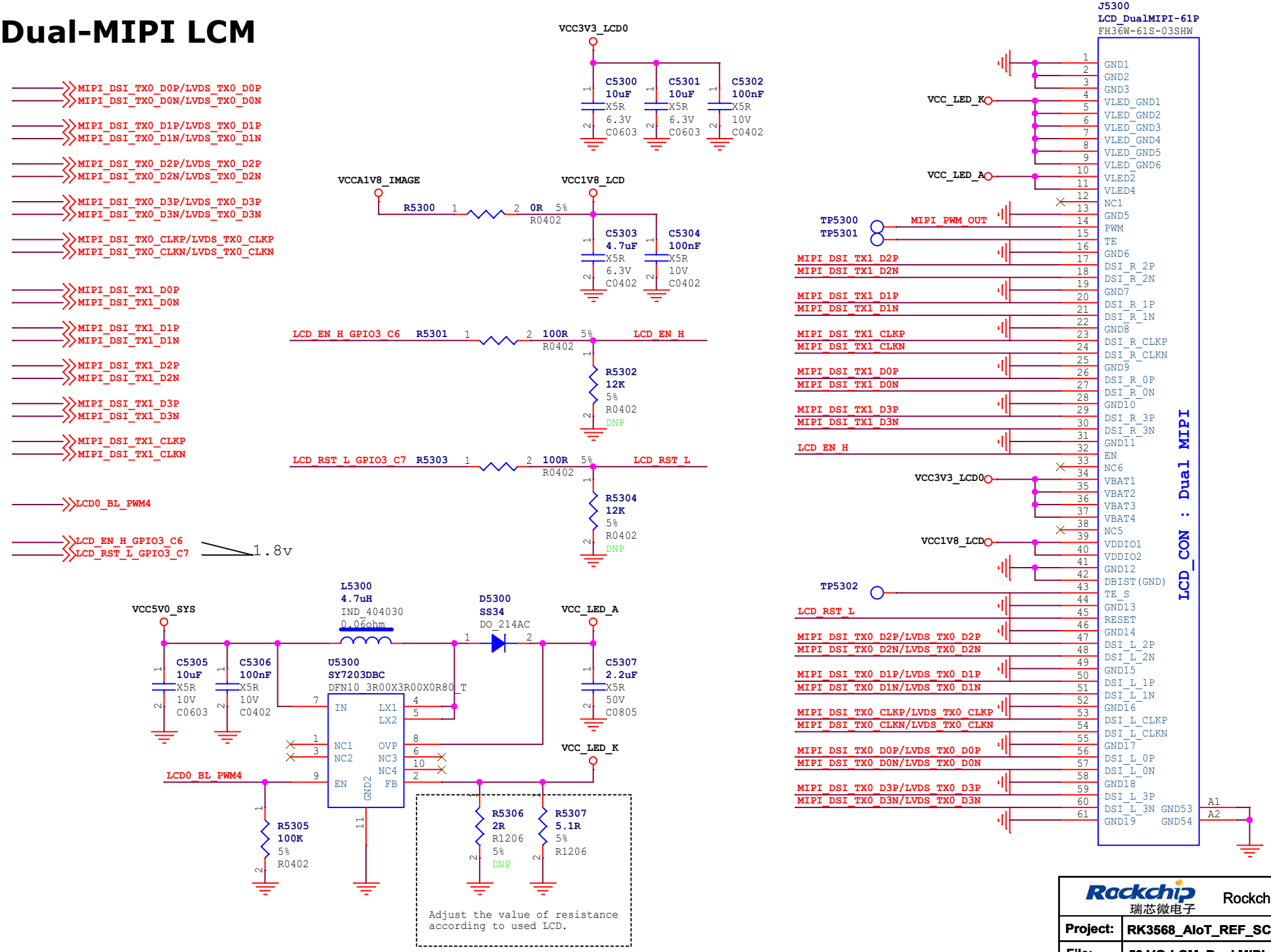
Single- MIPI1 LCM



Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	52.VO-LCM_MIPI_DSI_TX0/TX1				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	42 of 69

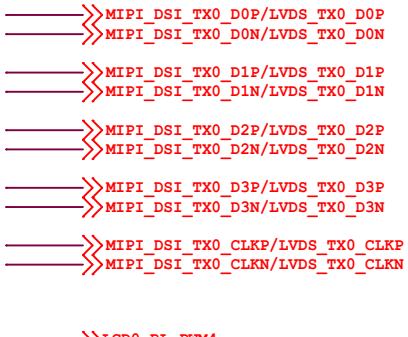
Dual-MIPI LCM

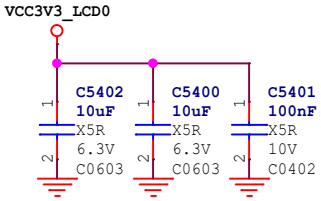


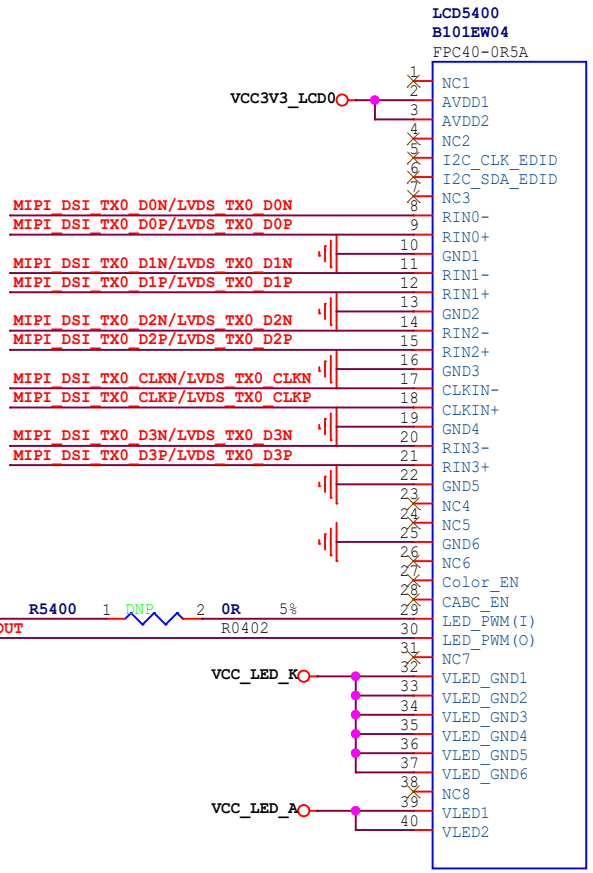
Rockchip Electronics Co., Ltd

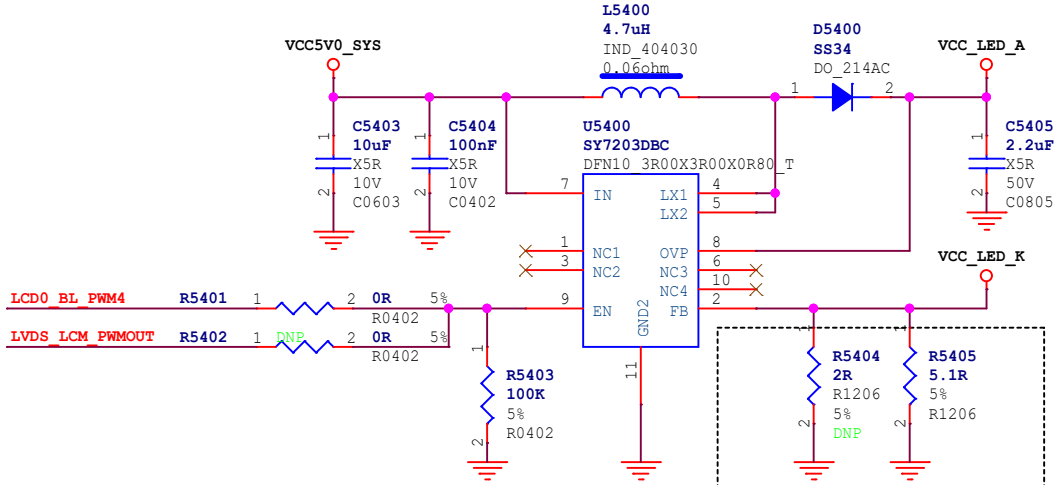
Project:	RK3568_AIoT_REF_SCH				
File:	53.VO-LCM_Dual MIPI_DSI TX				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	43 of 69

Single-LVDS LCM





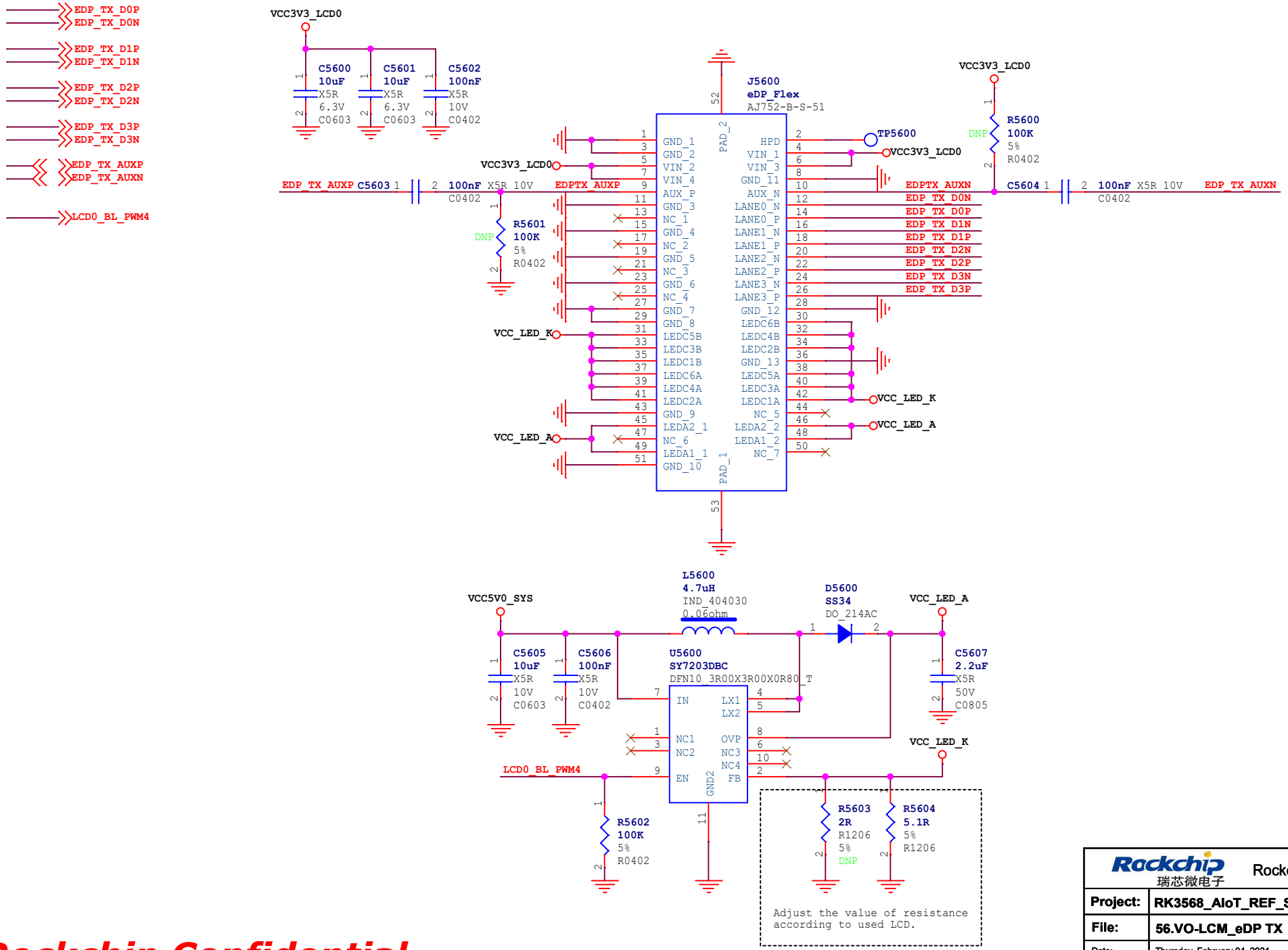




Rockchip Confidential

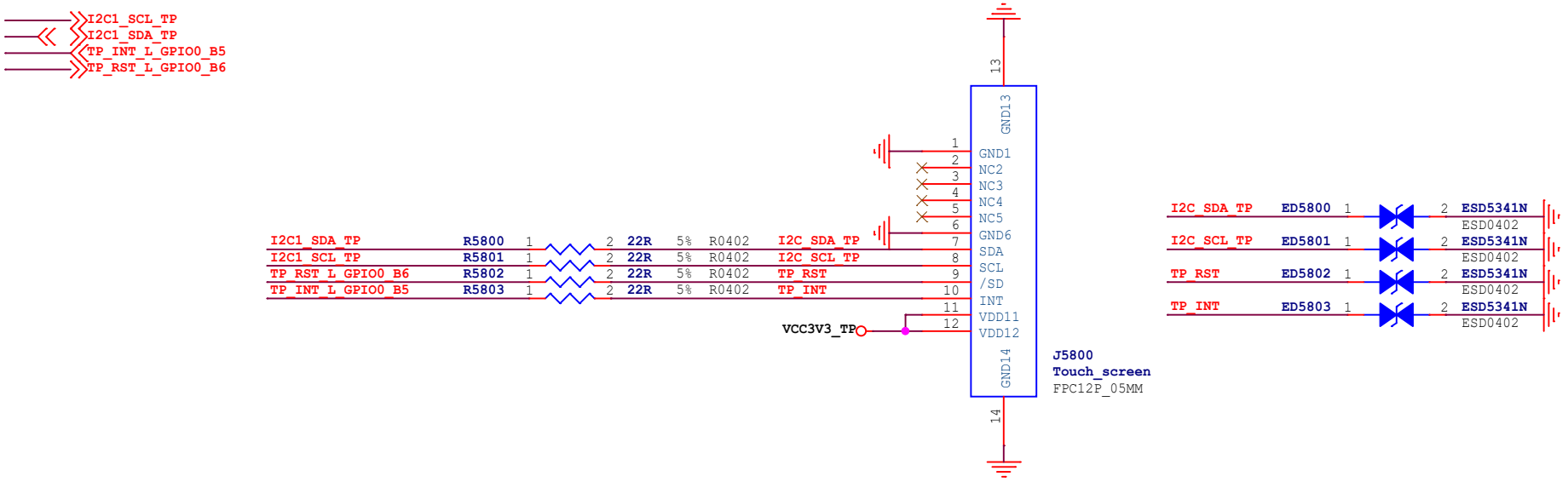
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	54.VO-LCM_LVDS TX				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	44 of 69

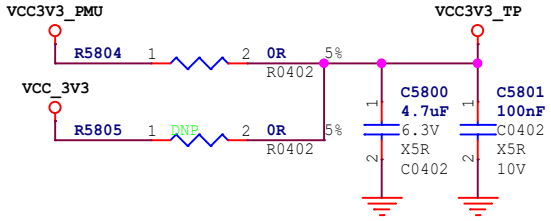
Single-eDP LCM



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	56.VO-LCM_eDP TX				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	45 of 69

Touch Panel connector





Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	58.TP Connector_COF				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	46 of 69

VGA OUT

Default:RTD2166

CH7517,IT6516:Can also support

EDP_TX_D0P
EDP_TX_D0N
EDP_TX_D1P
EDP_TX_D1N
EDP_TX_AUXP
EDP_TX_AUXN
VGA_HPDIN_GPIO0_C0
VGA_PWREN_H_GPIO0_D5
I2C5_SCL_M0
I2C5_SDA_M0

PMUIO2
3.3V
1.8V

Power Sequence:
5v-->3.3v-->1.2v

BLM18BB220SN1D

BAT54S

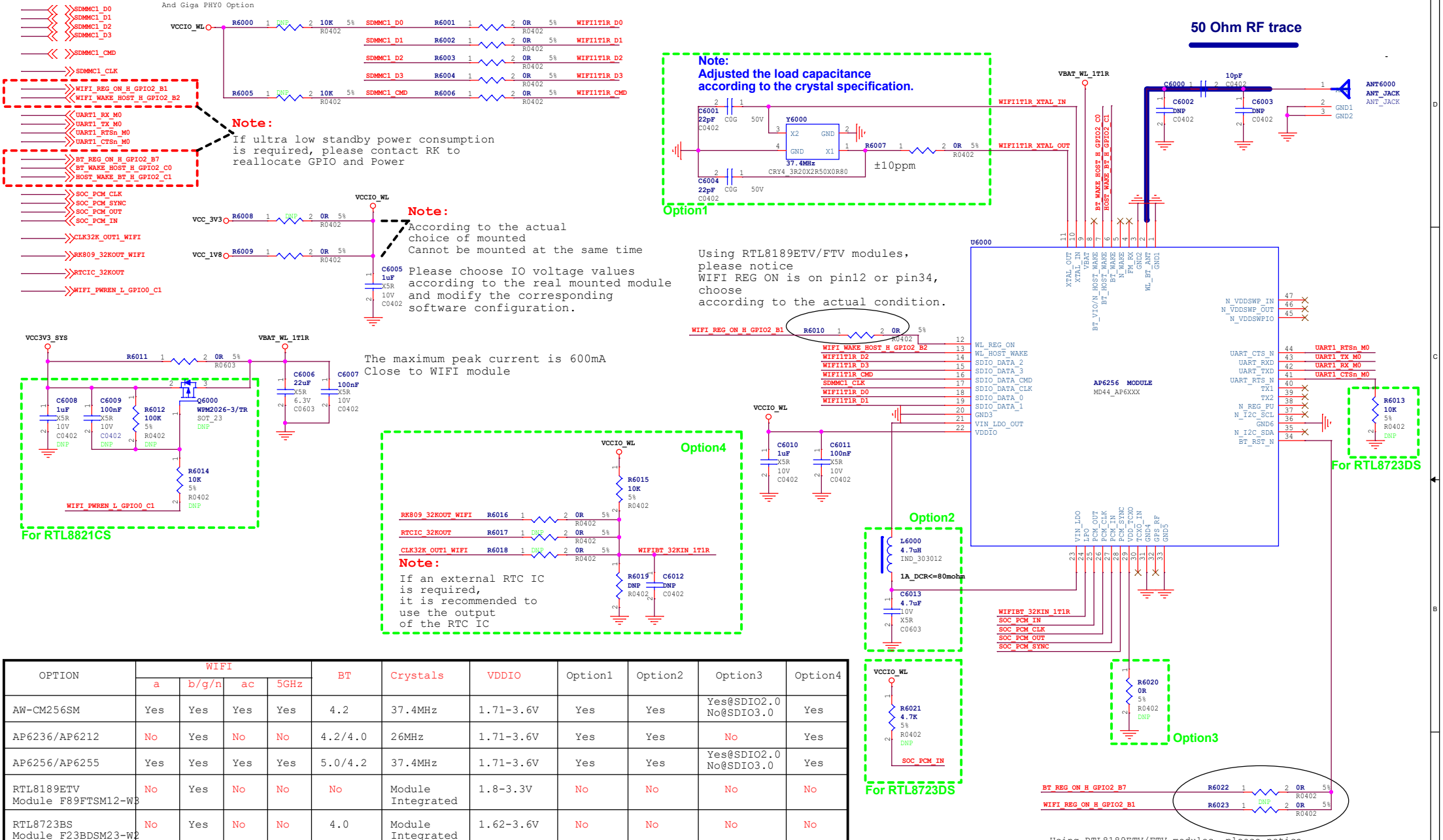
550mW

U5900 RTD2166 QFN32_4R00X4R00X0R90_T

J5900 VGA_DB15 DSUB15B

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	59.VO-VGA Output(eDP To VGA)				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	47 of 69

SDIO WIFI/BT MODULE



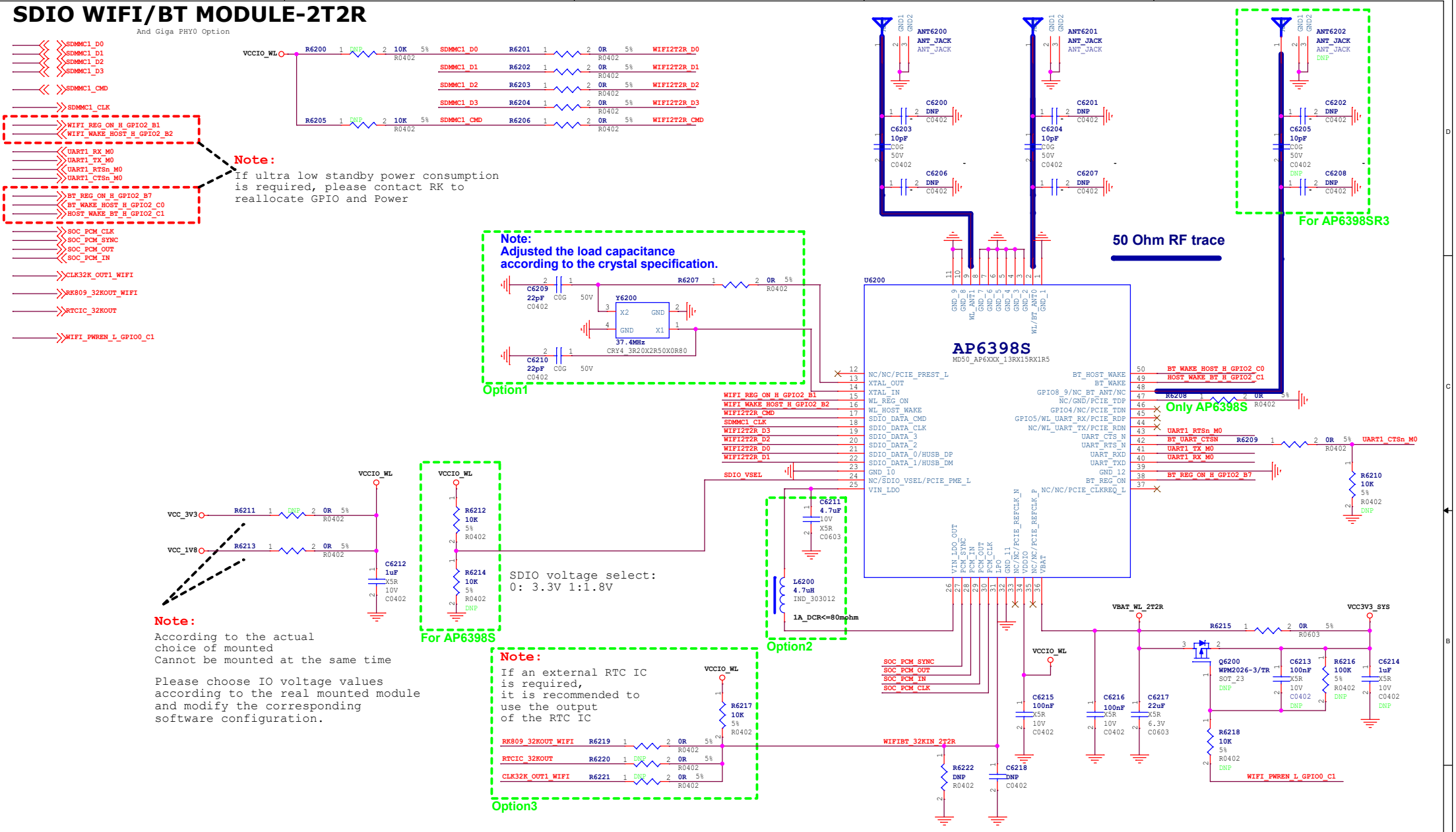
OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	60.WIFI/BT-SDMMC1_1T1R + UART		
Date:	Thursday, February 04, 2021	Rev:	V1.0
Designed by: Zhangdz	Reviewed by: Default	Sheet:	48 of 69

SDIO WIFI/BT MODULE-2T2R

And Giga PHY0 Option



OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3
	a	b/g/n	ac	5GHz						
AP6398S	Yes	Yes	Yes	Yes	5.0	37.4MHz	1.71-3.6V	Yes	Yes	Yes
AP6356S	Yes	Yes	Yes	Yes	4.1	37.4MHz	1.71-3.6V	Yes	Yes	Yes
RTL8822BS Module	Yes	Yes	Yes	Yes	4.1	Module Integrated	1.71-3.6V	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	62.WIFI/BT-SDMMC1_2T2R + UART				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	49 of 69

PCIe WIFI6/BT MODULE-2T2R

WIFI_REG_ON_H_GPIO2_B1
WIFI_WAKE_HOST_H_GPIO2_B2
UART1_RX_M0
UART1_TX_M0
UART1_RTSn_M0
UART1_CTSn_M0
BT_REG_ON_H_GPIO2_B7
BT_WAKE_HOST_H_GPIO2_C0
HOST_WAKE_BT_H_GPIO2_C1
SOC_PCM_CLK
SOC_PCM_SYNC
SOC_PCM_OUT
SOC_PCM_IN
CLK32K_OUT1_WIFI
RK809_32KOUT_WIFI
RTCIC_32KOUT

Note:
If ultra low standby power consumption is required, please contact RK to reallocate GPIO and Power

PCIE20_TXP
PCIE20_TXN
PCIE20_RXP
PCIE20_RXN
PCIE20_REFCLKP
PCIE20_REFCLKN
PCIE20_CLKREQn_M1
PCIE20_WAKEn_M1
PCIE20_PERSTn_M1

Note:
Adjusted the load capacitance according to the crystal specification.

ANT6400 ANT_JACK
ANT6401 ANT_JACK
ANT6402 ANT_JACK
C6400 DNP C0402
C6401 DNP C0402
C6402 DNP C0402
C6403 10pF C0G 50V C0402
C6404 DNP C0402
C6405 DNP C0402
C6406 DNP C0402
R6400 0R 5% R0402
R6401 0R 5% R0402

50 Ohm RF trace
For AP6275PR3

U6400
AP6275P/AP6275PR3
MD50_AP6XXX_13RX15RX1R5

C6407 22pF C0G 50V C0402
C6409 22pF C0G 50V C0402
Y6400 37.4MHz CRY4_3R20X2R50X0R80
R6402 0R 5% R0402

PCIE20_PERSTn_1V8
WIFI_REG_ON_H_GPIO2_B1
WIFI_WAKE_HOST_H_GPIO2_B2
SOC_PCM_IN
SOC_PCM_OUT
SOC_PCM_SYNC
SOC_PCM_CLK
PCIE20_WAKEn_1V8

BT_WAKE_HOST_H_GPIO2_C0
HOST_WAKE_BT_H_GPIO2_C1
PCIE_TDP C6408 100nF C0201 X5R 10V PCIE20_RXP
PCIE_TDN C6410 100nF C0201 X5R 10V PCIE20_RXN
PCIE_RDP C6411 100nF C0201 X5R 10V PCIE20_TXP
PCIE_RDN C6412 100nF C0201 X5R 10V PCIE20_TXN
UART1_RTSn_M0
UART1_CTSn_M0
UART1_TX_M0
UART1_RX_M0
BT_REG_ON_H_GPIO2_B7
PCIE20_CLKREQn_1V8

C6413 4.7uF 10V X5R C0603

VCCIO_WL
Q6400 2SK3018 SOT_323
R6403 10K 5% R0402
PCIE20_CLKREQn_M1
PCIE20_CLKREQn_1V8

Q6401 2SK3018 SOT_323
R6405 10K 5% R0402
PCIE20_WAKEn_M1
PCIE20_WAKEn_1V8

PCIE20_PERSTn_M1 R6407 10K 5% R0402 PCIE20_PERSTn_1V8
R6408 12K 5% R0402

L6400 2.2uH IND_303015 1A_DCR<=80mohm
L6401 2.2uH IND_303015 1A_DCR<=80mohm

VCC3V3_PCIEWL_VBAT
VCC3V3_SYS
R6404 0R 5% R0603
C6414 100nF X5R 10V C0402
C6415 22uF X5R 10V C0805
Max:1.2A

VCCIO_WL
VCC_1V8
R6406 0R 5% R0402
C6416 100nF X5R 10V C0402
C6417 4.7uF 10V X5R C0603
Max:0.3A

C6418 4.7uF 10V X5R C0603

PCIE_REFCLKP
PCIE_REFCLKN
C6419 100pF C0201 X5R 25V PCIE20_REFCLKP
C6420 100pF C0201 X5R 25V PCIE20_REFCLKN

R6409 10K 5% R0402
RK809_32KOUT_WIFI R6410 0R 5% R0402
RTCIC_32KOUT R6411 DNP 0R 5% R0402
CLK32K_OUT1_WIFI R6412 DNP 0R 5% R0402
PCIE_WIFIBT_32KIN
R6413 DNP R0402
C6421 DNP C0402

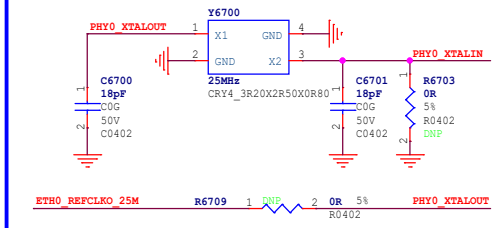
Rockchip Confidential

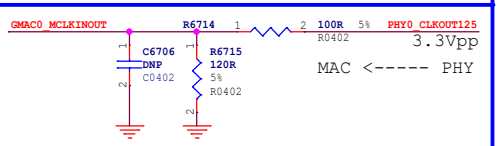
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	64.WIFI6/BT-PCIe_2T2R + UART				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	50 of 69

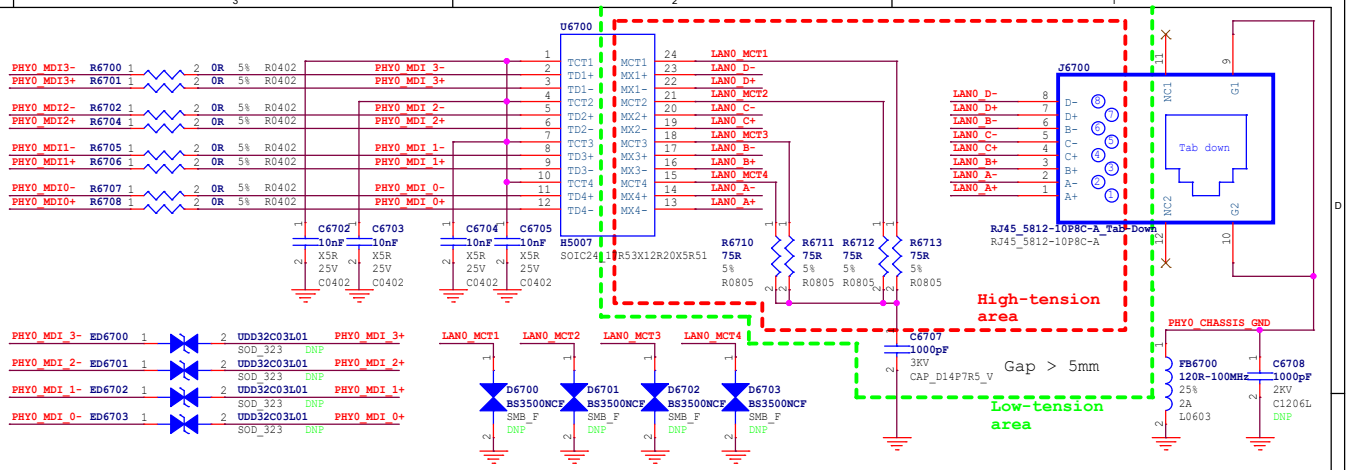
Giga PHY0

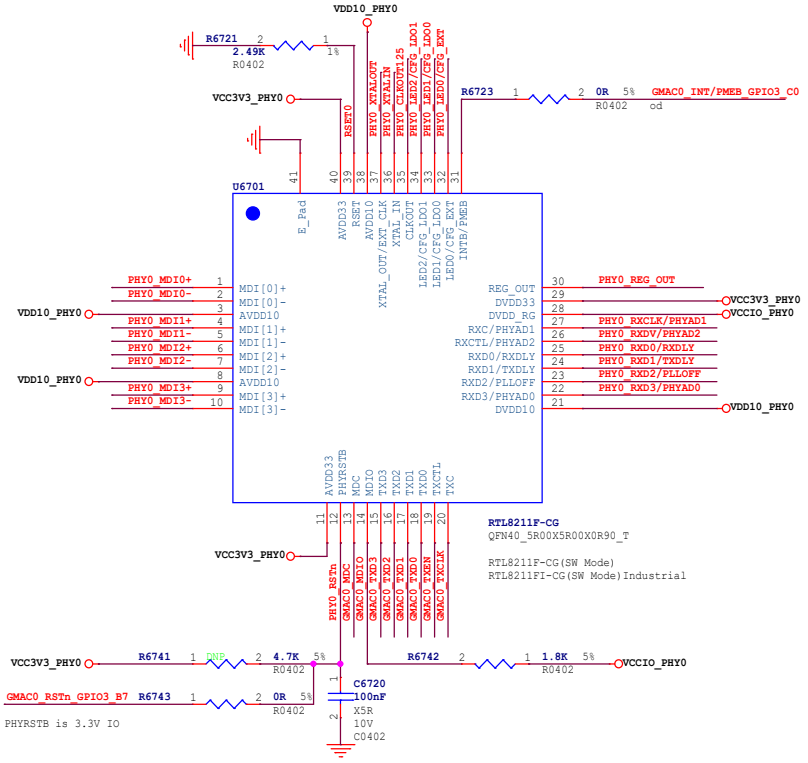
And WIFI/BT Option

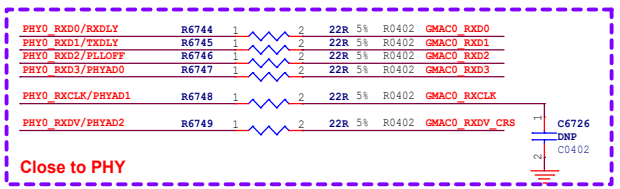
GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
ETH0_REFCLKO_25M
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
GMAC0_RSTn_GPIO3_B7
GMAC0_INT/PMEB_GPIO3_C0

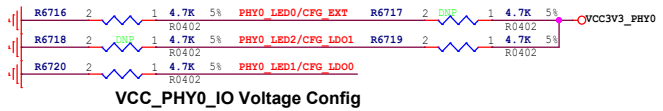


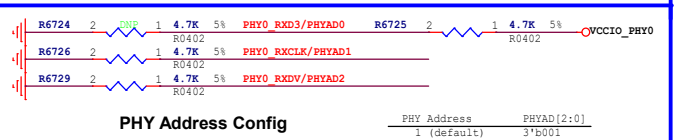


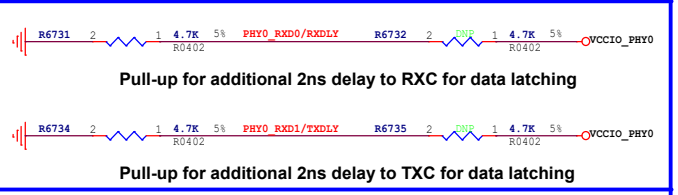


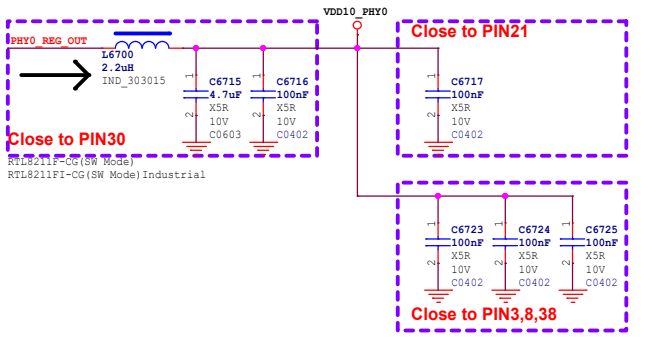




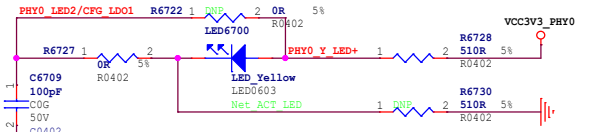






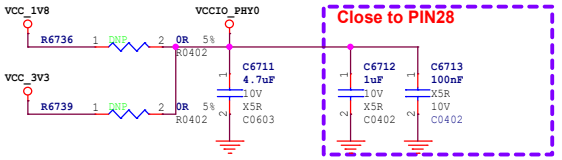


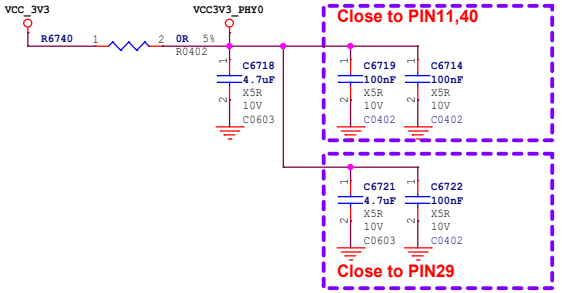
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	



Note:

According to the actual choice of mounted
Cannot be mounted at the same time

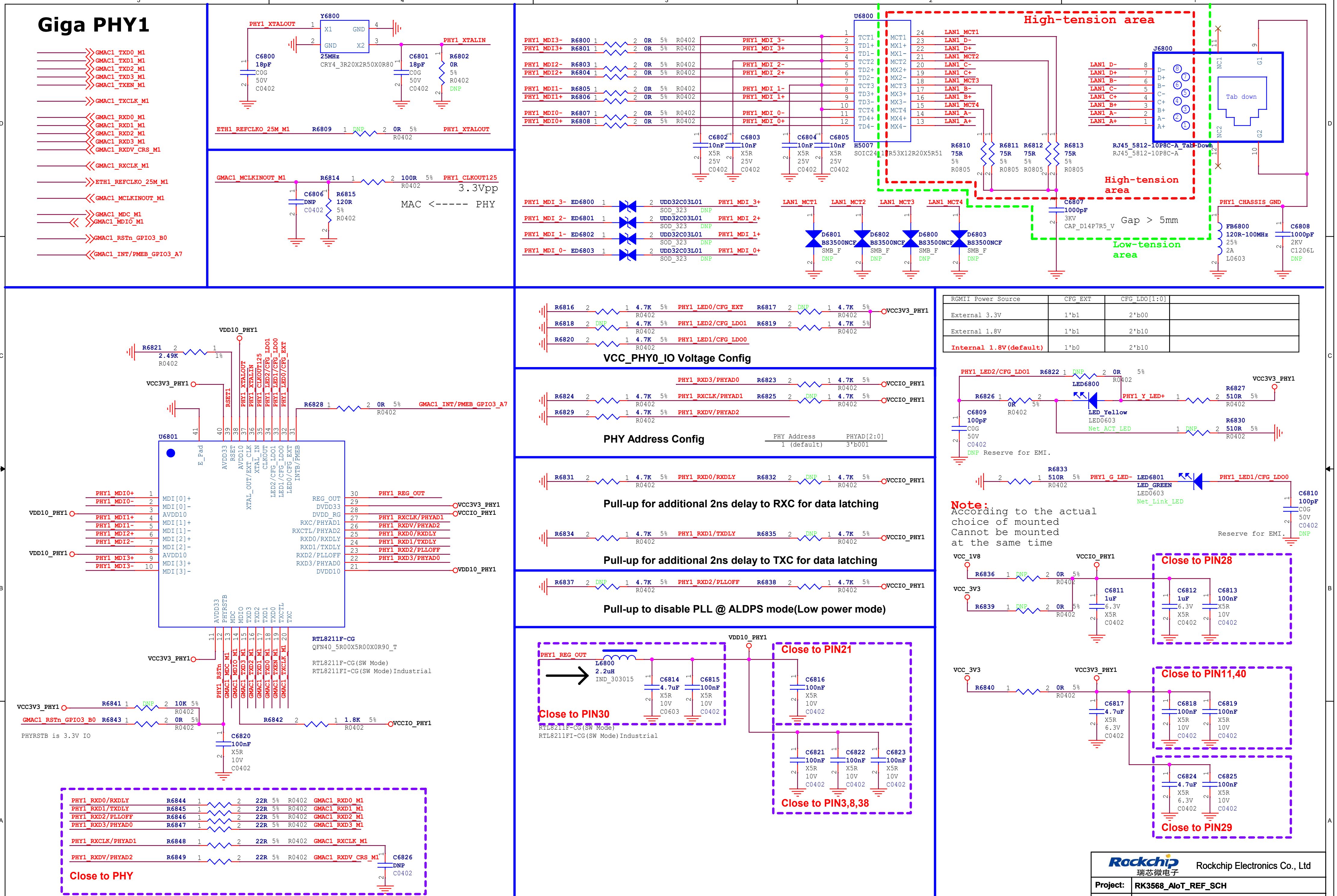




Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	67.Ethernet-GEPHY_RGMII0		
Date:	Thursday, February 04, 2021	Rev:	V1.0
Designed by:	Zhangdz	Reviewed by: Default	Sheet: 51 of 69

Giga PHY1

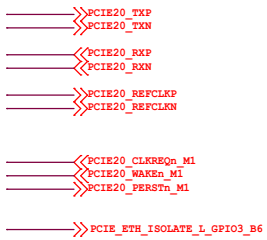


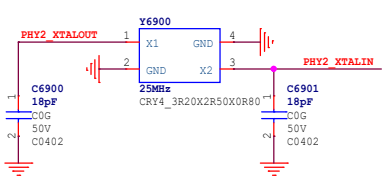
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V(default)	1'b0	2'b10

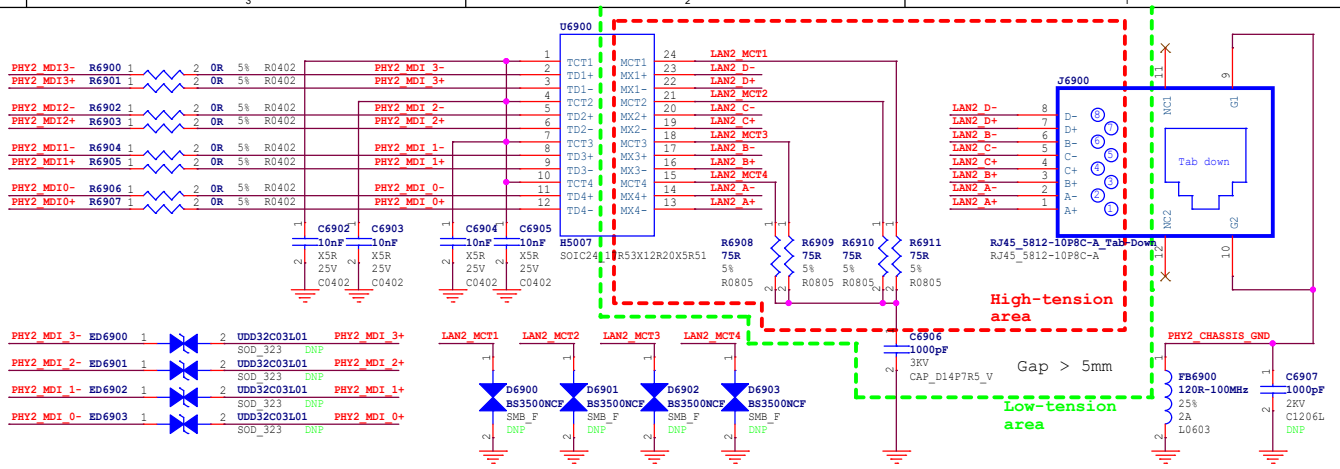
Rockchip Confidential

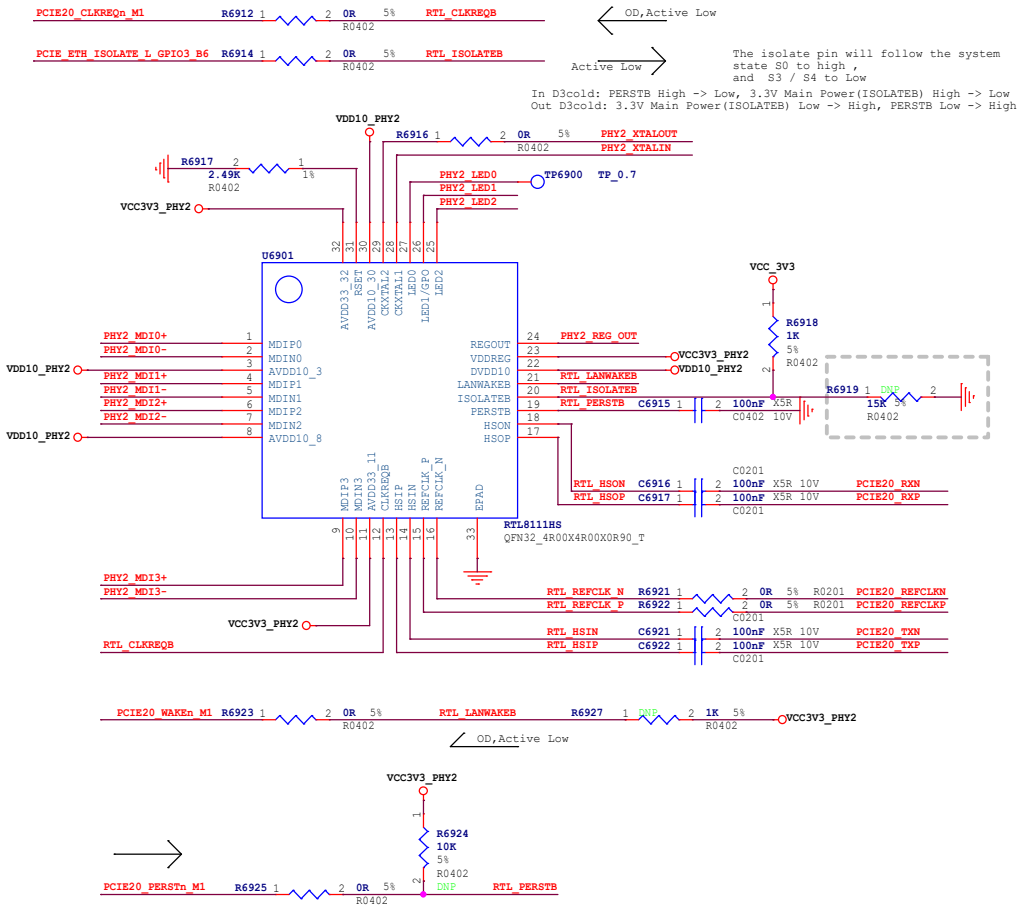
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	68.Ethernet-GEPHY_RGMII1_M1
Date:	Thursday, February 04, 2021 — Rev: V1.0
Designed by:	Zhangdz — Reviewed by: Default — Sheet: 52 of 69

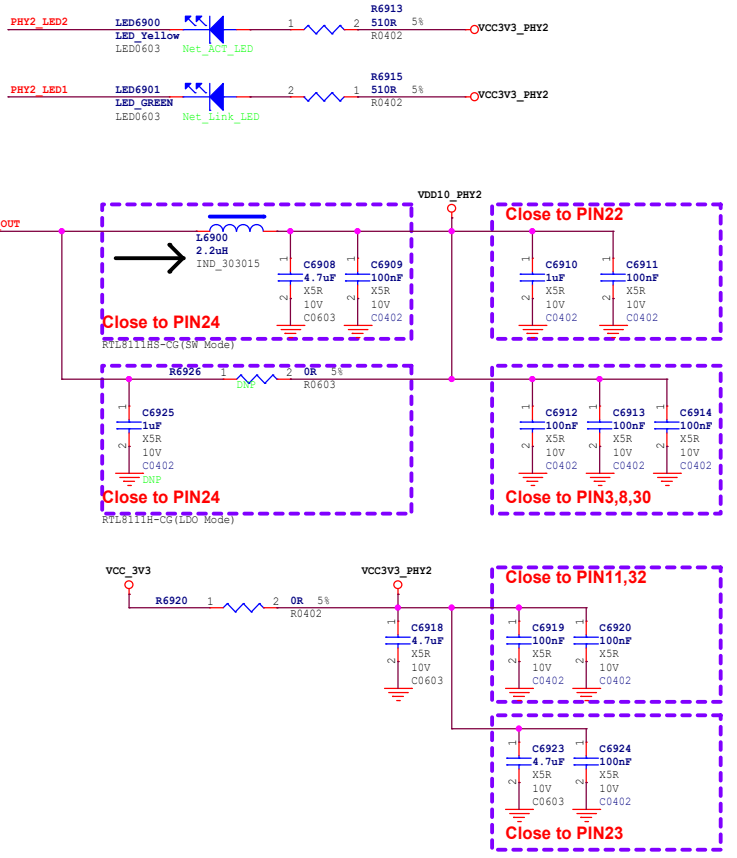
PCIE Ethernet



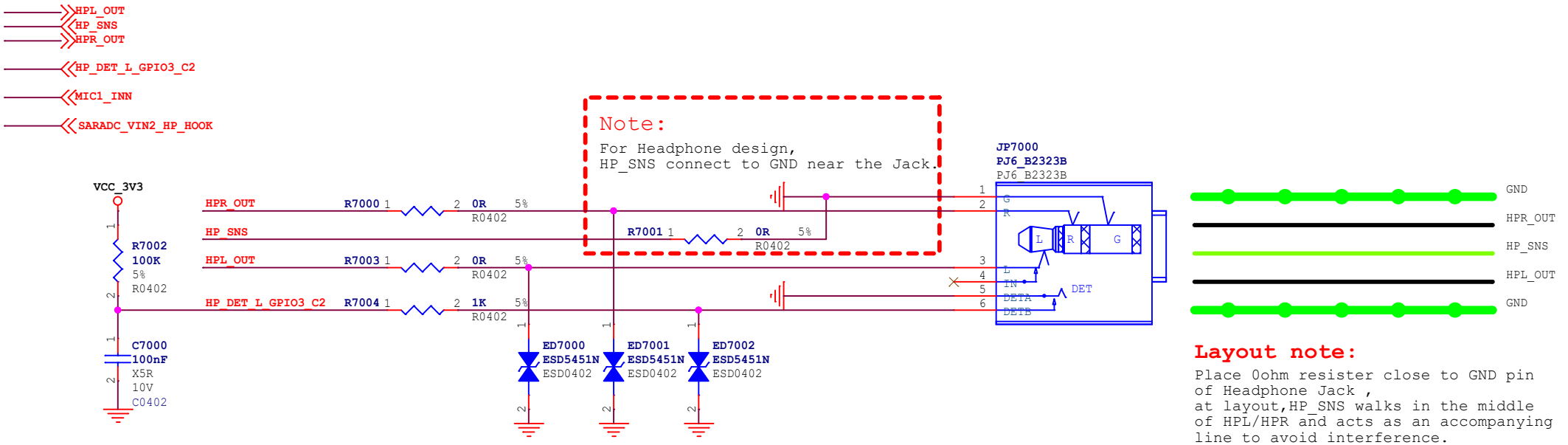








Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	69.Ethernet-PCIE Ethernet				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	53 of 69



Layout note:

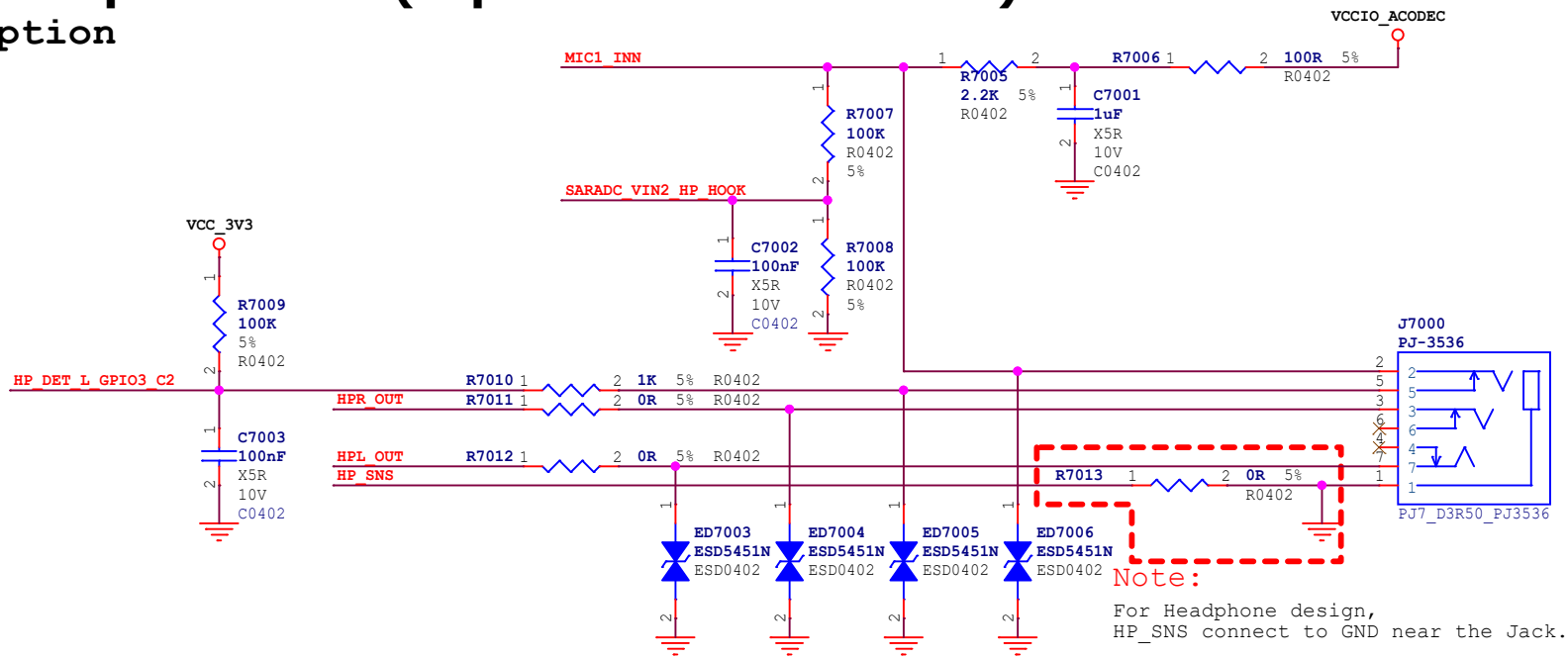
Place 0ohm resister close to GND pin of Headphone Jack , at layout,HP_SNS walks in the middle of HPL/HPR and acts as an accompanying line to avoid interference.

Default

Headphone Jack(3-pole with DET)

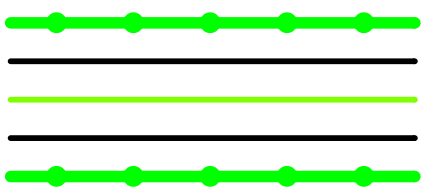
Headphone Jack(4-pole with DET & MIC)

Option



Layout note:

Place 0ohm resister close to GND pin of Headphone Jack , at layout,HP_SNS walks in the middle of HPL/HPR and acts as an accompanying line to avoid interference.



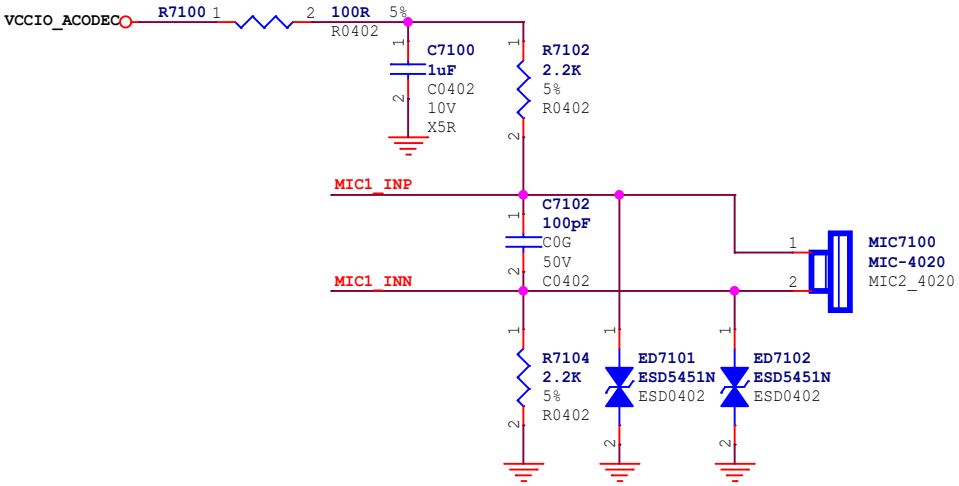
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	70.Audio-Headphone Port				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	54 of 69

SPKN_OUT
SPKP_OUT

MIC1_INP
MIC1_INN

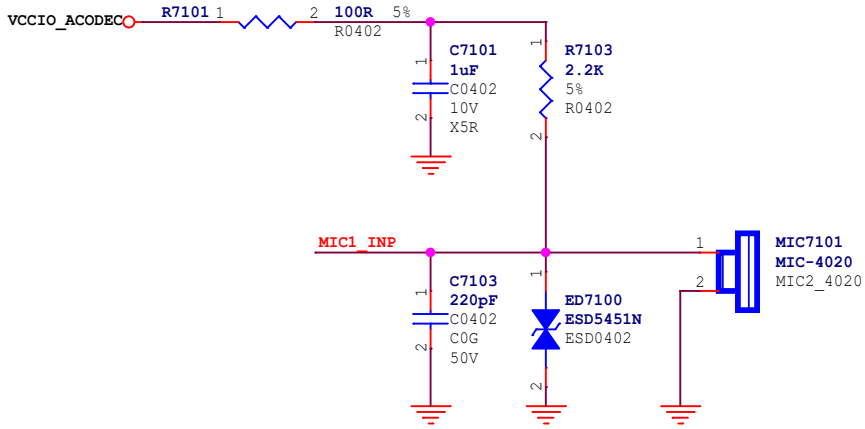
Default

MIC for 3-pole Headphone Jack



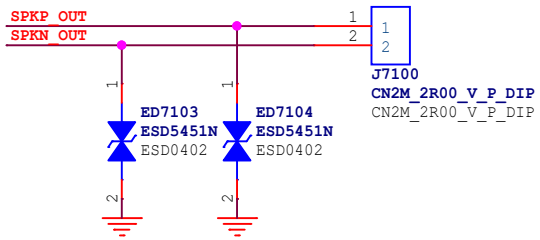
Option

MIC for 4-pole Headphone Jack



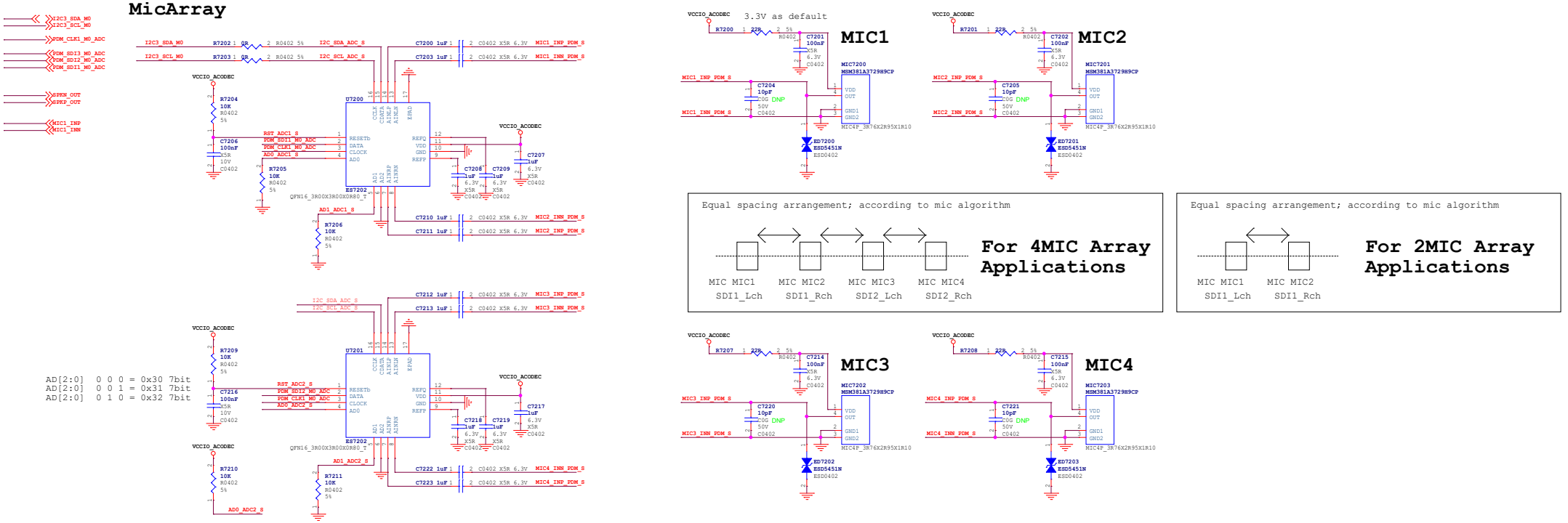
SPK

Note:8ohm/1.3W
Speaker Output



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	71.Audio-SingleMic+RK809_SPK				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	55 of 69

MicArray

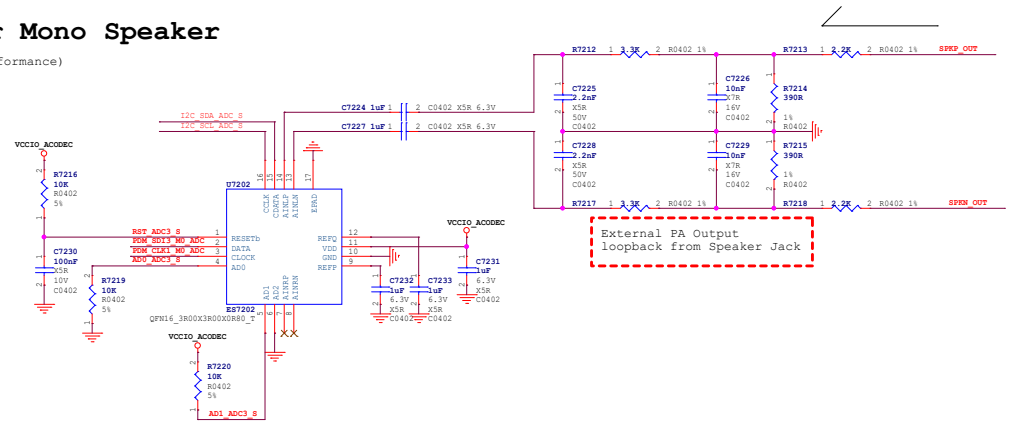


AD[2:0] 0 0 0 = 0x30 7bit
AD[2:0] 0 0 1 = 0x31 7bit
AD[2:0] 0 1 0 = 0x32 7bit

Option1

Loopback for Mono Speaker

(External ADC, better performance)

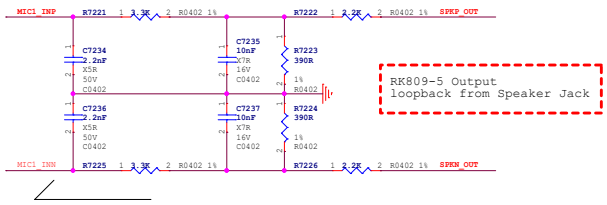


Option2

Loopback for Mono Speaker

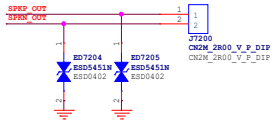
(Available while No MIC is connected to RK809-5)

(cost-effective)

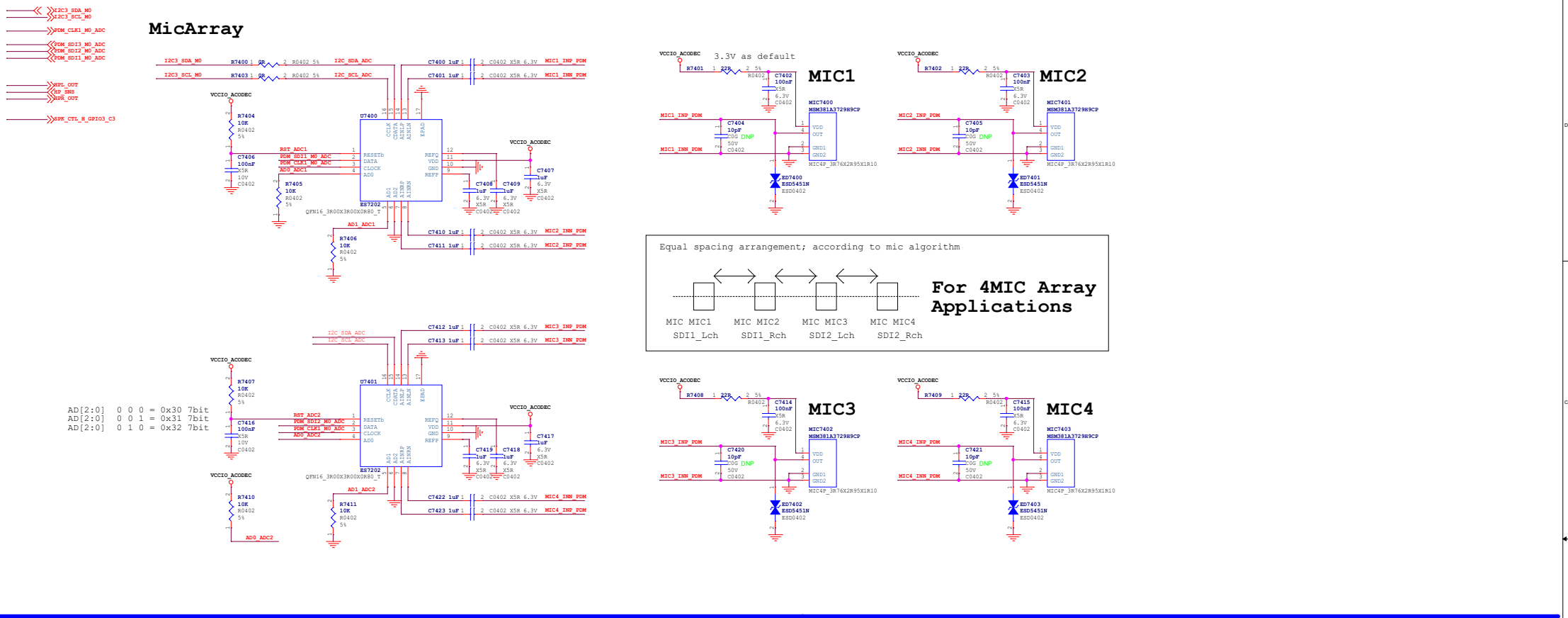


RK809-5 SPK

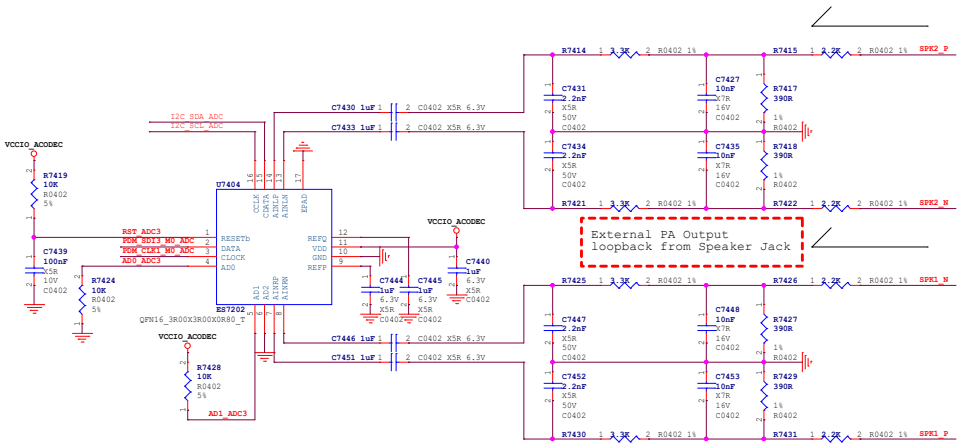
Note:8ohm/1.3W
Speaker Output



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	72.Audio-MicArray+RK809_SPK
Date:	Thursday, February 04, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	56 of 69

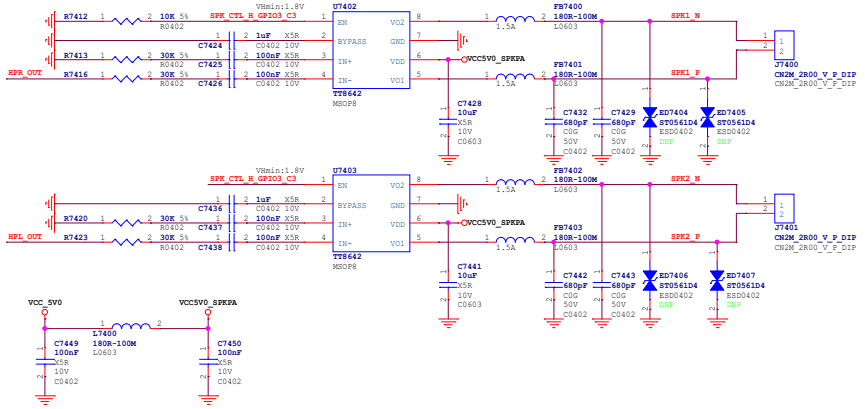


Loopback for Dual Speakers

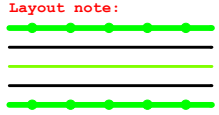


Speaker Output

Note:4ohm/3W



Layout note:



For NO Headphone design, HP_SNS connect to GND near the PMIC.

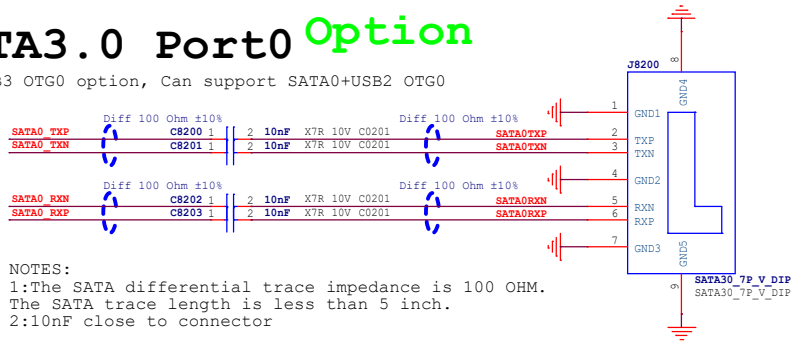
Rockchip Confidential

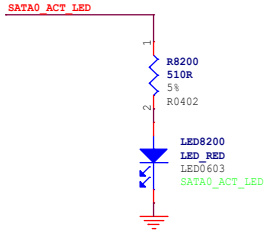
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	74.Audio-MicArray+EXT Dual_SPK		
Date:	Thursday, February 04, 2021	Rev:	V1.0
Designed by: Zhangdz	Reviewed by: Default	Sheet:	57 of 69

SATA0_TXP
SATA0_TXN
SATA0_RXP
SATA0_RXN
SATA1_TXP
SATA1_TXN
SATA1_RXP
SATA1_RXN
SATA2_TXP
SATA2_TXN
SATA2_RXP
SATA2_RXN
SATA0_ACT_LED
SATA1_ACT_LED
SATA2_ACT_LED

SATA3.0 Port0 Option

And USB3 OTG0 option, Can support SATA0+USB2 OTG0

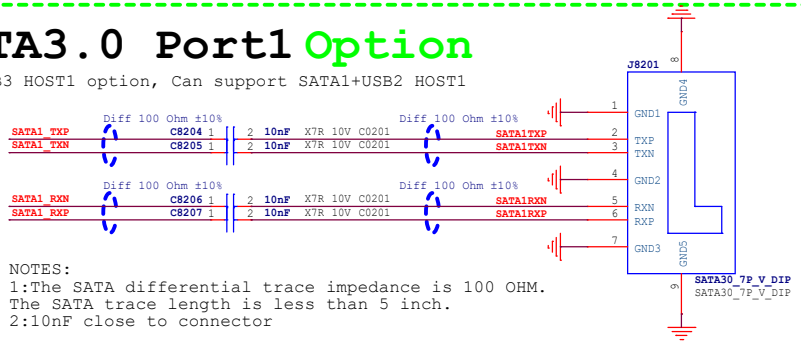


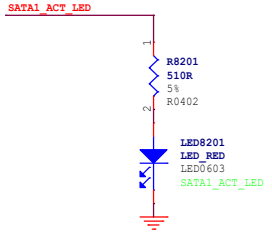


NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

SATA3.0 Port1 Option

And USB3 HOST1 option, Can support SATA1+USB2 HOST1

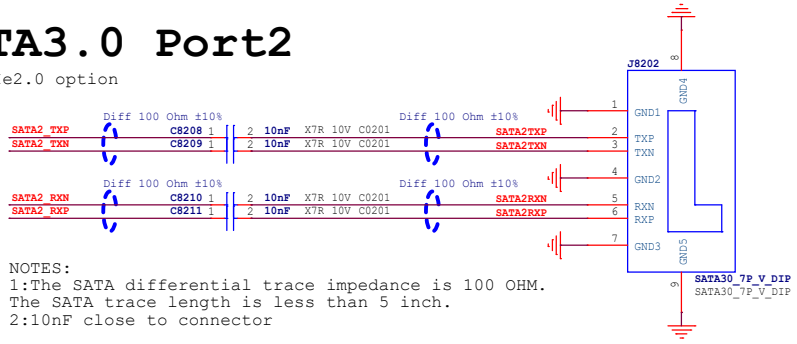


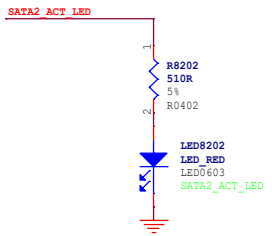


NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

SATA3.0 Port2

And PCIe2.0 option

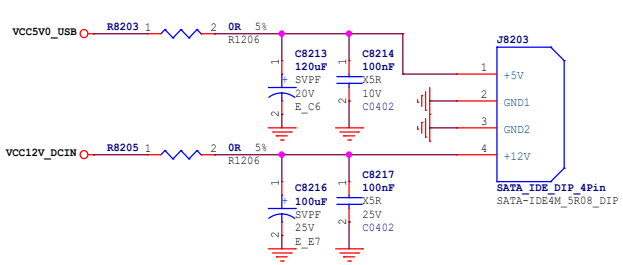


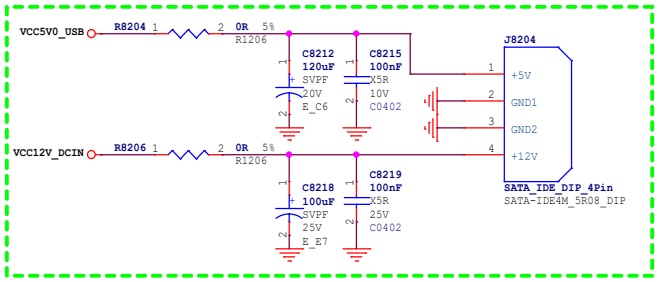


NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

SATA Power

The current is estimated according to the actual number of SATA
High power switching separate power supply is recommended for more than 2



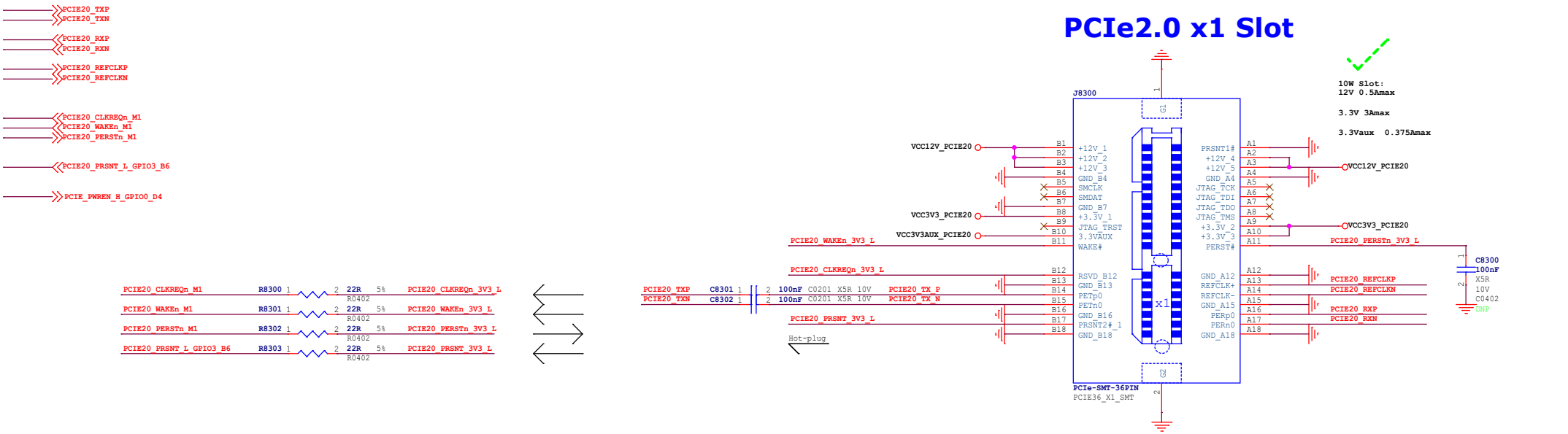


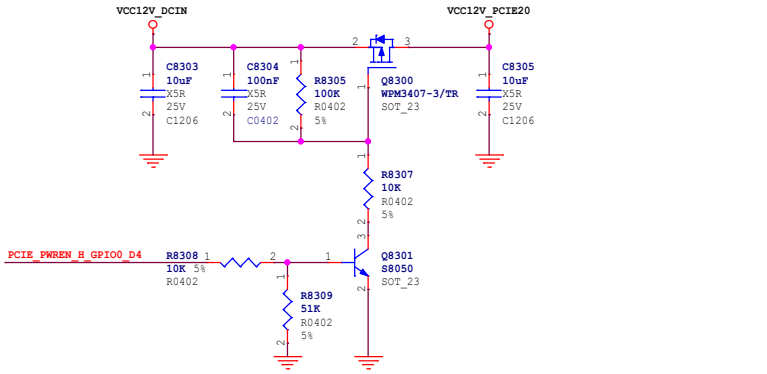
Option

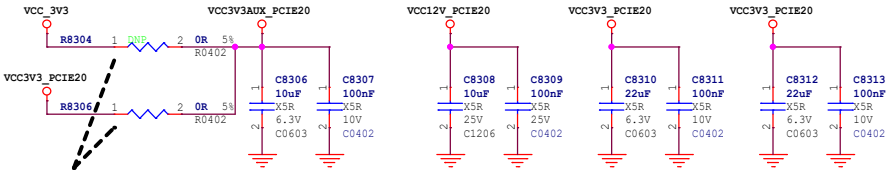
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	82.SATA-SATA3.0 Slot_7P				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	58 of 69

PCIe2.0 x1 Slot

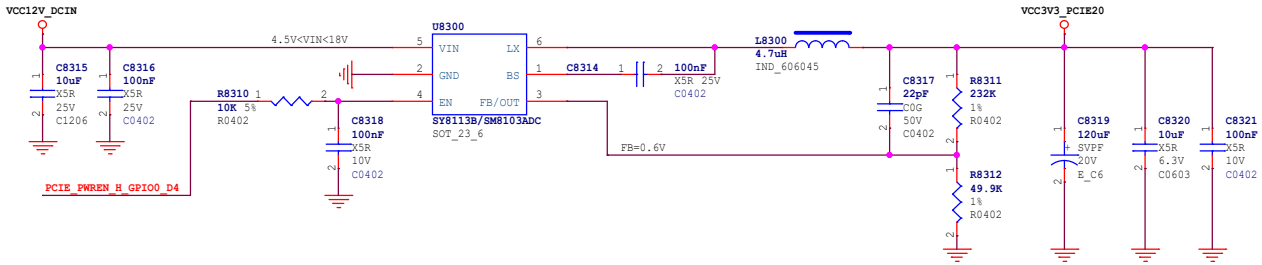






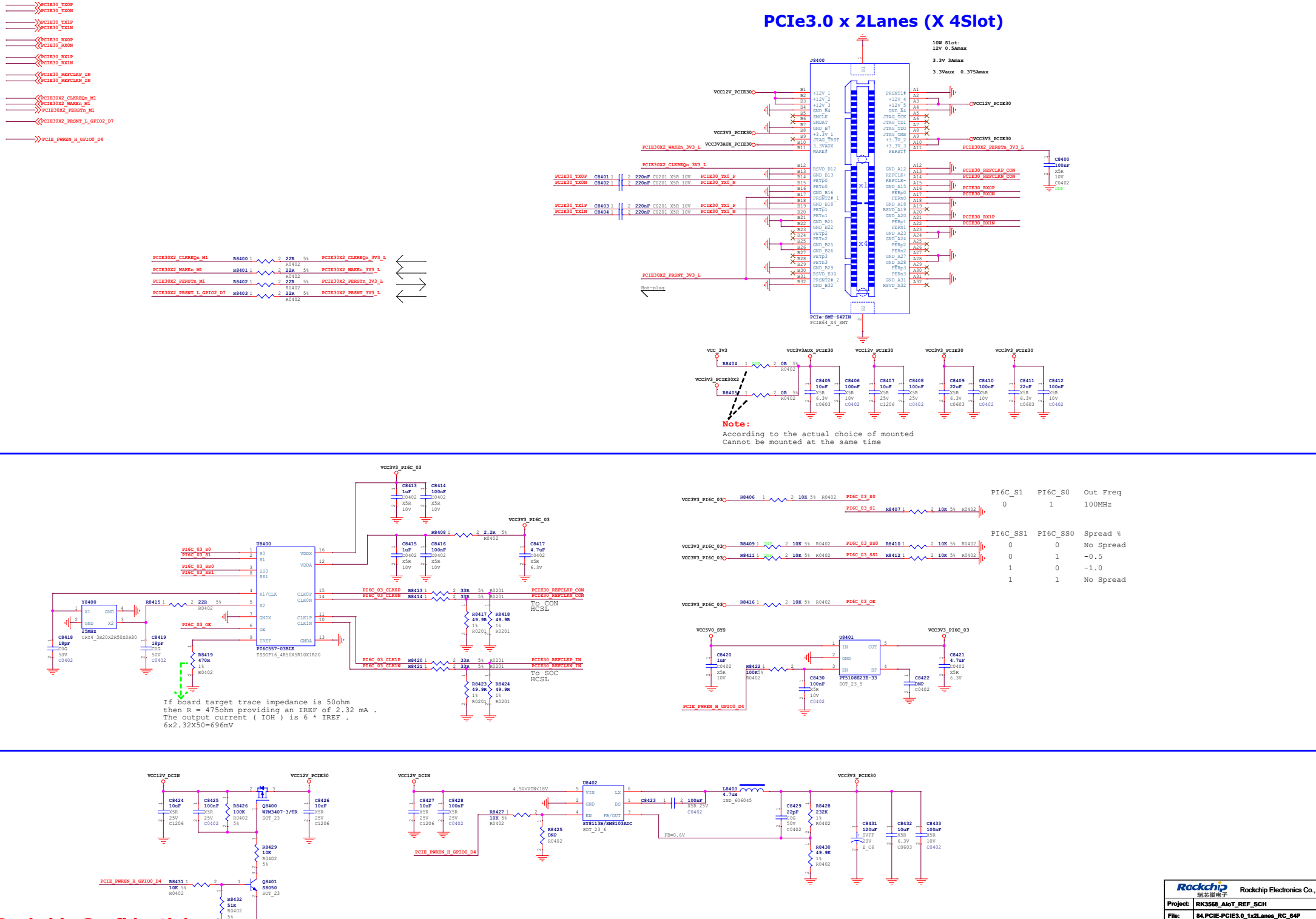
Note:

According to the actual choice of mounted
Cannot be mounted at the same time



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	83.PCIE-PCIE2.0_1x1Lane_RC_36P				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	59 of 69

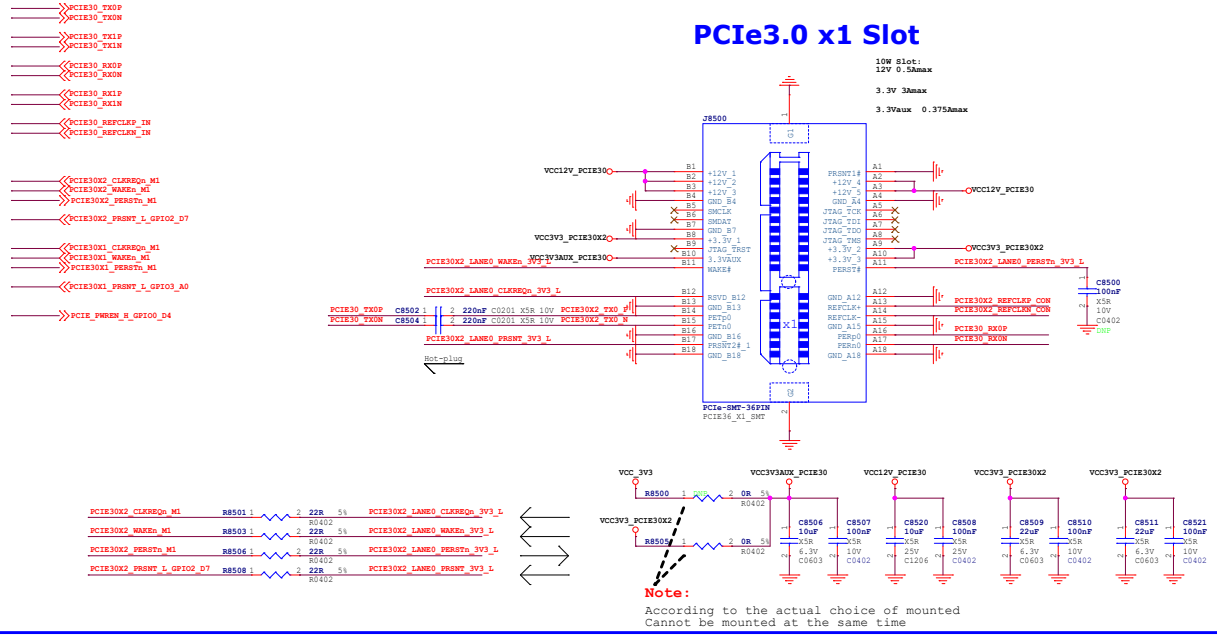
PCIe3.0 x 2Lanes (X 4Slot)



Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	84.PCIE-PCIE3.0_1x2Lanes_RC_64P		
Date:	Thursday, February 04, 2021	Rev:	V1.0
Designed by: Zhangtz	Reviewed by: Default	Sheet:	60 of 69

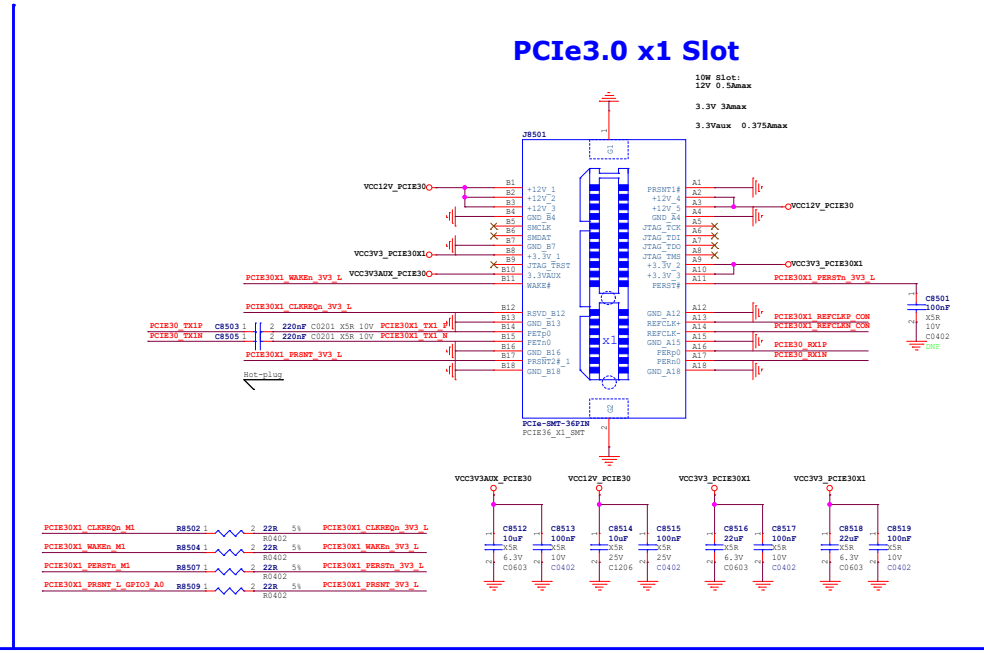
PCIe3.0 x1 Slot

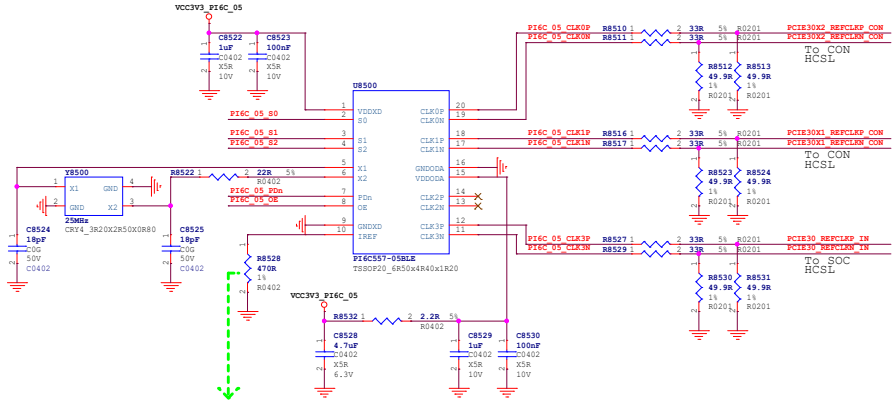


Note:

According to the actual choice of mounted
Cannot be mounted at the same time

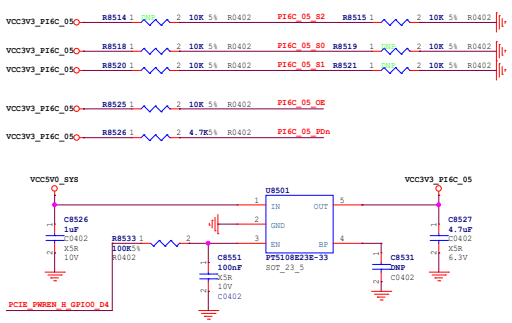
PCIe3.0 x1 Slot

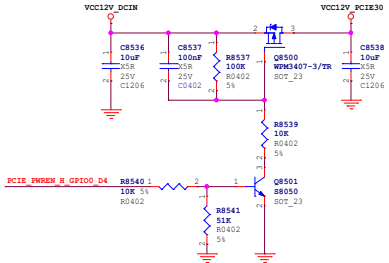


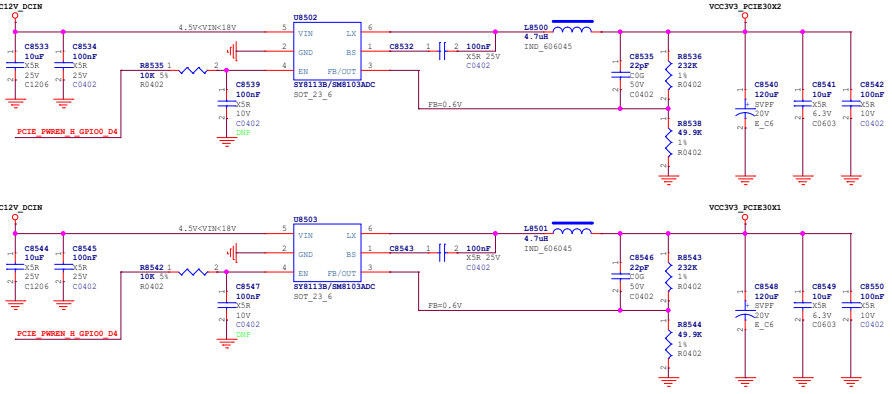


If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA . The output current (IOH) is 6 * IREF .
6x2.32X50=696mV

PI6C_S2	PI6C_S1	PI6C_S0	Spread %	Out Freq
0	0	0	-0.5	100MHz
0	0	1	-1.0	100MHz
0	1	0	-1.5	100MHz
0	1	1	No Spread	100MHz

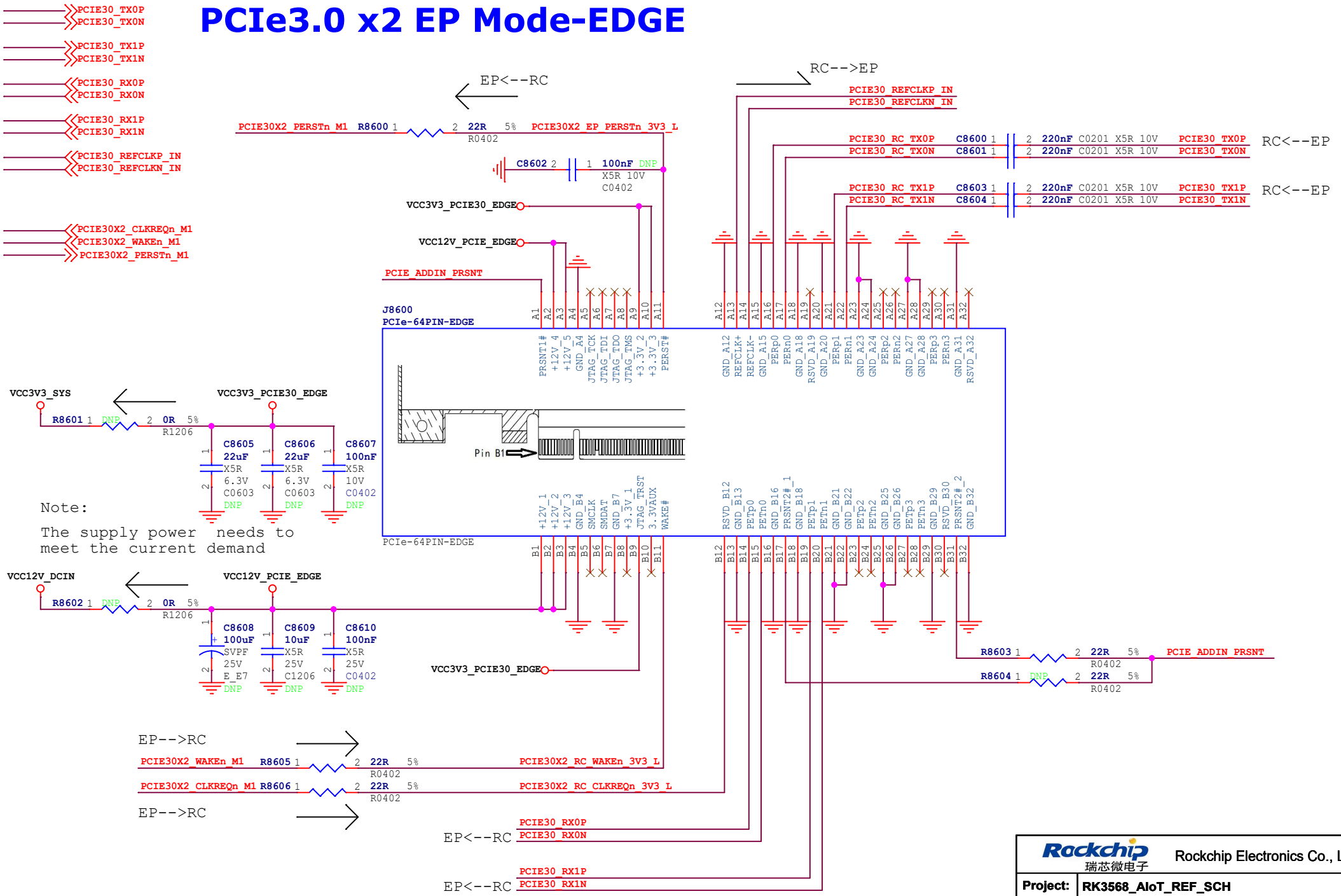






Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	85.PCIE-PCIE3.0_2x1Lane_RC_32P
Date:	Thursday, February 04, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	61 of 69

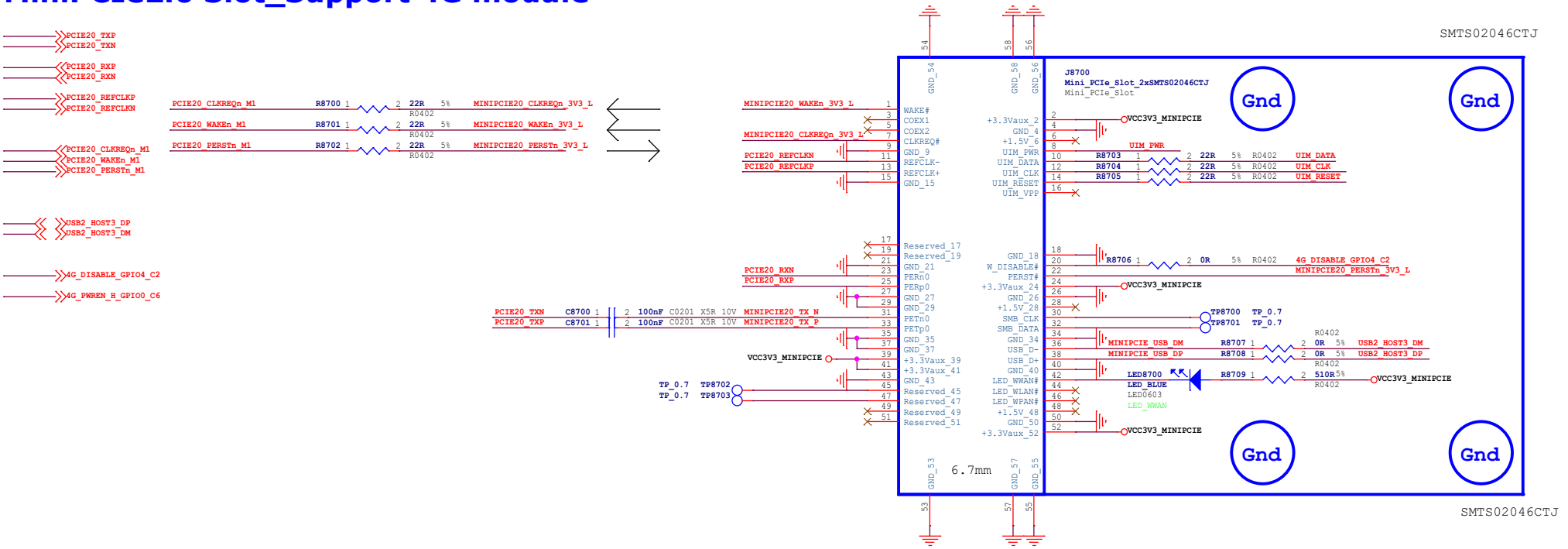
PCIe3.0 x2 EP Mode-EDGE

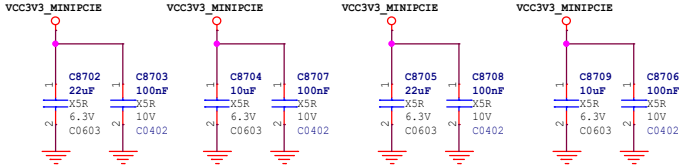


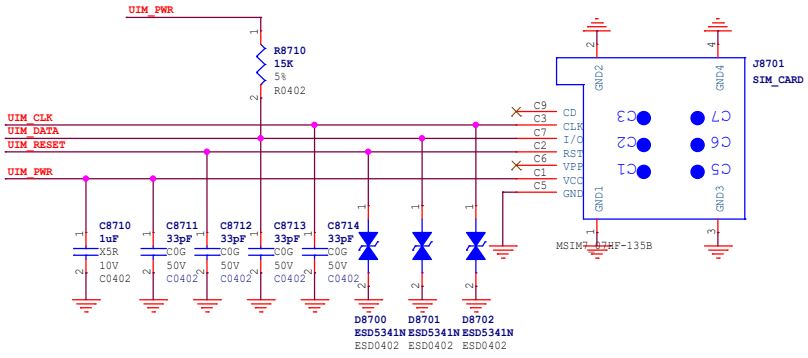
Rockchip Confidential

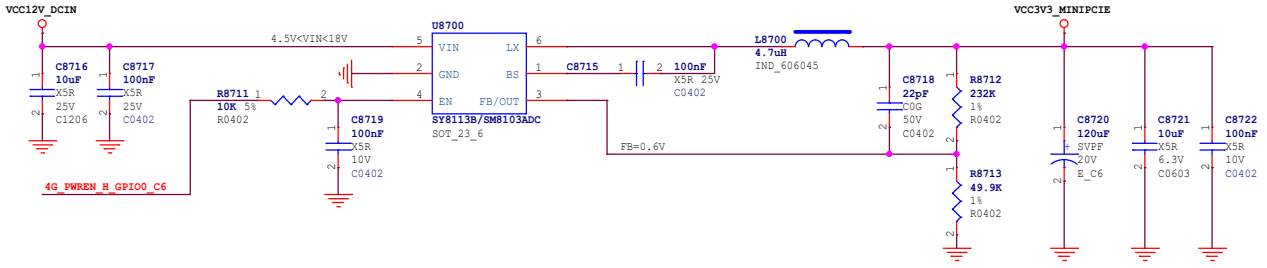
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	86.PCIE-PCIE3.0_1x2Lanes_EP_64P				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	62 of 69

MiniPCIe2.0 Slot_Support 4G module







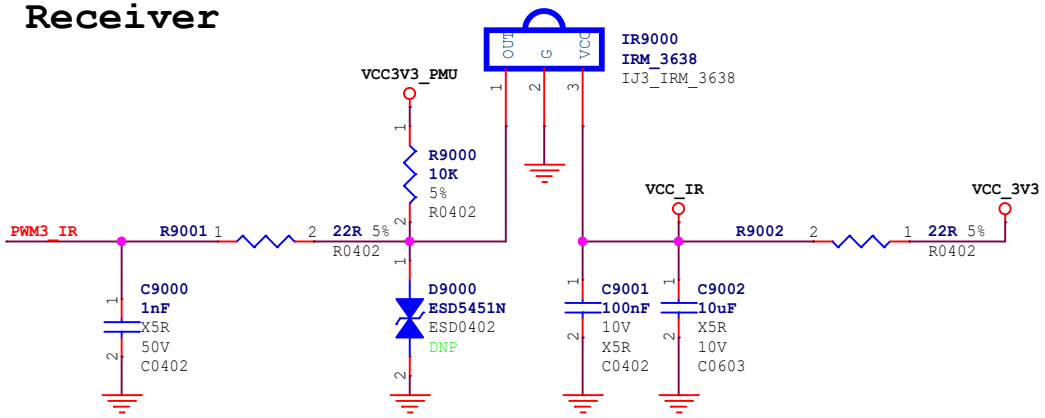


Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	87.MiniPCIe2.0 Slot_With 4G Fun				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	63 of 69

PWM3_IR

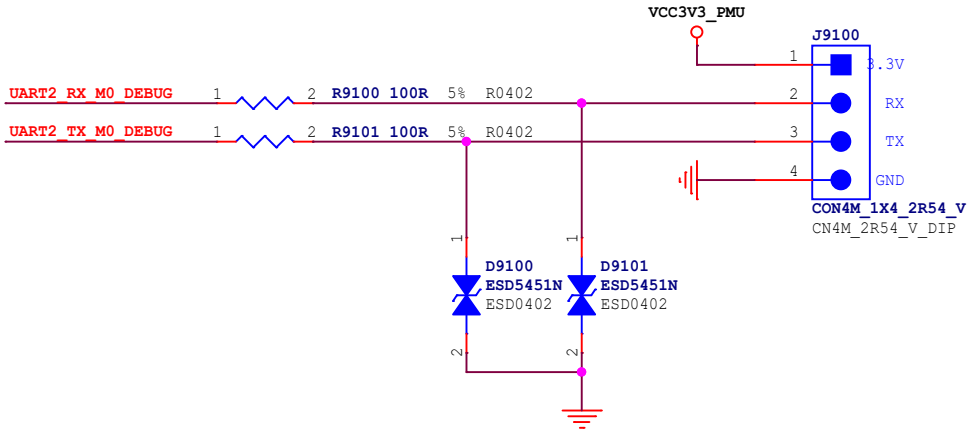
IR Receiver



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	90.IR Receiver				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	64 of 69

UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	91.Debug UART				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	65 of 69

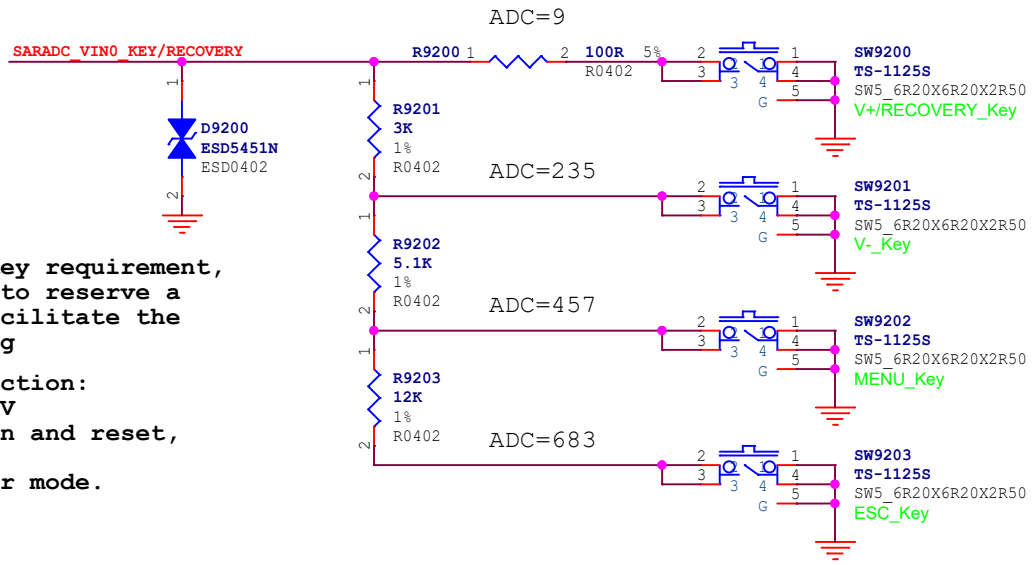
Key Array

SARADC_VIN0_KEY/RECOVERY

SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

RESETn

RK809_PWRON

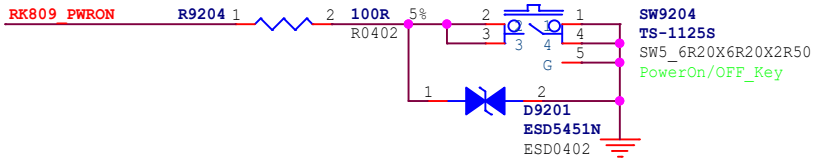


Note:

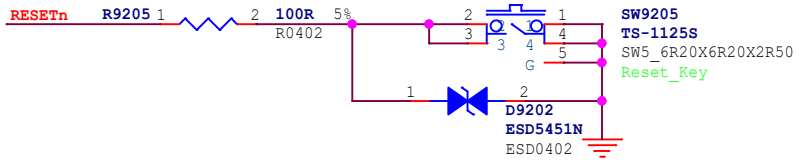
If there is no Key requirement, It is suggested to reserve a SW9200 Key to facilitate the development debug

RECOVERY_Key function:
If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

PowerOn/OFF_Key

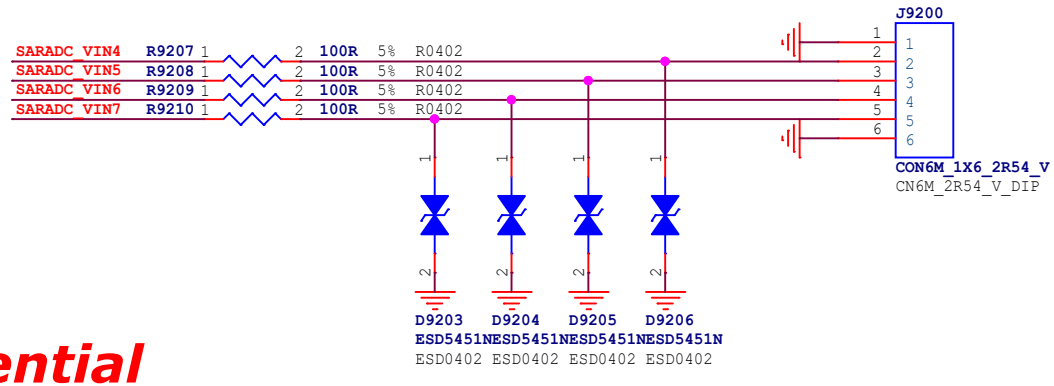


Reset_Key



SARADC

Voltage range:0v-1.8V



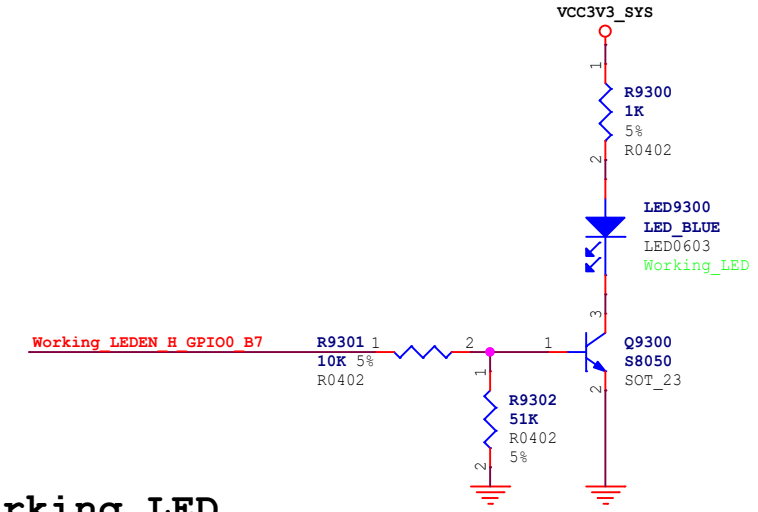
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	92.KEY Array/SARADC				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	66 of 69

Working_LEDEN_H_GPIO0_B7

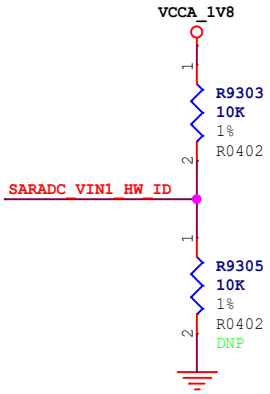
SARADC_VIN1_HW_ID

SARADC_VIN3_BOM_ID



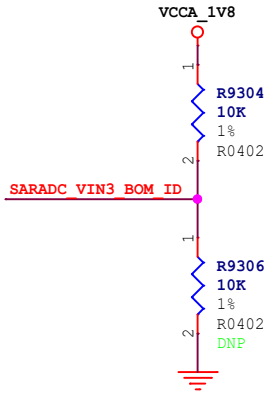
Working LED

HW_ID



SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K

BOM_ID



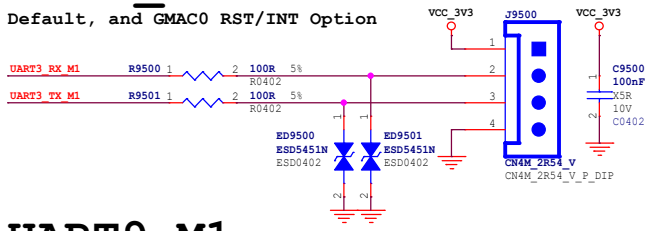
SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	93.LED/HW_ID/BOM_ID				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	67 of 69

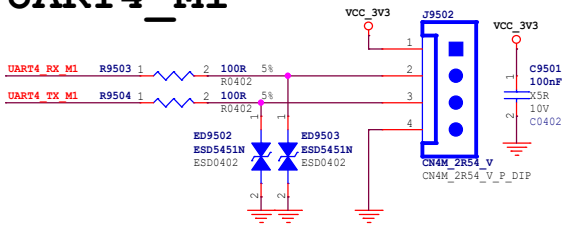
UART9_TX_M1
UART9_RX_M1
UART4_RX_M1
UART4_TX_M1
UART3_TX_M1
UART3_RX_M1
UART7_TX_M1
UART7_RX_M1
RS485_DIR_GPIO3_B5
UART6_TX_M1
UART6_RX_M1
CAN0_TX_M1
CAN0_RX_M1

UART3_M1

Default, and GMAC0 RST/INT Option

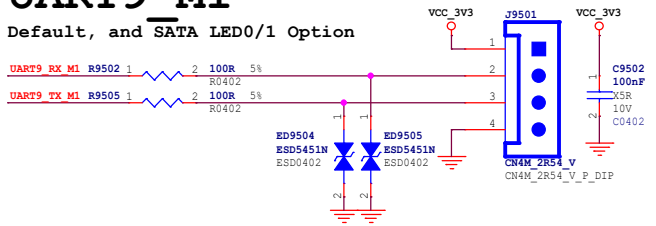


UART4_M1

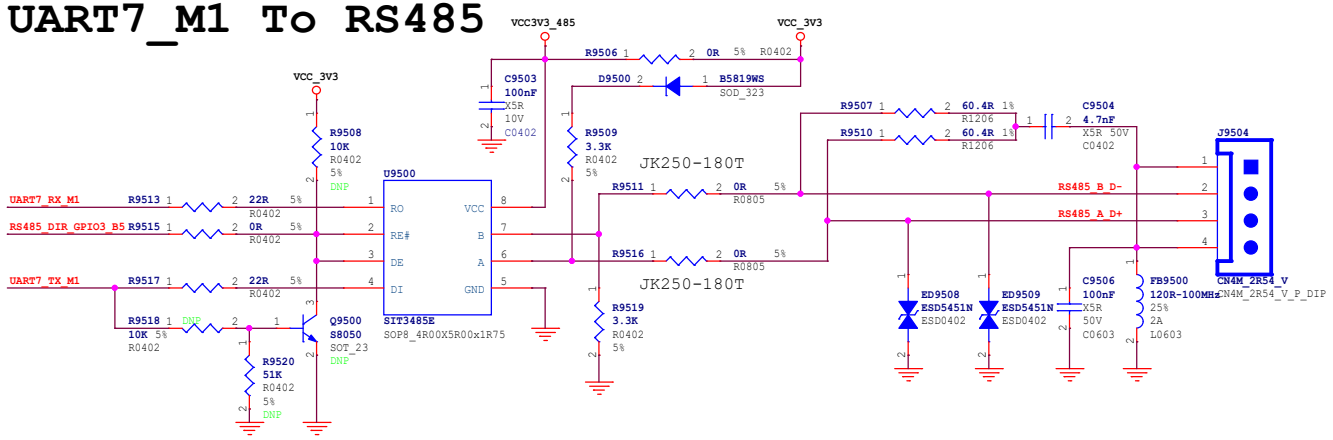


UART9_M1

Default, and SATA LED0/1 Option

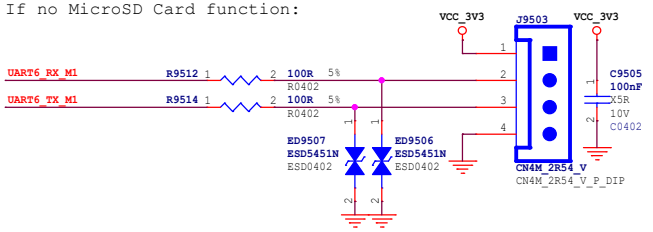


UART7_M1 To RS485



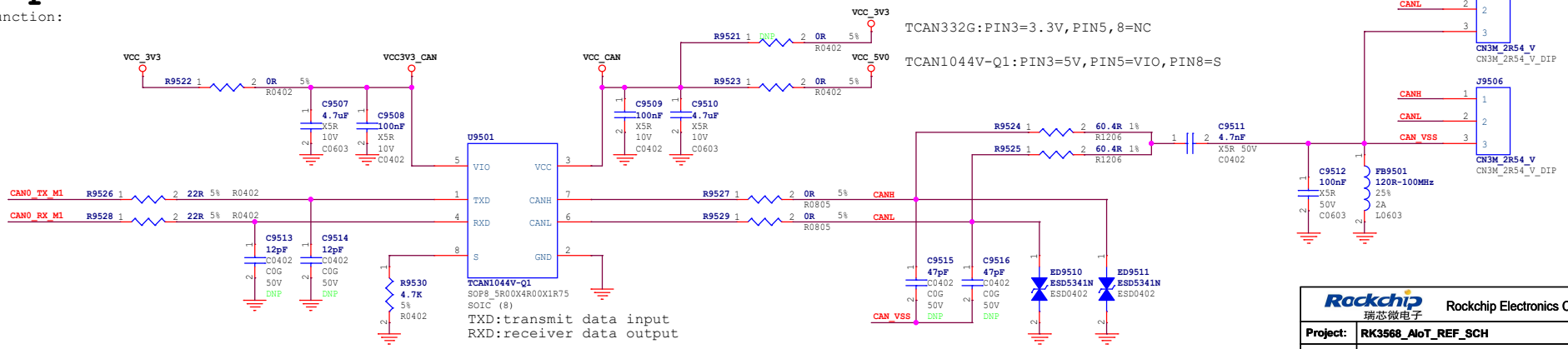
UART6_M1-Option

If no MicroSD Card function:



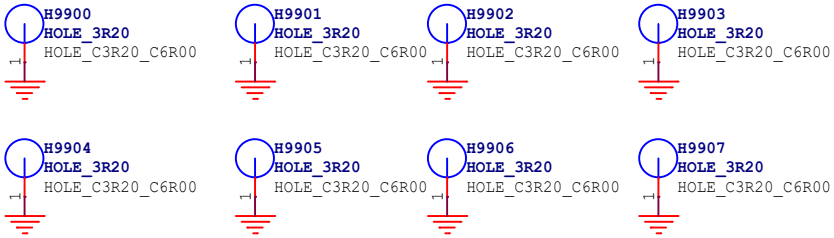
CAN0_M1-Option

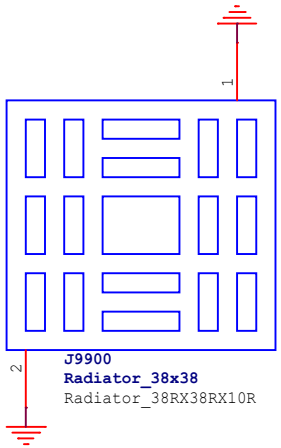
If no MicroSD Card function:



Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	95.UART/RS485/CAN Port				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	68 of 69





TOP Mark

BOTTOM Mark

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	99.Mark/Hole/Heatsink				
Date:	Thursday, February 04, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	69 of 69