ES7202

High Performance PDM Stereo Audio ADC

FEATURES

- High performance advanced delta-sigma audio ADC
- 100 dB signal to noise ratio
- -85 dB THD+N
- Low noise PGA
- 8 to 96 kHz sampling frequency
- Low power

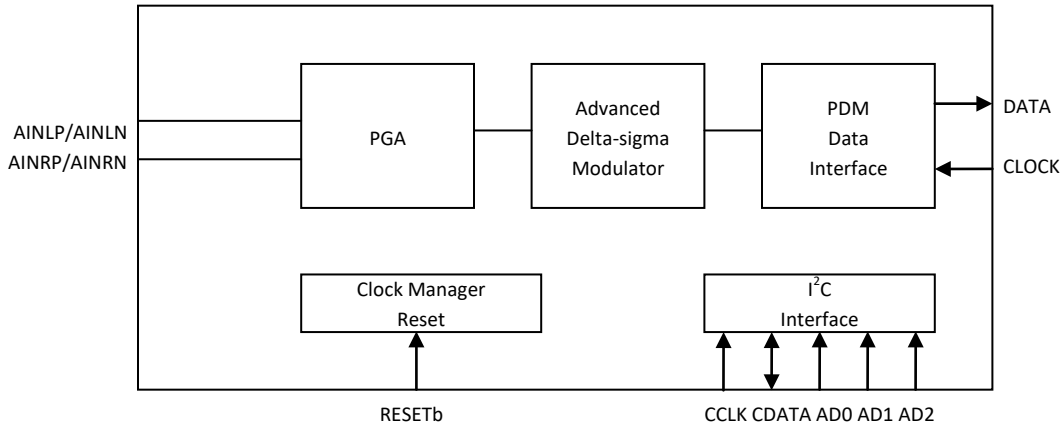
APPLICATIONS

- Mic Array
- Soundbar
- Audio Interface
- Digital TV
- A/V Receiver
- DVR
- NVR

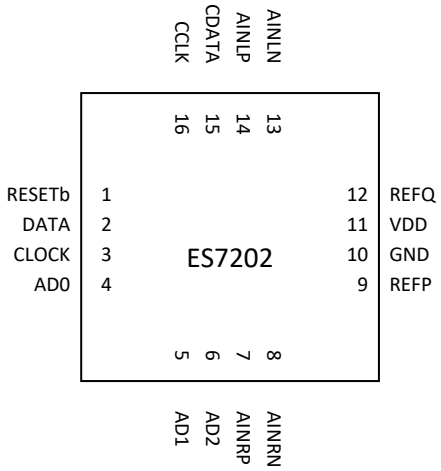
ORDERING INFORMATION

ES7202 -40°C ~ +85°C
QFN-16

BLOCK DIAGRAM



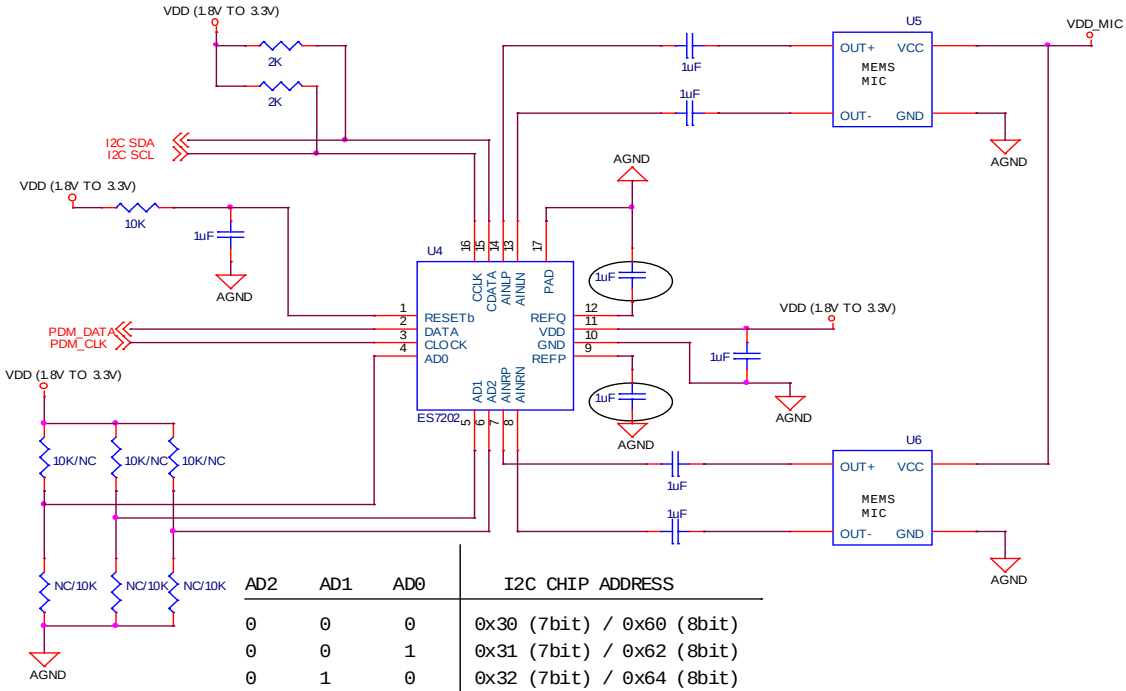
1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA	16, 15	I/O	I^2C clock and data
AD0, AD1, AD2	4, 5, 6	I	I^2C addresses
CLOCK, DATA	3, 2	I, O	PDM clock and data
RESETb	1	I	Active low reset
AINLP, AINLN AINRP, AINRN	14, 13 7, 8	I I	Analog left inputs Analog right inputs
VDD, GND	11, 10	I	Power supply
REFP	9	O	Filtering capacitor connection
REFQ	12	O	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT

The filter capacitors on REFP and REFQ pins must be located as close to ES7202 package as possible.
4.7uF or 10uF capacitor is for better audio performance.



AD2	AD1	AD0	I2C CHIP ADDRESS
0	0	0	0x30 (7bit) / 0x60 (8bit)
0	0	1	0x31 (7bit) / 0x62 (8bit)
0	1	0	0x32 (7bit) / 0x64 (8bit)
0	1	1	0x33 (7bit) / 0x66 (8bit)
1	0	0	0x34 (7bit) / 0x68 (8bit)
1	0	1	0x35 (7bit) / 0x6a (8bit)
1	1	0	0x36 (7bit) / 0x6c (8bit)
1	1	1	0x37 (7bit) / 0x6e (8bit)

3. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0110 x, where x equals AD2 AD1 AD0. The RW bit indicates the slave data transfer direction. Once an

acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a "stop" signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of "write" and "read" instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0010 AD2 AD1 AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

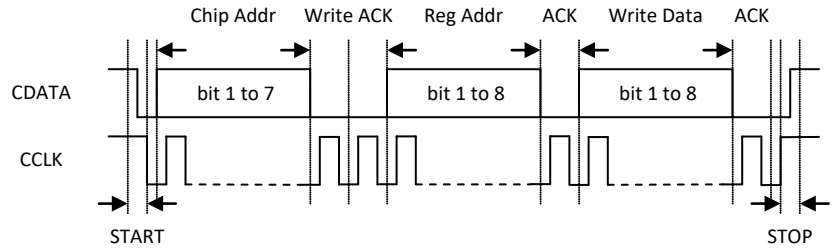


Figure 1a I^2C Write Timing

Table 2 Read Data from Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		
Start	0010 AD2 AD1 AD0	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0010 AD2 AD1 AD0	1	ACK	Data	NACK	Stop

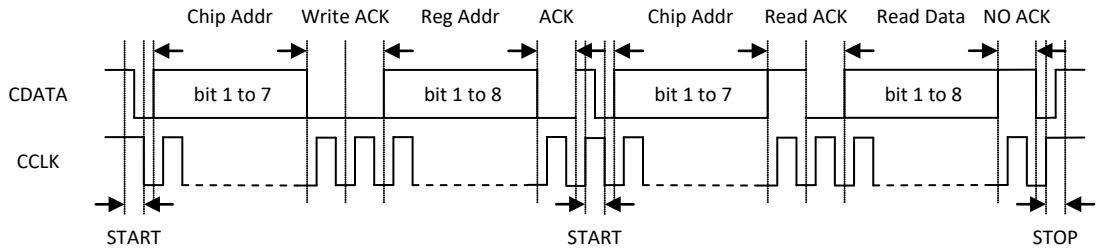


Figure 1b I^2C Read Timing

4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	GND-0.3V	VDD+0.3V
Digital Input Voltage Range	GND-0.3V	VDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDD	1.7	1.8/3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDD=3.3V, GND=0V, ambient temperature=25°C, CLOCK=6.144 MHz.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh, 0 dB PGA)	95	100	103	dB
THD+N (0 dB PGA)	-88	-85	-80	dB
Channel Separation (1KHz)	95	100	105	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Analog Input				
Full Scale Input Level		1.0*VDD/3.3		Vrms
ES7202 Input Impedance		19.2 (0 dB PGA)		KΩ

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDD=3.3V (16 kHz) VDD=1.8V (16 kHz)		22 4.6		mW
Power Down Mode		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*VDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		VDD		V
Output Low-level Voltage		0		V

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

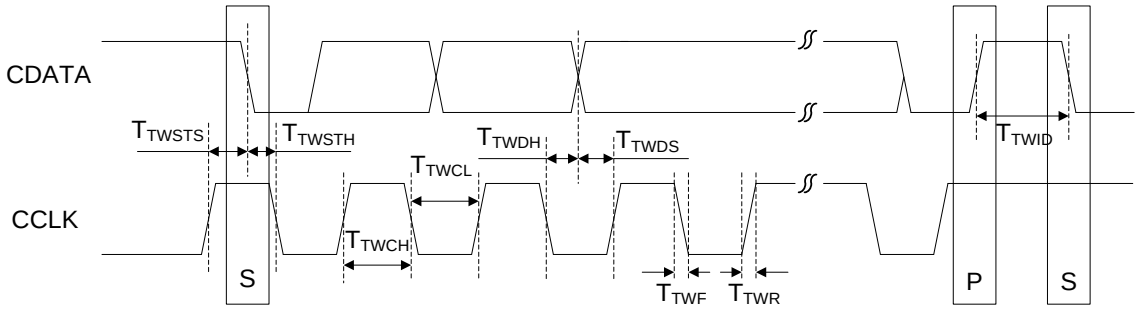


Figure 2 I²C Timing

PDM DATA SWITCHING SPECIFICATIONS

PARAMETER		Symbol	MIN	MAX	UNIT
CLOCK frequency			0.512	6.144	MHz
CLOCK duty cycle	< 3.072 MHz		40 45	60 55	%
DATA valid	VDDD=3.3V VDDD=1.8V	T_{VALID}	11 19	27 61	ns
DATA hold	VDDD=3.3V VDDD=1.8V	T_{HOLD}	10 18	26 56	ns

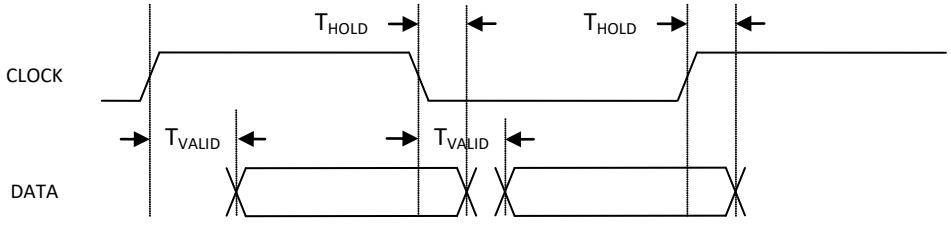


Figure 3 PDM Data Timing

5. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 –RESET CONTROL, DEFAULT 00010000

Bit Name	Bit	Description
Reserved	7:6	Reserved
RST_REGS	5	0–normal 1–reset control registers (except this bit)
RST_DIG	4	0–normal 1–reset digital (except control registers)
Reserved	3:2	Reserved
SEQ_DIS	1	Auto power sequence 0–enable 1–disable
CSM_ON	0	Chip state machine power down 0–disable 1–enable

REGISTER 0X01 – MODE CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:1	Reserved
SOFT_MODE_SEL	0	software mode/hardware mode select 0 – hardware mode 1 – software mode

REGISTER 0X02 – CLOCK DIVIDE, DEFAULT 00000100

Bit Name	Bit	Description
Reserved	7:4	Reserved
MCLK_DIV	3:0	clock divide 0/1 – divide by 16 2 – divide by 32 3 – divide by 48 4 – divide by 64 .... 15 – divide by 240

REGISTER 0X03 – CLOCK OFF, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:6	Reserved
MCLK_INVERT	2	0 – normal 1 – invert master clock
ANA_CLK_ON	1	0 – turn off ADC analog clock 1 – turn on ADC analog clock
MCLK_ON	0	0 – turn off master clock 1 – turn on master clock

REGISTER 0X04 – TIME CONTROL 1 FOR VMID CHARGE, DEFAULT 00000001

Bit Name	Bit	Description
VMID_T1	7:0	time control for VMID charging: Period=(VMID_T1[7:1]*128

		+VMID_T1[0]*2)*0.02ms(LRCK=48K)

REGISTER 0X05 – TIME CONTROL 2 FOR VMID CHARGE, DEFAULT 00011000

Bit Name	Bit	Description
VMID_T2	7:0	time control for VMID charging: Period=(VMID_T2[7:1]*128 +VMID_T2[0]*2)*0.02ms(LRCK=48K)

REGISTER 0X06 – CHIP STATUS, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:6	Reserved
CSM_STATE	5:4	Chip state machine state 00 – S0 01 – S1 10 – S2 11 – S3
Reserved	3	Reserved
FORCE_CSM	2:0	Force chip state machine 100 – force to S0 101 – force to S1 110 – force to S2 111 – force to S3 Other – no force

REGISTER 0X07 – PDM INTERFACE CONTRL, DEFAULT 00110000

Bit Name	Bit	Description
Reserved	7:6	Reserved
NEG_DATA_VALID	5	0–high-z negedge DATA of CLK 1–normal
POS_DATA_VALID	4	0–high-z posedge DATA of CLK 1–normal
PDM_CHN_CROSS	3	0–DATA1 at posedge of CLK, DATA2 at negedge of CLK 1– DATA1 at negedge of CLK, DATA2 at posedge of CLK
PDM_IF_DLY	2	PDM output delay select 0–normal delay 1–longer delay
PDM_DATA2_MUTE	1	0 – normal 1 – mute pdm output of DATA2
PDM_DATA1_MUTE	0	0 – normal 1 – mute pdm output of DATA1

REGISTER 0X08 –MISC CONTROL, DEFAULT 00000010

Bit Name	Bit	Description
Reserved	7:3	Reserved
CLKDET_RST_DIS	2	0 – will not reset system when master clock is off 1 – reset system when master clock is off
DSM_DITHER_ON	1	0 – open dsm dither 1 – close dsm dither
PDN_CLKDET	0	0 – normal 1 – power down clock detector

REGISTER 0X10 – ANALOG SYSTEM, DEFAULT 11111111

Bit Name	Bit	Description
PDN_ANA	7	0 – normal 1 – analog power down
PDN_ADCVREFGEN	6	0 – normal 1 – MIC1/MIC2 reference power down
MODTOP1_RST	5	0 – normal 1 – reset ADC1 state machine to power down state
MODTOP2_RST	4	0 – normal 1 – reset ADC2 state machine to power down state
PDN_MOD1	3	0 – normal 1 – ADC1 power down
PDN_MOD2	2	0 – normal 1 – ADC2 power down
PDN_PGA1	1	0 – normal 1 – PGA1 power down
PDN_PGA2	0	0 – normal 1 – PGA2 power down

REGISTER 0X11 – ANALOG SYSTEM, DEFAULT 00001100

Bit Name	Bit	Description
ADCBIAS_SWH0	7:6	Setting for 1.8v 00 – level0 01 – level1 10 – level2 11 – level3
ENDITHER	5	0 – close DSM dither 1 – open DSM dither
Reserved	4	Reserved
ADCBIAS_SWH1	3:2	00 – level0 01– level1 10 – level2 11– level3
VMIDSEL	1:0	0 – disable 1 – 50k ohm 2 – 500k ohm 3 – 5k ohm

REGISTER 0X12 – ANALOG SYSTEM, DEFAULT 01010101

Bit Name	Bit	Description
PGA1BIAS_SW0	7:4	Setting for 1.8v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9

		1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
PGA1BIAS_SW1	3:0	Setting for 3.3v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X13 – ANALOG SYSTEM, DEFAULT 01010101

Bit Name	Bit	Description
PGA2BIAS_SW0	7:4	Setting for 1.8v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
PGA2BIAS_SW1	3:0	Setting for 3.3v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7

		1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X14 – ANALOG SYSTEM, DEFAULT 10001100

Bit Name	Bit	Description
MODI1BIAS_SW0	7:4	Setting for 1.8v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
MODI1BIAS_SW1	3:0	Setting for 3.3v

REGISTER 0X15 – ANALOG SYSTEM, DEFAULT 00110011

Bit Name	Bit	Description
MODI2BIAS_SW0	7:4	Setting for 1.8v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
MODI2BIAS_SW1	3:0	Setting for 3.3v 0000 – not allowed

		0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X16 – ANALOG SYSTEM, DEFAULT 00110011

Bit Name	Bit	Description
VREFPBIAS_SW0	7:4	Setting for 1.8v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
VREFPBIAS_SW1	3:0	Setting for 3.3v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X17 – ANALOG SYSTEM, DEFAULT 00110011

Bit Name	Bit	Description
VMMODBIAS_SW0	7:4	Setting for 1.8v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
VMMODBIAS_SW1	3:0	Setting for 3.3v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X18 – ANALOG SYSTEM, DEFAULT 01000100

Bit Name	Bit	Description
MODSBIAS_SW0	7:4	Setting for 1.8v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11

		1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
MODSBIAS_SW1	3:0	Setting for 3.3v 0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X19 – ANALOG SYSTEM, DEFAULT 00000000

Bit Name	Bit	Description
LP_VRP	7	0 – normal 1 – low power
LP_VRPOUT	6	0 – normal 1 – low power
LP_VMMOD1	5	0 – normal 1 – low power
LP_VMMOD2	4	0 – normal 1 – low power
LP_MODS1	3	0 – normal 1 – low power
LP_MODS2	2	0 – normal 1 – low power
LP_MODI1	1	0 – normal 1 – low power
LP_MODI2	0	0 – normal 1 – low power

REGISTER 0X1A – ANALOG SYSTEM, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:6	Reserved
LP_PGA1	5	0 – normal 1 – low power
LP_PGA2	4	0 – normal 1 – low power
PDN_DETCT	3	0 – normal 1 – pdn
Reserved	2:0	Reserved

REGISTER 0X1B – ANALOG SYSTEM, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7	Reserved
OFFSETSEL1	6	0 – no offset 1 – offset enabled
OFFSETSEL0	5	0 – no offset 1 – offset enabled
SUPPLYSEL	4	0 – 1.8v voltage 1 – 3.3v voltage
Reserved	3	Reserved
DITHERSEL	2:0	000 – level0 dither 001 – level1 dither 011 – level2 dither 111 – level3 dither

REGISTER 0X1C – ANALOG SYSTEM, DEFAULT 11111000

Bit Name	Bit	Description
VX2OFF_SW0	7	Setting for 1.8v 0 – enable internal reference voltage VX2 1 – off
VX1SEL_SW0	6	0 – vx1=1.45v 1 – vx1=1.65v(default)
VMIDLOW_SW0	5:4	0 – vmid='vdda/2' 1 – vmid1 2 – vmid2 3 – vmid3
VX2OFF_SW1	3	Setting for 3.3v 0 – enable internal reference voltage VX2 1 – off(default)
VX1SEL_SW1	2	Setting for 3.3v 0 – vx1=1.45v 1 – vx1=1.65v
VMIDLOW_SW1	1:0	0 – vmid='vdda/2' 1 – vmid1 2 – vmid2 3 – vmid3

REGISTER 0X1D – ANALOG SYSTEM, DEFAULT 00011000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC1	4	0 – deselect 1 – select MIC1P and MIC1N as input
MIC1GAIN_SETTING	3:0	0 – 0 dB 1 – 2.25 dB 2 – 5.25 dB 3 – 8.25 dB 4 – 11.25 dB 5 – 14.25 dB 6 – 17.25 dB 7 – 20.25 dB 8 – 23.25 dB

		9 – 26.25 dB 10 – 29.25 dB 11 – 30.75 dB 12 – 32.25 dB

REGISTER 0X1E – ANALOG SYSTEM, DEFAULT 00011000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC2	4	0 – deselect 1 – select MIC2P and MIC2N as input
MIC2GAIN_SETTING	3:0	0 – 0 dB 1 – 2.25 dB 2 – 5.25 dB 3 – 8.25 dB 4 – 11.25 dB 5 – 14.25 dB 6 – 17.25 dB 7 – 20.25 dB 8 – 23.25 dB 9 – 26.25 dB 10 – 29.25 dB 11 – 30.75 dB 12 – 32.25 dB

REGISTER 0XFD – DEVICE ID1, DEFAULT 01110010

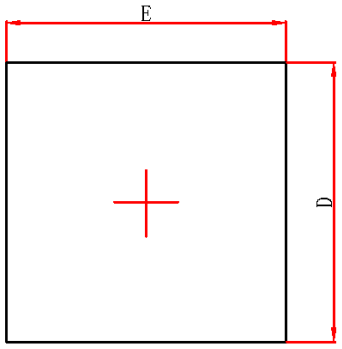
Bit Name	Bit	Description
Device_number_id1	7:0	Device ID

REGISTER 0XFE – DEVICE ID0, DEFAULT 00000001

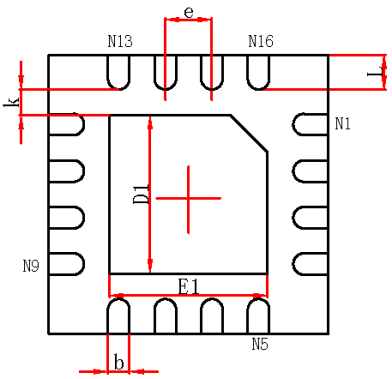
Bit Name	Bit	Description
Device_number_id0	7:0	Device ID

6. PACKAGE

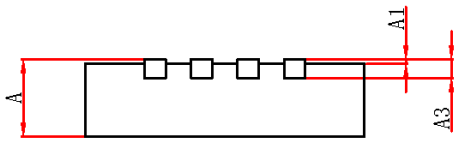
QFNWB3×3-16L(P0.50T0.75) PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.500TYP.	
L	0.300	0.500	0.012	0.020

7. CORPORATE INFORMATION

Everest Semiconductor Co., Ltd.

No. 1355 Jinjihu Drive, Suzhou Industrial Park, Jiangsu, P.R. China, Zip Code 215021

苏州工业园区金鸡湖大道 1355 号国际科技园, 邮编 215021

Email: info@everest-semi.com