

Schematic for Learn

Main Functions Introduction

- 1)PMIC: RK809-5+DiscretePower
- 2)RAM: DDR4 2x16Bit
- 3)ROM: eMMC
- 4)Support:1 x Micro SD Card
- 5)Support:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1
- 6)Support:1 x USB2.0 HOST2+ 1 x USB2.0 HOST3
- 7)Support:1 x HDMI2.0 TX
- 8)Support:a/b/g/n/ac 2X2 SDIO WIFI5
- 9)Support:1 x 10/100/1000 Ethernet(RGMII0)
- 10)Support:1 x 10/100/1000 Ethernet(RGMII1)
- 11)Support:Reset,Power on/off Key
- 12)Support: Debug UART
- 13)Support: 1 x Power LED,1 x CPU LED,1 x GPU LED,1 x NPU LED

项目名称	Learn		
电路名称	-00.Cover Page		
纸张大小	A4	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	1

Table of Content

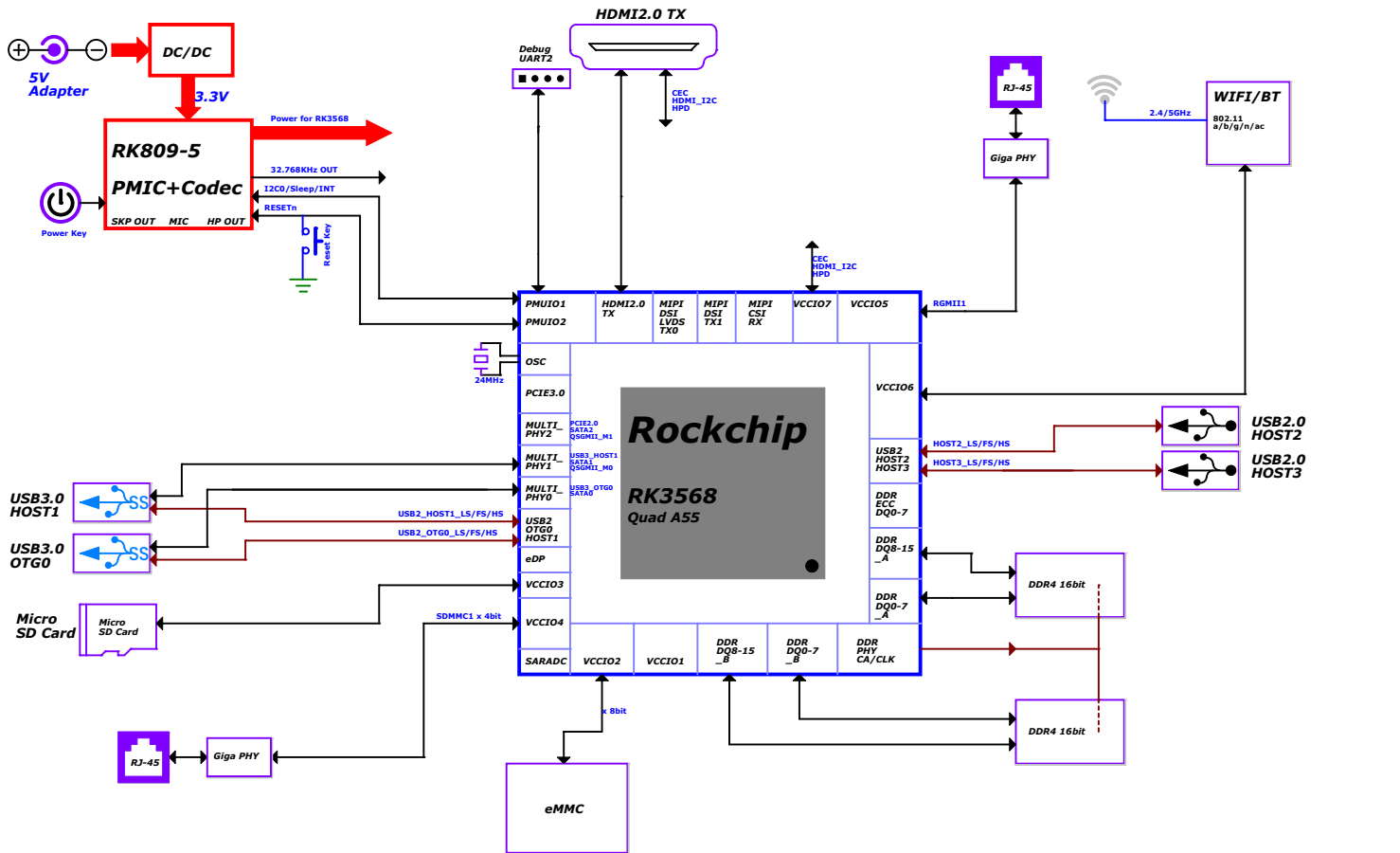
Page 1	-00.Cover Page	Default
Page 2	-01.Index	Default
Page 3	-02.Revision History	Default
Page 4	-03.Block Diagram	Default
Page 5	-04.Power Diagram	Default
Page 6	-05.Power Sequence/IO Domain Map	Default
Page 7	01.POWER_IN	Default
Page 8	02.POWER_PMIC	Default
Page 9	03.POWER_SOC	Default
Page 10	04.SOC_DDR_PHY	Default
Page 11	05.DDR4	Default
Page 12	06.SOC_OSC/PMU/SYSPLL	Default
Page 13	07.SOC_OTP_IO	Default
Page 14	08.SOC_EMMC/Flash_IO	Default
Page 15	09.EMMC	Default
Page 16	10.SOC_SDMMC_IO	Default
Page 17	11.SD_Card	Default
Page 18	12.SOC_ETH0_IO	Default
Page 19	13.ETH0_RTL8211_PHY	Default
Page 20	14.SOC_ETH1_IO	Default
Page 21	15.ETH1_RTL8211_PHY	Default
Page 22	16.SOC_SDIO_WiFi_IO	Default
Page 23	17.WIFI_RTL8821CS	Default
Page 24	18.SOC_HDMI_IO	Default
Page 25	19.HDMI_TX_PHY	Default
Page 26	20.SOC_USB_IO	Default
Page 27	21.USB2/3_PHY	Default
Page 28	22.UART/LED/Key_PHY	Default
Page 29	23.NOT_IO	Default
Page 30		
Page 31		

项目名称	<Title>		
电路名称	-01.Index		
纸张大小	A4	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	2

Revision History

Version	Date	Change Dscription	Approved
V1.0	Tuesday, August 06, 2024	1:Revision preliminary version	
V1.1	Tuesday,September 08, 2024	1:Modify the matching resistors of ETH0 and ETH1 2:Modify the NET naming of ETH0 and ETH1	

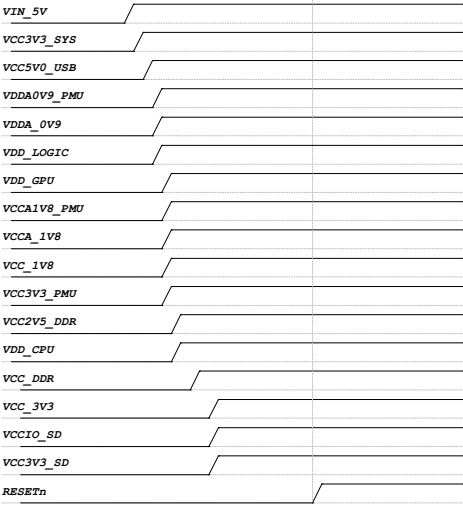
项目名称	<Title>		
电路名称	-02.Revision History		
纸张大小	A4	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	3



Rev: 0.0	<Title>		
Rev: 0.0	<03 Block Diagram		
Rev: 0.0	A2	0.0	120
Rev: 0.0	Project: Project 00_000	Rev: 0.0	Rev: 0.0
Rev: 0.0	Rev: 0.0	Rev: 0.0	Rev: 0.0

项目名称	<Title>		
电路名称	-04.Power Diagram		
纸张大小	A2	份数	T2H
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	5

Power Sequence



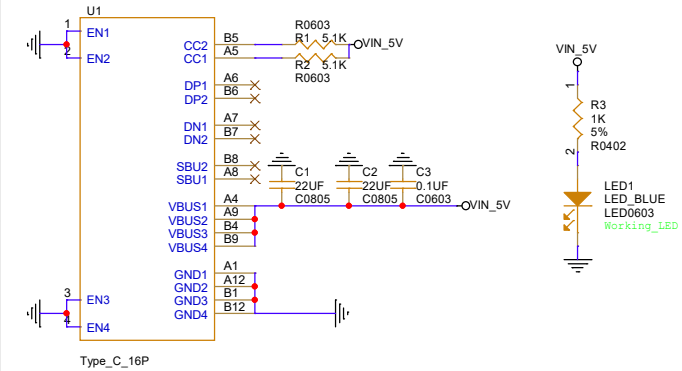
Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (VCCIO_FLASH)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETh			Slot:4+5					
VIN_5V	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

Default IO Power Domain Map

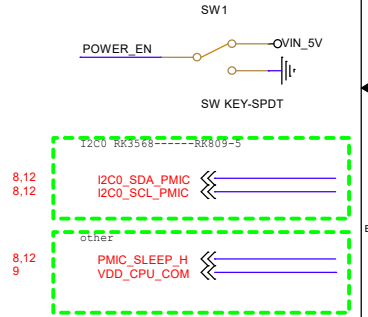
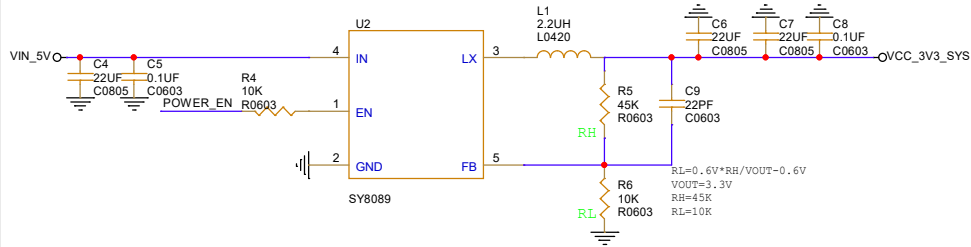
IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V, FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	3.3V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin P9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

项目名称	<Title>		
电路名称	-05.Power Sequence/IO Domain		
纸张大小	A3	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remark>		页码 6

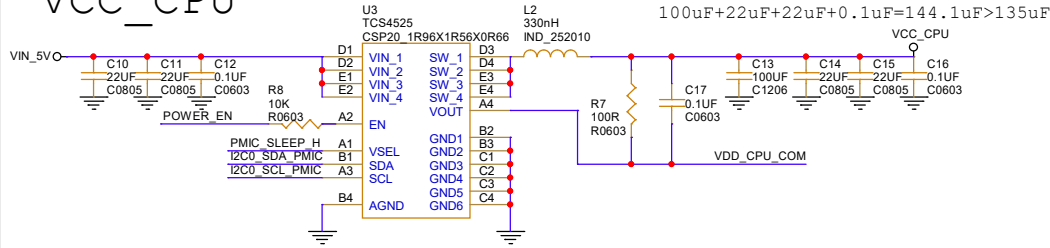
POWER IN



VCC3V3_SYS

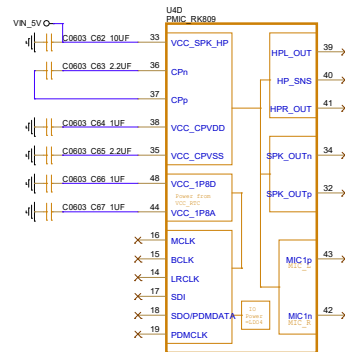
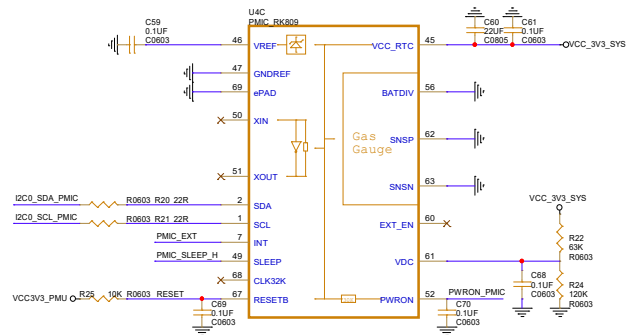
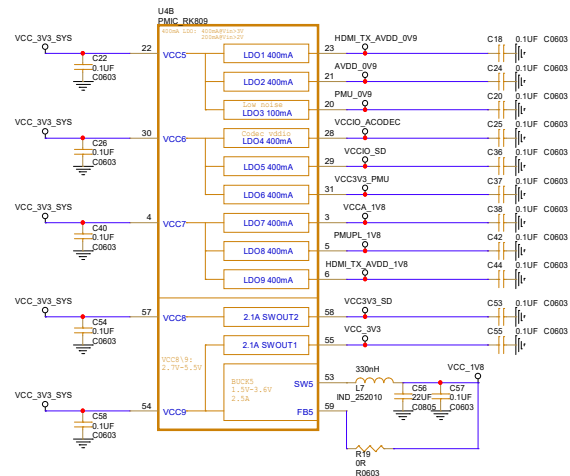
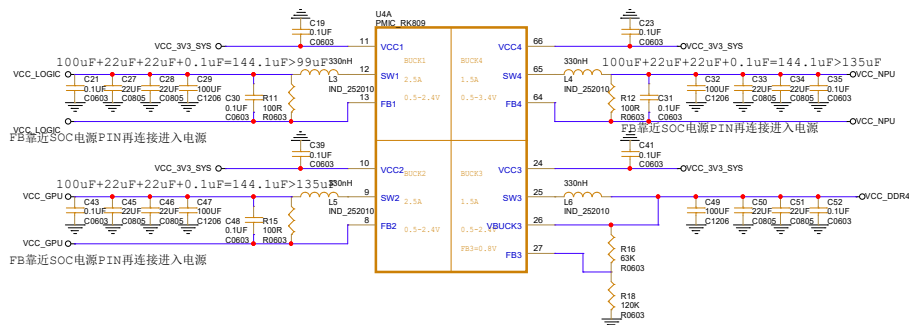


VCC_CPU



项目名称	<Title>		
电路名称	01.POWER_IN		
纸张大小	A4	作者	TZH
绘制时间	Saturday, June 22, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>		

PMIC RK809-5



PMIC_EXT
RESETR
PMIC_SLEEP_H
PWRON PMIC

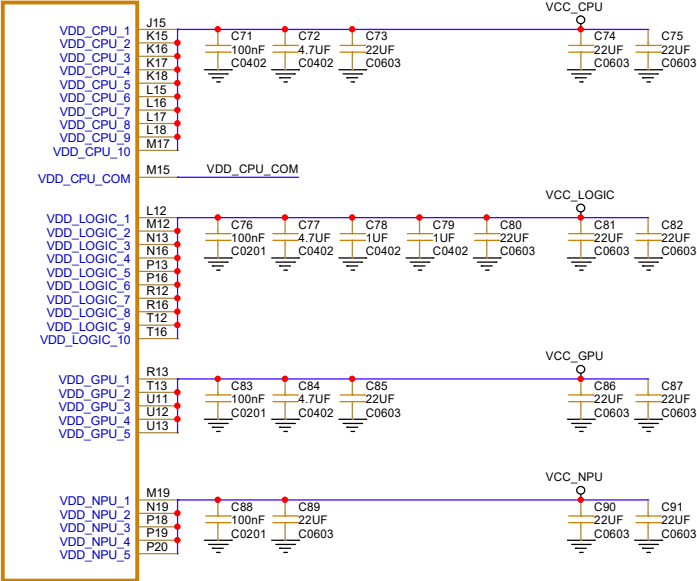
I2C0_RK3568-----RK809-5

I2C0_SDA_PMIC 

I2C0_SCL_PMIC 

项目名称	<Title>		
电路名称	02.POWER_PMIC		
纸张大小	A3	作者	TZH
绘制时间	Tuesday, July 09, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	8

POWER SOC



U5A
SOC_RK3568
BGA636_1

U5B
SOC_RK3568
BGA636_1

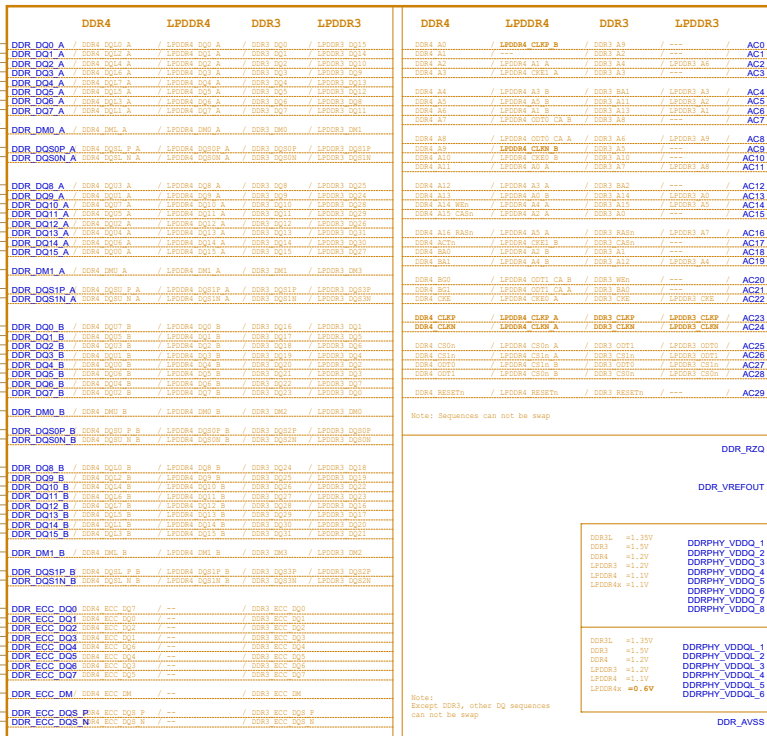
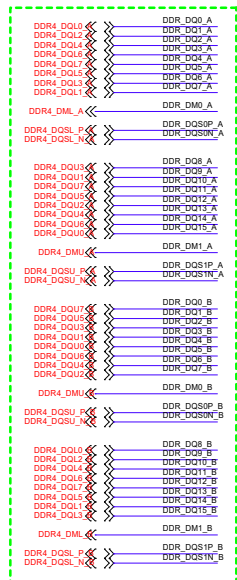
U5C
SOC_RK3568
BGA636_1

U5E
SOC_RK3568
BGA636_1

U5D
SOC_RK3568
BGA636_1

项目名称	<Title>		
电路名称	03.POWER_SOC		
纸张大小	A4	作者	TZH
绘制时间	Thursday, July 11, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>		页码 9

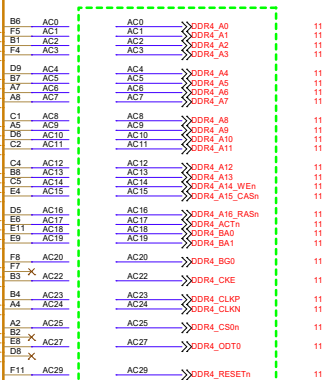
DDR4 DQ



Note: Sequences can not be swap

Note:
Except DQ03, other DQ sequences
can not be swap

DDR4 AC



DDR_RZQ

DDR_VREFOUT

DDRPHY_VDD0_1

DDRPHY_VDD0_2

DDRPHY_VDD0_3

DDRPHY_VDD0_4

DDRPHY_VDD0_5

DDRPHY_VDD0_6

DDRPHY_VDD0_7

DDRPHY_VDD0_8

DDRPHY_VDD0_9

DDRPHY_VDD0_10

DDRPHY_VDD0_11

DDRPHY_VDD0_12

DDRPHY_VDD0_13

DDRPHY_VDD0_14

DDRPHY_VDD0_15

DDRPHY_VDD0_16

DDRPHY_VDD0_17

DDRPHY_VDD0_18

DDRPHY_VDD0_19

DDRPHY_VDD0_20

DDRPHY_VDD0_21

DDRPHY_VDD0_22

DDRPHY_VDD0_23

DDRPHY_VDD0_24

DDRPHY_VDD0_25

DDRPHY_VDD0_26

DDRPHY_VDD0_27

DDRPHY_VDD0_28

DDRPHY_VDD0_29

DDRPHY_VDD0_30

DDRPHY_VDD0_31

DDRPHY_VDD0_32

DDRPHY_VDD0_33

DDRPHY_VDD0_34

DDRPHY_VDD0_35

DDRPHY_VDD0_36

DDRPHY_VDD0_37

DDRPHY_VDD0_38

DDRPHY_VDD0_39

DDRPHY_VDD0_40

DDRPHY_VDD0_41

DDRPHY_VDD0_42

DDRPHY_VDD0_43

DDRPHY_VDD0_44

DDRPHY_VDD0_45

DDRPHY_VDD0_46

DDRPHY_VDD0_47

DDRPHY_VDD0_48

DDRPHY_VDD0_49

DDRPHY_VDD0_50

DDRPHY_VDD0_51

DDRPHY_VDD0_52

DDRPHY_VDD0_53

DDRPHY_VDD0_54

DDRPHY_VDD0_55

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DDRPHY_VDD0_57

DDRPHY_VDD0_58

DDRPHY_VDD0_59

DDRPHY_VDD0_60

DDRPHY_VDD0_61

DDRPHY_VDD0_62

DDRPHY_VDD0_63

DDRPHY_VDD0_64

DDRPHY_VDD0_65

DDRPHY_VDD0_66

DDRPHY_VDD0_67

DDRPHY_VDD0_68

DDRPHY_VDD0_69

DDRPHY_VDD0_70

DDRPHY_VDD0_71

DDRPHY_VDD0_72

DDRPHY_VDD0_73

DDRPHY_VDD0_74

DDRPHY_VDD0_75

DDRPHY_VDD0_76

DDRPHY_VDD0_77

DDRPHY_VDD0_78

DDRPHY_VDD0_79

DDRPHY_VDD0_80

DDRPHY_VDD0_81

DDRPHY_VDD0_82

DDRPHY_VDD0_83

DDRPHY_VDD0_84

DDRPHY_VDD0_85

DDRPHY_VDD0_86

DDRPHY_VDD0_87

DDRPHY_VDD0_88

DDRPHY_VDD0_89

DDRPHY_VDD0_90

DDRPHY_VDD0_91

DDRPHY_VDD0_92

DDRPHY_VDD0_93

DDRPHY_VDD0_94

DDRPHY_VDD0_95

DDRPHY_VDD0_96

DDRPHY_VDD0_97

DDRPHY_VDD0_98

DDRPHY_VDD0_99

DDRPHY_VDD0_100

DDRPHY_VDD0_101

DDRPHY_VDD0_102

DDRPHY_VDD0_103

DDRPHY_VDD0_104

DDRPHY_VDD0_105

DDRPHY_VDD0_106

DDRPHY_VDD0_107

DDRPHY_VDD0_108

DDRPHY_VDD0_109

DDRPHY_VDD0_110

DDRPHY_VDD0_111

DDRPHY_VDD0_112

DDRPHY_VDD0_113

DDRPHY_VDD0_114

DDRPHY_VDD0_115

DDRPHY_VDD0_116

DDRPHY_VDD0_117

DDRPHY_VDD0_118

DDRPHY_VDD0_119

DDRPHY_VDD0_120

DDRPHY_VDD0_121

DDRPHY_VDD0_122

DDRPHY_VDD0_123

DDRPHY_VDD0_124

DDRPHY_VDD0_125

DDRPHY_VDD0_126

DDRPHY_VDD0_127

DDRPHY_VDD0_128

DDRPHY_VDD0_129

DDRPHY_VDD0_130

DDRPHY_VDD0_131

DDRPHY_VDD0_132

DDRPHY_VDD0_133

DDRPHY_VDD0_134

DDRPHY_VDD0_135

DDRPHY_VDD0_136

DDRPHY_VDD0_137

DDRPHY_VDD0_138

DDRPHY_VDD0_139

DDRPHY_VDD0_140

DDRPHY_VDD0_141

DDRPHY_VDD0_142

DDRPHY_VDD0_143

DDRPHY_VDD0_144

DDRPHY_VDD0_145

DDRPHY_VDD0_146

DDRPHY_VDD0_147

DDRPHY_VDD0_148

DDRPHY_VDD0_149

DDRPHY_VDD0_150

DDRPHY_VDD0_151

DDRPHY_VDD0_152

DDRPHY_VDD0_153

DDRPHY_VDD0_154

DDRPHY_VDD0_155

DDRPHY_VDD0_156

DDRPHY_VDD0_157

DDRPHY_VDD0_158

DDRPHY_VDD0_159

DDRPHY_VDD0_160

DDRPHY_VDD0_161

DDRPHY_VDD0_162

DDRPHY_VDD0_163

DDRPHY_VDD0_164

DDRPHY_VDD0_165

DDRPHY_VDD0_166

DDRPHY_VDD0_167

DDRPHY_VDD0_168

DDRPHY_VDD0_169

DDRPHY_VDD0_170

DDRPHY_VDD0_171

DDRPHY_VDD0_172

DDRPHY_VDD0_173

DDRPHY_VDD0_174

DDRPHY_VDD0_175

DDRPHY_VDD0_176

DDRPHY_VDD0_177

DDRPHY_VDD0_178

DDRPHY_VDD0_179

DDRPHY_VDD0_180

DDRPHY_VDD0_181

DDRPHY_VDD0_182

DDRPHY_VDD0_183

DDRPHY_VDD0_184

DDRPHY_VDD0_185

DDRPHY_VDD0_186

DDRPHY_VDD0_187

DDRPHY_VDD0_188

DDRPHY_VDD0_189

DDRPHY_VDD0_190

DDRPHY_VDD0_191

DDRPHY_VDD0_192

DDRPHY_VDD0_193

DDRPHY_VDD0_194

DDRPHY_VDD0_195

DDRPHY_VDD0_196

DDRPHY_VDD0_197

DDRPHY_VDD0_198

DDRPHY_VDD0_199

DDRPHY_VDD0_200

DDRPHY_VDD0_201

DDRPHY_VDD0_202

DDRPHY_VDD0_203

DDRPHY_VDD0_204

DDRPHY_VDD0_205

DDRPHY_VDD0_206

DDRPHY_VDD0_207

DDRPHY_VDD0_208

DDRPHY_VDD0_209

DDRPHY_VDD0_210

DDRPHY_VDD0_211

DDRPHY_VDD0_212

DDRPHY_VDD0_213

DDRPHY_VDD0_214

DDRPHY_VDD0_215

DDRPHY_VDD0_216

DDRPHY_VDD0_217

DDRPHY_VDD0_218

DDRPHY_VDD0_219

DDRPHY_VDD0_220

DDRPHY_VDD0_221

DDRPHY_VDD0_222

DDRPHY_VDD0_223

DDRPHY_VDD0_224

DDRPHY_VDD0_225

DDRPHY_VDD0_226

DDRPHY_VDD0_227

DDRPHY_VDD0_228

DDRPHY_VDD0_229

DDRPHY_VDD0_230

DDRPHY_VDD0_231

DDRPHY_VDD0_232

DDRPHY_VDD0_233

DDRPHY_VDD0_234

DDRPHY_VDD0_235

DDRPHY_VDD0_236

DDRPHY_VDD0_237

DDRPHY_VDD0_238

DDRPHY_VDD0_239

DDRPHY_VDD0_240

DDRPHY_VDD0_241

DDRPHY_VDD0_242

DDRPHY_VDD0_243

DDRPHY_VDD0_244

DDRPHY_VDD0_245

DDRPHY_VDD0_246

DDRPHY_VDD0_247

DDRPHY_VDD0_248

DDRPHY_VDD0_249

DDRPHY_VDD0_250

DDRPHY_VDD0_251

DDRPHY_VDD0_252

DDRPHY_VDD0_253

DDRPHY_VDD0_254

DDRPHY_VDD0_255

DDRPHY_VDD0_256

DDRPHY_VDD0_257

DDRPHY_VDD0_258

DDRPHY_VDD0_259

DDRPHY_VDD0_260

DDRPHY_VDD0_261

DDRPHY_VDD0_262

DDRPHY_VDD0_263

DDRPHY_VDD0_264

DDRPHY_VDD0_265

DDRPHY_VDD0_266

DDRPHY_VDD0_267

DDRPHY_VDD0_268

DDRPHY_VDD0_269

DDRPHY_VDD0_270

DDRPHY_VDD0_271

DDRPHY_VDD0_272

DDRPHY_VDD0_273

DDRPHY_VDD0_274

DDRPHY_VDD0_275

DDRPHY_VDD0_276

DDRPHY_VDD0_277

DDRPHY_VDD0_278

DDRPHY_VDD0_279

DDRPHY_VDD0_280

DDRPHY_VDD0_281

DDRPHY_VDD0_282

DDRPHY_VDD0_283

DDRPHY_VDD0_284

DDRPHY_VDD0_285

DDRPHY_VDD0_286

DDRPHY_VDD0_287

DDRPHY_VDD0_288

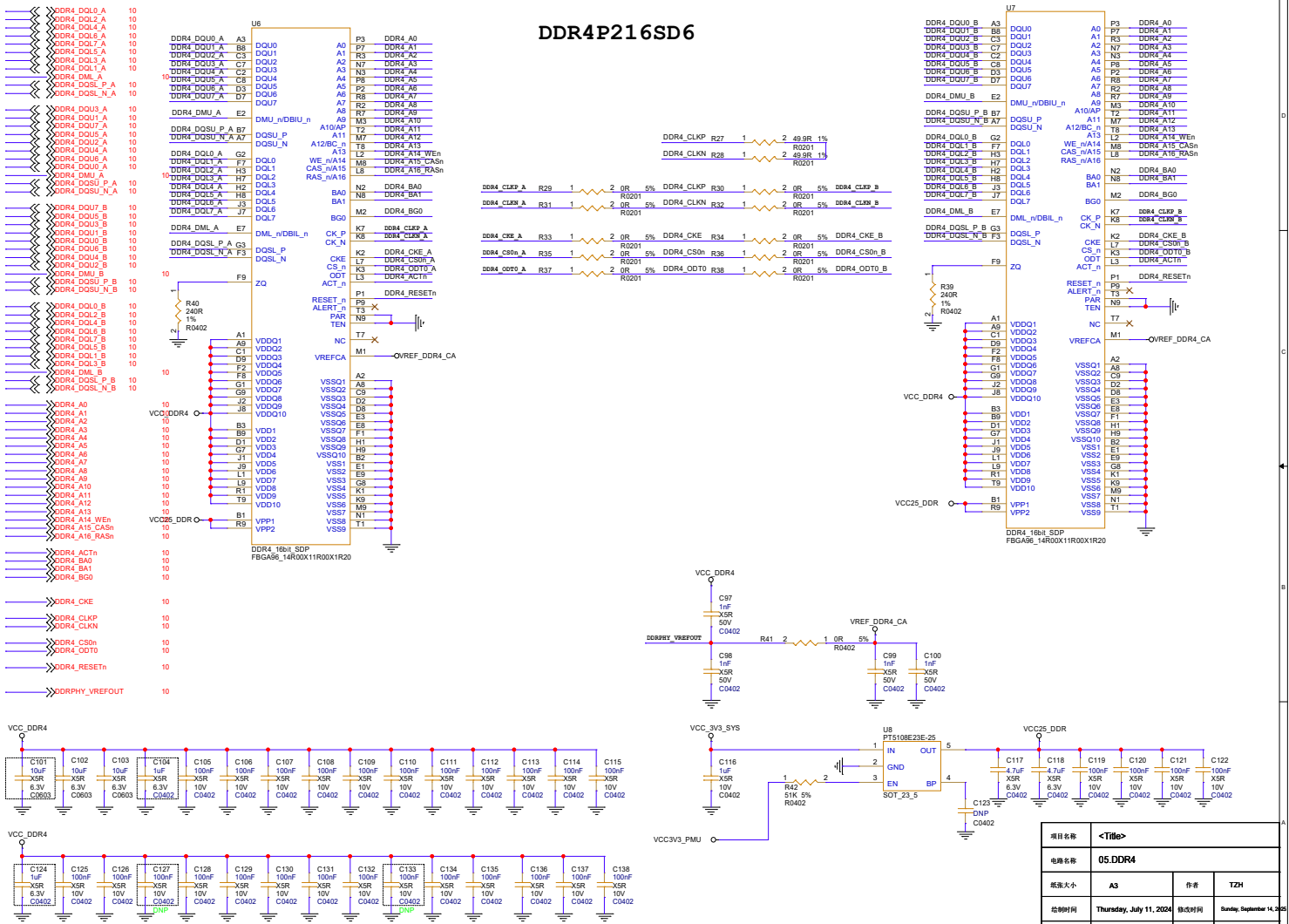
DDRPHY_VDD0_289

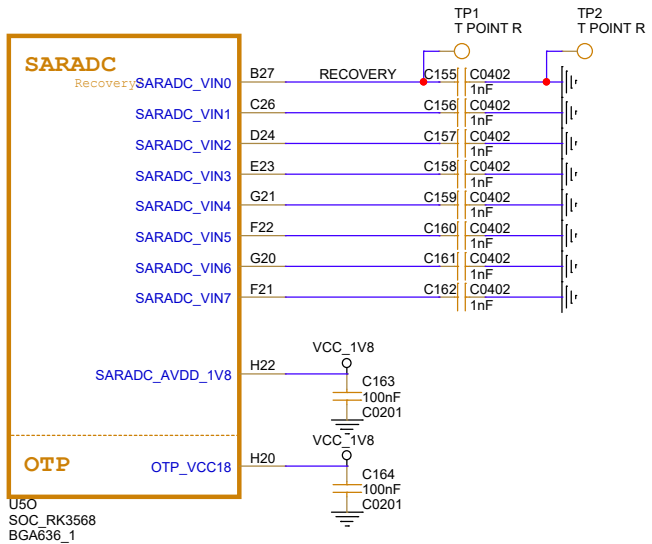
DDRPHY_VDD0_290

DDRPHY_VDD0_291

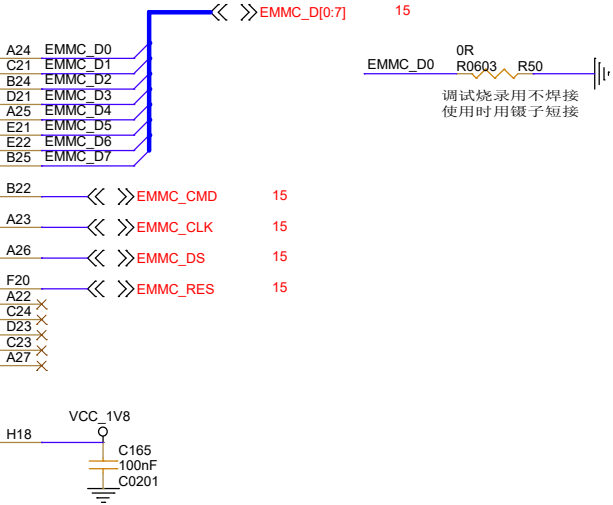
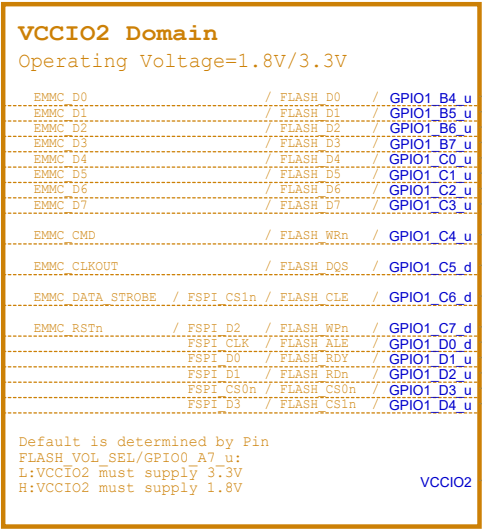
DDRPHY_VDD0_292

DDR4P216SD6

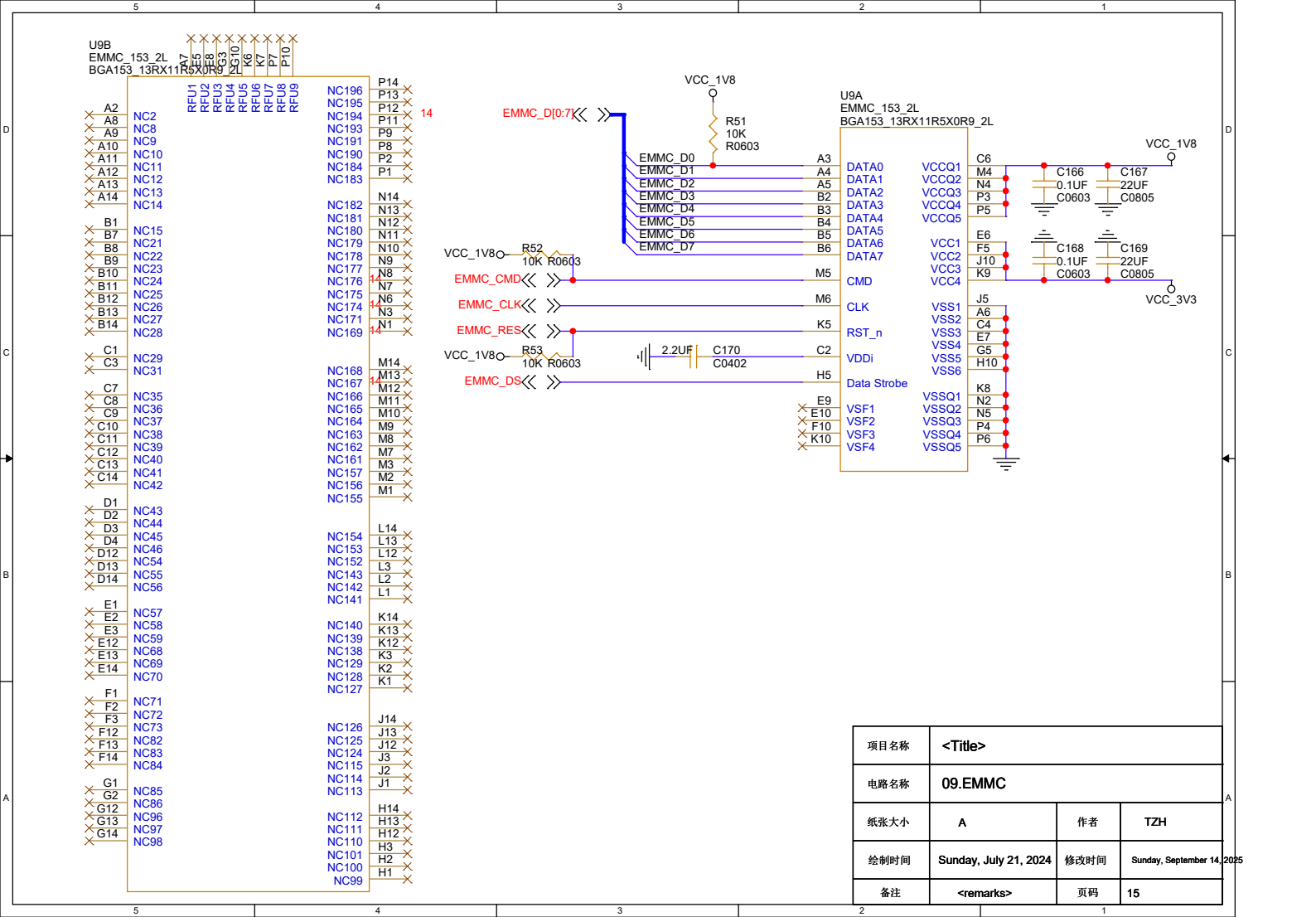




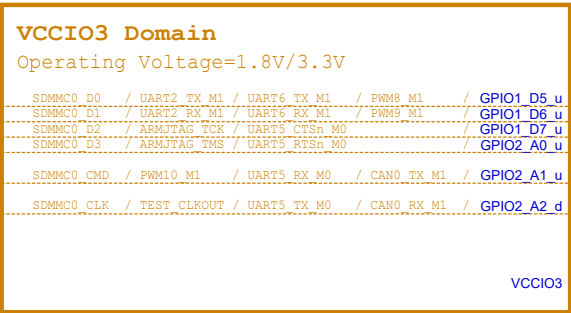
项目名称	<Title>		
电路名称	07.SOC_OTP_IO		
纸张大小	A	作者	TZH
绘制时间	Sunday, July 28, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	13



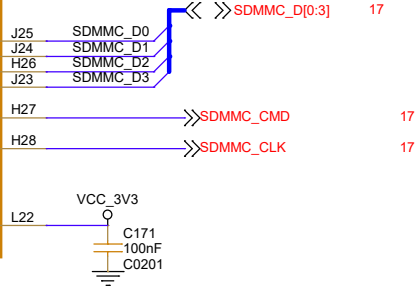
项目名称	<Title>		
电路名称	08.SOC_EMMC/Flash_IO		
纸张大小	A	作者	TZH
绘制时间	Friday, July 12, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	14



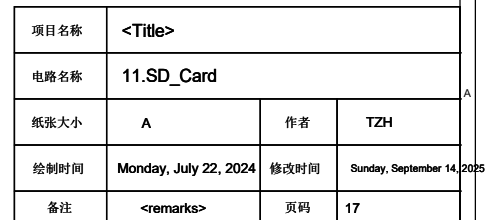
项目名称	<Title>		
电路名称	09.EMMC		
纸张大小	A	作者	TZH
绘制时间	Sunday, July 21, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>		
	页码	15	



U5J
SOC_RK3568
BGA636_1



项目名称	<Title>		
电路名称	10.SOC_SDMMC_IO		
纸张大小	A	作者	TZH
绘制时间	Friday, July 12, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	16



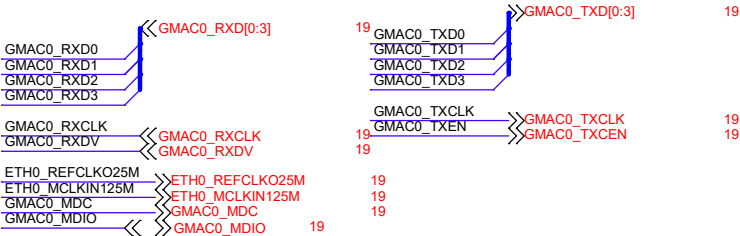
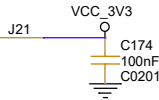
VCCIO4 Domain

Operating Voltage=1.8V/3.3V

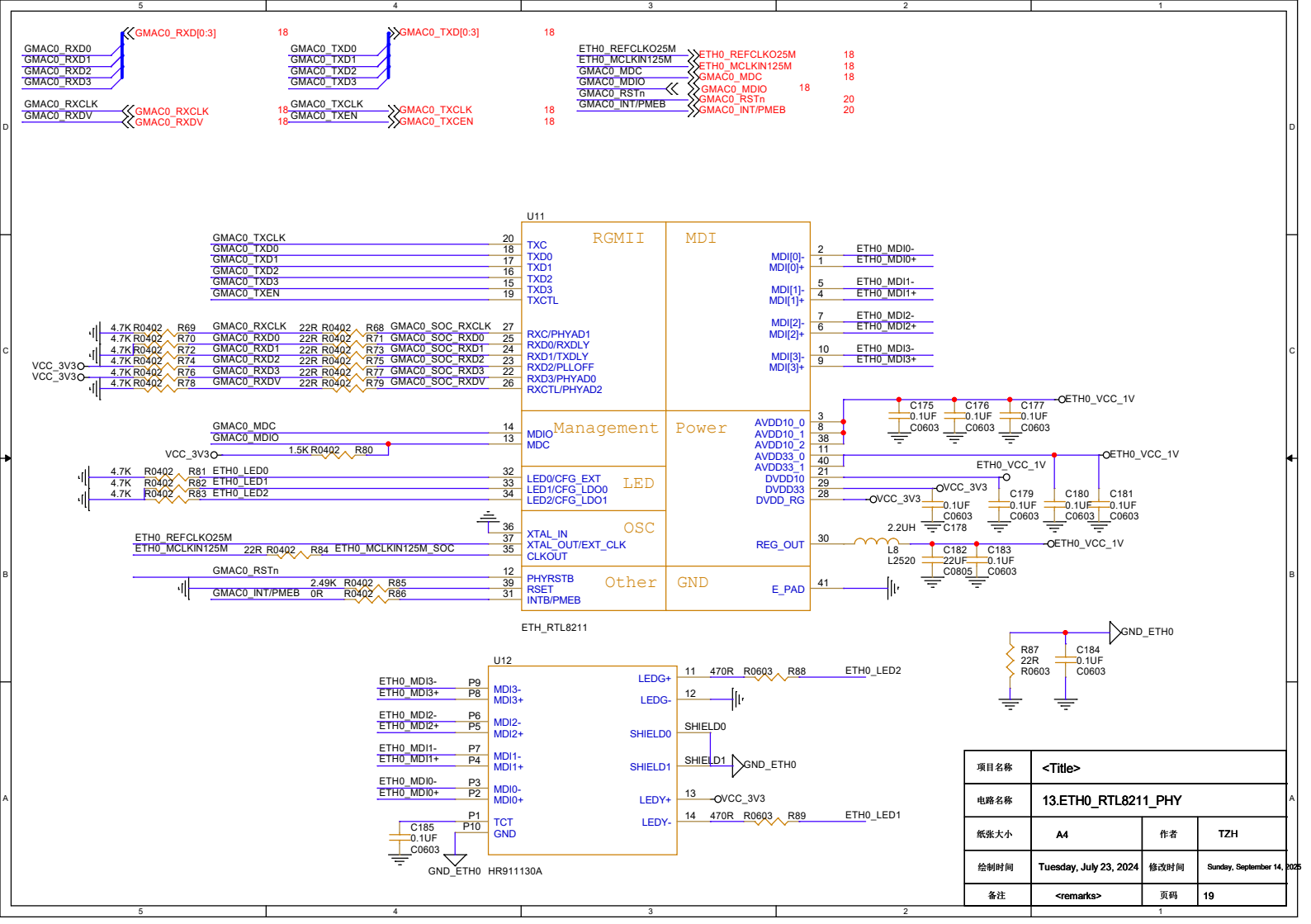
SDMMC1_D0	/	GMAC0_RXD2	/	UART6_RX_M0	/	GPIO2_A3_u
SDMMC1_D1	/	GMAC0_RXD3	/	UART6_TX_M0	/	GPIO2_A4_u
SDMMC1_D2	/	GMAC0_RXCLK	/	UART7_RX_M0	/	GPIO2_A5_u
SDMMC1_D3	/	GMAC0_TXD2	/	UART7_TX_M0	/	GPIO2_A6_u
SDMMC1_CMD	/	GMAC0_TXD3	/	UART9_RX_M0	/	GPIO2_A7_u
SDMMC1_CLK	/	GMAC0_TXCLK	/	UART9_TX_M0	/	GPIO2_B0_d
SDMMC1_PWREN	/	I2C4_SDA_M1	/	UART8_RTSn_M0	/	GPIO2_B1_d
SDMMC1_DET	/	I2C4_SCL_M1	/	UART8_CTSn_M0	/	GPIO2_B2_u
		GMAC0_TXD0	/	UART1_RX_M0	/	GPIO2_B3_u
		GMAC0_TXD1	/	UART1_TX_M0	/	GPIO2_B4_u
		GMAC0_TXEN	/	UART1_RTSn_M0	/	GPIO2_B5_u
		GMAC0_RXD0	/	UART1_CTSn_M0	/	GPIO2_B6_u
I2S2_SCLK_RX_M0	/	GMAC0_RXD1	/	UART6_RTSn_M0	/	GPIO2_B7_d
I2S2_LRCK_RX_M0	/	GMAC0_RXDV CRS	/	UART6_CTSn_M0	/	GPIO2_C0_d
I2S2_MCLK_M0	/	ETH0_REFCLKR0_25M	/	UART7_RTSn_M0	/	GPIO2_C1_d
I2S2_SCLK_TX_M0	/	GMAC0_MCLKINOUT	/	UART7_CTSn_M0	/	GPIO2_C2_d
I2S2_LRCK_TX_M0	/	GMAC0_MDC	/	UART9_RTSn_M0	/	GPIO2_C3_d
I2S2_SDO_M0	/	GMAC0_MDIO	/	UART9_CTSn_M0	/	GPIO2_C4_d
I2S2_SDI_M0	/	GMAC0_RXER	/	UART8_TX_M0	/	GPIO2_C5_d
CLK32K_OUT1	/		/	UART8_RX_M0	/	GPIO2_C6_u

U5K
SOC_RK3568
BGA636_1

E27	GMAC0_RXD2			
E28	GMAC0_RXD3			
B28	GMAC0_RXCLK			
C27	GMAC0_SOC_TXD2	22R R0402	R60	GMAC0_TXD2
C28	GMAC0_SOC_TXD3	22R R0402	R61	GMAC0_TXD3
D27	GMAC0_SOC_TXCLK	22R R0402	R62	GMAC0_TXCLK
D26	>> GMAC0_INT/PMEB			19
E25				
F28	GMAC0_SOC_TXD0	22R R0402	R63	GMAC0_TXD0
G27	GMAC0_SOC_TXD1	22R R0402	R64	GMAC0_TXD1
G28	GMAC0_SOC_TXEN	22R R0402	R65	GMAC0_TXEN
F27	GMAC0_RXD0			
H25	GMAC0_RXD1			
F24	GMAC0_RXDV			
G23	ETH0_REFCLK025M SOC	22R R0402	R66	ETH0_REFCLK025M
F25	ETH0_MCLKIN125M			
H24	GMAC0_SOC_MDC	22R R0402	R67	GMAC0_MDC
H23	GMAC0_MDIO			
F26				
E26				



项目名称	<Title>		
电路名称	12.SOC_ETH0_IO		
纸张大小	A	作者	TZH
绘制时间	Monday, July 22, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	18



VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC D0 / VOP BT656 D0 M0 / SPI0 MISO M1 / PCIE20 CLKREqn M1 / I2S1 MCLK M2 / GPIO2_D0 d
LCDC D1 / VOP BT656 D1 M0 / SPI0 MOSI M1 / PCIE20 WAKEn M1 / I2S1 SCLK TX M2 / GPIO2_D1 d
LCDC D2 / VOP BT656 D2 M0 / SPI0 CS0 M1 / PCIE30X1 CLKREqn M1 / I2S1 LRCK TX M2 / GPIO2_D2 d
LCDC D3 / VOP BT656 D3 M0 / SPI0 CLK M1 / PCIE30X1 WAKEn M1 / I2S1 SDI0 M2 / GPIO2_D3 d
LCDC D4 / VOP BT656 D4 M0 / SPI2 CS1 M1 / PCIE30X2 CLKREqn M1 / I2S1 SDI1 M2 / GPIO2_D4 d
LCDC D5 / VOP BT656 D5 M0 / SPI2 CS0 M1 / PCIE30X2 WAKEn M1 / I2S1 SDI2 M2 / GPIO2_D5 d
LCDC D6 / VOP BT656 D6 M0 / SPI2 MOSI M1 / PCIE30X2 PERStn M1 / I2S1 SDI3 M2 / GPIO2_D6 d
LCDC D7 / VOP BT656 D7 M0 / SPI2 MISO M1 / UART8 TX M1 / I2S1 SDO0 M2 / GPIO2_D7 d

LCDC CLK / VOP BT656 CLK M0 / SPI2 CLK M1 / UART8 RX M1 / I2S1 SDO1 M2 / GPIO3_A0 d

LCDC D8 / VOP BT1120 D0 / SPI1 CS0 M1 / PCIE30X1 PERStn M1 / SDMMC2 D0 M1 / GPIO3_A1 d
LCDC D9 / VOP BT1120 D1 / GMAC1 TXD2 M0 / I2S3 MCLK M0 / SDMMC2 D1 M1 / GPIO3_A2 d
LCDC D10 / VOP BT1120 D2 / GMAC1 TXD3 M0 / I2S3 SCLK M0 / SDMMC2 D2 M1 / GPIO3_A3 d
LCDC D11 / VOP BT1120 D3 / GMAC1 RXD2 M0 / I2S3 LRCK M0 / SDMMC2 D3 M1 / GPIO3_A4 d
LCDC D12 / VOP BT1120 D4 / GMAC1 RXD3 M0 / I2S3 SDO M0 / SDMMC2 CMD M1 / GPIO3_A5 d
LCDC D13 / VOP BT1120 CLK / GMAC1 TXCLK M0 / I2S3 SDI M0 / SDMMC2 CLK M1 / GPIO3_A6 d
LCDC D14 / VOP BT1120 D5 / GMAC1 RXCLK M0 / I2S3 SDI M0 / SDMMC2 DET M1 / GPIO3_A7 d
LCDC D15 / VOP BT1120 D6 / ETH1 REFCLK0 25M M0 / SDMMC2 WAKEn M1 / GPIO3_B0 d

LCDC D16 / VOP BT1120 D7 / GMAC1 RXD0 M0 / UART4 RX M1 / PWM8 M0 / GPIO3_B1 d
LCDC D17 / VOP BT1120 D8 / GMAC1 RXD1 M0 / UART4 TX M1 / PWM9 M0 / GPIO3_B2 d
LCDC D18 / VOP BT1120 D9 / GMAC1 RXDV CRS M0 / I2C5 SCL M0 / PDM SDI0 M2 / GPIO3_B3 d
LCDC D19 / VOP BT1120 D10 / GMAC1 RXER M0 / I2C5 SDA M0 / PDM SDI1 M2 / GPIO3_B4 d
LCDC D20 / VOP BT1120 D11 / GMAC1 TXD0 M0 / I2C3 SCL M1 / PWM10 M0 / GPIO3_B5 d
LCDC D21 / VOP BT1120 D12 / GMAC1 TXD1 M0 / I2C3 SDA M1 / PWM11 IR M0 / GPIO3_B6 d
LCDC D22 / PWM12 M0 / GMAC1 TXEN M0 / UART3 TX M1 / PDM SDI2 M2 / GPIO3_B7 d
LCDC D23 / PWM13 M0 / GMAC1 MCLKINOUT M0 / UART3 RX M1 / PDM SDI3 M2 / GPIO3_C0 d

LCDC HSYNC / VOP BT1120 D13 / SPI1 MOSI M1 / PCIE20 PERStn M1 / I2S1 SDO2 M2 / GPIO3_C1 d
LCDC VSYNC / VOP BT1120 D14 / SPI1 MISO M1 / UART5 TX M1 / I2S1 SDO3 M2 / GPIO3_C2 d
LCDC DEN / VOP BT1120 D15 / SPI1 CLK M1 / UART5 RX M1 / I2S1 SCLK RX M2 / GPIO3_C3 d

PWM14 M0 / VOP PWM M1 / GMAC1 MDC M0 / UART7 TX M1 / PDM CLK1 M2 / GPIO3_C4 d
PWM15 IR M0 / SPDIF TX M1 / GMAC1 MDIO M0 / UART7 RX M1 / I2S1 LRCK RX M2 / GPIO3_C5 d

VCCIO5_1
VCCIO5_2

AG6
AD7
AC8
AC7
AF5
AF6
AD6
AH5

AH4

AB8

AE5

AG4

AF4

AG3

AG3

AH2

AG2

AG1

AF2

AF1

AE2

AE3

AD4

AD2

AD1

AA7

AC4

AC3

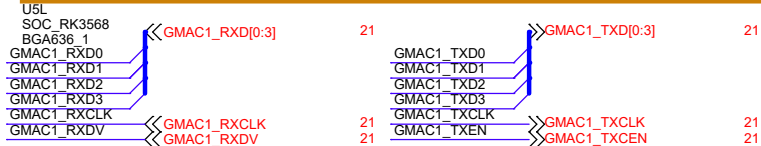
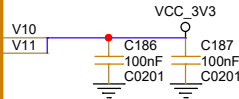
AC2

GMAC1_SOC_TXD2 22R R0402 R90 GMAC1_TXD2
GMAC1_SOC_TXD3 22R R0402 R91 GMAC1_TXD3
GMAC1_TXD2
GMAC1_RXD3
GMAC1_TXCLK
GMAC1_RXCLK
ETH1_REFCLK025M_SOC 22R R0402 R93 ETH1_REFCLK025M

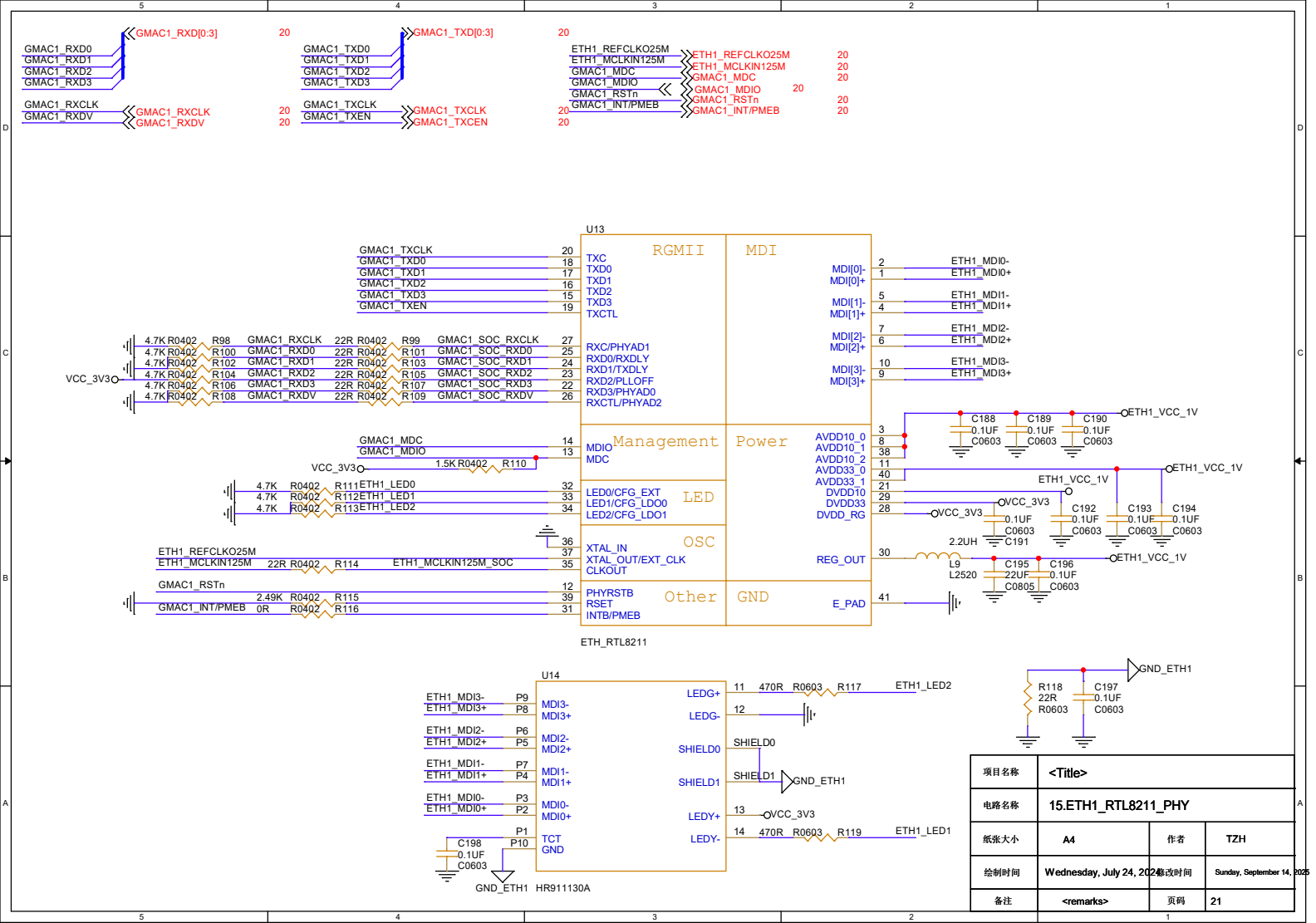
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXDV
GMAC1_SOC_TXD0 22R R0402 R94 GMAC1_TXD0
GMAC1_SOC_TXD1 22R R0402 R95 GMAC1_TXD1
GMAC1_SOC_TXEN 22R R0402 R96 GMAC1_TXEN
ETH1_MCLKIN125M

GMAC1_INT/PMBE
GMAC1_RSTn

GMAC1_SOC_MDC 22R R0402 R97 GMAC1_MDC
GMAC1_MDIO



项目名称	<Title>		
电路名称	14.SOC_ETH1_IO		
纸张大小	A	作者	TZH
绘制时间	Tuesday, July 23, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>		
	页码	20	

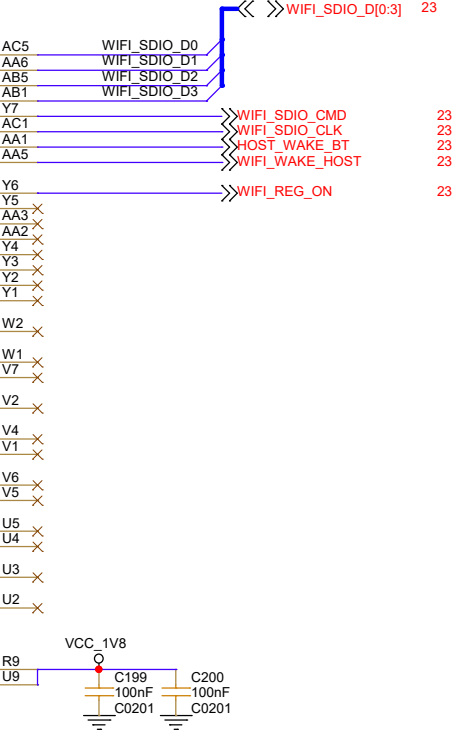


VCCIO6 Domain

Operating Voltage=1.8V/3.3V

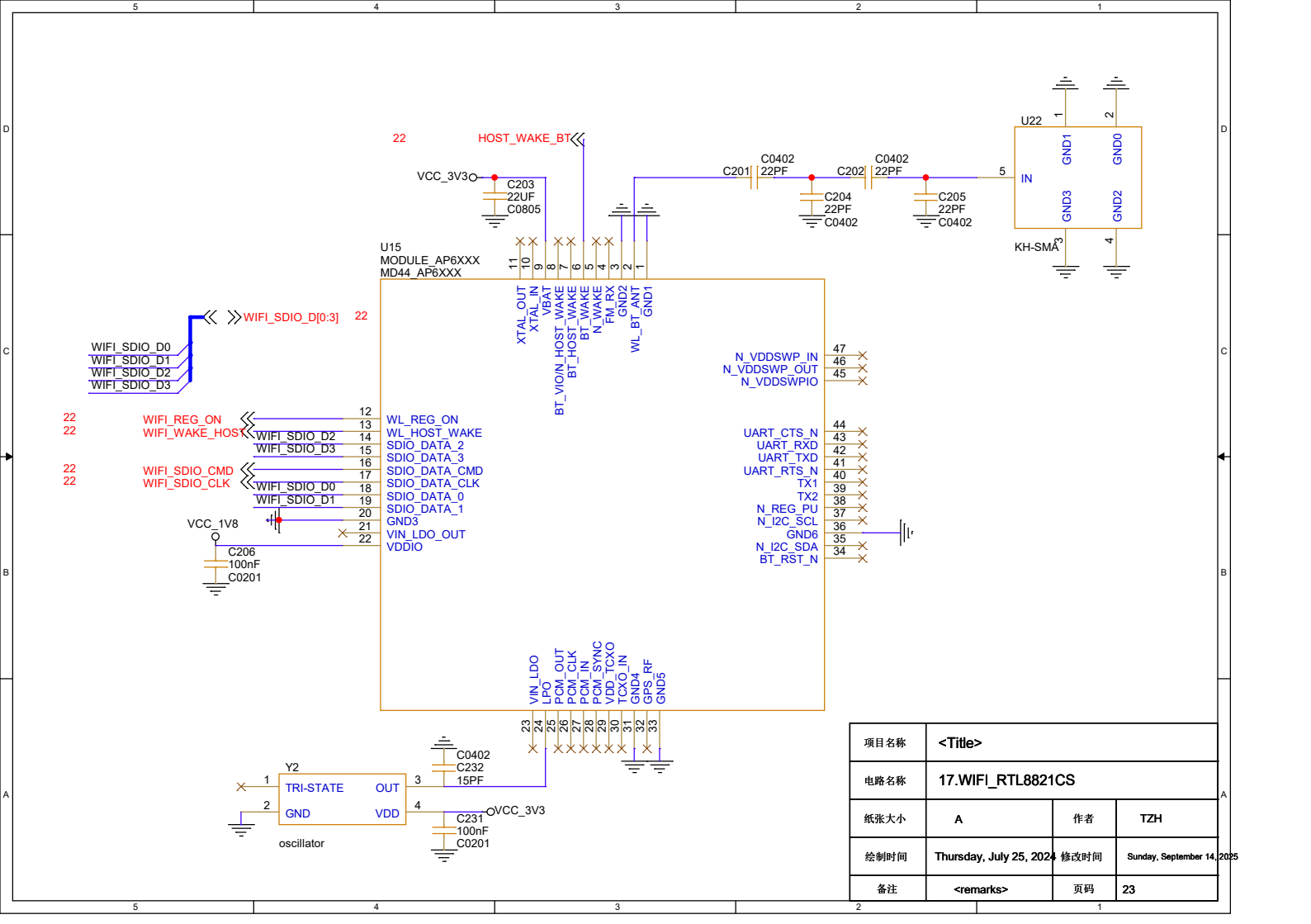
CIF_D0	/ EBC SDD00	/ SDMMC2_D0_M0	/ I2S1_MCLK_M1	/ VOP_BT656_D0_M1	/ GPIO3_C6_d
CIF_D1	/ EBC SDD01	/ SDMMC2_D1_M0	/ I2S1_SCLK_TX_M1	/ VOP_BT656_D1_M1	/ GPIO3_C7_d
CIF_D2	/ EBC SDD02	/ SDMMC2_D2_M0	/ I2S1_LRCK_TX_M1	/ VOP_BT656_D2_M1	/ GPIO3_D0_d
CIF_D3	/ EBC SDD03	/ SDMMC2_D3_M0	/ I2S1_SDO0_M1	/ VOP_BT656_D3_M1	/ GPIO3_D1_d
CIF_D4	/ EBC SDD04	/ SDMMC2_CMD_M0	/ I2S1_SDI0_M1	/ VOP_BT656_D4_M1	/ GPIO3_D2_d
CIF_D5	/ EBC SDD05	/ SDMMC2_CLK_M0	/ I2S1_SDI1_M1	/ VOP_BT656_D5_M1	/ GPIO3_D3_d
CIF_D6	/ EBC SDD06	/ SDMMC2_DET_M0	/ I2S1_SDI2_M1	/ VOP_BT656_D6_M1	/ GPIO3_D4_d
CIF_D7	/ EBC SDD07	/ SDMMC2_PWREN_M0	/ I2S1_SDI3_M1	/ VOP_BT656_D7_M1	/ GPIO3_D5_d
CIF_D8	/ EBC SDD08	/ GMAC1_TXD2_M1	/ UART1_TX_M1	/ PDM_CLK0_M1	/ GPIO3_D6_d
CIF_D9	/ EBC SDD09	/ GMAC1_TXD3_M1	/ UART1_RX_M1	/ PDM_SDI0_M1	/ GPIO3_D7_d
CIF_D10	/ EBC SDD010	/ GMAC1_TXCLK_M1		/ PDM_CLK1_M1	/ GPIO4_A0_d
CIF_D11	/ EBC SDD011	/ GMAC1_RXD2_M1		/ PDM_SDI1_M1	/ GPIO4_A1_d
CIF_D12	/ EBC SDD012	/ GMAC1_RXD3_M1	/ UART7_TX_M2	/ PDM_SDI2_M1	/ GPIO4_A2_d
CIF_D13	/ EBC SDD013	/ GMAC1_RXCLK_M1	/ UART7_RX_M2	/ PDM_SDI3_M1	/ GPIO4_A3_d
CIF_D14	/ EBC SDD014	/ GMAC1_TXD0_M1	/ UART9_TX_M2	/ I2S2_LRCK_TX_M1	/ GPIO4_A4_d
CIF_D15	/ EBC SDD015	/ GMAC1_TXD1_M1	/ UART9_RX_M2	/ I2S2_LRCK_RX_M1	/ GPIO4_A5_d
ISP_FLASHTRIGOUT	/ EBC_SDCE0	/ GMAC1_TXEN_M1	/ SPI3_CS0_M0	/ I2S1_SCLK_RX_M1	/ GPIO4_A6_d
CAM_CLKOUT0	/ EBC_SDCE1	/ GMAC1_RXD0_M1	/ SPI3_CS1_M0	/ I2S1_LRCK_RX_M1	/ GPIO4_A7_d
CAM_CLKOUT1	/ EBC_SDCE2	/ GMAC1_RXD1_M1	/ SPI3_MISO_M0	/ I2S1_SDO1_M1	/ GPIO4_B0_d
ISP_PRELIGHT_TRIG	/ EBC_SDCE3	/ GMAC1_RXDV_CRS_M1		/ I2S1_SDO2_M1	/ GPIO4_B1_d
I2C4_SDA_M0	/ EBC_VCOM	/ GMAC1_RXER_M1	/ SPI3_MOSI_M0	/ I2S2_SDI_M1	/ GPIO4_B2_d
I2C4_SCL_M0	/ EBC_GDOE	/ ETH1_REFCLK_25M_M1	/ SPI3_CLK_M0	/ I2S2_SDO_M1	/ GPIO4_B3_d
I2C2_SDA_M1	/ EBC_GDSP	/ CAN2_RX_M0	/ ISP_FLASH_TRIGIN	/ VOP_BT656_CLK_M1	/ GPIO4_B4_d
I2C2_SCL_M1	/ EBC_SDSHR	/ CAN2_TX_M0		/ I2S1_SDO3_M1	/ GPIO4_B5_d
CIF_HREF	/ EBC_SDLE	/ GMAC1_MDC_M1	/ UART1_RTSn_M1	/ I2S2_MCLK_M1	/ GPIO4_B6_d
CIF_VSYNC	/ EBC_SDOE	/ GMAC1_MDIO_M1		/ I2S2_SCLK_TX_M1	/ GPIO4_B7_d
CIF_CLKOUT	/ EBC_GDCLK		/ PWM11_IR_M1		/ GPIO4_C0_d
CIF_CLKIN	/ EBC_SCLK	/ GMAC1_MCLKINOUT_M1	/ UART1_CTSn_M1	/ I2S2_SCLK_RX_M1	/ GPIO4_C1_d

VCCIO6_1
VCCIO6_2



U5M
SOC_RK3568
BGA636_1

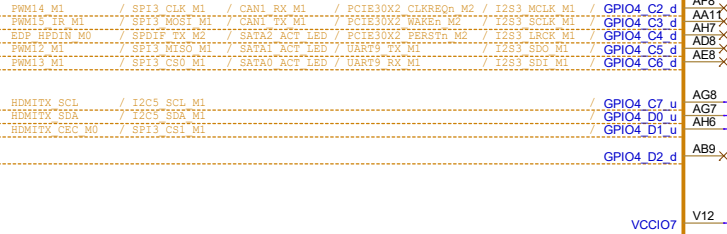
项目名称	<Title>		
电路名称	16.SOC_SDIO_WiFi_IO		
纸张大小	A	作者	TZH
绘制时间	Wednesday, July 24, 2025	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	22



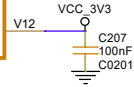
项目名称	<Title>		
电路名称	17.WIFI_RTL8821CS		
纸张大小	A	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>		
	页码	23	

VCCIO7 Domain

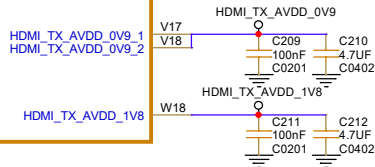
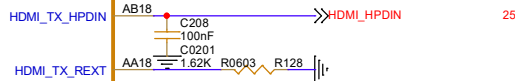
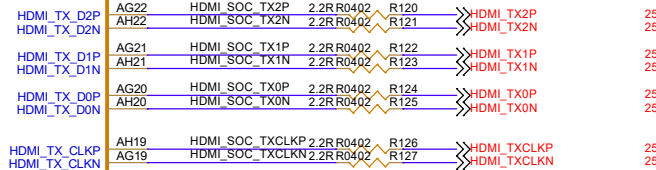
Operating Voltage=1.8V/3.3V



U5N
SOC_RK3568
BGA636_1

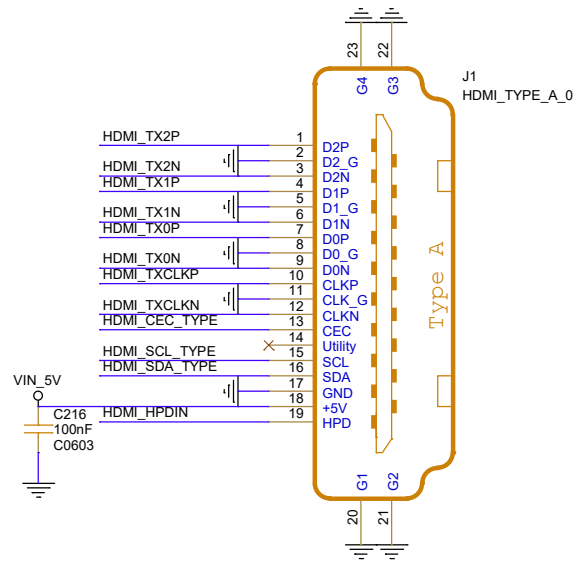
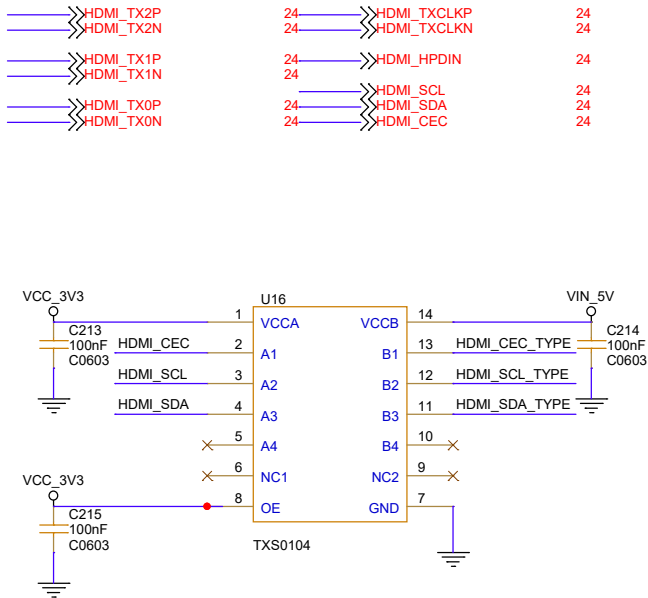


HDMI2.0 TX

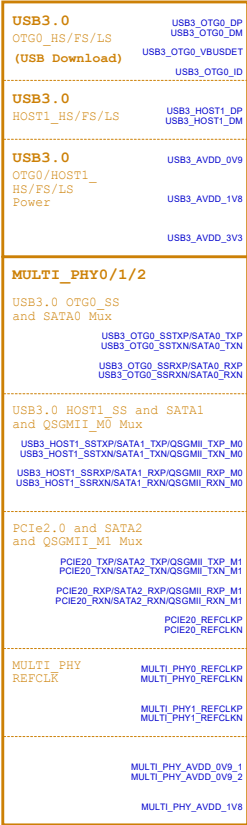


U5Q
SOC_RK3568
BGA636_1

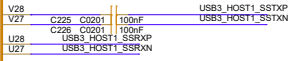
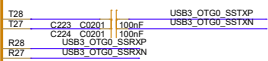
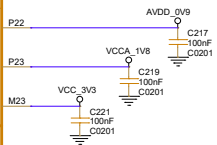
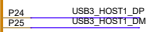
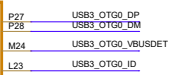
项目名称	<Title>		
电路名称	18.SOC_HDMI_IO		
纸张大小	A4	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>		页码 24



项目名称	<Title>		
电路名称	19.HDMI_TX_PHY		
纸张大小	A	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	25



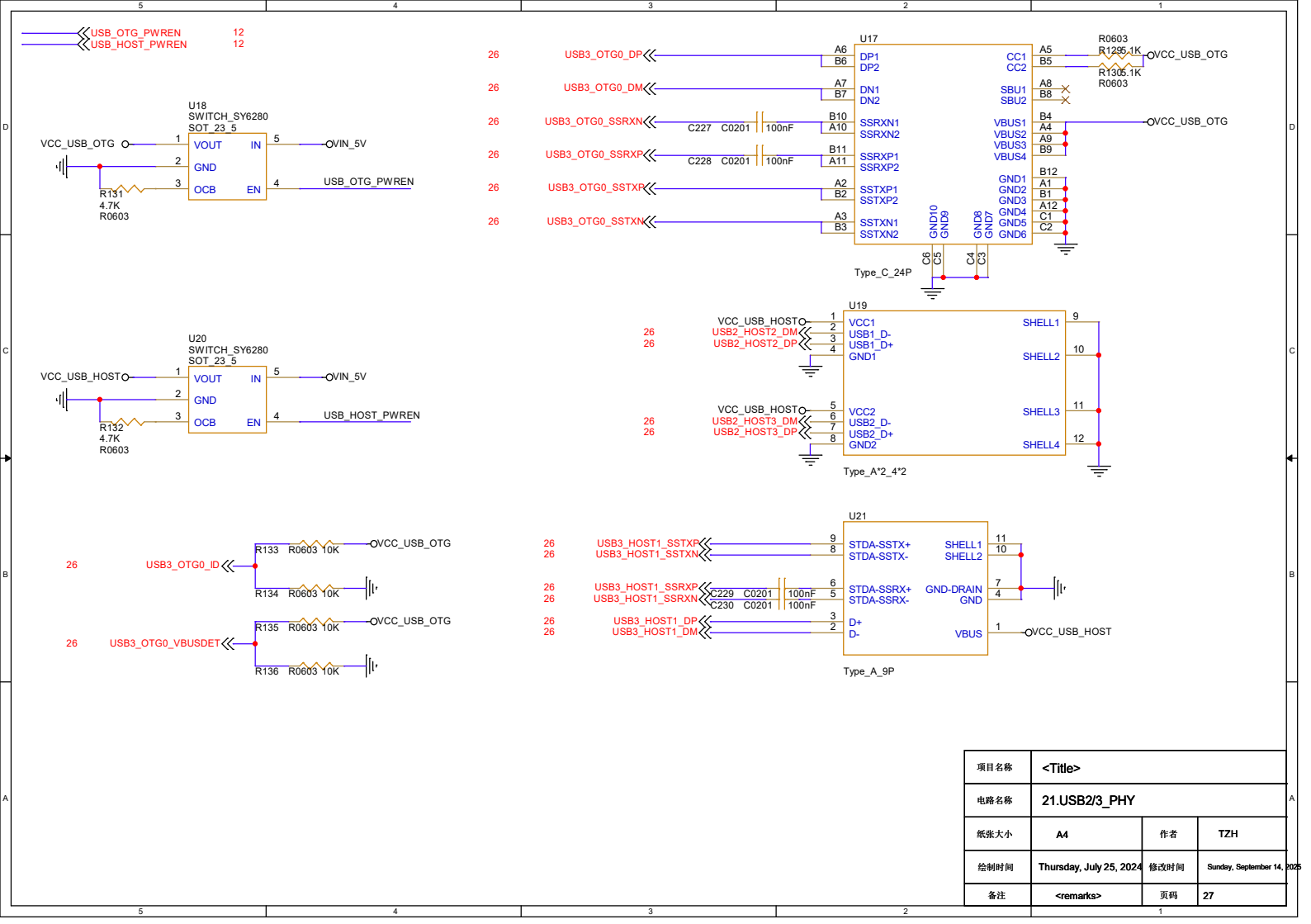
USU
SOC_RK3568
BGA636_1

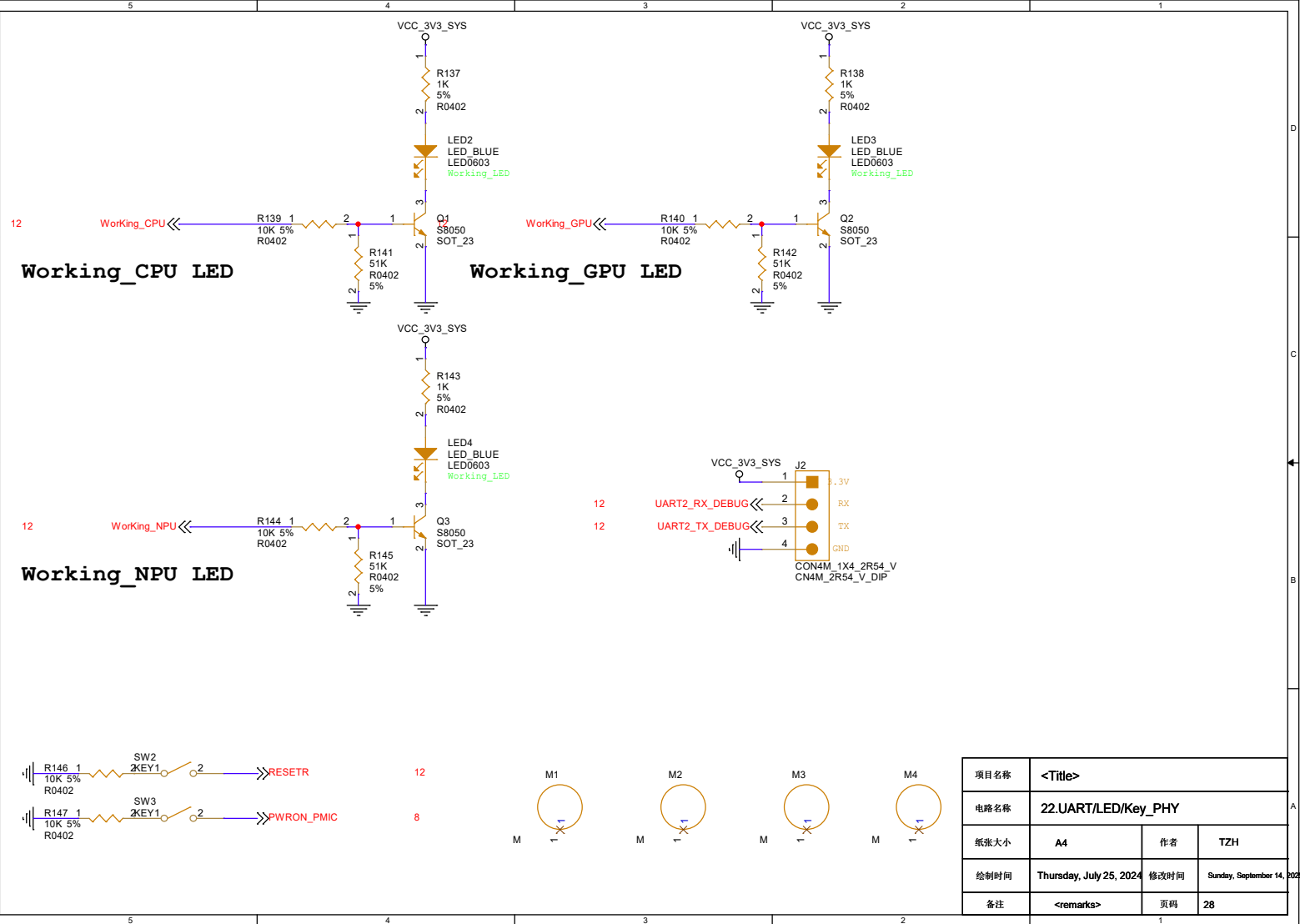


USV
SOC_RK3568
BGA636_1

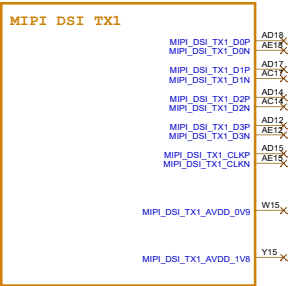


项目名称	<Title>		
电路名称	20.SOC_USB_IO		
纸张大小	Custom	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	26

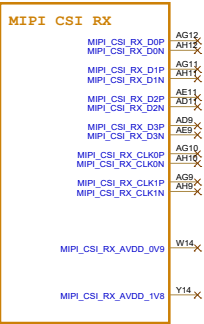




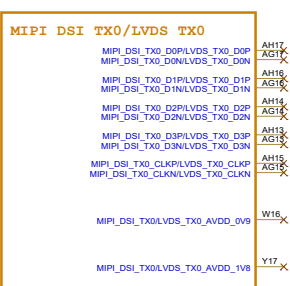
项目名称	<Title>		
电路名称	22.UART/LED/Key_PHY		
纸张大小	A4	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>		页码 28



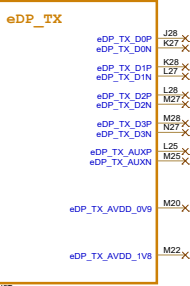
US5
SOC_RK3568
BGA636_1



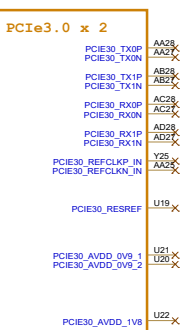
USP
SOC_RK3568
BGA636_1



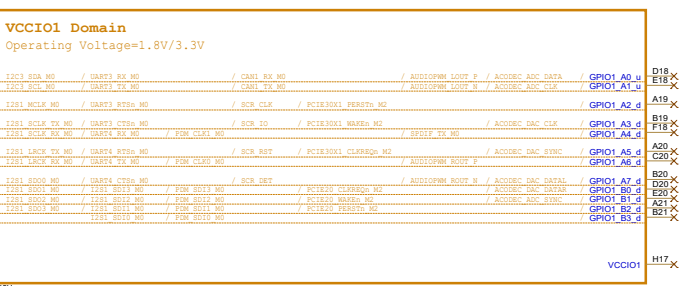
USR
SOC_RK3568
BGA636_1



UBT
SOC_RK3568
BGA636_1



USW
SOC_RK3568
BGA636_1



USH
SOC_RK3568
BGA636_1

项目名称	<Title>			
电路名称	23.NOT_IO			
纸张大小	A3	作者	TZH	
印制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025	
备注	<remarks>		页码	29