400mA,Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

General Description

The LP3983S is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3983S performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. A noise bypass pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The LP3983S also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3983S consumes less than 0.01μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. It is available in the 5-lead of SOT23-5 packages.

Ordering Information

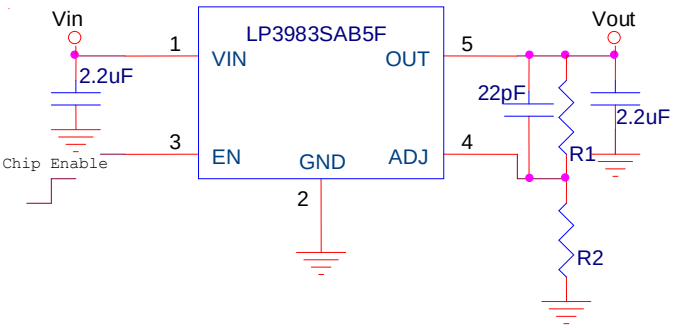
LP3983S □ □ □ □ □ □

- FB voltage
  - 09: 0.9V
  - 08: 0.8V
- F: Pb-Free
- Package Type
  - B5: SOT23-5
  - B6: SOT23-6
- Output Voltage Type
  - A: Adjustable

Features

- Ultra-Low-Noise for RF Application
- 2V- 6V Input Voltage Range
- Low Dropout : 300mV @ 400mA
- 400mA Output Current, 550mA Peak Current
- High PSRR: -68dB at 1KHz
- < 0.01uA Standby Current When Shutdown
- Available in SOT23-5/6 Package
- TTL-Logic-Controlled Shutdown Input
- Ultra-Fast Response in Line/Load transient
- Current Limiting and Thermal Shutdown Protection
- Quick start-up (typically 20uS)

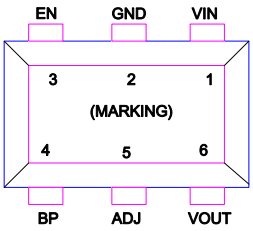
Typical Application Circuit

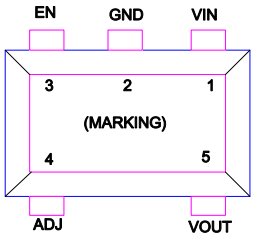


Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- LCD
- DSC Sensor
- Wireless Card

Pin Configurations





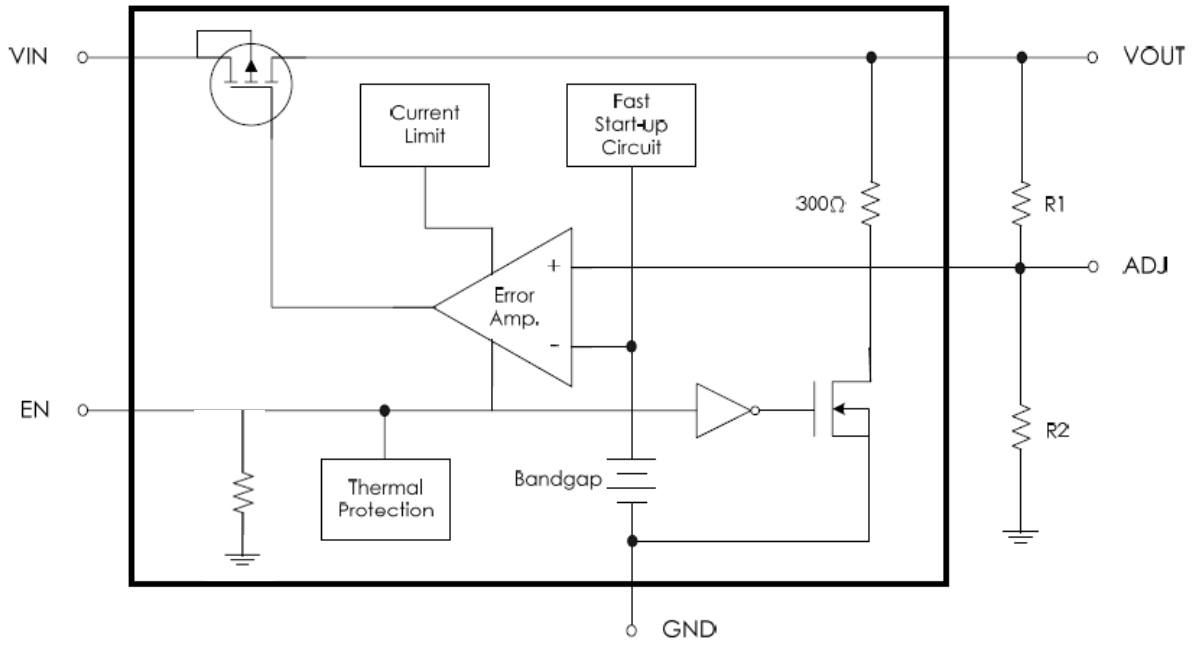
Marking Information

Device	Marking	Package	Shipping
LP3983S	LPS 1FXXX	SOT23-5 SOT23-6	3K/REEL
X: Batch number.			

Functional Pin Description

Pin Name	Pin NO.		Pin Function
	SOT23-5	SOT23-6	
VIN	1	1	Power Input Voltage.
GND	2	2	Ground.
EN	3	3	Chip Enable (Active High). There is an integrated pull low 1MΩ resistor connected to GND when the control signal is floating.
ADJ	4	5	Adjustable pin.
BP	-	4	Reference Noise Bypass.
VOUT	5	6	Output Voltage.

Function Block Diagram



Absolute Maximum Ratings

Supply Input Voltage----------6.5V

Power Dissipation, P_D @ T_A = 25°C

SOT23-5/6 ----------400mW

Package Thermal Resistance

SOT23-5/6, θ_{JA} ----------250°C/W

Lead Temperature (Soldering, 10 sec.) ----------260°C

Storage Temperature Range ---------- −65°C to 150°C

ESD Susceptibility

HBM (Human Body Mode) ----------2kV

MM(Machine-Mode)----------200V

Recommended Operating Conditions

Supply Input Voltage----------2V to 6.0V

Operation Junction Temperature Range ---------- −40°C to 125°C

Operation Ambient Temperature Range---------- −20°C to 85°C

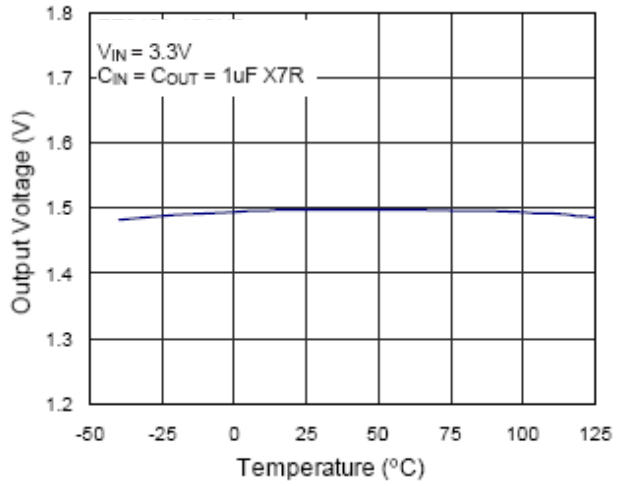
Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, C_{IN} = C_{OUT} =2.2μF, C_{FB} = 22pF, T_A = 25° C, unless otherwise specified)

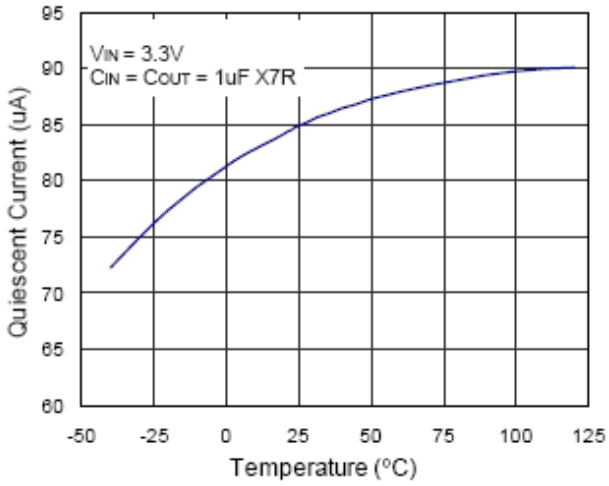
Parameter		Symbol	Test Conditions	Min	Typ.	Max	Units
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT} = 1mA	−2	--	+2	%
Output Loading Current		I_{LOAD}	V_{EN}=V_{IN},V_{IN}>2.5V		400		mA
Current Limit		I_{LIM}	R_{LOAD} = 1Ω		500		mA
Adjustable voltage reference		V_{FB}	LP3983SAB5F-09		0.9		V
			LP3983SAB5F-08		0.8		V
Quiescent Current		I_Q	V_{EN} ≥ 1.2V, I_{OUT} = 0mA		75	130	μA
Dropout Voltage		V_{DROP}	I_{OUT} = 200mA, V_{OUT} >2.8V		160	200	mV
			I_{OUT} = 400mA, V_{OUT} >2.8V		320	400	
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1mA			0.3	%
Load Regulation		Δ_{LOAD}	1mA < I_{OUT} < 400mA			0.6	%
Standby Current		I_{STBY}	V_{EN} = GND, Shutdown		0.01	1	μA
EN Input Bias Current		I_{IBSD}	V_{EN} = GND or V_{IN}		0.1	100	nA
EN Threshold	Logic-Low Voltage	V_{IL}	V_{IN} = 3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	V_{IN} = 3V to 5.5V, Start-Up	1.4			
Output Noise Voltage			10Hz to 100kHz, I_{OUT} = 200mA, C_{OUT} = 1μF		100		uVRMS
Power Supply Rejection Rate	f = 100Hz	PSRR	C_{OUT} = 1μF, I_{OUT} = 10mA		−76		dB
	f = 10kHz				−68		
Thermal Shutdown Temperature		T_{SD}			165		°C

Typical Operating Characteristics

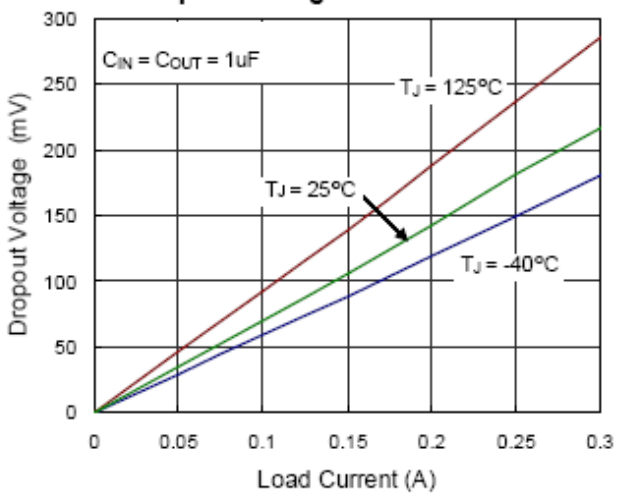
Output Voltage vs. Temperature



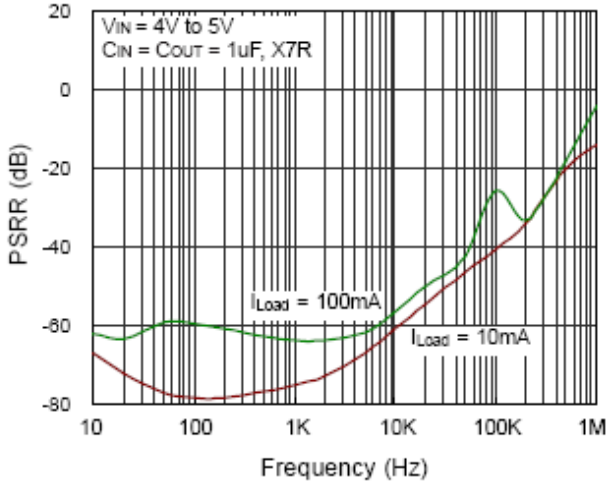
Quiescent Current vs. Temperature



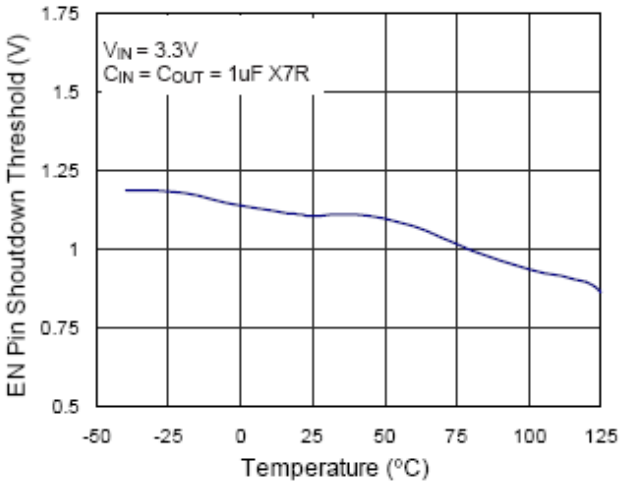
Dropout Voltage vs. Load Current



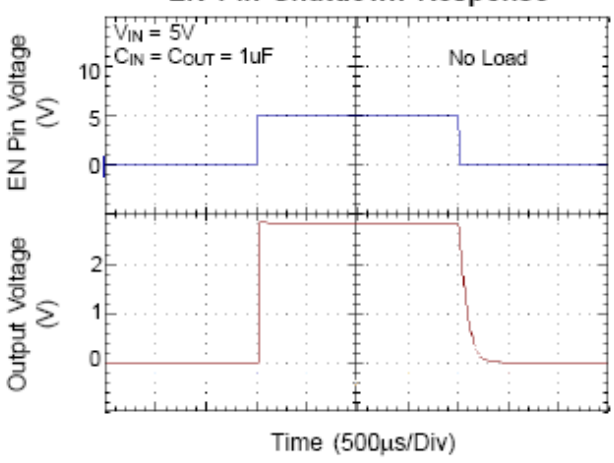
PSRR

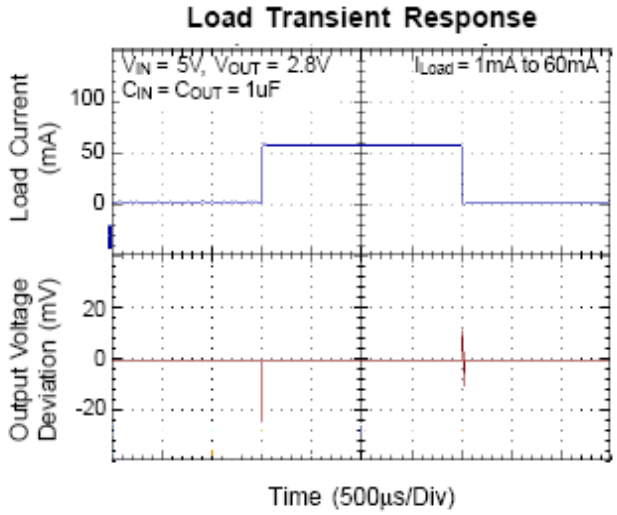


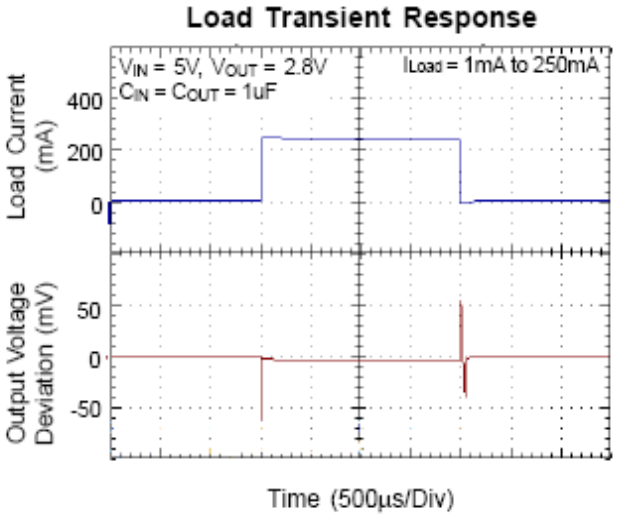
EN Pin Shoutdown Threshold vs. Temperature

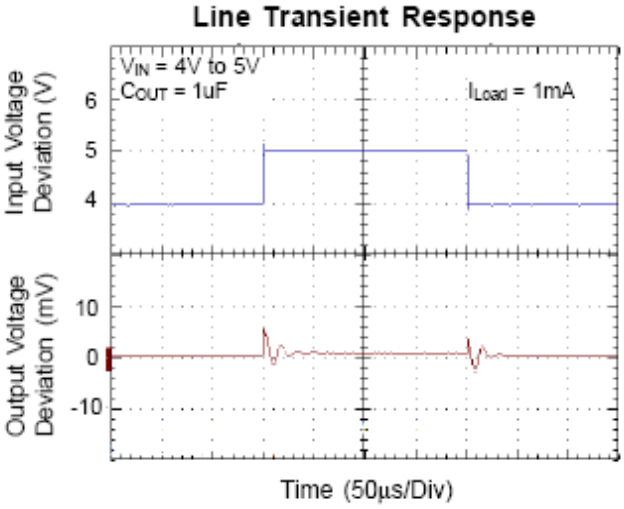


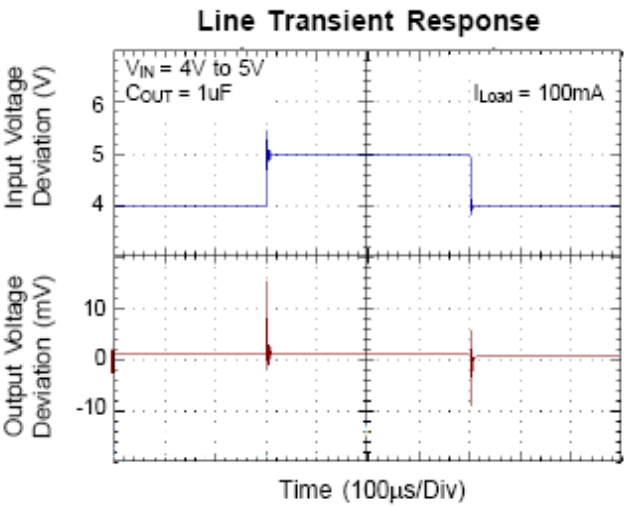
EN Pin Shutdown Response

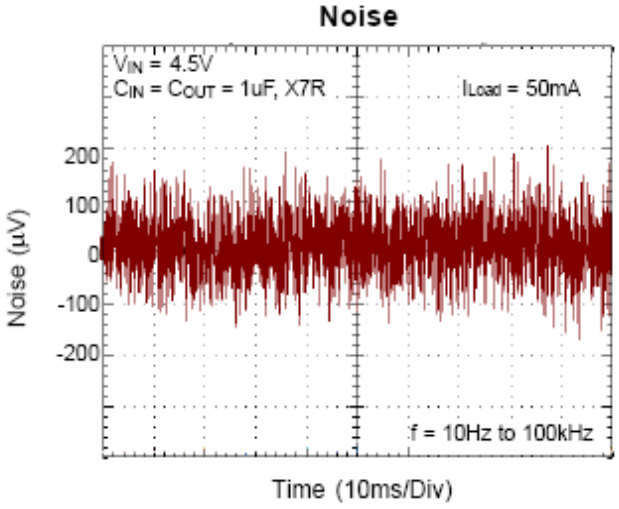


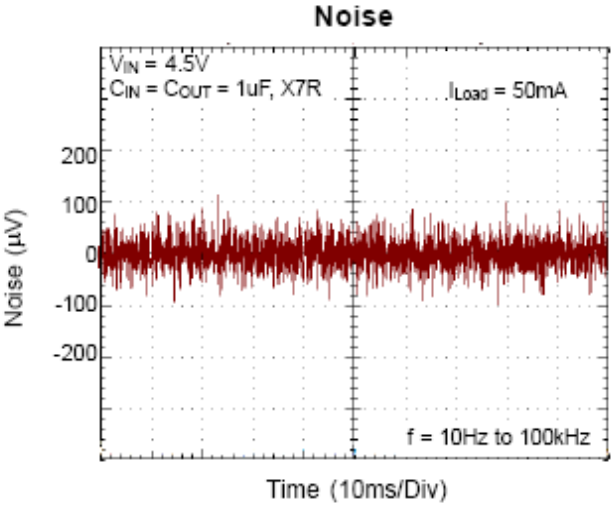

Load Transient Response
VIN = 5V, VOUT = 2.8V
CIN = COUT = 1uF
ILoad = 1mA to 60mA
Load Current (mA)
100
50
0
Output Voltage Deviation (mV)
20
0
-20
Time (500µs/Div)


Load Transient Response
VIN = 5V, VOUT = 2.8V
CIN = COUT = 1uF
ILoad = 1mA to 250mA
Load Current (mA)
400
200
0
Output Voltage Deviation (mV)
50
0
-50
Time (500µs/Div)


Line Transient Response
VIN = 4V to 5V
COUT = 1uF
ILoad = 1mA
Input Voltage Deviation (V)
6
5
4
Output Voltage Deviation (mV)
10
0
-10
Time (50µs/Div)


Line Transient Response
VIN = 4V to 5V
COUT = 1uF
ILoad = 100mA
Input Voltage Deviation (V)
6
5
4
Output Voltage Deviation (mV)
10
0
-10
Time (100µs/Div)

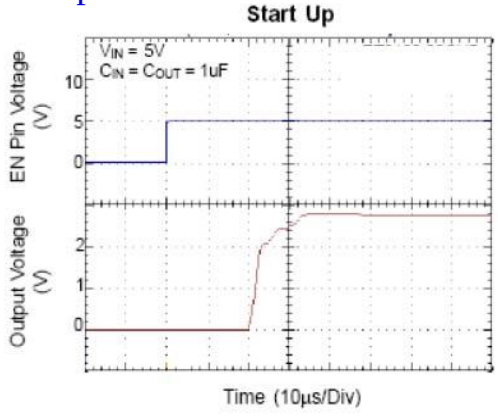

Noise
VIN = 4.5V
CIN = COUT = 1uF, X7R
ILoad = 50mA
Noise (µV)
200
100
0
-100
-200
f = 10Hz to 100kHz
Time (10ms/Div)


Noise
VIN = 4.5V
CIN = COUT = 1uF, X7R
ILoad = 50mA
Noise (µV)
200
100
0
-100
-200
f = 10Hz to 100kHz
Time (10ms/Div)

Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3983S must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the LP3983S input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3983S is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the LP3983S output ensures stability. The LP3983S still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin of the LP3983S and returned to a clean analog ground.

Start-up Function Enable Function



The LP3983S features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the LP3983S have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

Feedback Capacitor and Bypass Capacitor

For adjustable version, connecting a 22pF between output pin and FB pin significantly reduces output voltage ripple, it is critical that the capacitor connection should be direct and PCB traces should be as short as possible.

For LP3983SB6F08/9, connecting a 10nF between the BP pin and GND pin significantly reduces noise on the regulator output, it is critical that the capacitor connection between the BP pin and GND pin be direct and PCB traces should be as short as possible. There is a relationship between the bypass capacitor value and the LDO regulator turn on time. DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance.

Thermal Considerations

Thermal protection limits power dissipation in LP3983S. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 30°C. For continue operation, do not exceed absolute maximum operation junction temperature 125°C.

The power dissipation definition in device is:

$$P_D = (V_{IN}-V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of

surroundings airflow and temperature difference between junction to ambient.

The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where

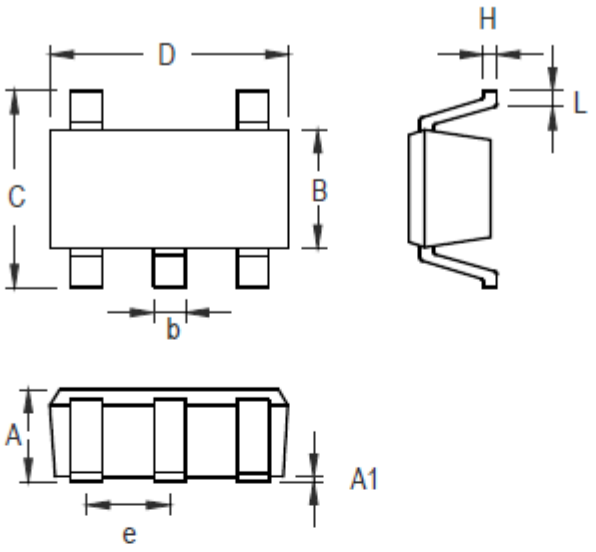
$T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3983S, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT23-5 package is 250°C/W.

$$P_{D(MAX)} = (125°C-25°C) / 250 = 400mW \text{ (SOT23-5)}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}.

Packaging Information

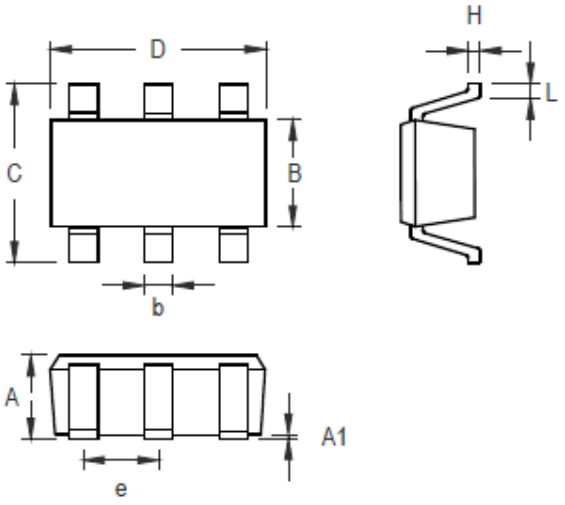
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package