Schematics For RK3568 NVR

RK_NVR_DEMO_RK3568_DDR4P216SD4_V12

Main Functions Introduction

1) PMIC: DiscretePower
2) RAM: DDR4 2x16Bit
3) ROM: eMMC5.1+SPI Falsh
4) Support: 1 x USB3.0 OTG + 3 x USB2.0 HOST
5) Support: 6 x SATA3.0 Connector (7pin)
6) Support: 2 x 1Lanes Mini PCIe Connector
7) Support: 1 x HDMI2.0 TX
8) Support: 1 x HDMI1.4 TX
9) Support: 1 x VGA TX
10) Support: 1 x 4Lanes MIPI DSI or LVDS with Touch Connector
11) Support: 2 x 10/100/1000 Ethernet(RGMII)
12) Support: 1 x IR Receiver
13) Support: 1 x Line Out, 1 x Line In,
14) Support: 1 x Buzzer
15) Support: 1 x Power LED,1 x Ethernet LED,1 x HDD LED
16) Support: 1 x Recovery Key
17) Support: 1 x RS232
18) Support: 1 x RS485
19) Support: 1 x UART
20) Support: Debug UART

Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	00.Cover Page				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	1 of 37

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

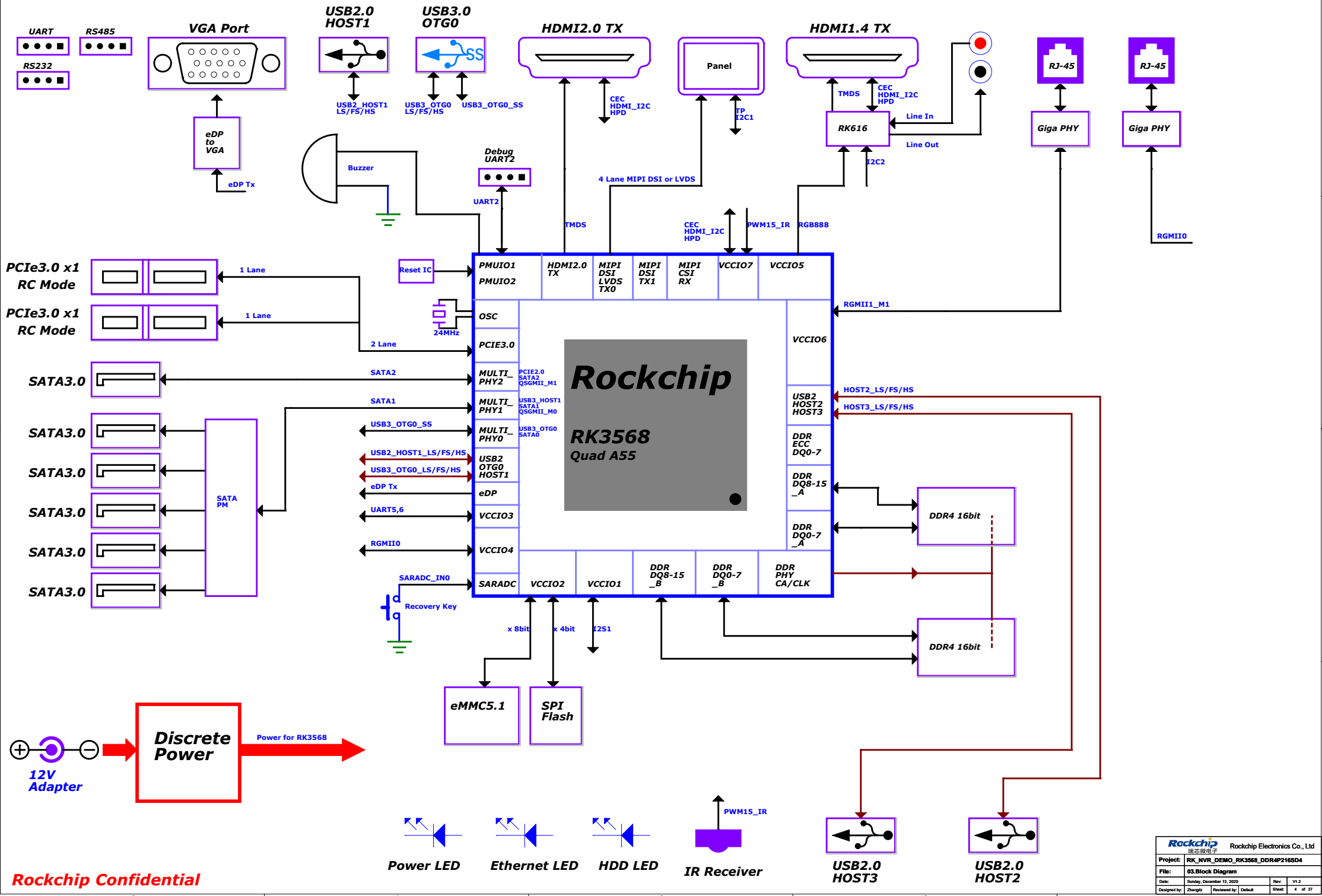
NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	01.Index and Notes				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	2 of 37

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2020-11-04	Zhangdz	1:Revision preliminary version	
V1.1	2020-12-07	Zhangdz	1:Change ED6701,ED6702,ED6703,ED6704, ED6801,ED6802,ED6803,ED6804 to UDD32C03L01 2:VDD_LOGIC change to independent buck power supply 3:VDD_GPU and VDD_NPU change to the same buck power supply 4:Change C2150 to VDD_GPU/NPU power net 5:Add C1007	
V1.2	2020-12-17	Zhangdz	1:Optimize PCB layout 1) Change C1003 to 4.7uF,Add C1021(4.7uF) 2) Change C1009 to 4.7uF,Add C1023(4.7uF) 3) Change C1018 to 4.7uF,Add C1022(4.7uF) 4) Change C1104 to 4.7uF,Add C1105(4.7uF) 2:Add power on sequence 3:Remove R1613 and R1618,Pin W14,Y14 connection to VSS 4:Remove R1701 and R1703,Pin W15,Y15 connection to VSS 5:Change R2123 to 100K,Change R2125 to 10K, 6:VDD_LOGIC Voltage range : 0.81-1.0V Change R2111 to 51K 1%,Change R2115 to 300K 1%, Change R2114 to 18K 1%,Change R2110 to 18K 1%, 7:VDD_GPU/NPU Voltage range :0.81-1.1V Change R2113 to 51K 1%,Change R2117 to 150K 1%, Change R2112 to 10K 1% 8:PCIE_PWREN_H_GPIO0_D4 Connect to SOC	

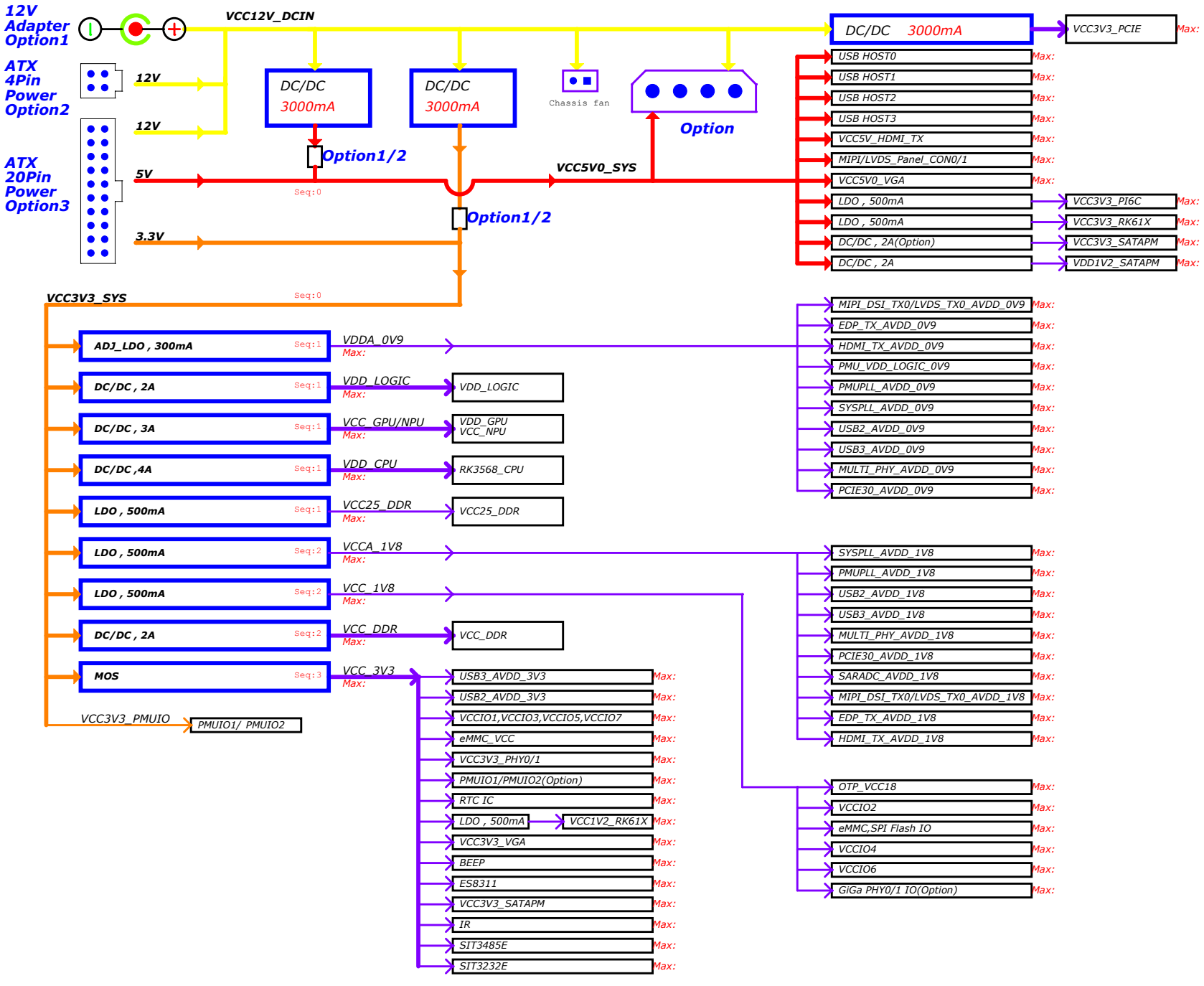
RK3568 NVR DEMO Block Diagram



Rockchip Confidential

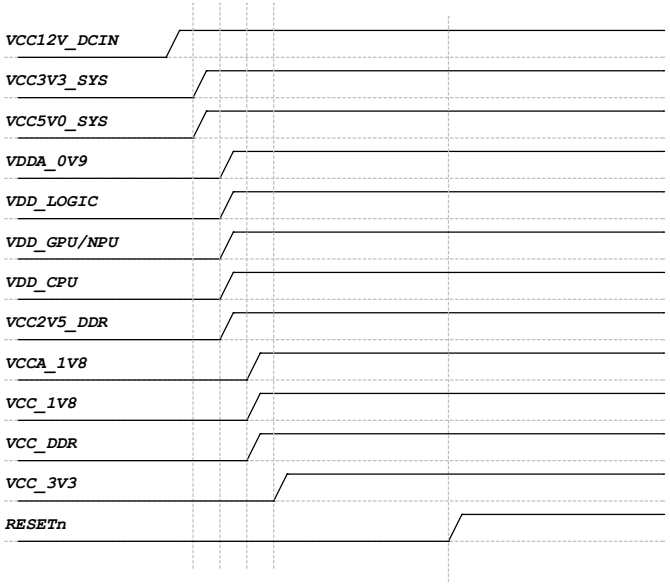
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4
File:	03.Block Diagram
Date:	Sunday, December 13, 2020
Rev:	V1.2
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	4 of 37

Power Diagram



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4
File:	04.Power Diagram
Date:	Tuesday, December 22, 2020
Rev:	V1.2
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	5 of 37

Power Sequence



Power Supply	Channel	Supply Limit	Power Name	Time Slot	Default Voltage
VCC12V_DCIN	BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V
VCC12V_DCIN	BUCK	3.0A	VCC5V0_SYS	Slot:0	5.2V
VCC3V3_SYS			VCC3V3_PMUIO	Slot:0	3.3V
VCC3V3_SYS	LDO	0.3A	VDDA_0V9	Slot:1	0.9V
VCC3V3_SYS	BUCK	1.5A	VDD_LOGIC	Slot:1	0.9V
VCC3V3_SYS	BUCK	3.0A	VDD_GPU/NPU	Slot:1	0.9V
VCC3V3_SYS	BUCK	5.0A	VDD_CPU	Slot:1	0.9V
VCC3V3_SYS	LDO	0.3A	VCC2V5_DDR	Slot:1	2.5V
VCC3V3_SYS	LDO	0.5A	VCC_1V8	Slot:2	1.8V
VCC3V3_SYS	LDO	0.5A	VCCA_1V8	Slot:2	1.8V
VCC3V3_SYS	BUCK	1.5A	VCC_DDR	Slot:2	1.2V DDR4
VCC3V3_SYS	MOS	2A	VCC_3V3	Slot:3	3.3V
VCC3V3_PMUIO	RESETn				

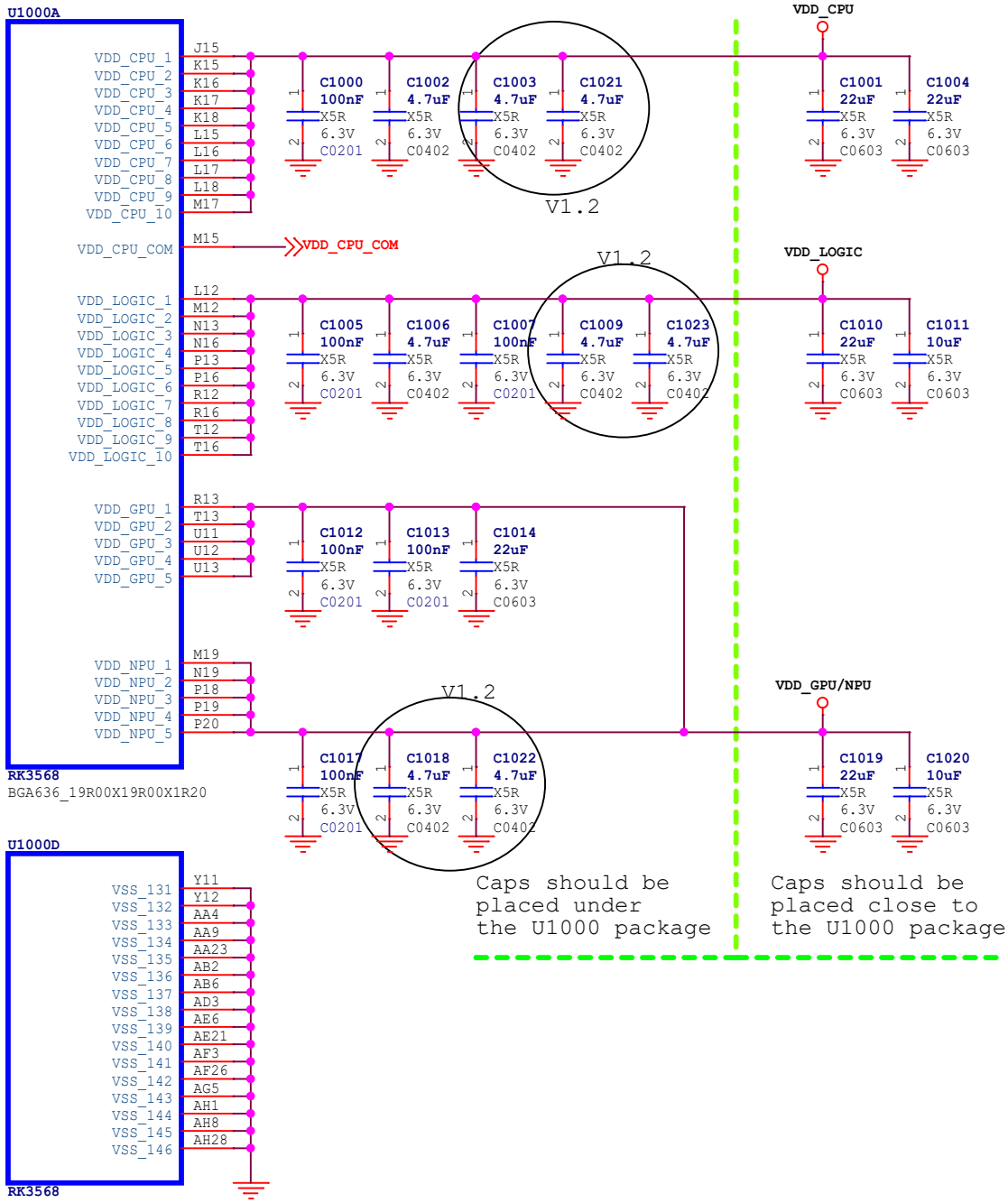
IO Power Domain Map

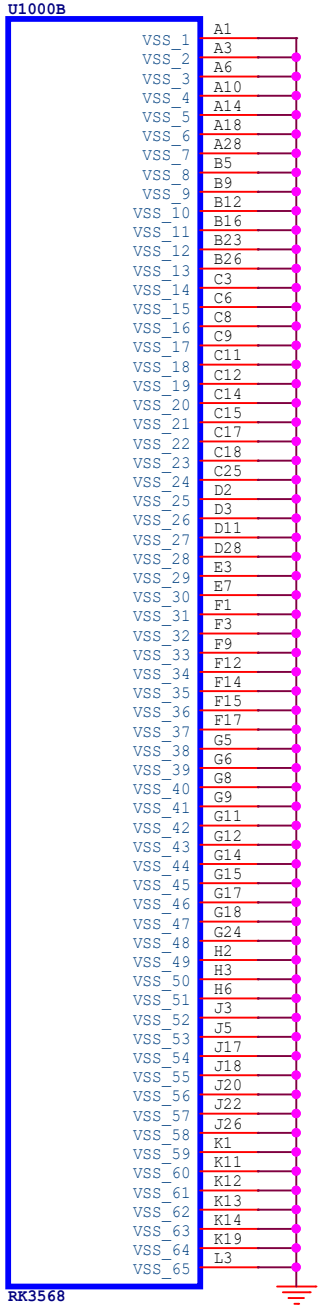
Updates must be Revision accordingly!

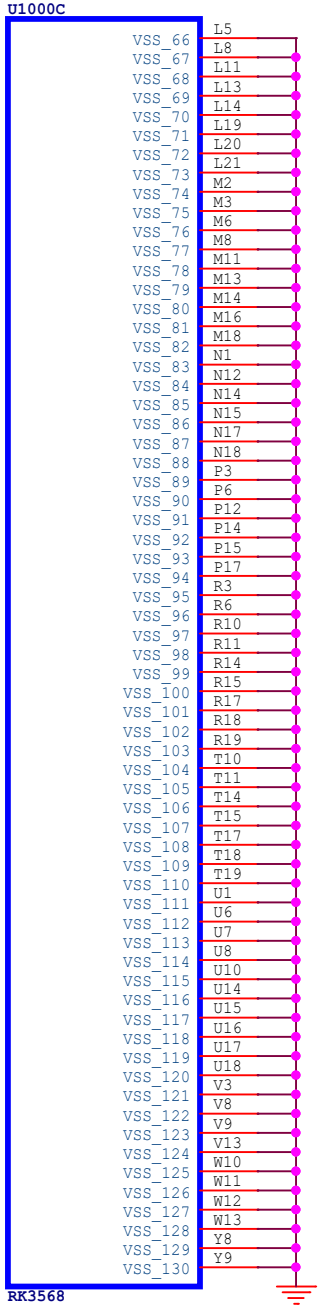
IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC_3V3	VCC_3V3	3.3V	
PMUIO2	Pin W19	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO1	Pin H17	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO4	Pin J21	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCC_3V3	VCC_3V3	3.3V	

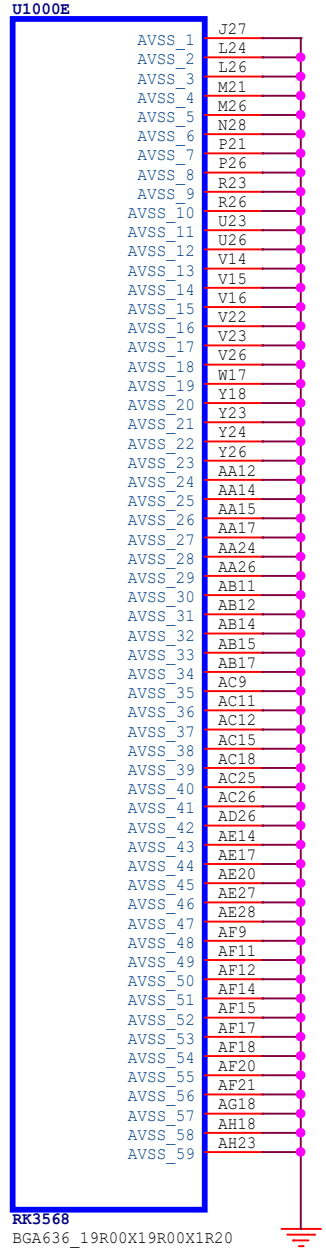
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	05.Power Sequence/IO Domain Map				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	6 of 37

RK3568_ABCDE (Power&Gnd)



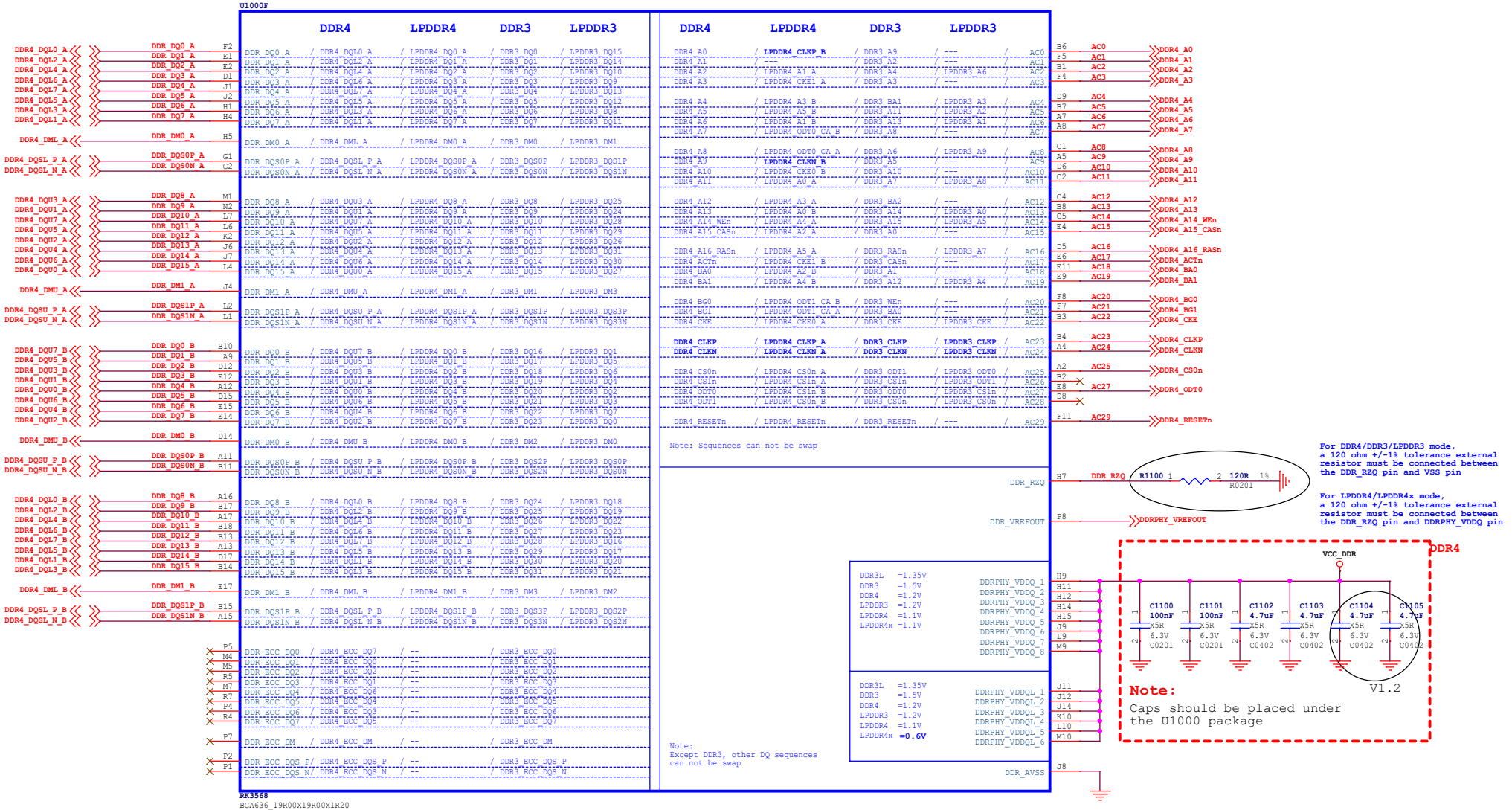






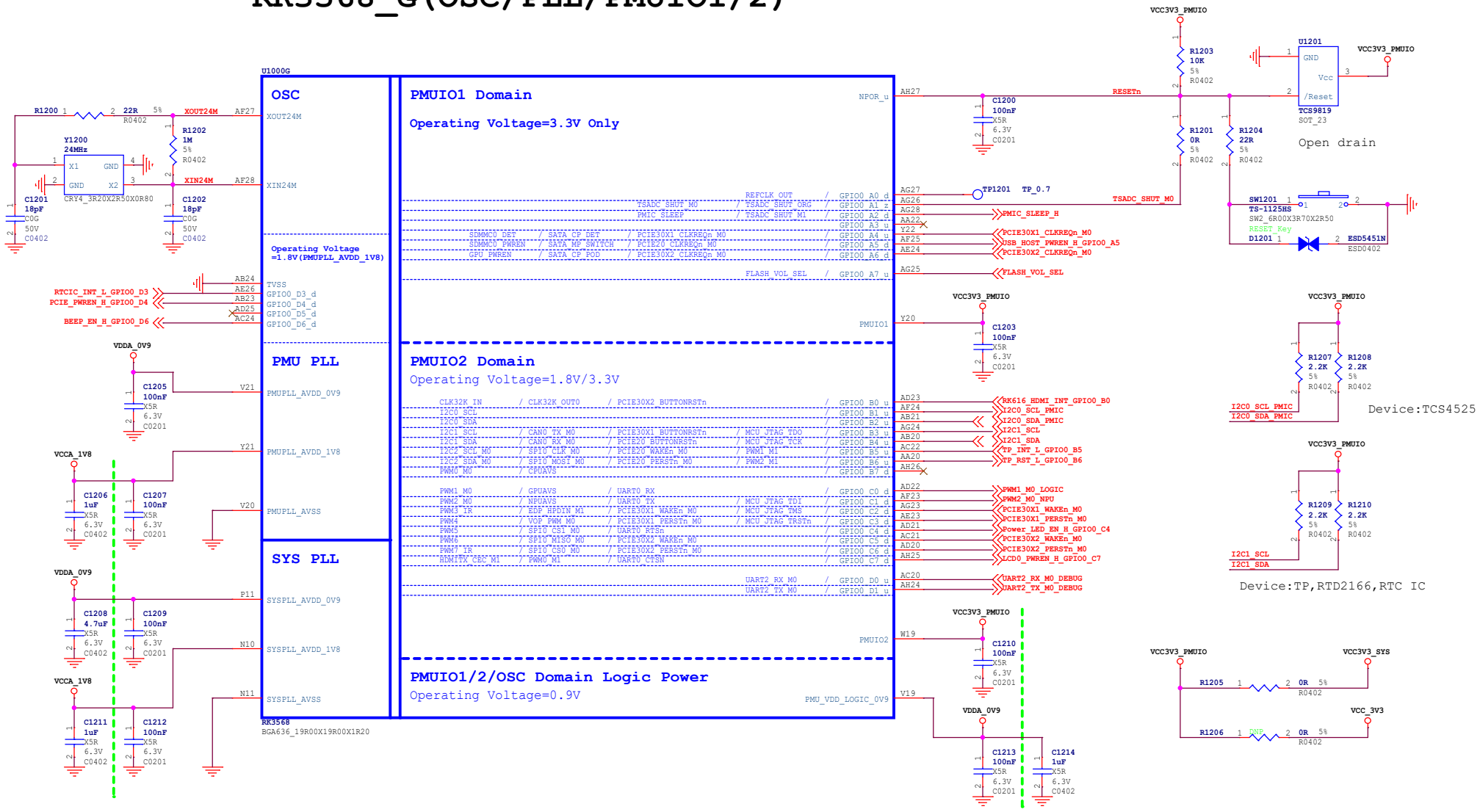
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	10.RK3568_Power/GND				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	7 of 37

RK3568_F (DDR PHY)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	11.RK3568_DDR PHY				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	8 of 37

RK3568_G(OSC/PLL/PMUIO1/2)

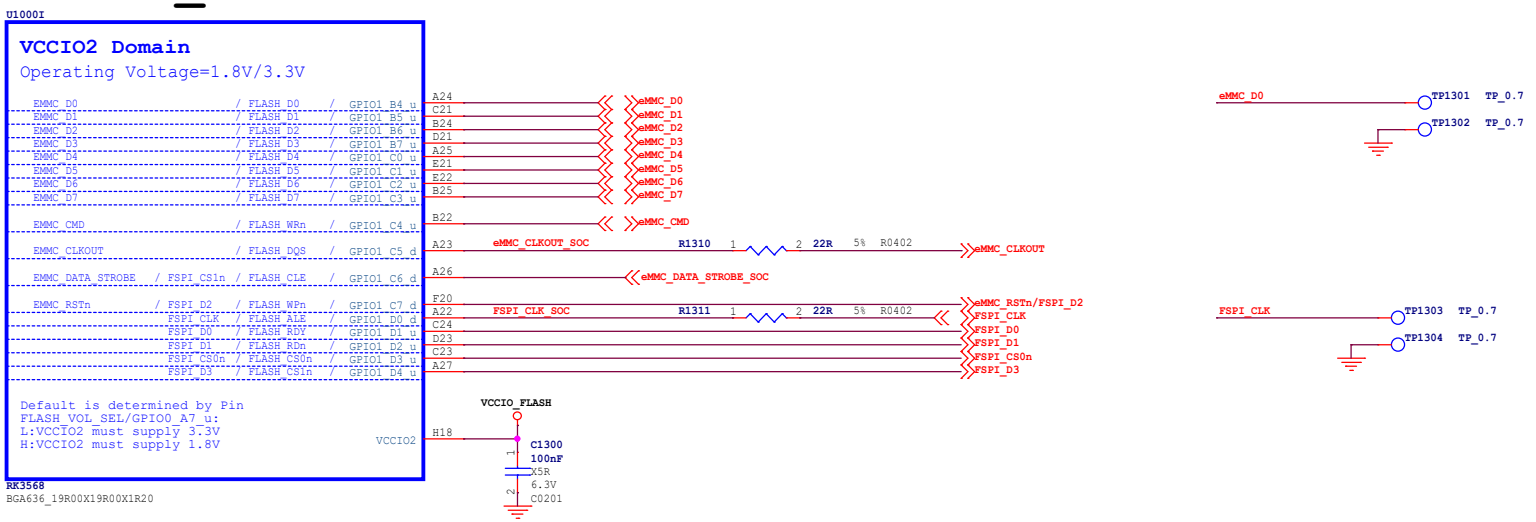


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

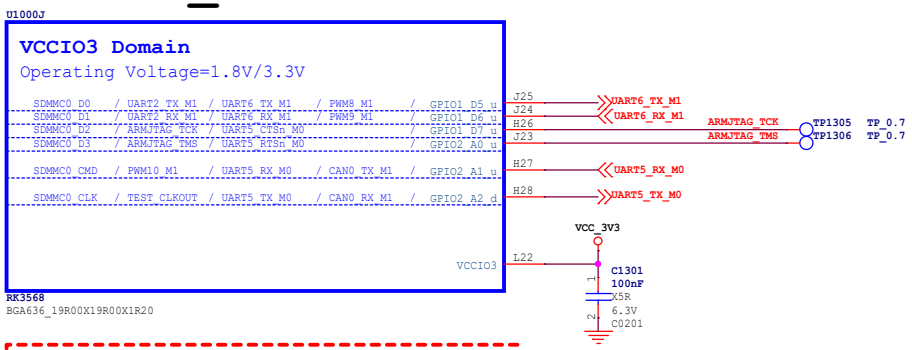
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	12.RK3568_OSC/PLL/PMUIO				
Date:	Thursday, December 17, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	9 of 37

RK3568_I(VCCIO2 Domain)



RK3568_J(VCCIO3 Domain)

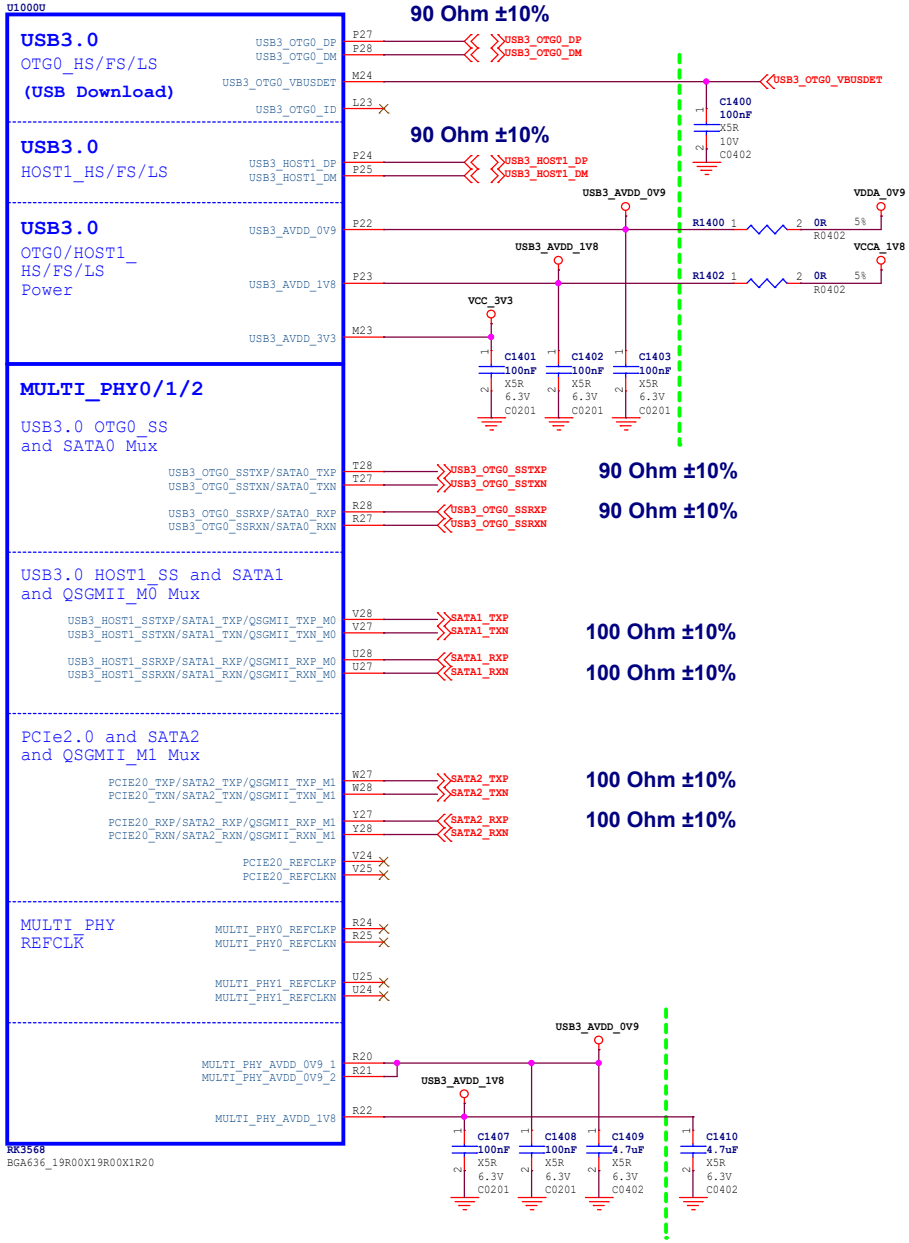


Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	13.RK3568_Flash/SD Controller				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	10 of 37

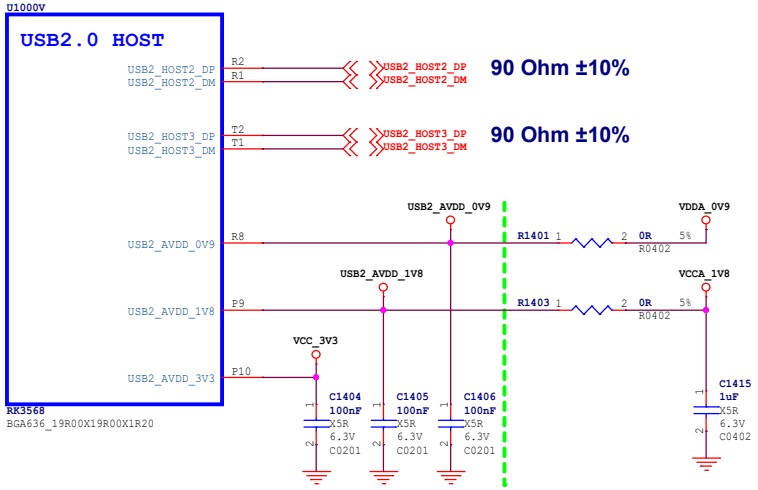
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



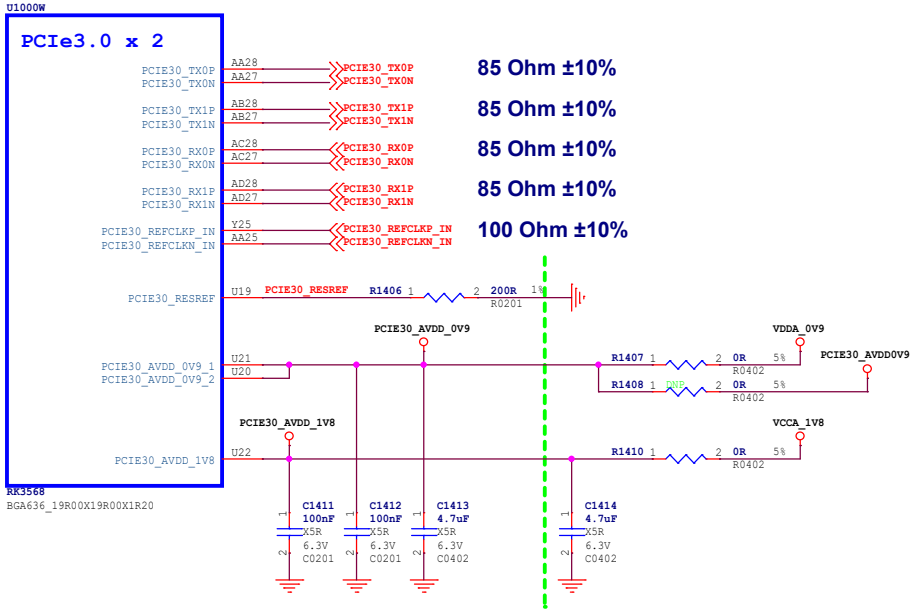
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_V(USB2.0 HOST)

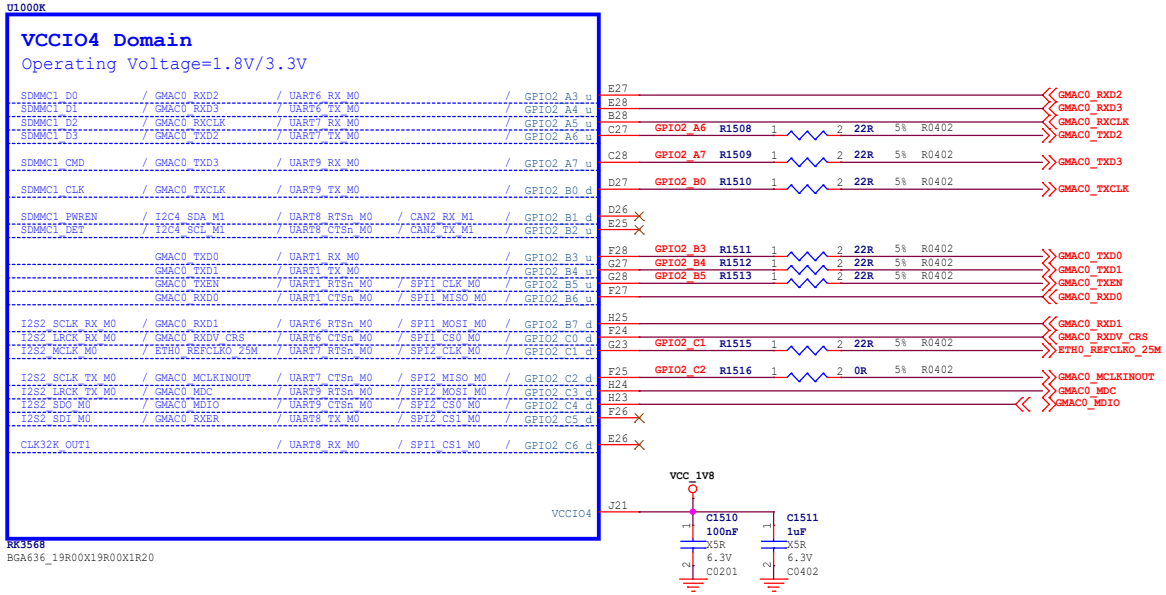


RK3568_W(PCIe3.0 x2)

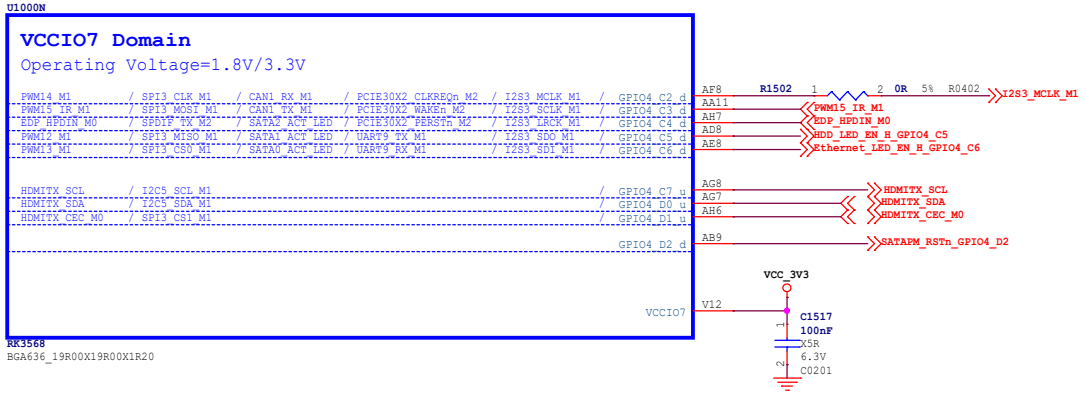


Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	14.RK3568_USB/PCIe/SATA PHY				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	11 of 37

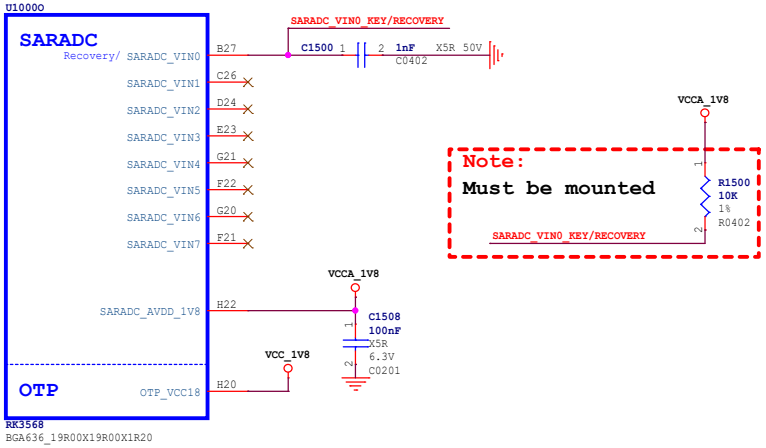
RK3568_K(VCCIO4 Domain)

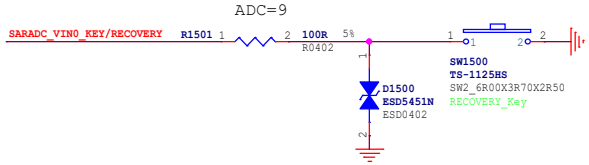


RK3568_N(VCCIO7 Domain)



RK3568_O(SARADC/OTP)



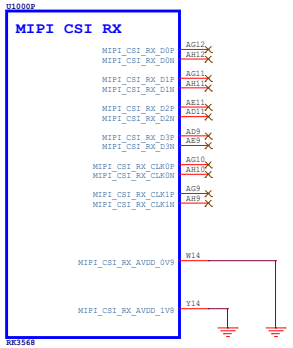


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

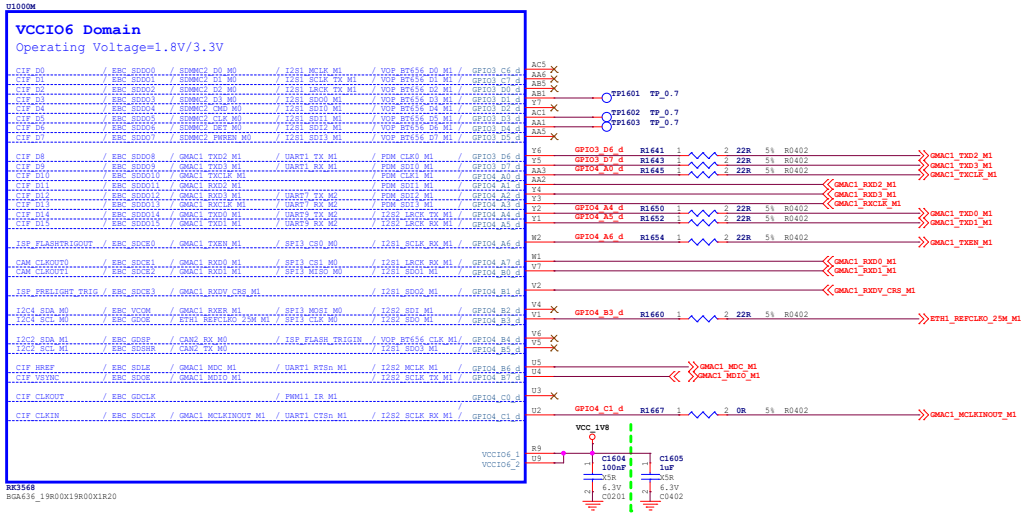
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	15.RK3568_SARADC/GPIO				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	12 of 37

RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



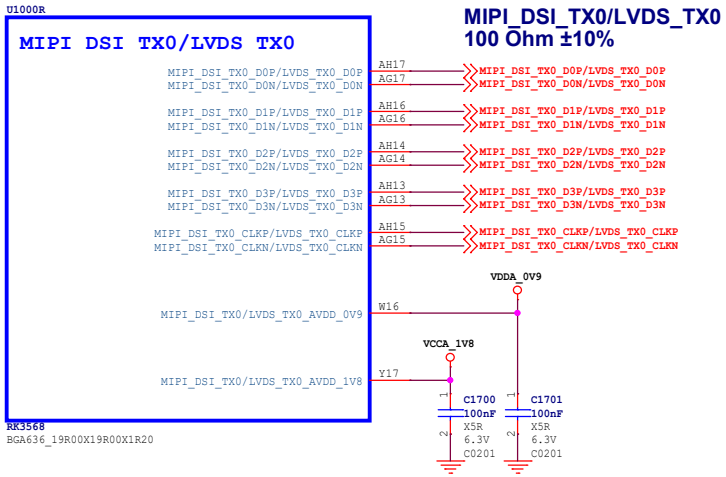
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

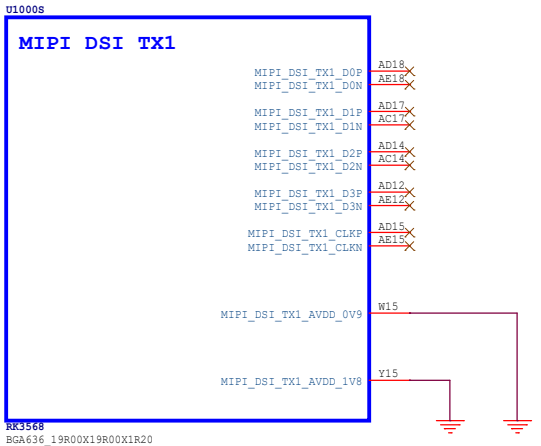
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4
File:	16.RK3568_VI Interface
Date:	Sunday, December 13, 2020
Rev:	V1.2
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	13 of 37

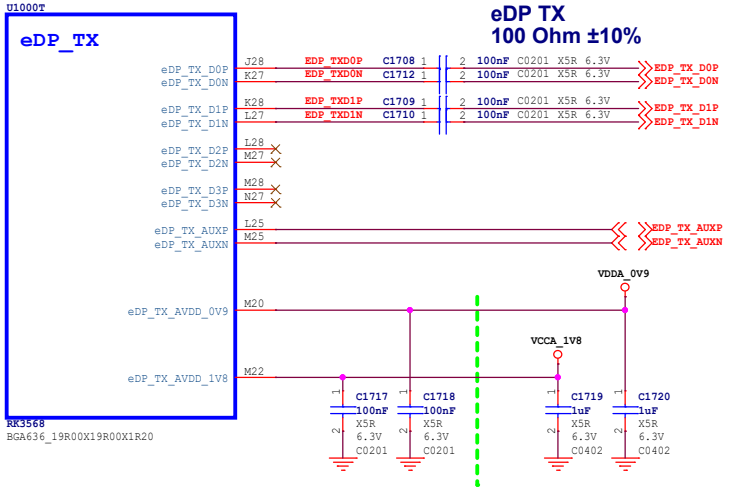
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



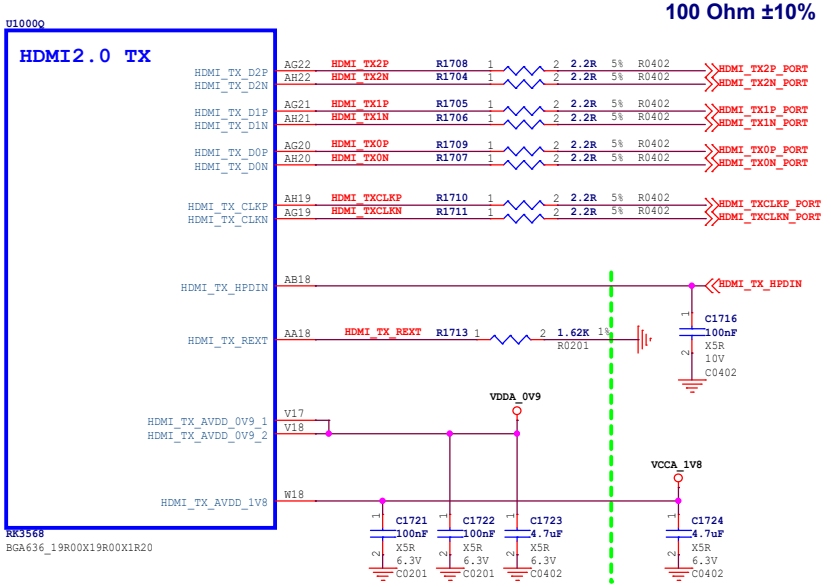
RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_Q(HDMI2.0 TX)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	17.RK3568_VO Interface_1				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	14 of 37

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3568
BGA636_19R00X19R00X1R20

AG6 LCDC_D0
AD7 LCDC_D1
AC8 LCDC_D2
AC7 LCDC_D3
AF5 LCDC_D4
AF6 LCDC_D5
AD6 LCDC_D6
AH5 LCDC_D7

AH4 LCDC_CLK_SOC R1813 1 2 22R 5% R0402 LCDC_CLK

AB8 LCDC_D8
AE5 LCDC_D9
AG4 LCDC_D10
AF4 LCDC_D11
AH3 LCDC_D12
AG3 LCDC_D13
AH2 LCDC_D14
AG2 LCDC_D15

AG1 LCDC_D16
AF2 LCDC_D17
AF1 LCDC_D18
AE1 LCDC_D19
AE2 LCDC_D20
AE3 LCDC_D21
AD4 LCDC_D22
AD2 LCDC_D23

AD1 LCDC_HSYNC
AA7 LCDC_VSYNC
AC4 LCDC_DEN

AC3
AC2 R1803 1 2 0R 5% R0402 LCD0_BL_PWM14_M0 / SPDIF_TX_M1

VCC_3V3

V10
V11

C1800 100nF X5R 6.3V C0201
C1801 1uF X5R 6.3V C0402

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	18.RK3568_VO Interface_2				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	15 of 37

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

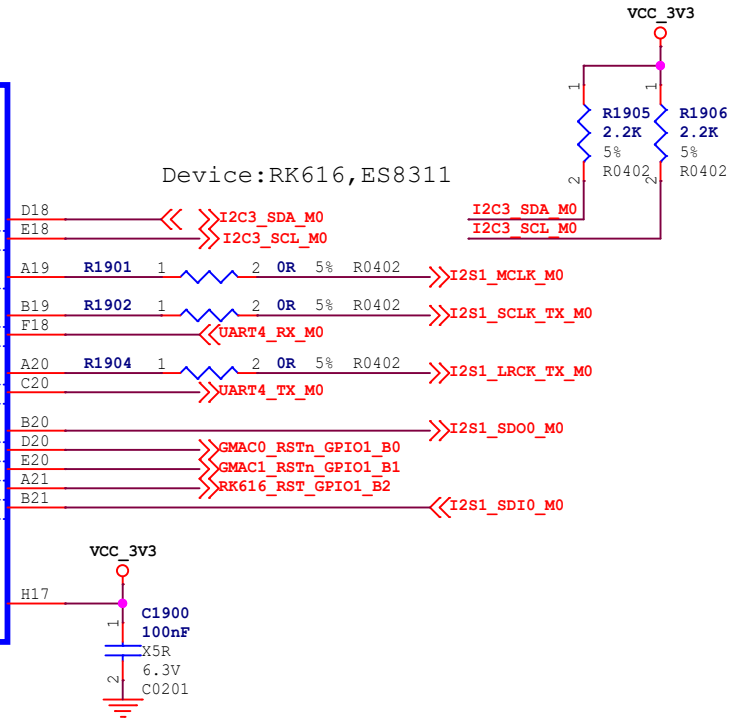
I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20

Device:RK616,ES8311



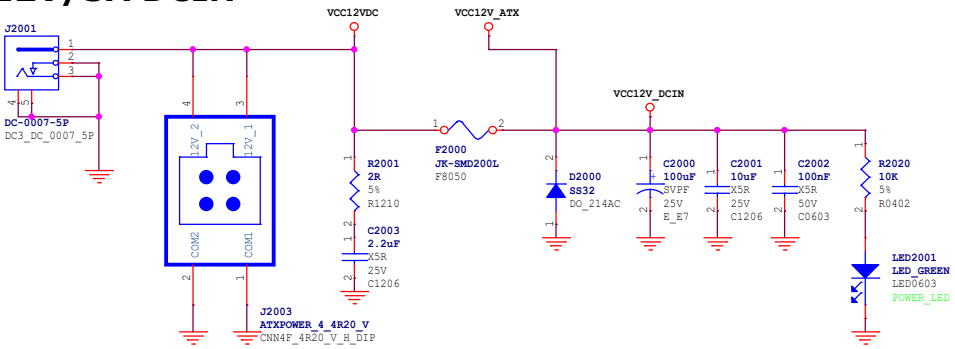
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

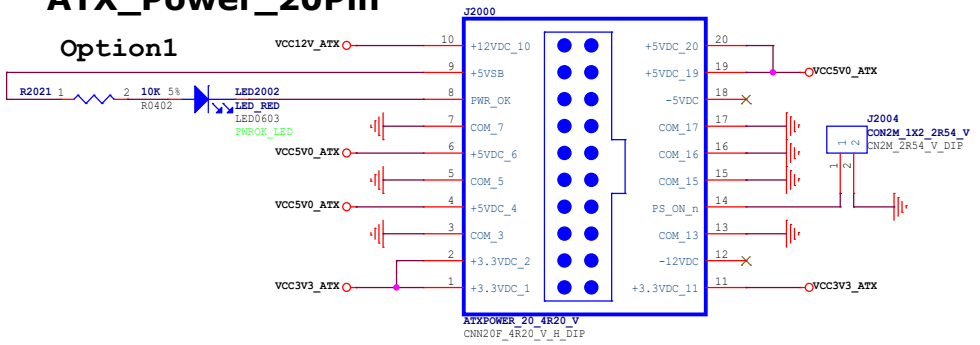
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	19.RK3568_Audio Interface				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	16 of 37

12V/3A DCIN

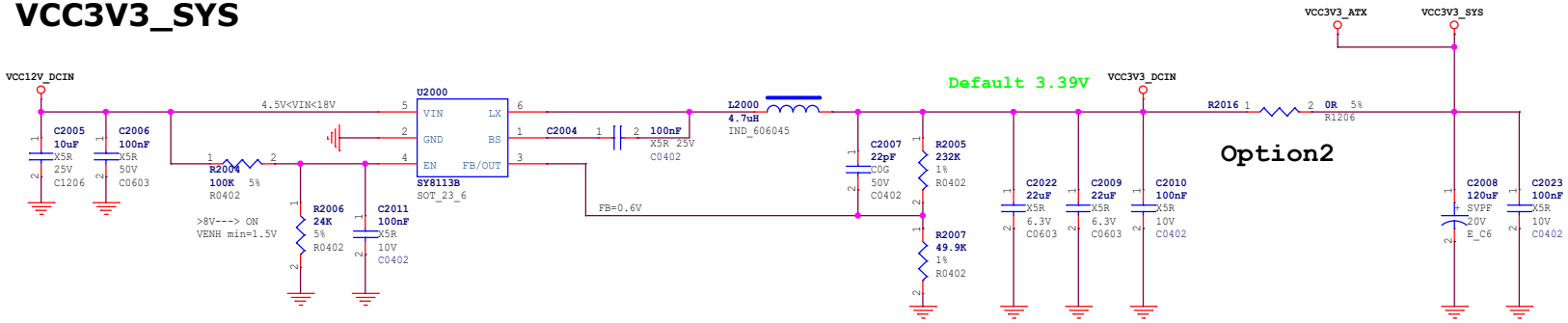


ATX_Power_20Pin

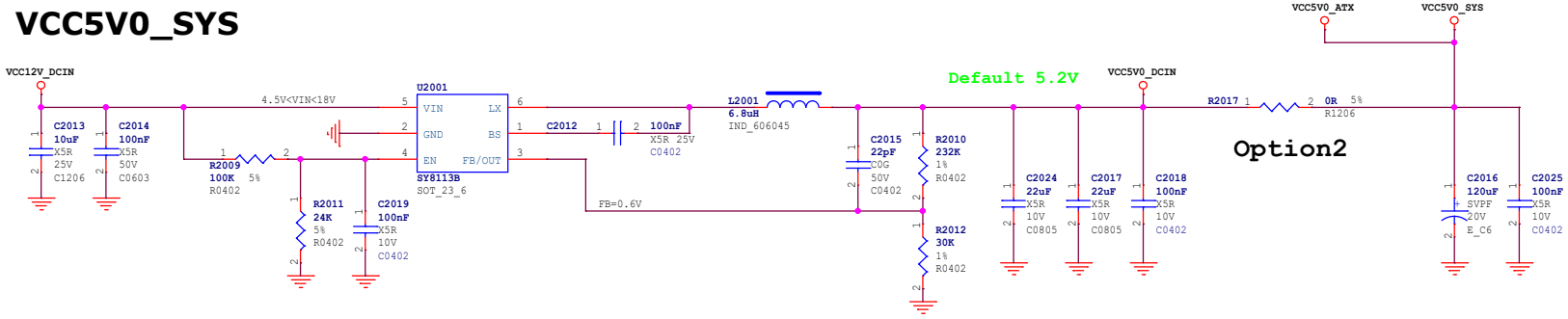
Option1

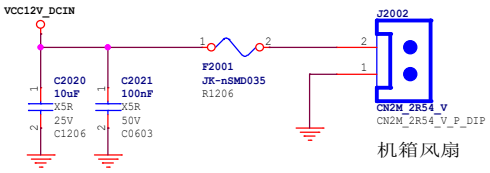


VCC3V3_SYS

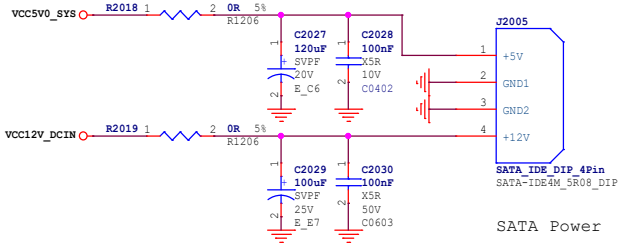


VCC5V0_SYS





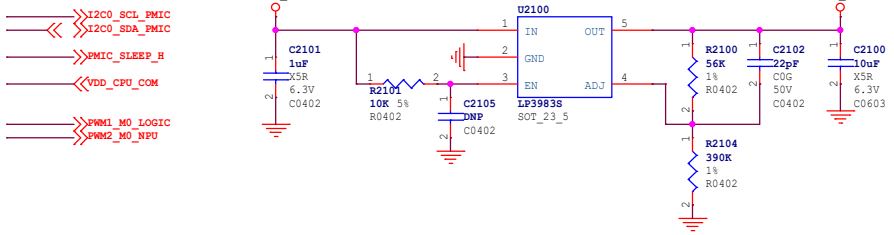
机箱风扇



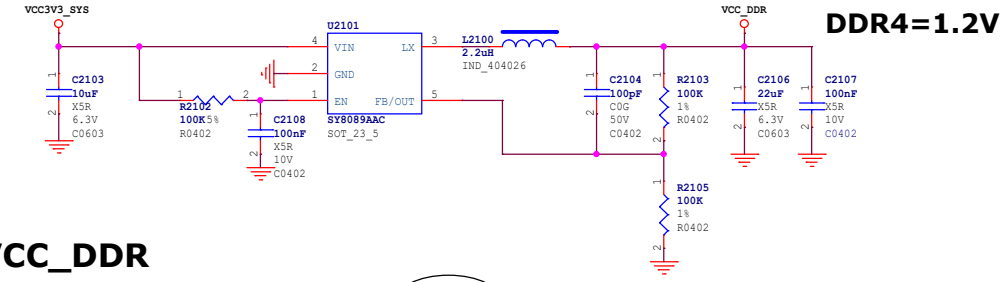
SATA Power

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	20.Power_DC IN				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	17 of 37

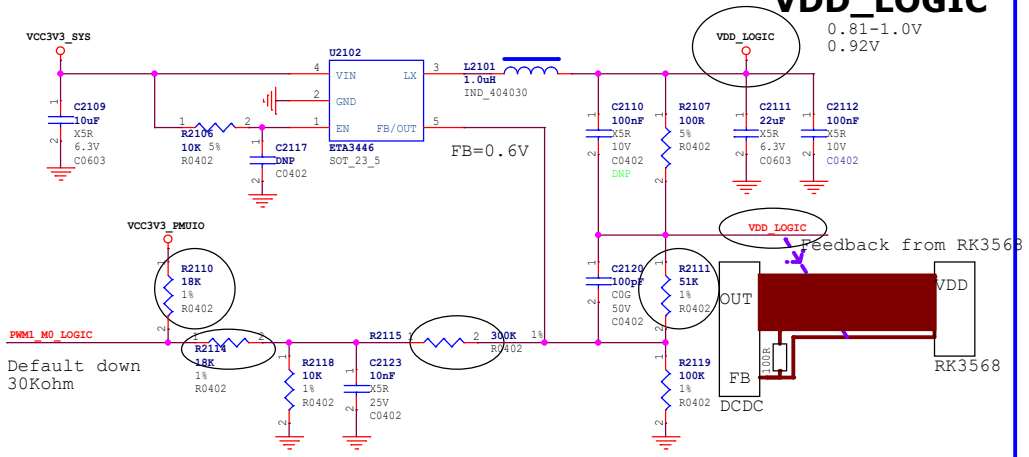


VDDA_0V9

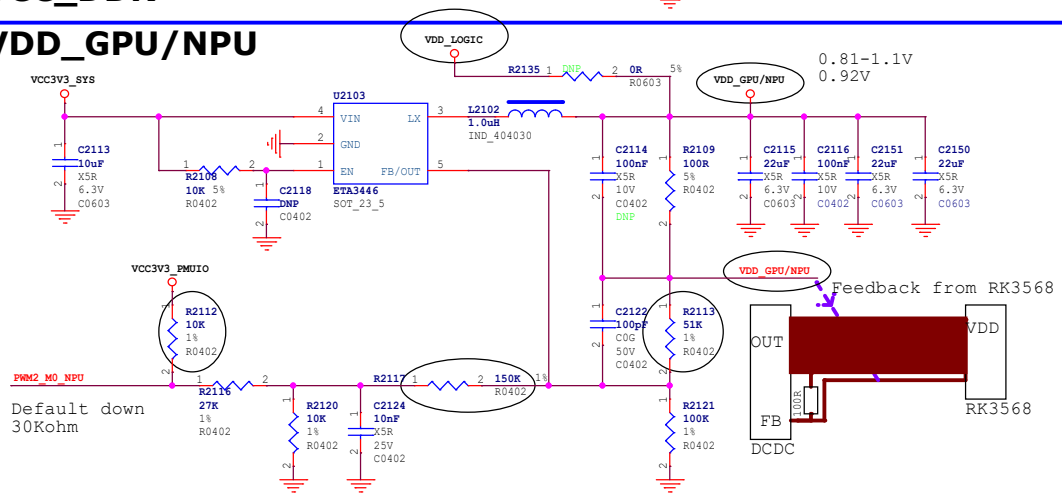


VCC_DDR

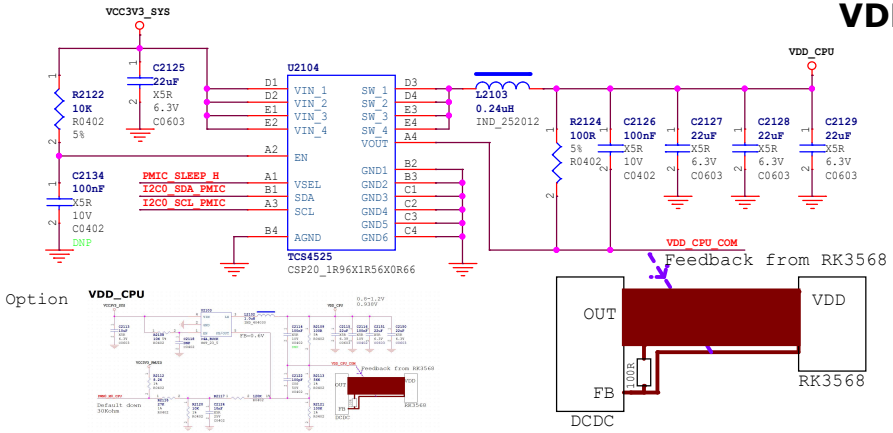
VDD_LOGIC



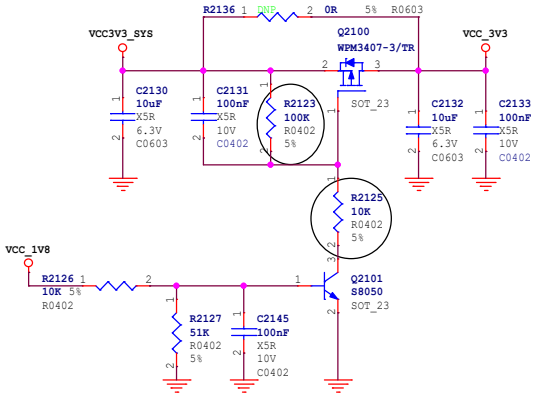
VDD_GPU/NPU



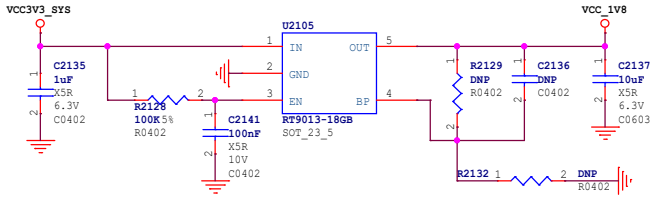
VDD_CPU



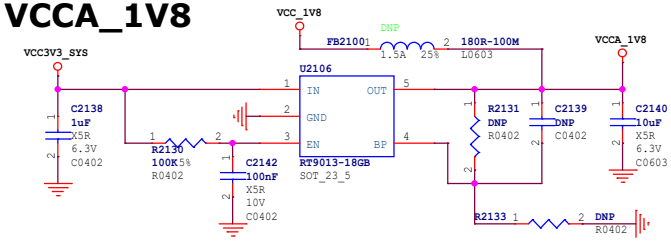
VCC_3V3



VCC_1V8

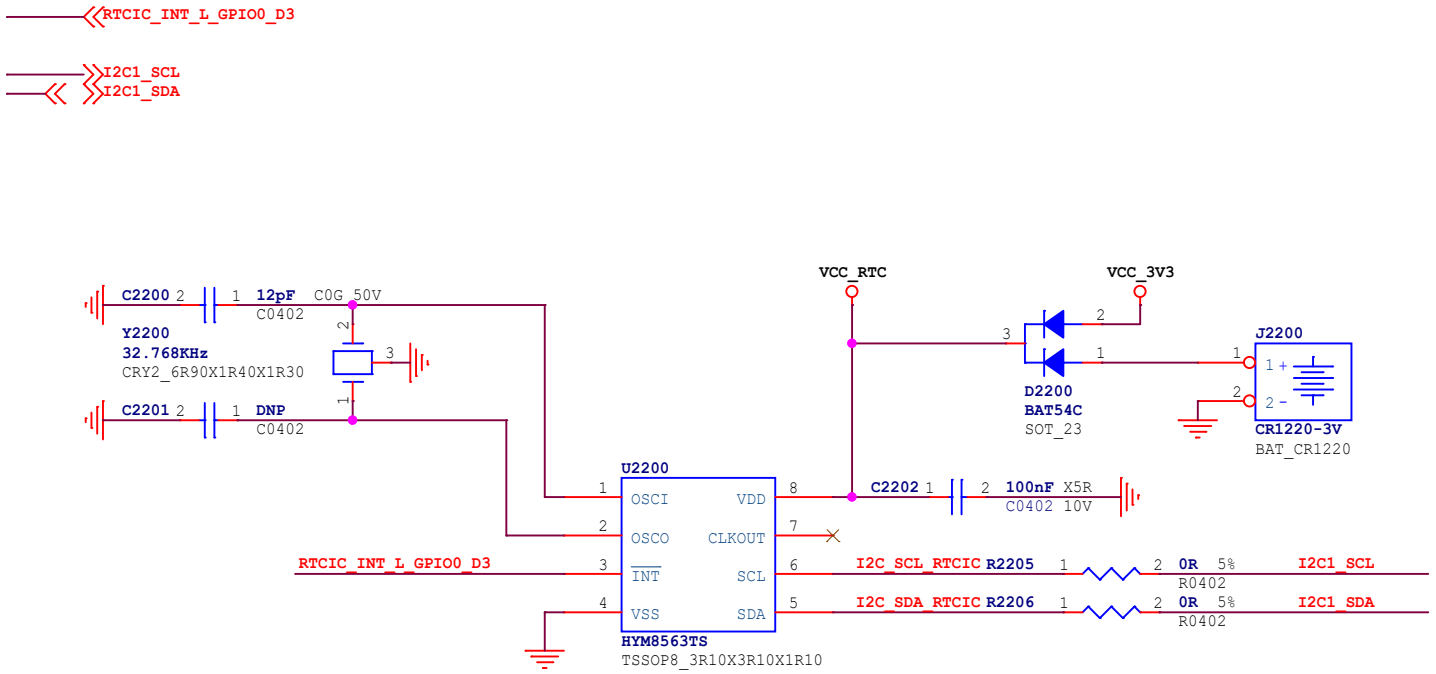


VCCA_1V8



Rockchip Confidential

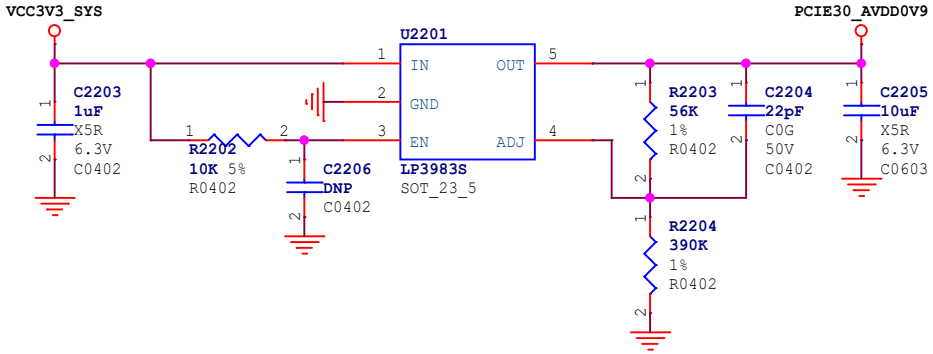
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	21.Power_DiscretePower				
Date:	Monday, December 21, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	18 of 37



Address:Read A3H,Write A2H

RTC IC

Back-up Power



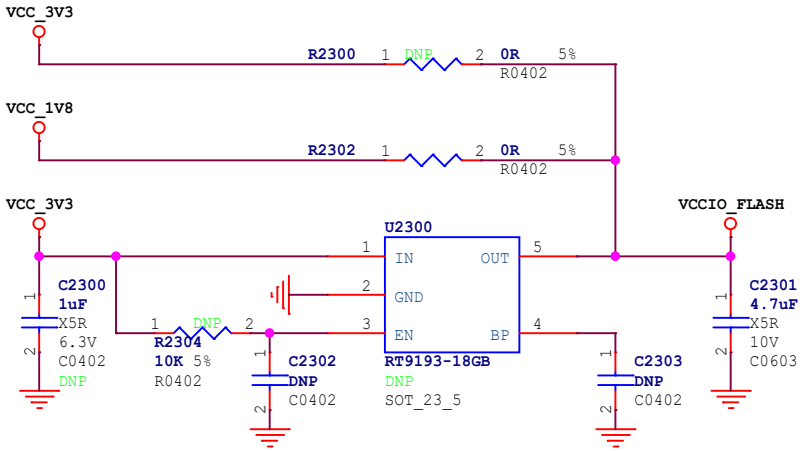
Rockchip Confidential

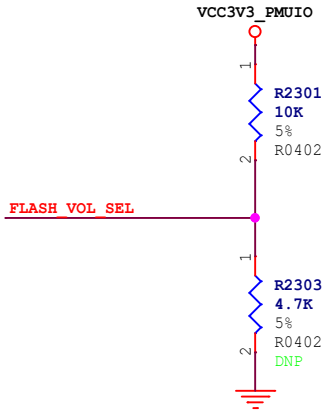
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	22.Power_other				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	19 of 37

FLASH_VOL_SEL

Flash Power Manage

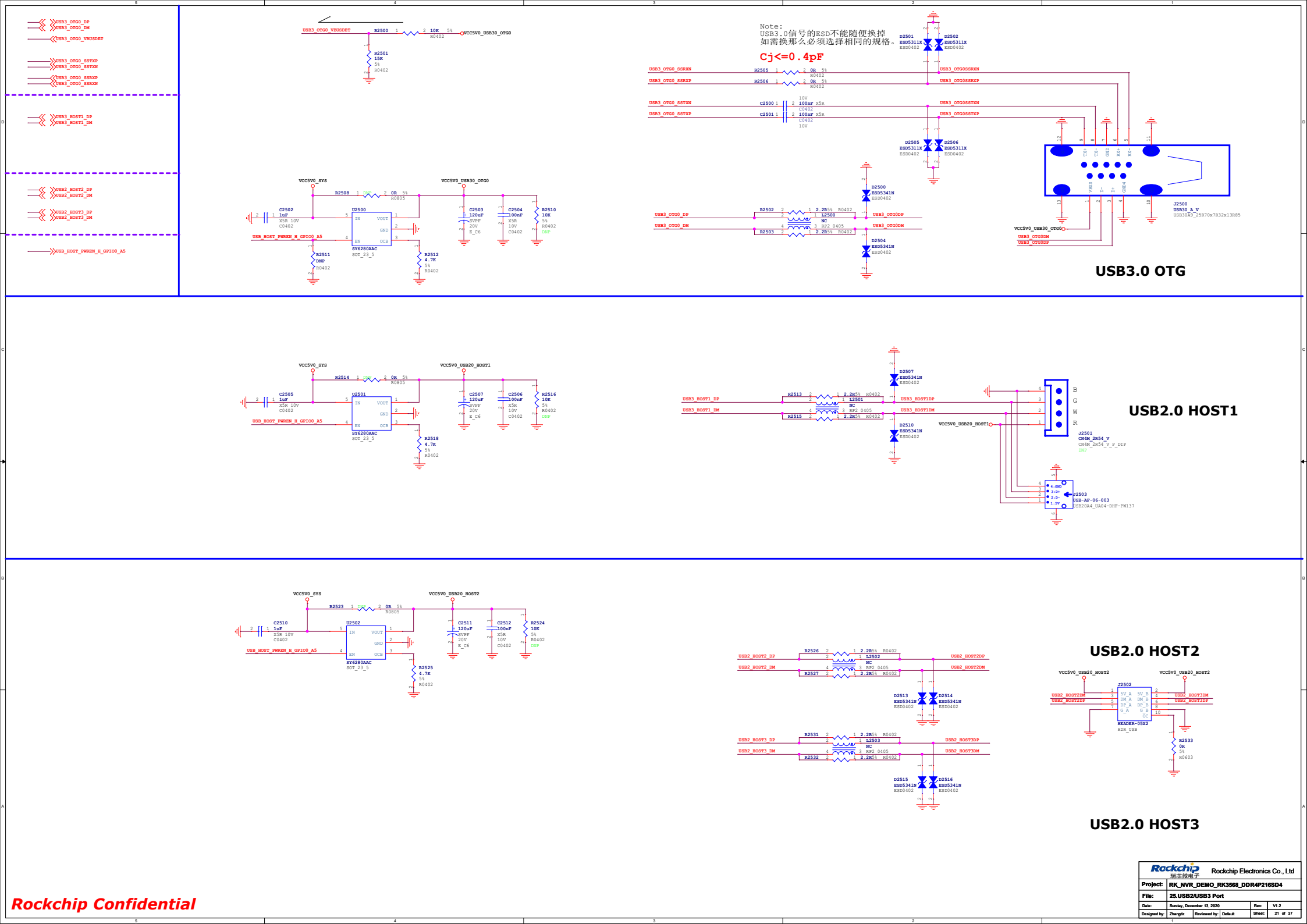
	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



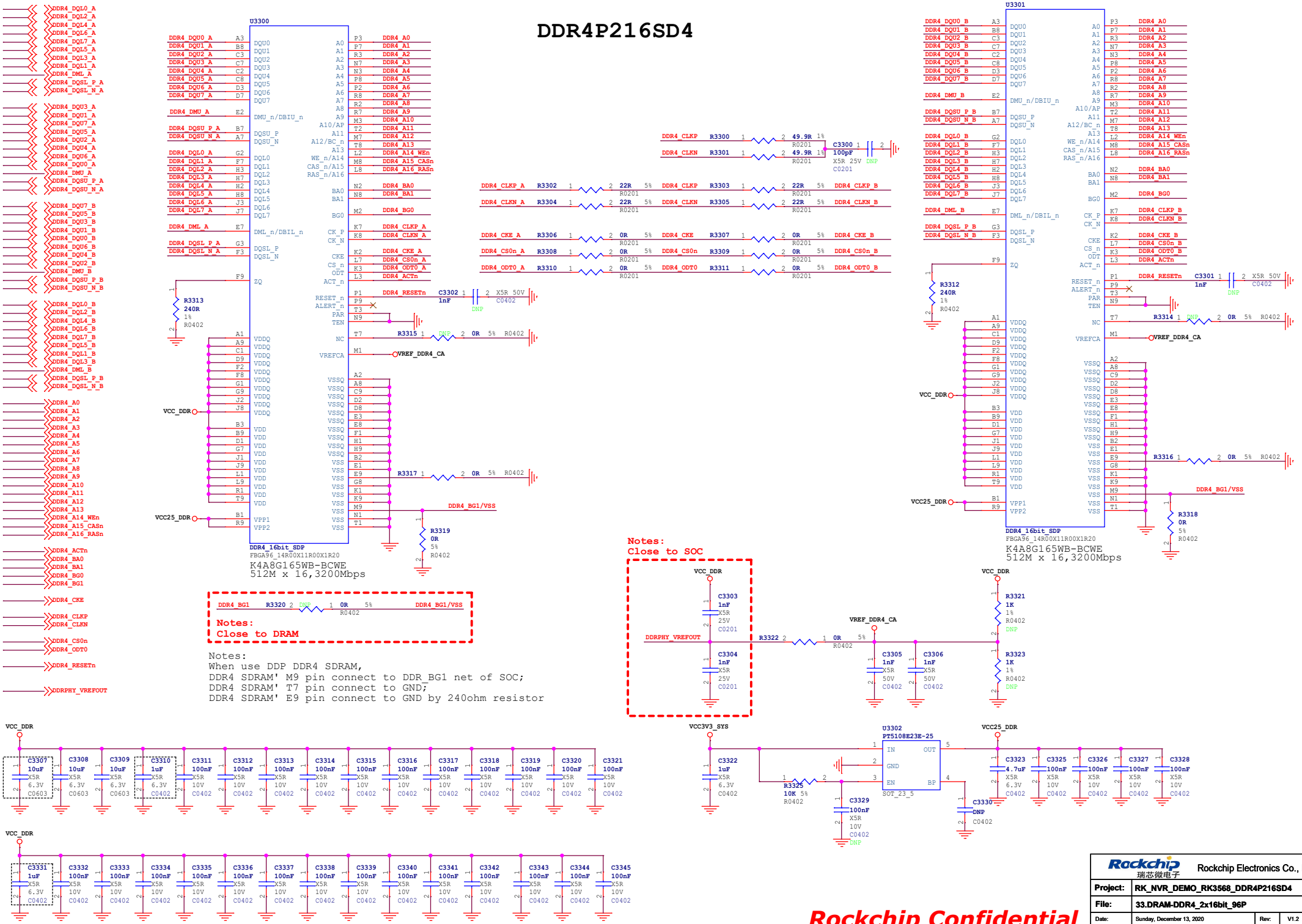


Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

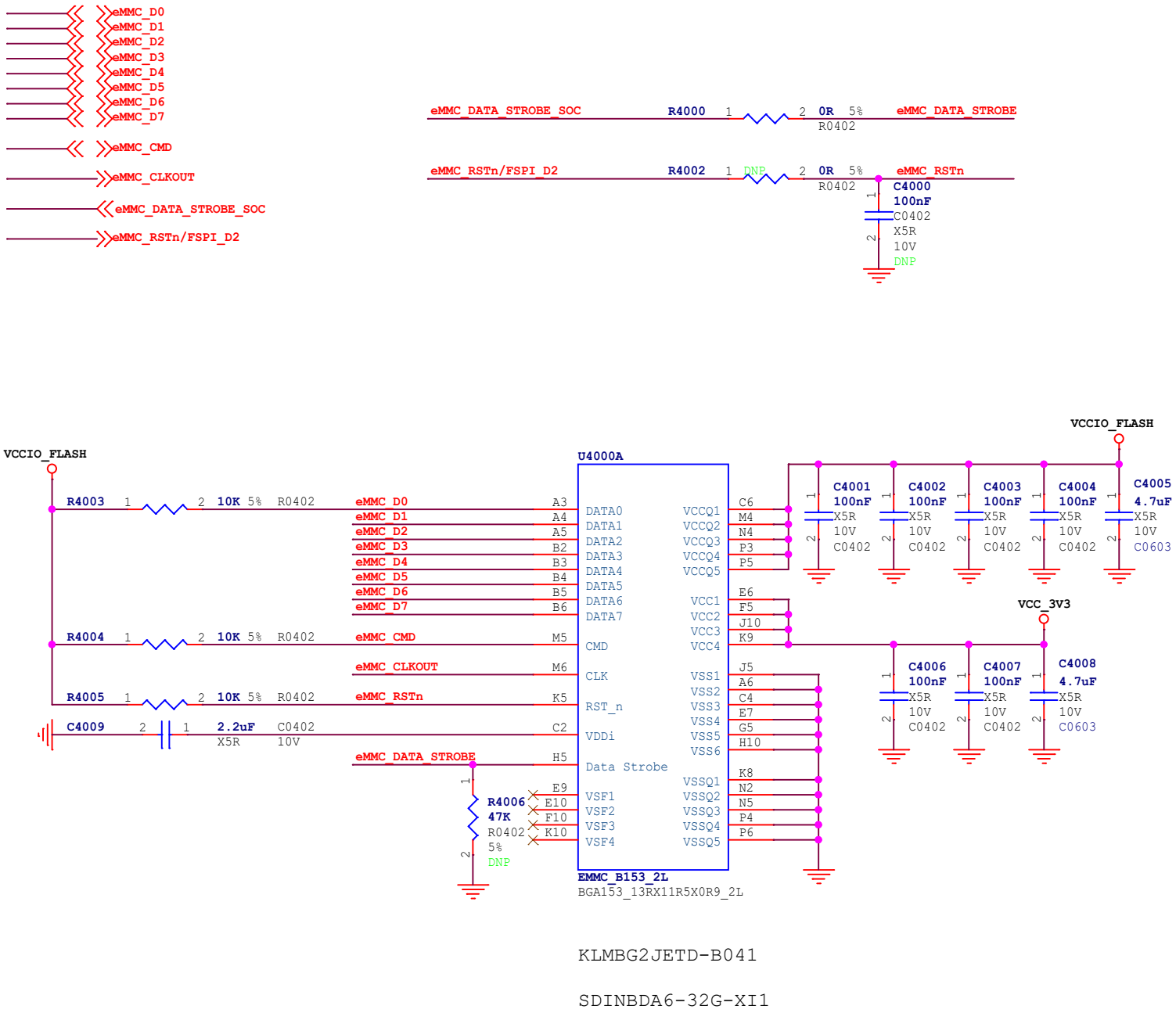
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	23.Power_Flash Power Manage				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	20 of 37


USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_VBUSDET
USB3_OTG0_SSTXP
USB3_OTG0_SSTXN
USB3_OTG0_SSRXP
USB3_OTG0_SSRXN
USB3_HOST1_DP
USB3_HOST1_DM
USB2_HOST2_DP
USB2_HOST2_DM
USB2_HOST3_DP
USB2_HOST3_DM
USB_HOST_PWREN_H_GPIO0_A5
USB3_OTG_VBUSDET
R2500 10K 5% R0402
VCC5V0_USB30_OTG0
R2501 15K 5% R0402
Note:
USB3.0信号的ESD不能随便换掉
如需换那么必须选择相同的规格。
Cj<=0.4pF
D2501 ESD5311X
D2502 ESD5311X
D2505 ESD5311X
D2506 ESD5311X
R2505 0R 5% R0402
R2506 0R 5% R0402
C2500 100nF X5R C0402 10V
C2501 100nF X5R C0402 10V
D2500 ESD5341N
D2504 ESD5341N
R2502 2.2R 5% R0402
R2503 2.2R 5% R0402
L2500 NC RP2 0405
J2500 USB30_A_V
USB30A9_25R70x7R32x13R85
VCC5V0_SYS
VCC5V0_USB30_OTG0
R2508 DNP 0R 5% R0805
C2502 1uF X5R 10V C0402
U2500 SY6280AAC SOT_23_5
C2503 120uF SVPF 20V E_C6
C2504 100nF X5R 10V C0402
R2510 10K 5% R0402 DNP
R2511 DNP R0402
R2512 4.7K 5% R0402
USB3.0 OTG
VCC5V0_SYS
VCC5V0_USB20_HOST1
R2514 DNP 0R 5% R0805
C2505 1uF X5R 10V C0402
U2501 SY6280AAC SOT_23_5
C2507 120uF SVPF 20V E_C6
C2506 100nF X5R 10V C0402
R2516 10K 5% R0402 DNP
R2518 4.7K 5% R0402
D2507 ESD5341N
D2510 ESD5341N
R2513 2.2R 5% R0402
R2515 2.2R 5% R0402
L2501 NC RP2 0405
J2501 CN4M_2R54_V
CN4M_2R54_V_P_DIP
DNP
J2503 USB-AF-06-003
USB20A4_UA04-DHF-PW137
USB2.0 HOST1
VCC5V0_SYS
VCC5V0_USB20_HOST2
R2523 DNP 0R 5% R0805
C2510 1uF X5R 10V C0402
U2502 SY6280AAC SOT_23_5
C2511 120uF SVPF 20V E_C6
C2512 100nF X5R 10V C0402
R2524 10K 5% R0402 DNP
R2525 4.7K 5% R0402
D2513 ESD5341N
D2514 ESD5341N
R2526 2.2R 5% R0402
R2527 2.2R 5% R0402
L2502 NC RP2 0405
D2515 ESD5341N
D2516 ESD5341N
R2531 2.2R 5% R0402
R2532 2.2R 5% R0402
L2503 NC RP2 0405
J2502 HEADER-05X2 HDR_USB
R2533 0R 5% R0603
USB2.0 HOST2
USB2.0 HOST3
Rockchip Confidential
Rockchip Electronics Co., Ltd
瑞芯微电子
Project: RK_NVR_DEMO_RK3568_DDR4P216SD4
File: 25.USB2/USB3 Port
Date: Sunday, December 13, 2020
Rev: V1.2
Designed by: Zhangtz
Reviewed by: Default
Sheet: 21 of 37

DDR4P216SD4

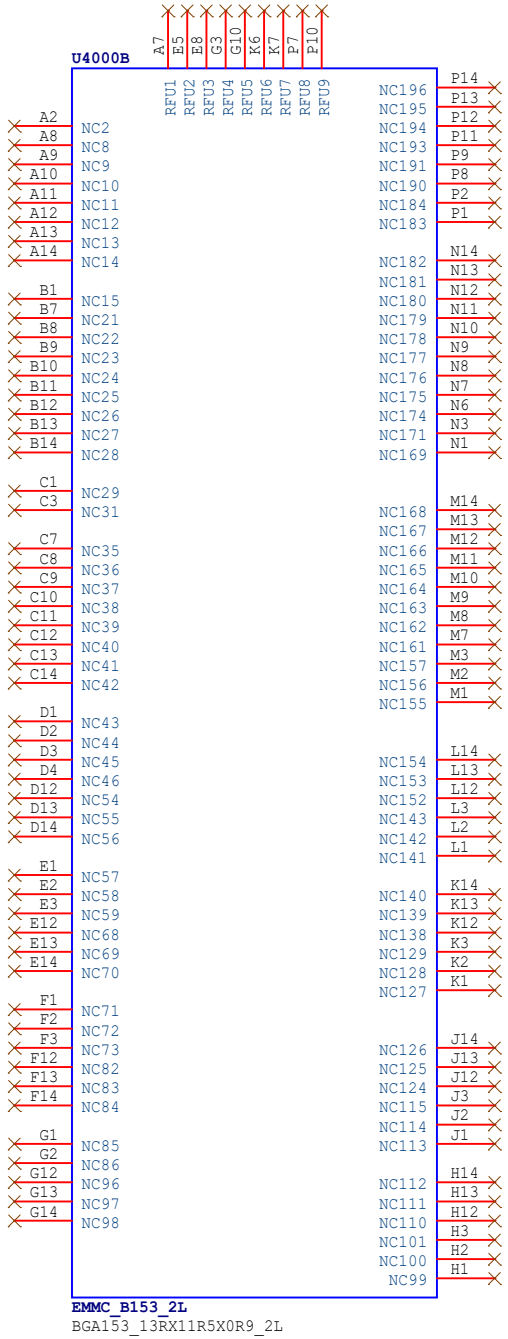


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	33.DRAM-DDR4_2x16bit_96P				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	22 of 37

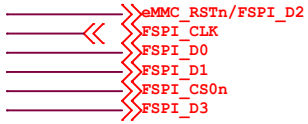


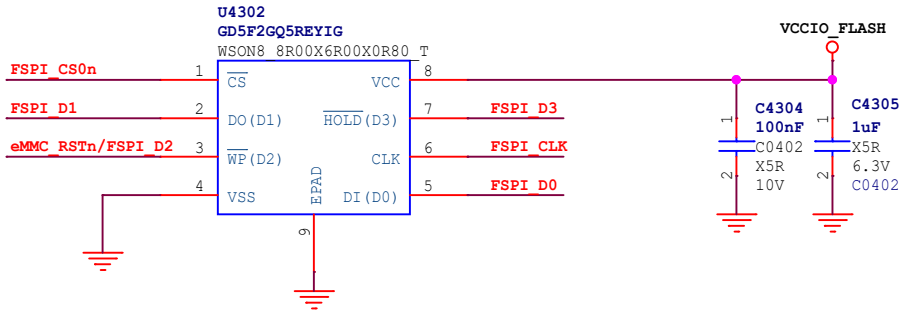
KLMBG2JETD-B041

SDINBDA6-32G-XI1



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	40.Flash-eMMC Flash				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	23 of 37

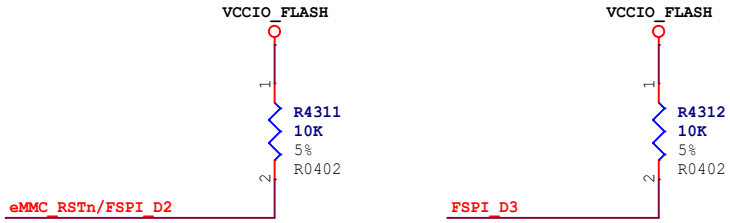




Default: 1.8V

SPI Nor: W25Q256JWEIQ 1.8V

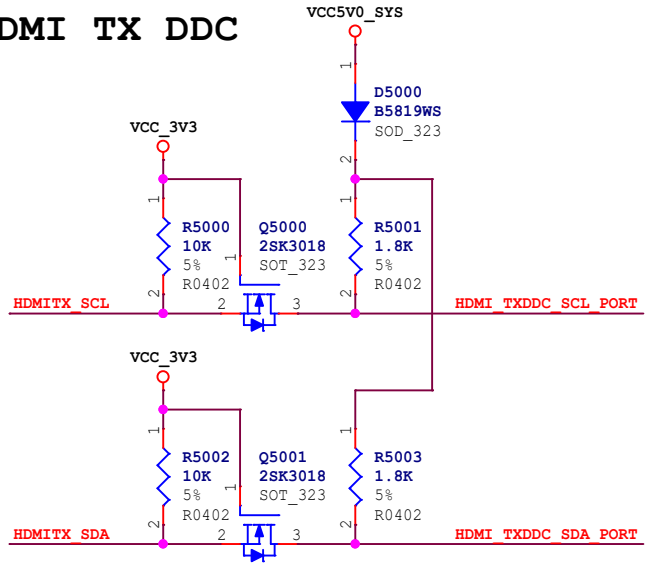
W25Q256FV, GD25Q256D 3.3V



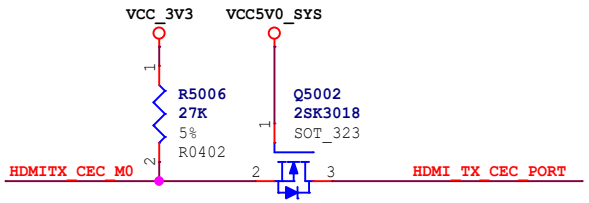
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	43.Flash-SPI FLASH				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	24 of 37

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMITX_SCL
HDMITX_SDA
HDMITX_CEC_M0
HDMI_TX_HPDIN

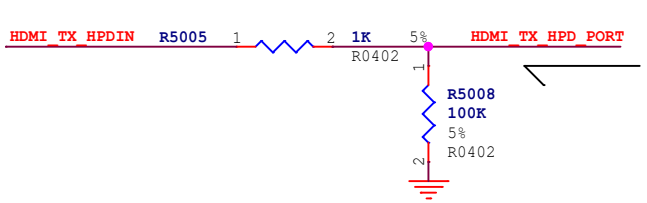
HDMI TX DDC



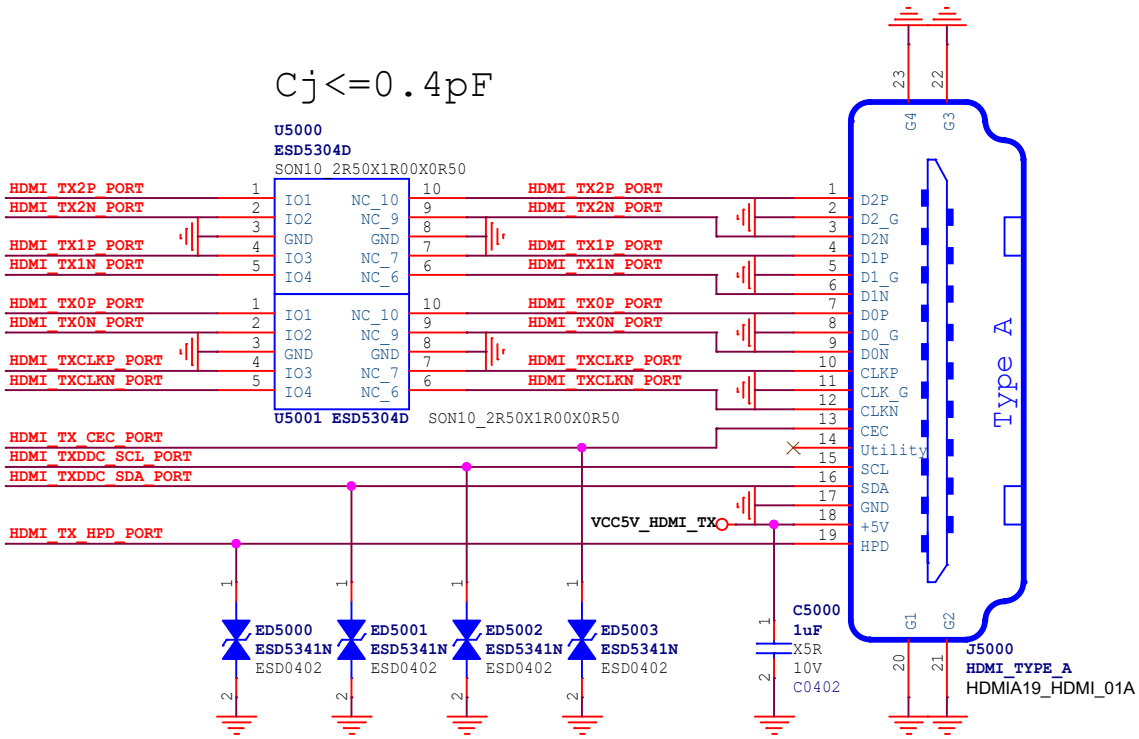
HDMI TX CEC

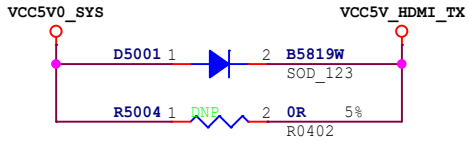


HDMI TX HPD



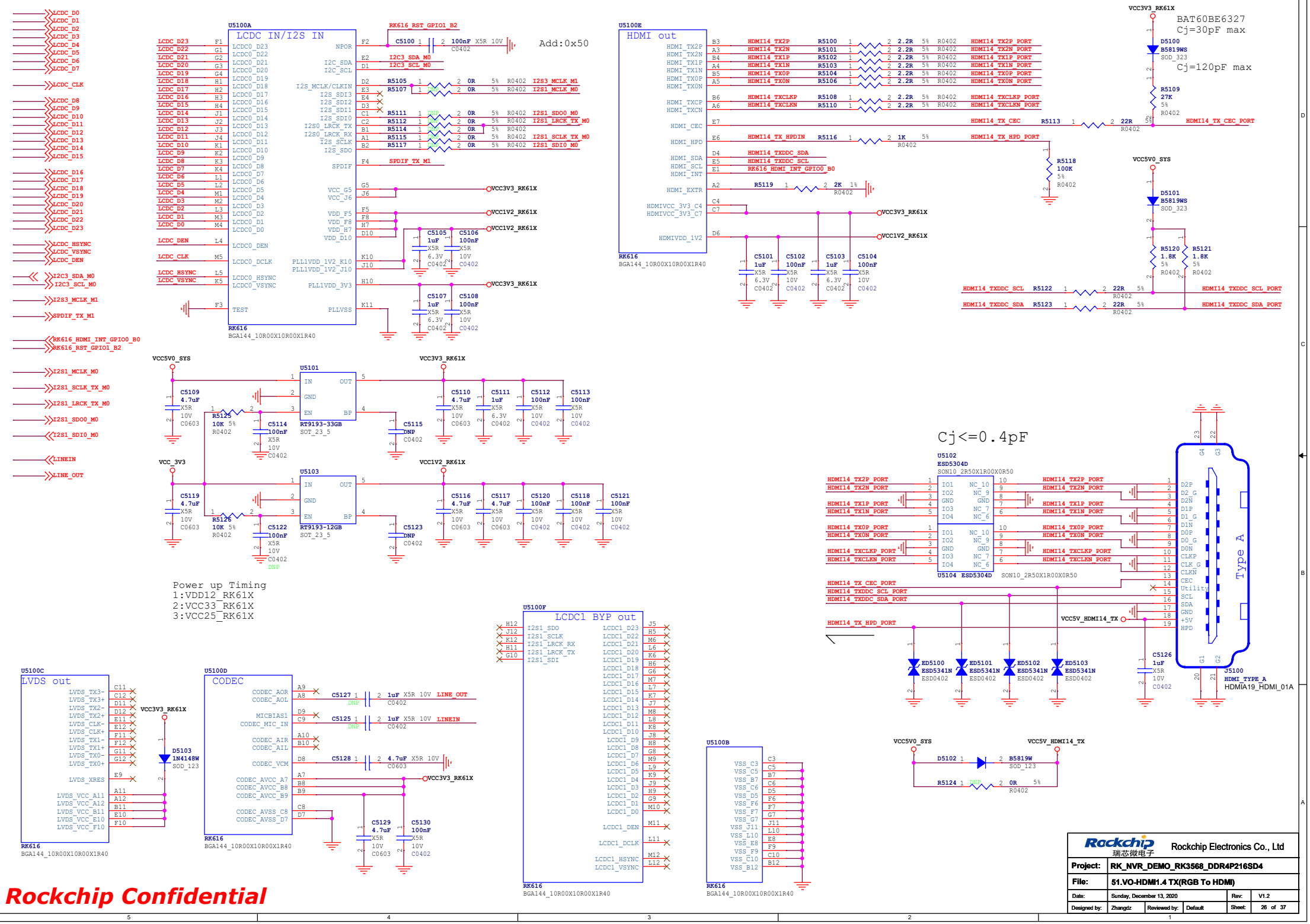
Cj<=0.4pF

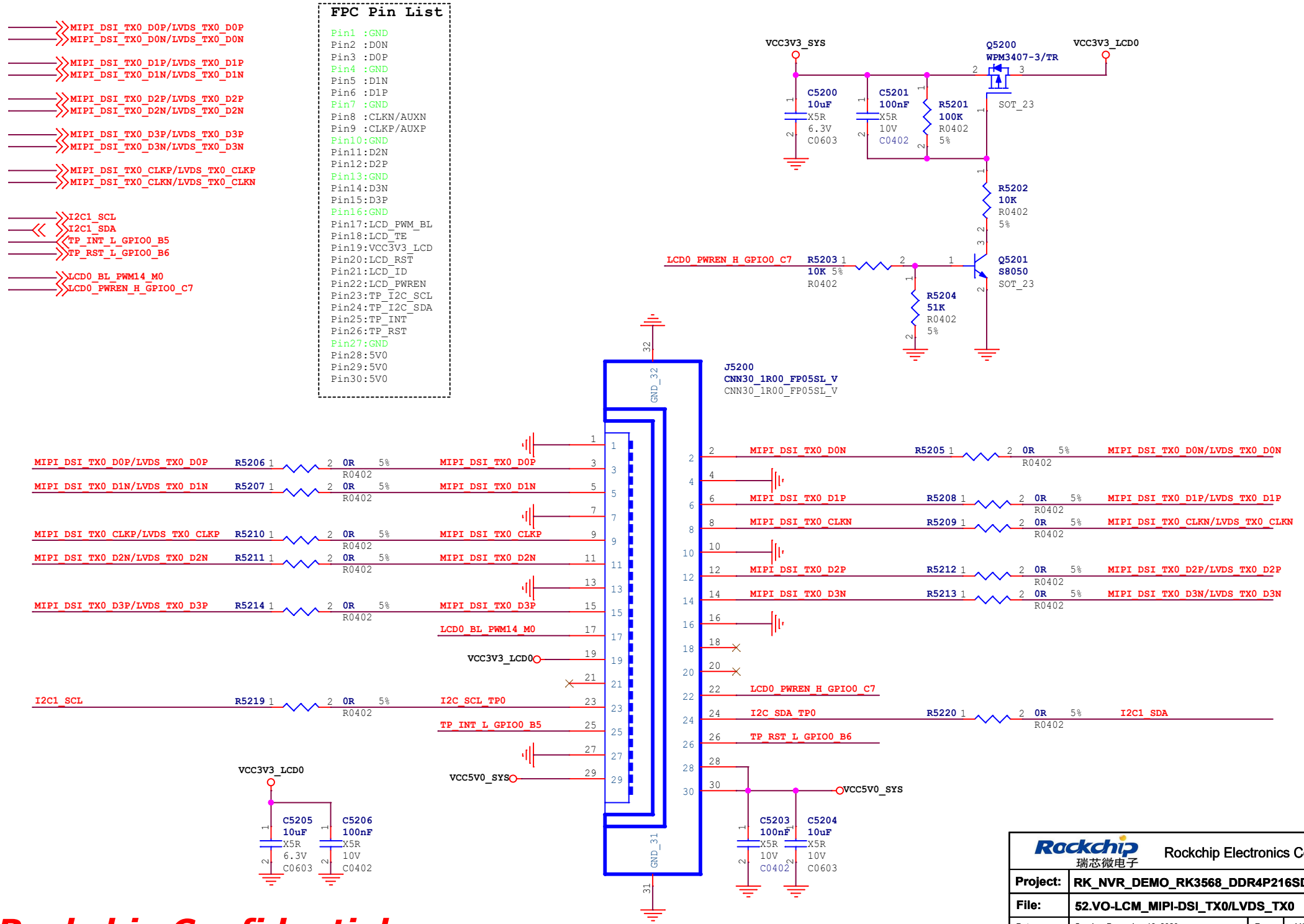




Rockchip Confidential

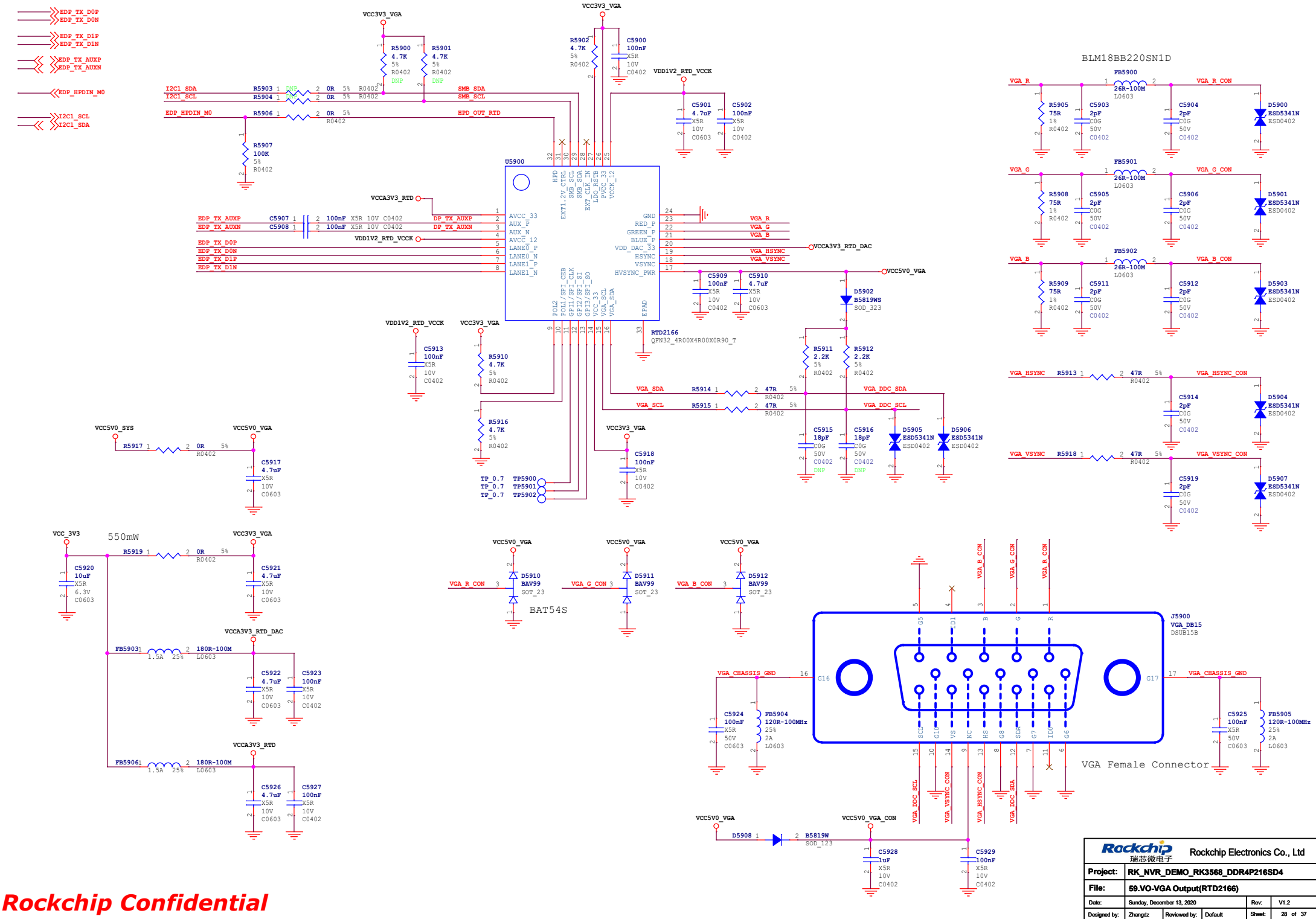
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	50.VO-HDMI2.0 TX				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	25 of 37

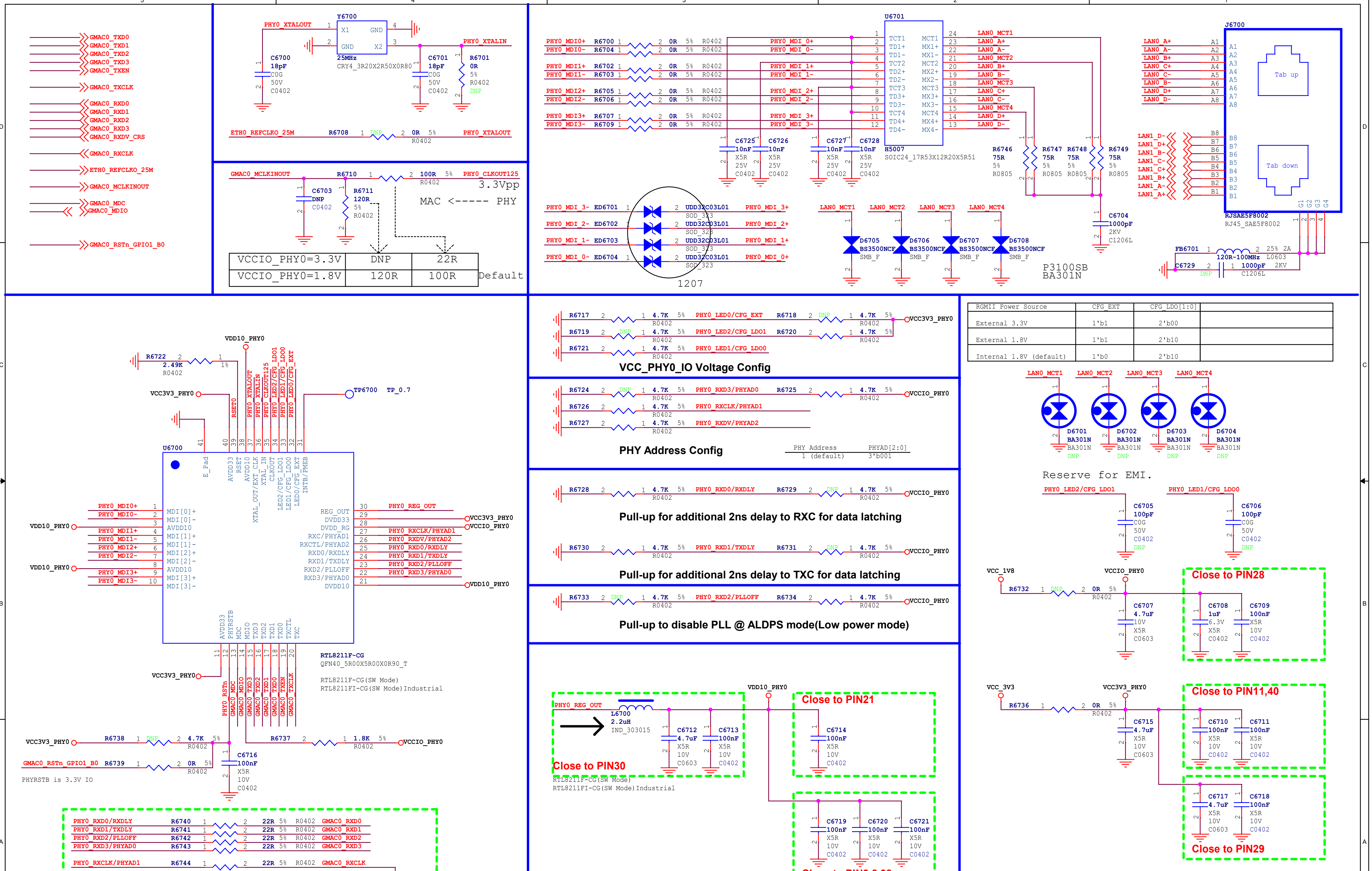

LCDC_D0
LCDC_D1
LCDC_D2
LCDC_D3
LCDC_D4
LCDC_D5
LCDC_D6
LCDC_D7
LCDC_CLK
LCDC_D8
LCDC_D9
LCDC_D10
LCDC_D11
LCDC_D12
LCDC_D13
LCDC_D14
LCDC_D15
LCDC_D16
LCDC_D17
LCDC_D18
LCDC_D19
LCDC_D20
LCDC_D21
LCDC_D22
LCDC_D23
LCDC_HSYNC
LCDC_VSYNC
LCDC_DEN
I2C3_SDA_M0
I2C3_SCL_M0
I2S3_MCLK_M1
SPDIF_TX_M1
RK616_HDMI_INT_GPIO0_B0
RK616_RST_GPIO1_B2
I2S1_MCLK_M0
I2S1_SCLK_TX_M0
I2S1_LRCK_TX_M0
I2S1_SDO0_M0
I2S1_SDI0_M0
LINEIN
LINE_OUT
U5100A
LCDC IN/I2S IN
RK616
BGA144_10R00X10R00X1R40
RK616_RST_GPIO1_B2
C5100 100nF X5R 10V C0402
Add:0x50
I2C3_SDA_M0
I2C3_SCL_M0
R5105 0R R5107 0R I2S3_MCLK_M1 I2S1_MCLK_M0
R5111 DNP R5112 0R R5114 0R R5115 0R R5117 0R
I2S1_SDO0_M0 I2S1_LRCK_TX_M0 I2S1_SCLK_TX_M0 I2S1_SDI0_M0
SPDIF_TX_M1
VCC3V3_RK61X
VCC1V2_RK61X
C5105 1uF X5R 6.3V C0402
C5106 100nF X5R 10V C0402
C5107 1uF X5R 6.3V C0402
C5108 100nF X5R 10V C0402
U5100E
HDMI out
RK616
BGA144_10R00X10R00X1R40
HDMI14_TX2P HDMI14_TX2N HDMI14_TX1P HDMI14_TX1N HDMI14_TX0P HDMI14_TX0N HDMI14_TXCLKP HDMI14_TXCLKN
R5100 R5101 R5102 R5103 R5104 R5106 R5108 R5110
2.2R 5% R0402
HDMI14_TX_CEC R5113 22R R0402 HDMI14_TX_CEC_PORT
HDMI14_TX_HPDIN R5116 1K R0402 HDMI14_TX_HPD_PORT
HDMI14_TXDDC_SDA HDMI14_TXDDC_SCL RK616_HDMI_INT_GPIO0_B0
R5119 2K 1% R0402
C5101 1uF X5R 6.3V C0402
C5102 100nF X5R 10V C0402
C5103 1uF X5R 6.3V C0402
C5104 100nF X5R 10V C0402
VCC3V3_RK61X
BAT60BE6327
Cj=30pF max
D5100 B5819WS SOD_323
Cj=120pF max
R5109 27K 5% R0402
R5118 100K 5% R0402
VCC5V0_SYS
D5101 B5819WS SOD_323
R5120 1.8K 5% R0402
R5121 1.8K 5% R0402
HDMI14_TXDDC_SCL R5122 22R R0402 HDMI14_TXDDC_SCL_PORT
HDMI14_TXDDC_SDA R5123 22R R0402 HDMI14_TXDDC_SDA_PORT
VCC5V0_SYS
VCC3V3_RK61X
U5101
RT9193-33GB
SOT_23_5
C5109 4.7uF X5R 10V C0603
R5125 10K 5% R0402
C5114 100nF X5R 10V C0402
C5115 DNP C0402
C5110 4.7uF X5R 10V C0603
C5111 1uF X5R 6.3V C0402
C5112 100nF X5R 10V C0402
C5113 100nF X5R 10V C0402
VCC_3V3
VCC1V2_RK61X
U5103
RT9193-12GB
SOT_23_5
C5119 4.7uF X5R 10V C0603
R5126 10K 5% R0402
C5122 100nF X5R 10V C0402 DNP
C5123 DNP C0402
C5116 4.7uF X5R 10V C0603
C5117 4.7uF X5R 10V C0603
C5120 100nF X5R 10V C0402
C5118 100nF X5R 10V C0402
C5121 100nF X5R 10V C0402
Power up Timing
1:VDD12_RK61X
2:VCC33_RK61X
3:VCC25_RK61X
Cj<=0.4pF
U5102
ESD5304D
SON10_2R50X1R00X0R50
U5104 ESD5304D SON10_2R50X1R00X0R50
HDMI14_TX2P_PORT HDMI14_TX2N_PORT HDMI14_TX1P_PORT HDMI14_TX1N_PORT HDMI14_TX0P_PORT HDMI14_TX0N_PORT HDMI14_TXCLKP_PORT HDMI14_TXCLKN_PORT
HDMI14_TX_CEC_PORT
HDMI14_TXDDC_SCL_PORT
HDMI14_TXDDC_SDA_PORT
HDMI14_TX_HPD_PORT
VCC5V_HDMI14_TX
ED5100 ESD5341N ESD0402
ED5101 ESD5341N ESD0402
ED5102 ESD5341N ESD0402
ED5103 ESD5341N ESD0402
C5126 1uF X5R 10V C0402
Type A
J5100
HDMI_TYPE_A
HDMIA19_HDMI_01A
U5100C
LVDS out
RK616
BGA144_10R00X10R00X1R40
VCC3V3_RK61X
D5103 1N4148W SOD_123
U5100D
CODEC
RK616
BGA144_10R00X10R00X1R40
C5127 DNP 1uF X5R 10V C0402 LINE_OUT
C5125 DNP 1uF X5R 10V C0402 LINEIN
C5128 4.7uF X5R 10V C0603
VCC3V3_RK61X
C5129 4.7uF X5R 10V C0603
C5130 100nF X5R 10V C0402
U5100F
LCDC1 BYP out
RK616
BGA144_10R00X10R00X1R40
U5100B
RK616
BGA144_10R00X10R00X1R40
VCC5V0_SYS
VCC5V_HDMI14_TX
D5102 B5819W SOD_123
R5124 DNP 0R 5% R0402
Rockchip Confidential
Rockchip Electronics Co., Ltd
瑞芯微电子
Project: RK_NVR_DEMO_RK3568_DDR4P216SD4
File: 51.VO-HDMI1.4 TX(RGB To HDMI)
Date: Sunday, December 13, 2020
Rev: V1.2
Designed by: Zhangdz
Reviewed by: Default
Sheet: 26 of 37



Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	52.VO-LCM_MIPI-DSI_TX0/LVDS_TX0				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	27 of 37


EDP_TX_D0P
EDP_TX_D0N
EDP_TX_D1P
EDP_TX_D1N
EDP_TX_AUXP
EDP_TX_AUXN
EDP_HPDIN_M0
I2C1_SCL
I2C1_SDA
VCC3V3_VGA
R5900 4.7K 5% R0402 DNP
R5901 4.7K 5% R0402 DNP
R5902 4.7K 5% R0402
C5900 100nF X5R 10V C0402
VDD1V2_RTD_VCCK
C5901 4.7uF X5R 10V C0603
C5902 100nF X5R 10V C0402
R5903 DNP
R5904 DNP
0R 5% R0402
SMB_SDA
SMB_SCL
R5906 0R 5% R0402
HPD_OUT_RTD
R5907 100K 5% R0402
U5900
VCCA3V3_RTD
C5907 100nF X5R 10V C0402
C5908 100nF X5R 10V C0402
DP_TX_AUXP
DP_TX_AUXN
AVCC_33
AUX_P
AUX_N
AVCC_12
LANE0_P
LANE0_N
LANE1_P
LANE1_N
GND
RED_P
GREEN_P
BLUE_P
VDD_DAC_33
HSYNC
VSYNC
HVSYNC_PWR
EPAD
VGA_R
VGA_G
VGA_B
VGA_HSYNC
VGA_VSYNC
VCCA3V3_RTD_DAC
C5909 100nF X5R 10V C0402
C5910 4.7uF X5R 10V C0603
VCC5V0_VGA
D5902 B5819WS SOD_323
RTD2166
QFN32_4R00X4R00X0R90_T
C5913 100nF X5R 10V C0402
R5910 4.7K 5% R0402
R5916 4.7K 5% R0402
C5918 100nF X5R 10V C0402
R5911 2.2K 5% R0402
R5912 2.2K 5% R0402
VGA_SDA
VGA_SCL
R5914 47R 5% R0402
R5915 47R 5% R0402
VGA_DDC_SDA
VGA_DDC_SCL
C5915 18pF C0G 50V C0402 DNP
C5916 18pF C0G 50V C0402 DNP
D5905 ESD5341N ESD0402
D5906 ESD5341N ESD0402
TP_0.7 TP5900
TP_0.7 TP5901
TP_0.7 TP5902
BLM18BB220SN1D
VGA_R
VGA_G
VGA_B
FB5900 26R-100M L0603
FB5901 26R-100M L0603
FB5902 26R-100M L0603
R5905 75R 1% R0402
R5908 75R 1% R0402
R5909 75R 1% R0402
C5903 2pF C0G 50V C0402
C5905 2pF C0G 50V C0402
C5911 2pF C0G 50V C0402
C5904 2pF C0G 50V C0402
C5906 2pF C0G 50V C0402
C5912 2pF C0G 50V C0402
VGA_R_CON
VGA_G_CON
VGA_B_CON
D5900 ESD5341N ESD0402
D5901 ESD5341N ESD0402
D5903 ESD5341N ESD0402
VGA_HSYNC
VGA_VSYNC
R5913 47R 5% R0402
R5918 47R 5% R0402
C5914 2pF C0G 50V C0402
C5919 2pF C0G 50V C0402
VGA_HSYNC_CON
VGA_VSYNC_CON
D5904 ESD5341N ESD0402
D5907 ESD5341N ESD0402
VCC5V0_SYS
R5917 0R 5% R0402
C5917 4.7uF X5R 10V C0603
VCC_3V3
550mW
R5919 0R 5% R0402
C5920 10uF X5R 6.3V C0603
C5921 4.7uF X5R 10V C0603
VCCA3V3_RTD_DAC
FB5903 180R-100M 1.5A 25% L0603
C5922 4.7uF X5R 10V C0603
C5923 100nF X5R 10V C0402
VCCA3V3_RTD
FB5906 180R-100M 1.5A 25% L0603
C5926 4.7uF X5R 10V C0603
C5927 100nF X5R 10V C0402
VGA_R_CON
VGA_G_CON
VGA_B_CON
D5910 BAV99 SOT_23
D5911 BAV99 SOT_23
D5912 BAV99 SOT_23
BAT54S
J5900 VGA_DB15 DSUB15B
VGA Female Connector
VGA_CHASSIS_GND
C5924 100nF X5R 50V C0603
FB5904 120R-100MHz 25% 2A L0603
C5925 100nF X5R 50V C0603
FB5905 120R-100MHz 25% 2A L0603
VCC5V0_VGA_CON
D5908 B5819W SOD_123
C5928 1uF X5R 10V C0402
C5929 100nF X5R 10V C0402
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK_NVR_DEMO_RK3568_DDR4P216SD4
File: 59.VO-VGA Output(RTD2166)
Date: Sunday, December 13, 2020
Rev: V1.2
Designed by: Zhangdz
Reviewed by: Default
Sheet: 28 of 37



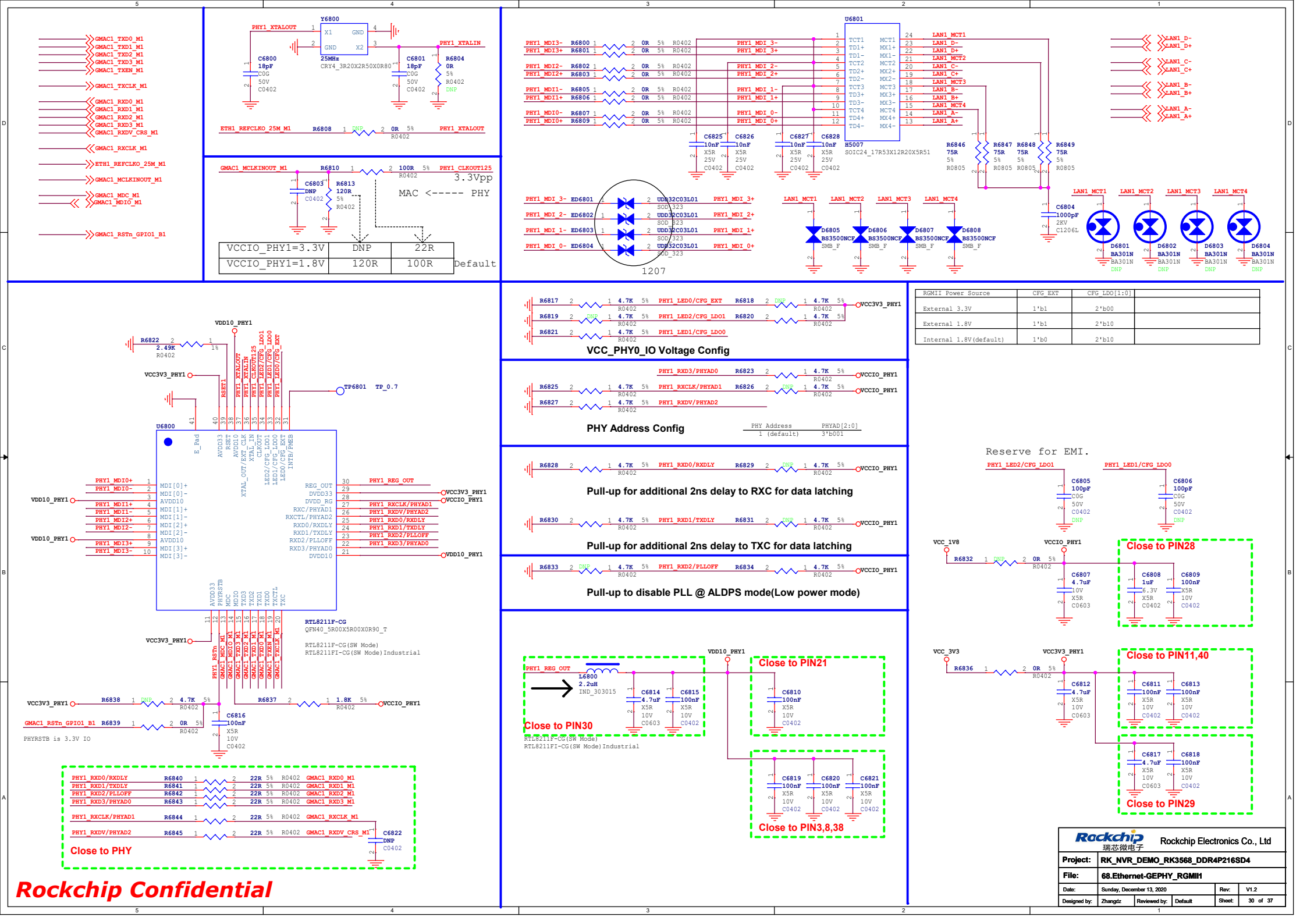
	DNP	22R	
VCCIO_PHY0=3.3V	DNP	22R	
VCCIO_PHY0=1.8V	120R	100R	Default

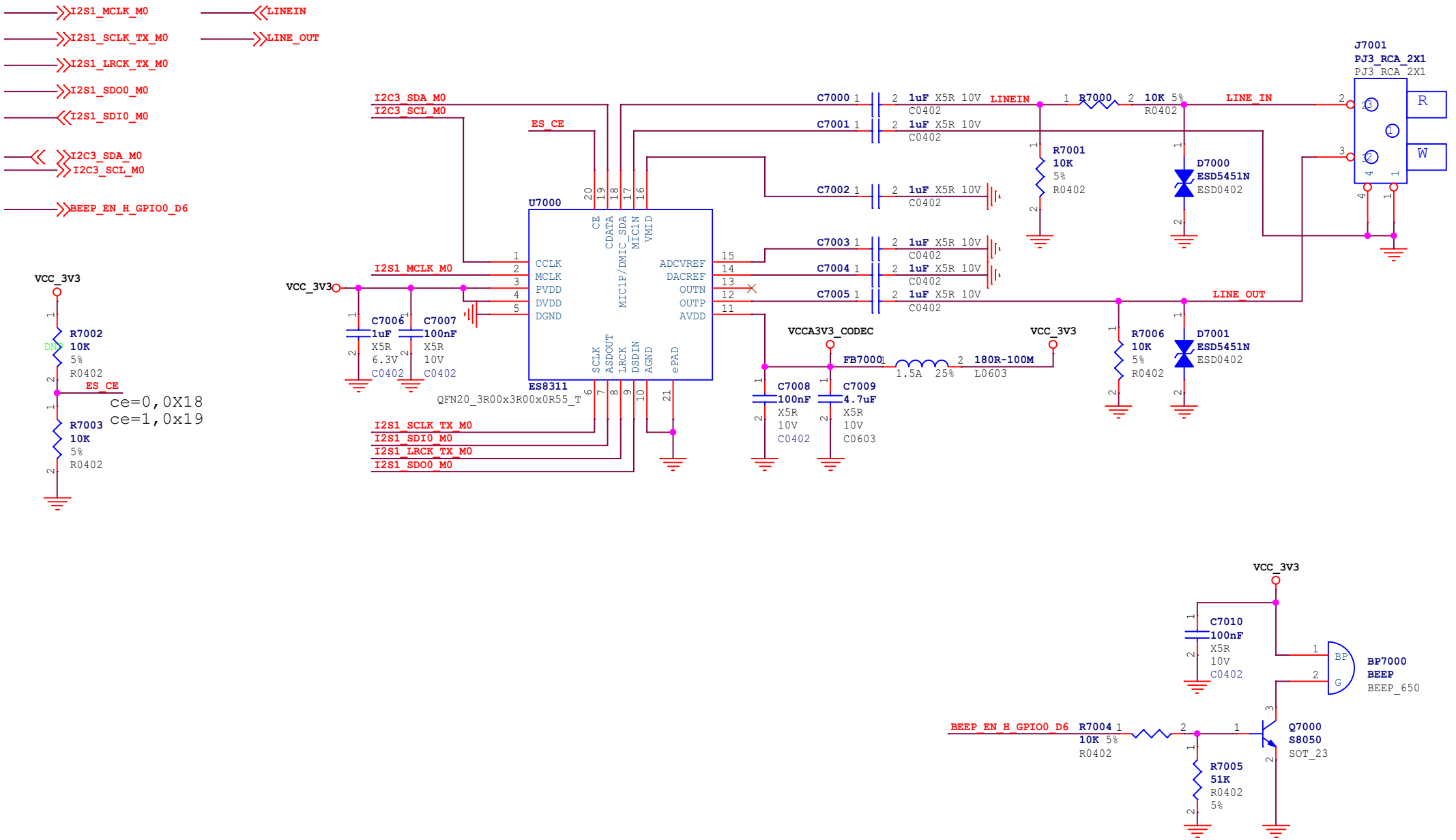
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V (default)	1'b0	2'b10

PHY Address	PHYAD[2:0]
1 (default)	3'b001

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	67.Ethernet-GEPHY_RGMII0				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	29 of 37

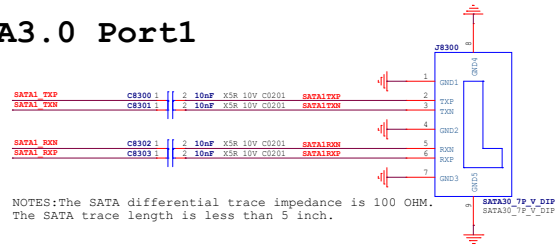

GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXDV_CRS_M1
GMAC1_RXCLK_M1
ETH1_REFCLKO_25M_M1
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO1_B1
Y6800
PHY1_XTALOUT
PHY1_XTALIN
25MHz
CRY4_3R20X2R50X0R80
C6800 18pF C0G 50V C0402
C6801 18pF C0G 50V C0402
R6804 0R 5% R0402 DNP
ETH1_REFCLKO_25M_M1 R6808 DNP 0R 5% R0402 PHY1_XTALOUT
GMAC1_MCLKINOUT_M1 R6810 100R 5% R0402 PHY1_CLKOUT125
C6803 DNP C0402
R6813 120R 5% R0402
3.3Vpp
MAC <----- PHY
VCCIO_PHY1=3.3V DNP 22R
VCCIO_PHY1=1.8V 120R 100R Default
U6801
PHY1_MDI3- R6800 0R 5% R0402 PHY1_MDI_3-
PHY1_MDI3+ R6801 0R 5% R0402 PHY1_MDI_3+
PHY1_MDI2- R6802 0R 5% R0402 PHY1_MDI_2-
PHY1_MDI2+ R6803 0R 5% R0402 PHY1_MDI_2+
PHY1_MDI1- R6805 0R 5% R0402 PHY1_MDI_1-
PHY1_MDI1+ R6806 0R 5% R0402 PHY1_MDI_1+
PHY1_MDI0- R6807 0R 5% R0402 PHY1_MDI_0-
PHY1_MDI0+ R6809 0R 5% R0402 PHY1_MDI_0+
TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-
MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-
LAN1_MCT1 LAN1_D- LAN1_D+ LAN1_MCT2 LAN1_C- LAN1_C+ LAN1_MCT3 LAN1_B- LAN1_B+ LAN1_MCT4 LAN1_A- LAN1_A+
C6825 10nF X5R 25V C0402
C6826 10nF X5R 25V C0402
C6827 10nF X5R 25V C0402
C6828 10nF X5R 25V C0402
H5007 SOIC24_17R53X12R20X5R51
R6846 75R 5% R0805
R6847 75R 5% R0805
R6848 75R 5% R0805
R6849 75R 5% R0805
PHY1_MDI_3- ED6801 UDD32C03L01 SOD_323 PHY1_MDI_3+
PHY1_MDI_2- ED6802 UDD32C03L01 SOD_323 PHY1_MDI_2+
PHY1_MDI_1- ED6803 UDD32C03L01 SOD_323 PHY1_MDI_1+
PHY1_MDI_0- ED6804 UDD32C03L01 SOD_323 PHY1_MDI_0+
1207
LAN1_MCT1 LAN1_MCT2 LAN1_MCT3 LAN1_MCT4
D6805 BS3500NCF SMB_F
D6806 BS3500NCF SMB_F
D6807 BS3500NCF SMB_F
D6808 BS3500NCF SMB_F
C6804 1000pF 2KV C1206L
D6801 BA301N BA301N DNP
D6802 BA301N BA301N DNP
D6803 BA301N BA301N DNP
D6804 BA301N BA301N DNP
VDD10_PHY1
R6822 2.49K R0402
VCC3V3_PHY1
TP6801 TP_0.7
U6800
E_Pad
AVDD33 RSET AVDD10 XTAL_OUT/EXT_CLK XTAL_IN CLKOUT LED2/CFG_LDO1 LED1/CFG_LDO0 LED0/CFG_EXT INTB/PMEB
PHY1_XTALOUT PHY1_XTALIN PHY1_CLKOUT125 PHY1_LED2/CFG_LDO1 PHY1_LED1/CFG_LDO0 PHY1_LED0/CFG_EXT RSET1
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-
PHY1_MDI0+ PHY1_MDI0- PHY1_MDI1+ PHY1_MDI1- PHY1_MDI2+ PHY1_MDI2- PHY1_MDI3+ PHY1_MDI3-
REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY1_REG_OUT PHY1_RXCLK/PHYAD1 PHY1_RXDV/PHYAD2 PHY1_RXD0/RXDLY PHY1_RXD1/TXDLY PHY1_RXD2/PLLOFF PHY1_RXD3/PHYAD0
VCC3V3_PHY1 VCCIO_PHY1 VDD10_PHY1
AVDD33 PHYRSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC
PHY1_RSTn GMAC1_MDC_M1 GMAC1_MDIO_M1 GMAC1_TXD3_M1 GMAC1_TXD2_M1 GMAC1_TXD1_M1 GMAC1_TXD0_M1 GMAC1_TXEN_M1 GMAC1_TXCLK_M1
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
R6838 DNP 4.7K R0402
R6837 1.8K R0402
VCCIO_PHY1
GMAC1_RSTn_GPIO1_B1 R6839 0R R0402
PHYRSTB is 3.3V IO
C6816 100nF X5R 10V C0402
PHY1_RXD0/RXDLY R6840 22R R0402 GMAC1_RXD0_M1
PHY1_RXD1/TXDLY R6841 22R R0402 GMAC1_RXD1_M1
PHY1_RXD2/PLLOFF R6842 22R R0402 GMAC1_RXD2_M1
PHY1_RXD3/PHYAD0 R6843 22R R0402 GMAC1_RXD3_M1
PHY1_RXCLK/PHYAD1 R6844 22R R0402 GMAC1_RXCLK_M1
PHY1_RXDV/PHYAD2 R6845 22R R0402 GMAC1_RXDV_CRS_M1
C6822 DNP C0402
Close to PHY
R6817 4.7K R0402 PHY1_LED0/CFG_EXT R6818 DNP 4.7K R0402 VCC3V3_PHY1
R6819 DNP 4.7K R0402 PHY1_LED2/CFG_LDO1 R6820 DNP 4.7K R0402
R6821 4.7K R0402 PHY1_LED1/CFG_LDO0
VCC_PHY0_IO Voltage Config
R6825 4.7K R0402 PHY1_RXD3/PHYAD0 R6823 4.7K R0402 VCCIO_PHY1
R6827 4.7K R0402 PHY1_RXCLK/PHYAD1 R6826 DNP 4.7K R0402 VCCIO_PHY1
PHY1_RXDV/PHYAD2
PHY Address Config
PHY Address PHYAD[2:0]
1 (default) 3'b001
R6828 4.7K R0402 PHY1_RXD0/RXDLY R6829 DNP 4.7K R0402 VCCIO_PHY1
Pull-up for additional 2ns delay to RXC for data latching
R6830 4.7K R0402 PHY1_RXD1/TXDLY R6831 DNP 4.7K R0402 VCCIO_PHY1
Pull-up for additional 2ns delay to TXC for data latching
R6833 DNP 4.7K R0402 PHY1_RXD2/PLLOFF R6834 4.7K R0402 VCCIO_PHY1
Pull-up to disable PLL @ ALDPS mode(Low power mode)
VDD10_PHY1
PHY1_REG_OUT
L6800 2.2uH IND_303015
C6814 4.7uF X5R 10V C0603
C6815 100nF X5R 10V C0402
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
C6810 100nF X5R 10V C0402
Close to PIN21
C6819 100nF X5R 10V C0402
C6820 100nF X5R 10V C0402
C6821 100nF X5R 10V C0402
Close to PIN3,8,38
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V | 1'b1 | 2'b10
Internal 1.8V(default) | 1'b0 | 2'b10
Reserve for EMI.
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
C6805 100pF C0G 50V C0402 DNP
C6806 100pF C0G 50V C0402 DNP
VCC_1V8
R6832 DNP 0R R0402
VCCIO_PHY1
C6807 4.7uF 10V X5R C0603
C6808 1uF 6.3V X5R C0402
C6809 100nF X5R 10V C0402
Close to PIN28
VCC_3V3
R6836 0R R0402
VCC3V3_PHY1
C6812 4.7uF X5R 10V C0603
C6811 100nF X5R 10V C0402
C6813 100nF X5R 10V C0402
C6817 4.7uF X5R 10V C0603
C6818 100nF X5R 10V C0402
Close to PIN11,40
Close to PIN29
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK_NVR_DEMO_RK3568_DDR4P216SD4
File: 68.Ethernet-GEPHY_RGMII
Date: Sunday, December 13, 2020
Rev: V1.2
Designed by: Zhangdz
Reviewed by: Default
Sheet: 30 of 37



Rockchip Confidential

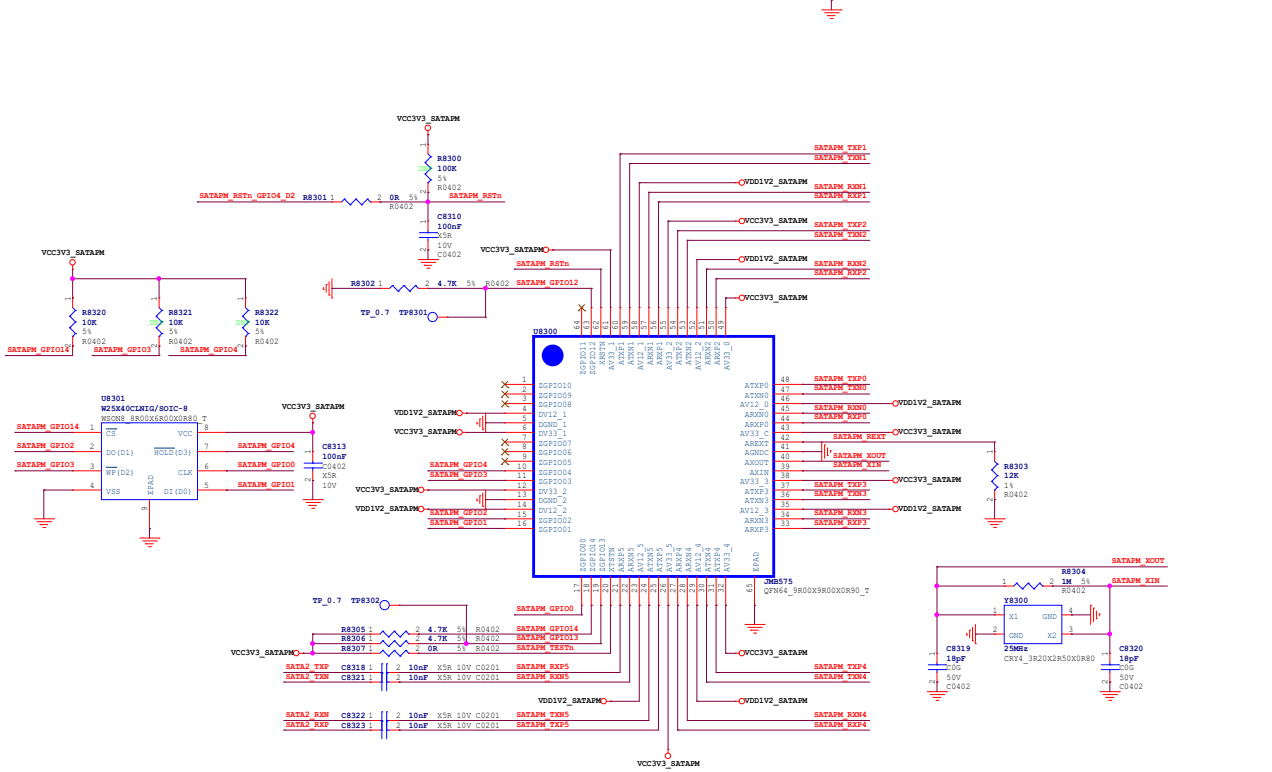
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	70.Audio Port				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	31 of 37

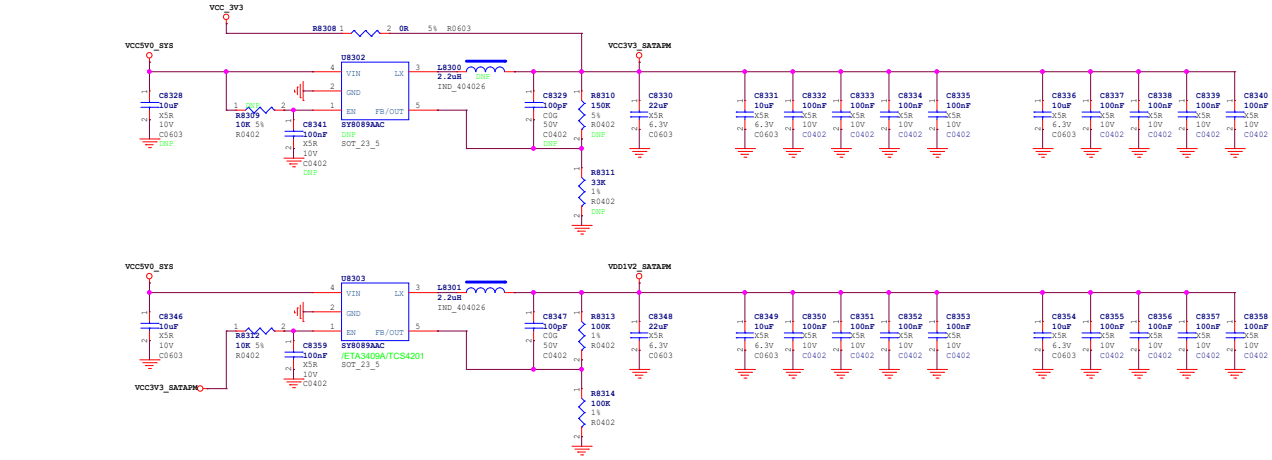
SATA3.0 Port1



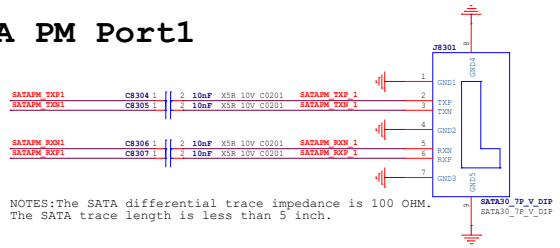
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATAPM_RSTn_GPIO4_D2



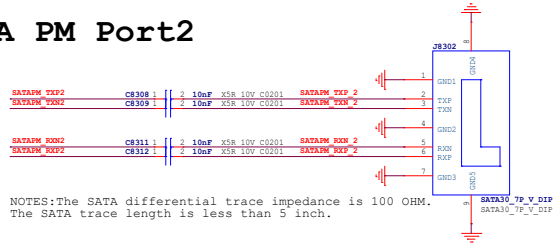


SATA PM Port1



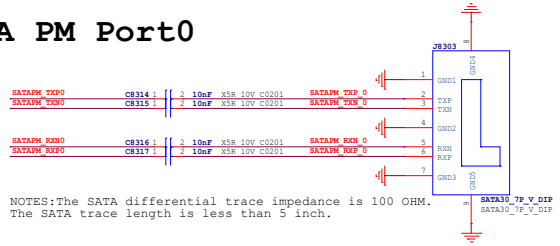
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM Port2



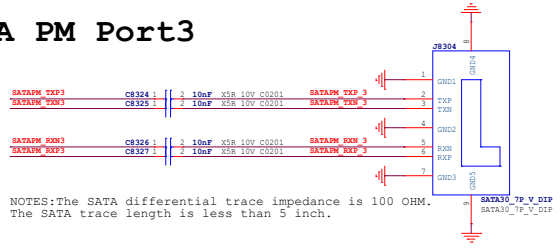
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM Port0



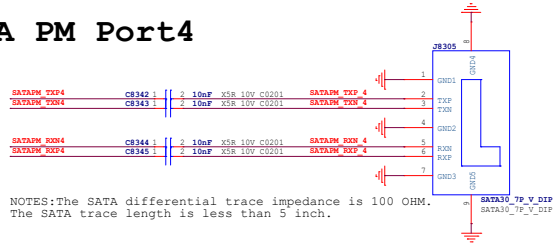
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM Port3



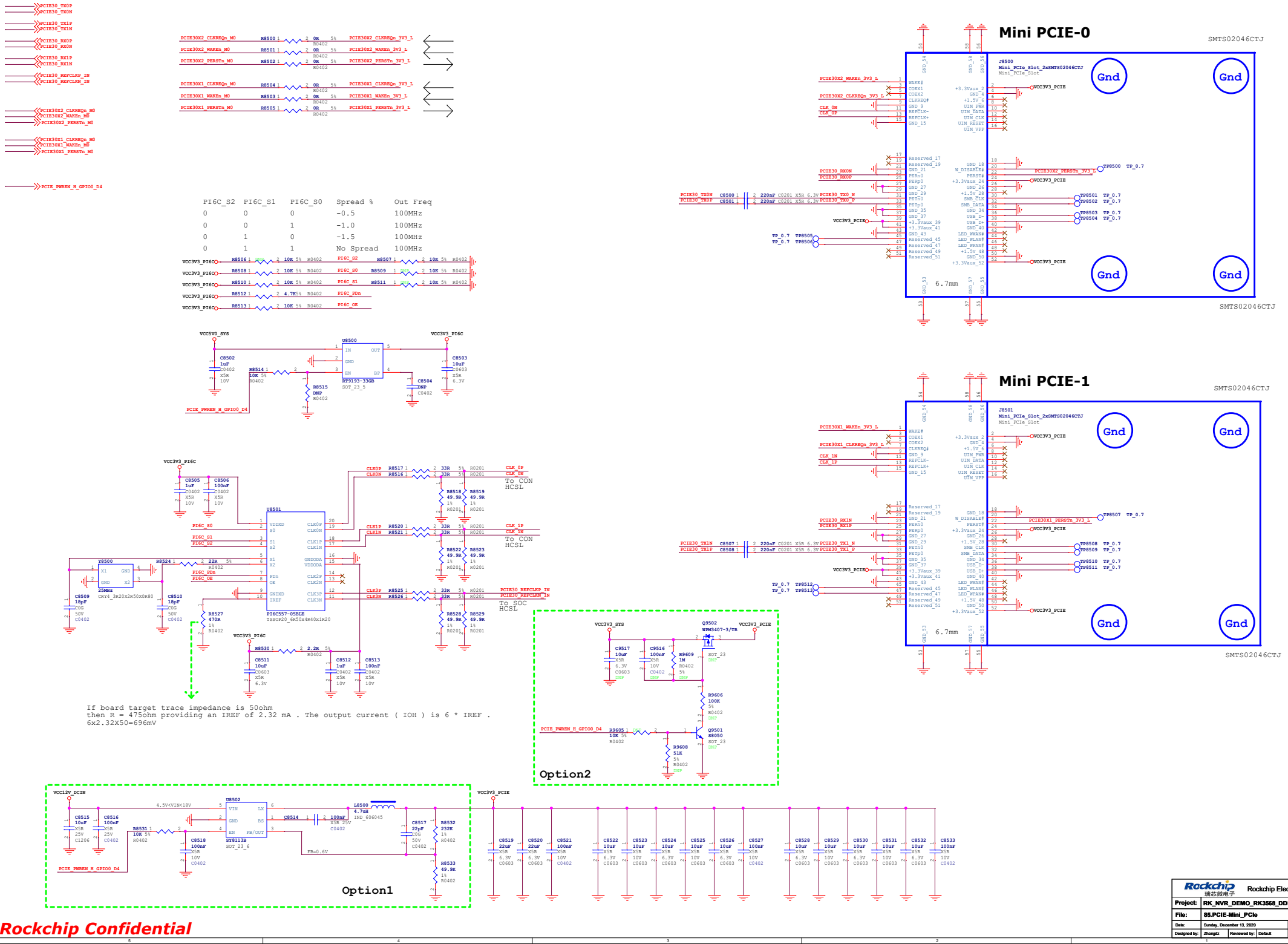
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM Port4



NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4
File:	83.SATA-SATA3.0 Slot_7P
Date:	Sunday, December 13, 2020
Rev:	V1.2
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	32 of 37


PCIE30_TX0P
PCIE30_TX0N
PCIE30_TX1P
PCIE30_TX1N
PCIE30_RX0P
PCIE30_RX0N
PCIE30_RX1P
PCIE30_RX1N
PCIE30_REFCLKP_IN
PCIE30_REFCLKN_IN
PCIE30X2_CLKREQn_M0
PCIE30X2_WAKEn_M0
PCIE30X2_PERSTn_M0
PCIE30X1_CLKREQn_M0
PCIE30X1_WAKEn_M0
PCIE30X1_PERSTn_M0
PCIE_PWREN_H_GPIO0_D4
PCIE30X2_CLKREQn_3V3_L
PCIE30X2_WAKEn_3V3_L
PCIE30X2_PERSTn_3V3_L
PCIE30X1_CLKREQn_3V3_L
PCIE30X1_WAKEn_3V3_L
PCIE30X1_PERSTn_3V3_L
R8500 R8501 R8502 R8503 R8504 R8505
0R 5% R0402
PI6C_S2 PI6C_S1 PI6C_S0 Spread % Out Freq
0 0 0 -0.5 100MHz
0 0 1 -1.0 100MHz
0 1 0 -1.5 100MHz
0 1 1 No Spread 100MHz
VCC3V3_PI6C
R8506 R8508 R8510 R8512 R8513
10K 5% R0402
4.7K 5% R0402
PI6C_S2 PI6C_S0 PI6C_S1 PI6C_PDn PI6C_OE
R8507 R8509 R8511
VCC5V0_SYS
C8502 1uF X5R 10V C0402
U8500 RT9193-33GB SOT_23_5
R8514 10K 5% R0402
R8515 DNP R0402
C8504 DNP C0402
C8503 10uF X5R 6.3V C0603
PCIE_PWREN_H_GPIO0_D4
VCC3V3_PI6C
C8505 1uF X5R 10V C0402
C8506 100nF X5R 10V C0402
U8501 PI6C557-05BLE TSSOP20_6R50x4R40x1R20
VDXD S0 S1 S2 PDn OE GNDXD IREF
CLK0P CLK0N CLK1P CLK1N CLK2P CLK2N CLK3P CLK3N
GNDDDA VDDDDA GNDA VDDA
Y8500 25MHz CRY4_3R20X2R50X0R80
R8524 22R 5% R0402
C8509 18pF 50V C0402
C8510 18pF 50V C0402
PI6C_S0 PI6C_S1 PI6C_S2 PI6C_PDn PI6C_OE
R8517 R8516 R8520 R8521 R8525 R8526 33R 5% R0201
R8518 R8519 R8522 R8523 R8528 R8529 49.9R 1% R0201
CLK0P CLK0N CLK_0P CLK_0N
CLK1P CLK1N CLK_1P CLK_1N
CLK3P CLK3N PCIE30_REFCLKP_IN PCIE30_REFCLKN_IN
To CON HCSL
To SOC HCSL
R8527 470R 1% R0402
R8530 2.2R 5% R0402
C8511 10uF X5R 6.3V C0603
C8512 1uF X5R 10V C0402
C8513 100nF X5R 10V C0402
If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA . The output current (IOH) is 6 * IREF .
6x2.32X50=696mV
VCC3V3_SYS
Q9502 WPM3407-3/TR SOT_23
VCC3V3_PCIE
C9517 10uF X5R 6.3V C0603 DNP
C9516 100nF X5R 10V C0402 DNP
R9609 1M 5% R0402 DNP
R9606 100K 5% R0402 DNP
PCIE_PWREN_H_GPIO0_D4
R9605 10K 5% R0402 DNP
Q9501 S8050 SOT_23 DNP
R9608 51K 5% R0402 DNP
Option2
VCC12V_DCIN
U8502 SY8113B SOT_23_6
4.5V<VIN<18V
C8515 10uF X5R 25V C1206
C8516 100nF X5R 25V C0402
R8531 10K 5% R0402
C8518 100nF X5R 10V C0402
C8514 100nF X5R 25V C0402
L8500 4.7uH IND_606045
FB=0.6V
C8517 22pF C0G 50V C0402
R8532 232K 1% R0402
R8533 49.9K 1% R0402
PCIE_PWREN_H_GPIO0_D4
Option1
VCC3V3_PCIE
C8519 22uF X5R 6.3V C0603
C8520 22uF X5R 6.3V C0603
C8521 100nF X5R 10V C0402
C8522 10uF X5R 6.3V C0603
C8523 10uF X5R 10V C0603
C8524 10uF X5R 6.3V C0603
C8525 10uF X5R 10V C0603
C8526 10uF X5R 6.3V C0603
C8527 100nF X5R 10V C0402
C8528 10uF X5R 6.3V C0603
C8529 10uF X5R 10V C0603
C8530 10uF X5R 6.3V C0603
C8531 10uF X5R 10V C0603
C8532 10uF X5R 6.3V C0603
C8533 100nF X5R 10V C0402
Mini PCIE-0
SMTS02046CTJ
J8500 Mini_PCIe_Slot_2xSMTS02046CTJ Mini_PCIe_Slot
PCIE30X2_WAKEn_3V3_L
PCIE30X2_CLKREQn_3V3_L
CLK_ON CLK_OP
PCIE30_RX0N PCIE30_RX0P
PCIE30_TX0N C8500 220nF C0201 X5R 6.3V PCIE30_TX0_N
PCIE30_TX0P C8501 220nF C0201 X5R 6.3V PCIE30_TX0_P
VCC3V3_PCIE
TP_0.7 TP8505
TP_0.7 TP8506
PCIE30X2_PERSTn_3V3_L
TP8500 TP_0.7
TP8501 TP_0.7
TP8502 TP_0.7
TP8503 TP_0.7
TP8504 TP_0.7
Gnd
6.7mm
Mini PCIE-1
SMTS02046CTJ
J8501 Mini_PCIe_Slot_2xSMTS02046CTJ Mini_PCIe_Slot
PCIE30X1_WAKEn_3V3_L
PCIE30X1_CLKREQn_3V3_L
CLK_1N CLK_1P
PCIE30_RX1N PCIE30_RX1P
PCIE30_TX1N C8507 220nF C0201 X5R 6.3V PCIE30_TX1_N
PCIE30_TX1P C8508 220nF C0201 X5R 6.3V PCIE30_TX1_P
VCC3V3_PCIE
TP_0.7 TP8512
TP_0.7 TP8513
PCIE30X1_PERSTn_3V3_L
TP8507 TP_0.7
TP8508 TP_0.7
TP8509 TP_0.7
TP8510 TP_0.7
TP8511 TP_0.7
Gnd
6.7mm
Rockchip Confidential
Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd
Project: RK_NVR_DEMO_RK3568_DDR4P216SD4
File: 85.PCIE-Mini_PCIe
Date: Sunday, December 13, 2020
Rev: V1.2
Designed by: Zhangtz
Reviewed by: Default
Sheet: 33 of 37

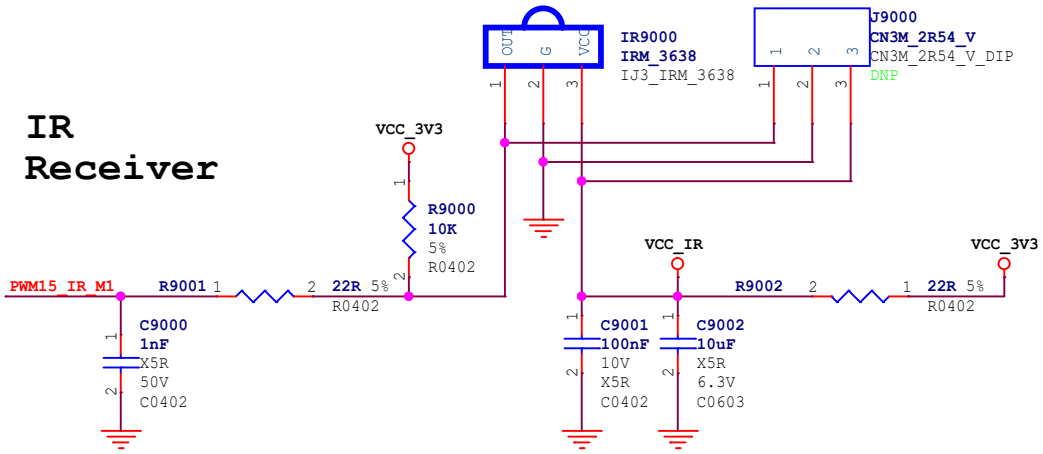
PWM15_IR_M1

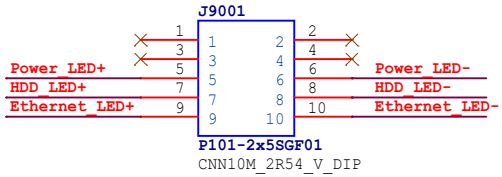
Power_LED_EN_H_GPIO0_C4

Ethernet_LED_EN_H_GPIO4_C6

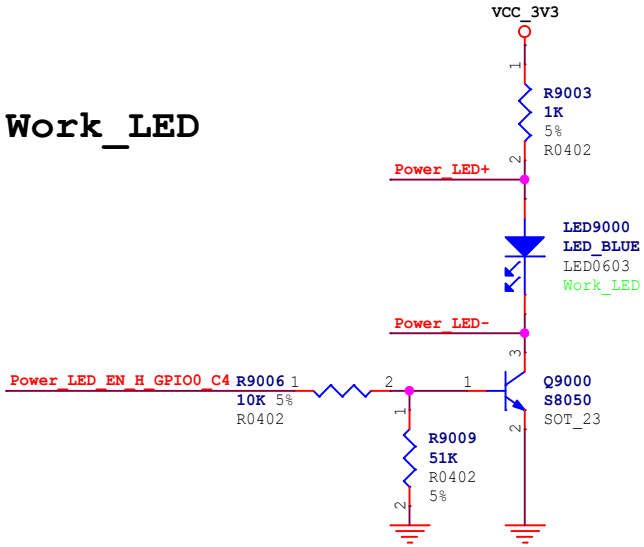
HDD_LED_EN_H_GPIO4_C5

IR Receiver

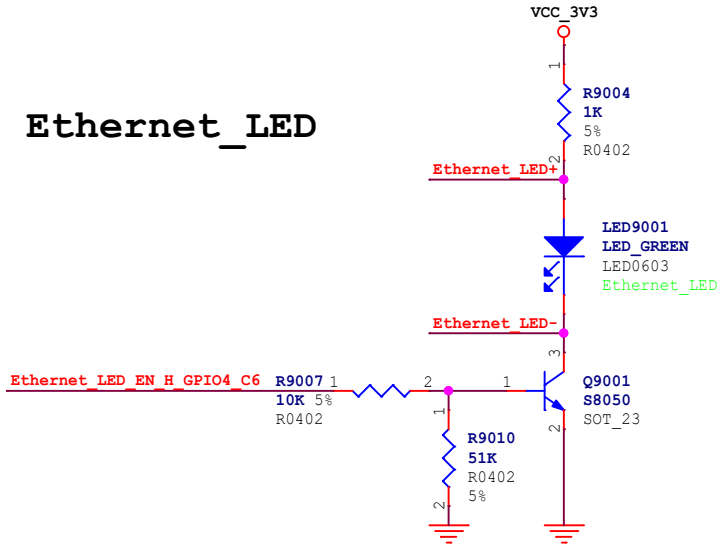




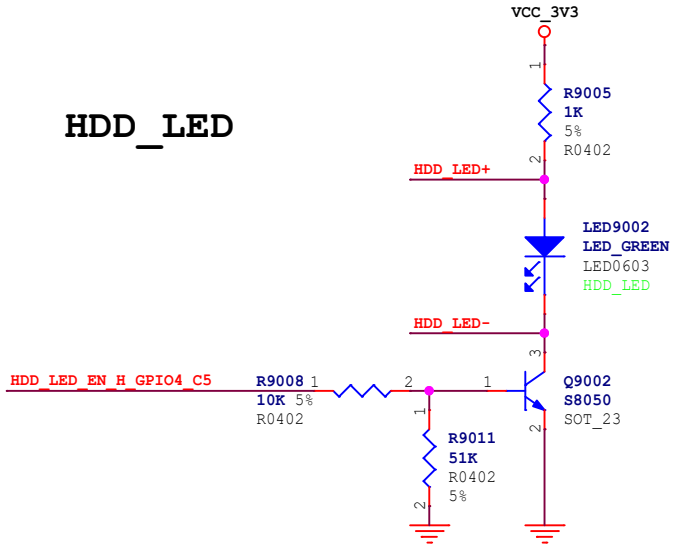
Work_LED



Ethernet_LED



HDD_LED

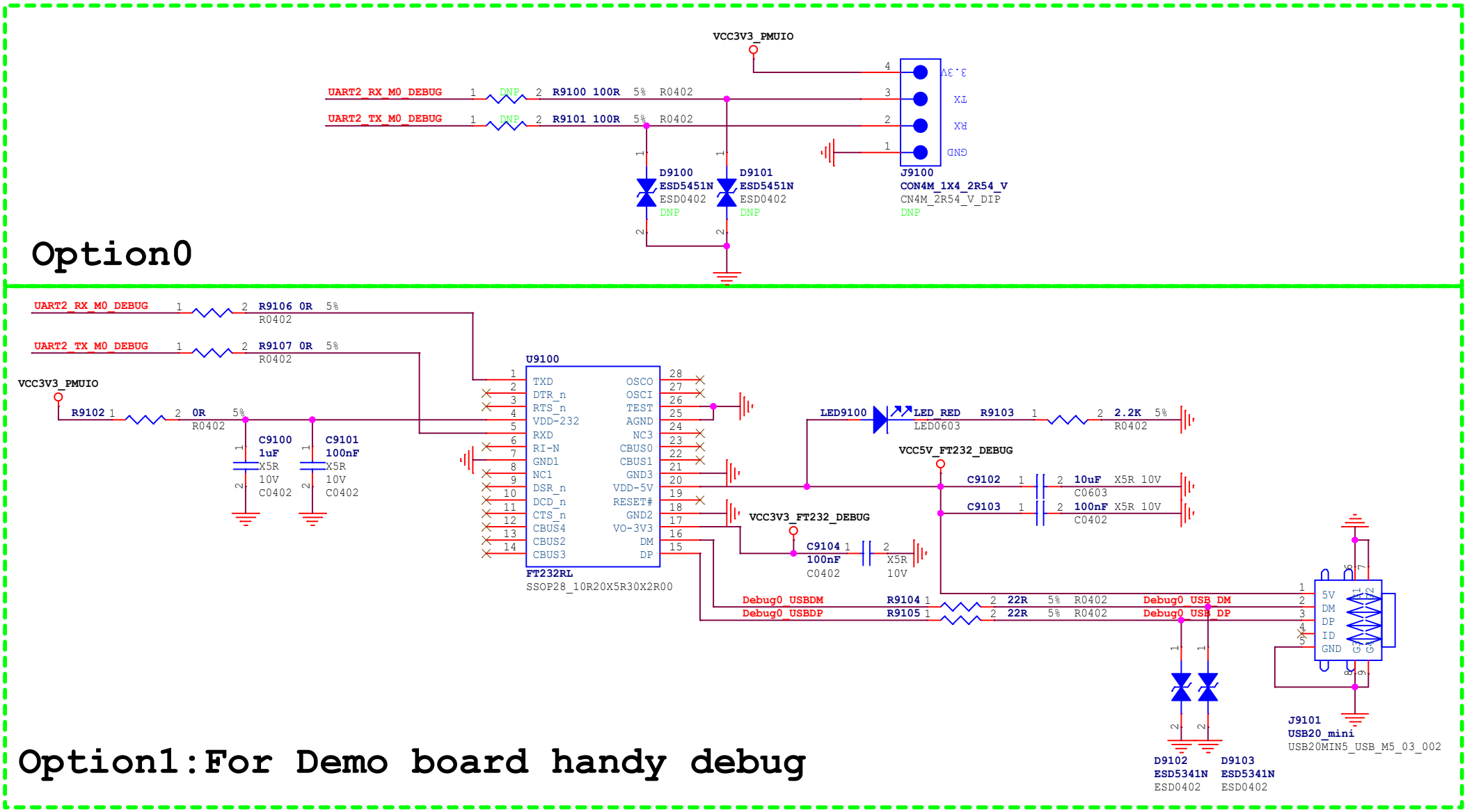


Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	90.IR Receiver/LED/RESET/PWRKEY				
Date:	Thursday, December 17, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	34 of 37

UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

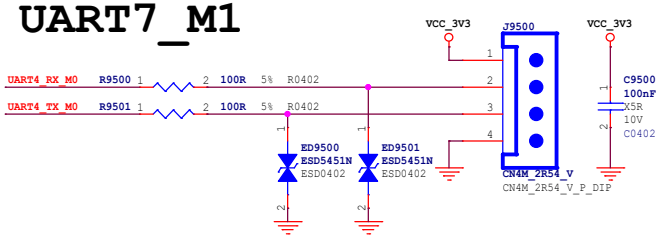
Debug UART2

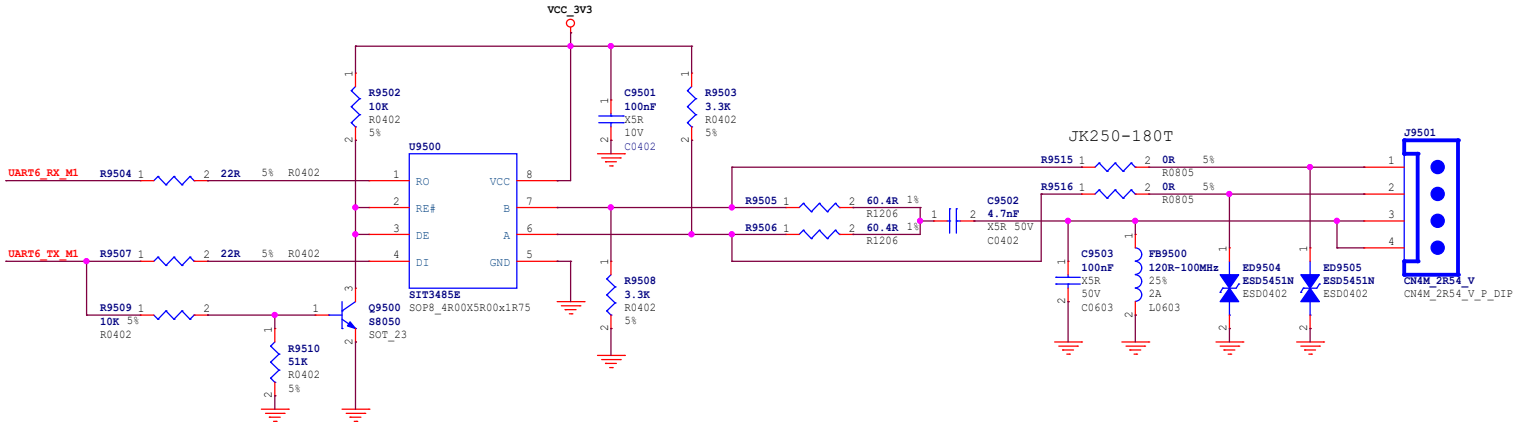


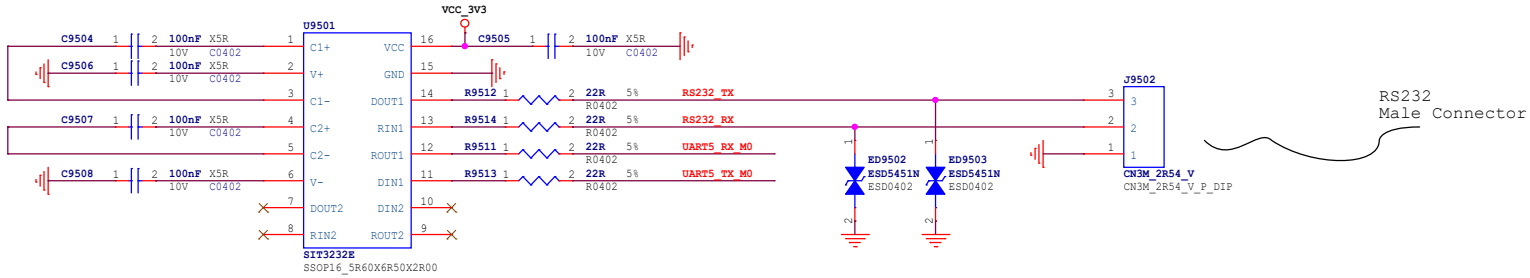
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	91.Debug UART				
Date:	Thursday, December 17, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	35 of 37

UART5_RX_M0
UART5_TX_M0
UART6_TX_M1
UART6_RX_M1
UART4_TX_M0
UART4_RX_M0

UART7_M1







RS232
Male Connector

Pin1:DCD,<---,Data Carrier Detect
Pin2:RXD,<---,Receive Data
Pin3:TXD,--->,Transmit Data
Pin4:DTR,--->,Data Terminal Ready
Pin5:COM
Pin6:DSR,<---,Data Set Ready
Pin7:RTS,--->,Request to Send
Pin8:CTS,<---,Clear to Send
Pin9:RI ,<---,Ring Indicator

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	95.UART/RS485/RS232				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	36 of 37

H9900
HOLE_3R20
HOLE_C3R20_C6R00

H9901
HOLE_3R20
HOLE_C3R20_C6R00

H9902
HOLE_3R20
HOLE_C3R20_C6R00

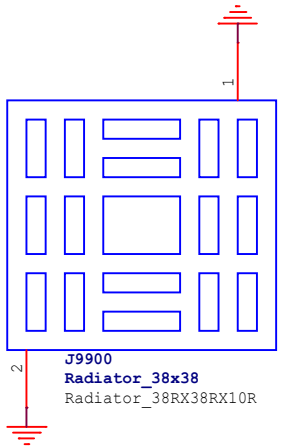
H9903
HOLE_3R20
HOLE_C3R20_C6R00

H9904
HOLE_3R20
HOLE_C3R20_C6R00

H9905
HOLE_3R20
HOLE_C3R20_C6R00

H9906
HOLE_3R20
HOLE_C3R20_C6R00

H9907
HOLE_3R20
HOLE_C3R20_C6R00



J9900
Radiator_38x38
Radiator_38RX38RX10R

TOP Mark

M9900
MARK
MARK

M9901
MARK
MARK

M9902
MARK
MARK

BOTTOM Mark

M9903
MARK
MARK

M9904
MARK
MARK

M9905
MARK
MARK

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO_RK3568_DDR4P216SD4				
File:	99.Mark/Hole/Heatsink				
Date:	Sunday, December 13, 2020			Rev:	V1.2
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	37 of 37