Schematic for Learn

Main Functions Introduction

1)PMIC: RK809-5+DiscretePower
2)RAM: DDR4 2x16Bit
3)ROM: eMMC
4)Support:1 x Micro SD Card
5)Support:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1
6)Support:1 x USB2.0 HOST2+ 1 x USB2.0 HOST3
7)Support:1 x HDMI2.0 TX
8)Support:a/b/g/n/ac 2X2 SDIO WIFI5
9)Support:1 x 10/100/1000 Ethernet(RGMII0)
10)Support:1 x 10/100/1000 Ethernet(RGMII1)
11)Support:Reset,Power on/off Key
12)Support: Debug UART
13)Support: 1 x Power LED,1 x CPU LED,1 x GPU LED,1 x NPU LED

项目名称	Learn		
电路名称	-00.Cover Page		
纸张大小	A4	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	1

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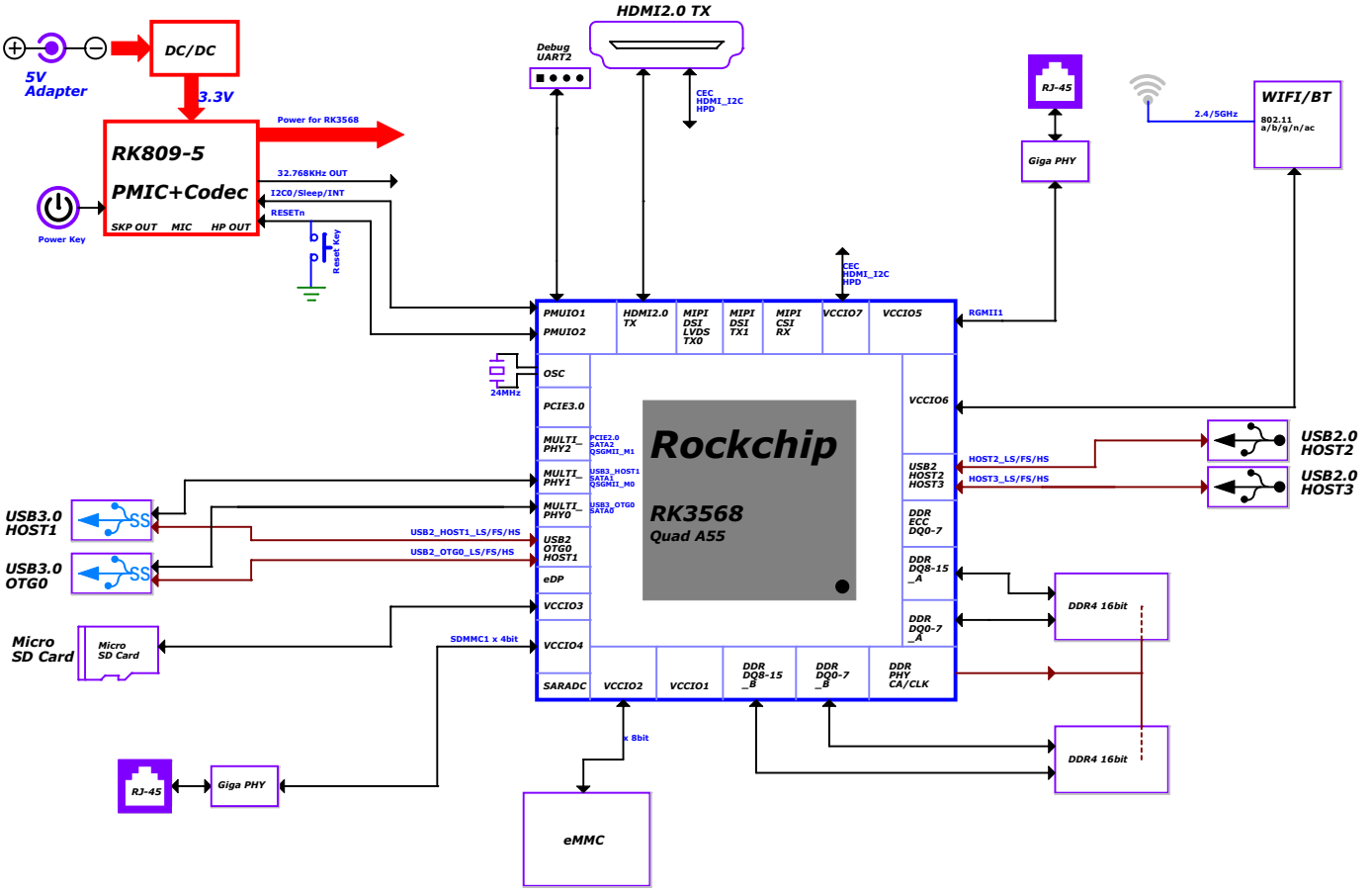
纸张大小	A4	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	2

Revision History

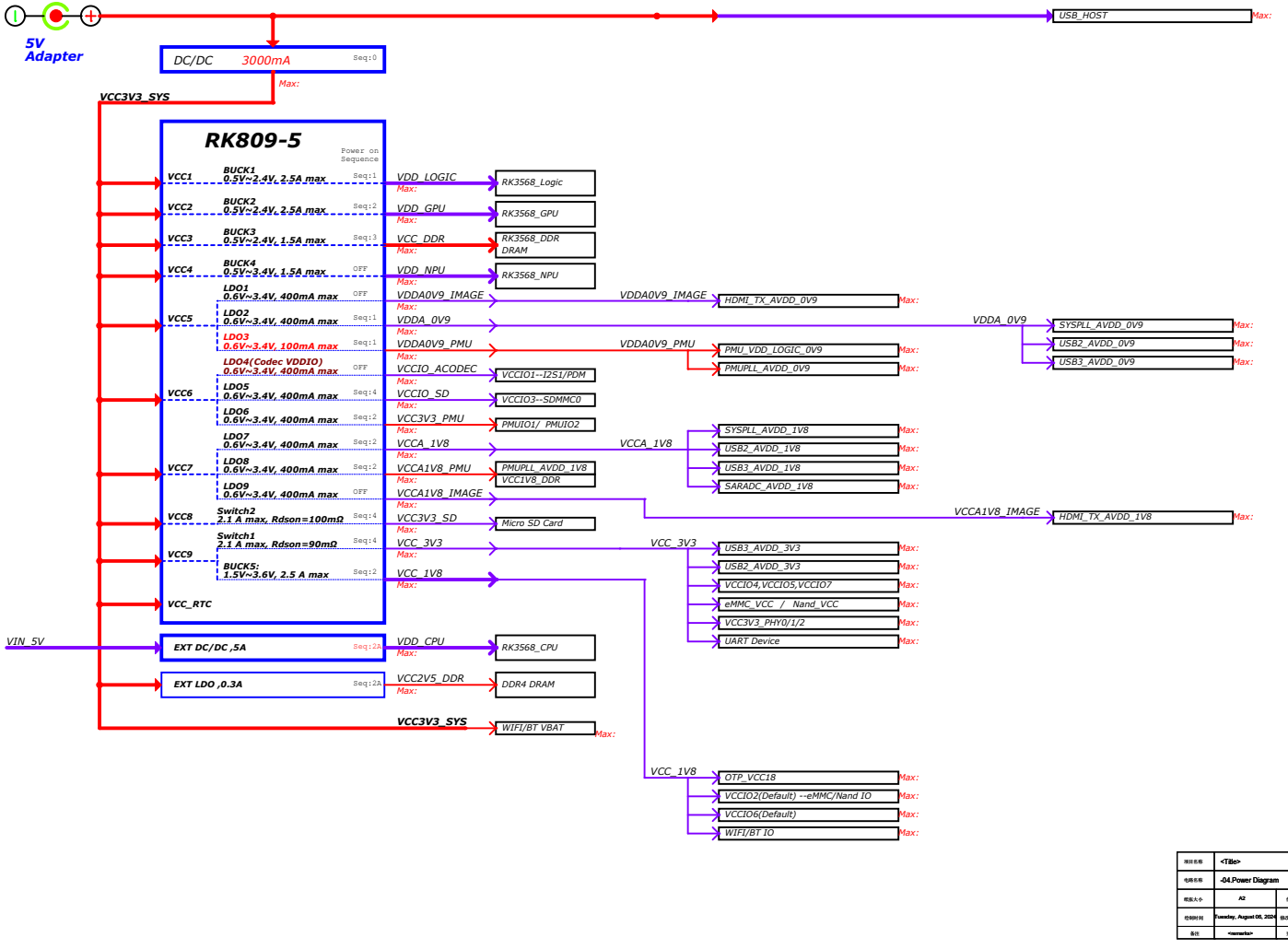
Version	Date	Change Dsecription	Approved
V1.0	Tuesday, August 06, 2024	1:Revision preliminary version	
V1.1	Tuesday,September 08, 2024	1:Modify the matching resistors of ETH0 and ETH1 2:Modify the NET naming of ETH0 and ETH1	

项目名称	<Title>		
电路名称	-02.Revision History		
纸张大小	A4	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	3



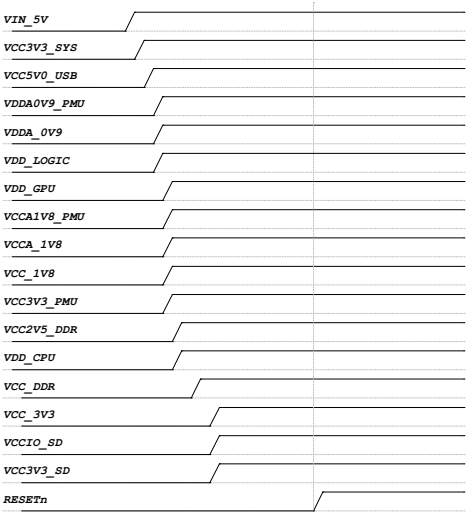
项目名称	<Title>		
电路名称	-03.Block Diagram		
模板大小	A2	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 15, 2024
备注	<remarks>	版本	4

Default Power Diagram



项目名称	<Title>		
电路名称	-04.Power Diagram		
模板大小	A2	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	5

Power Sequence



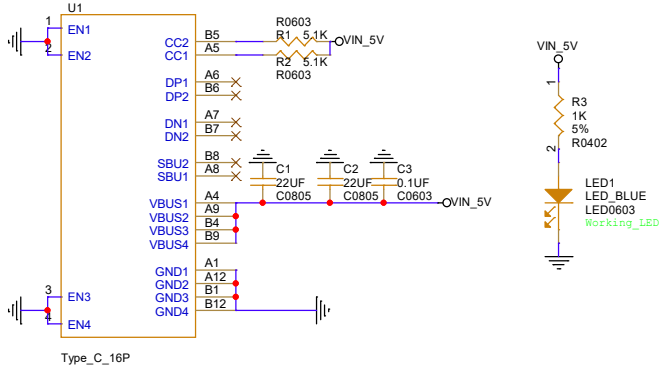
Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD卡1.8V,SD卡3.3V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VIN_5V	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

Default IO Power Domain Map

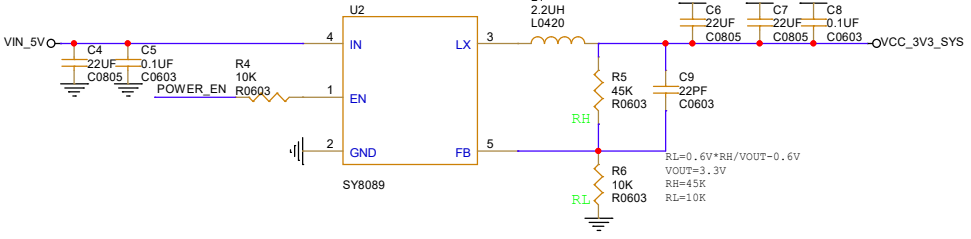
IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	3.3V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

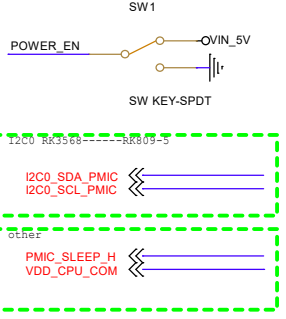
项目名称	<Title>		
电路名称	-05.Power Sequence/IO Domain		
纸张大小	A3	作者	TZH
绘制时间	Tuesday, August 06, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	6

POWER IN

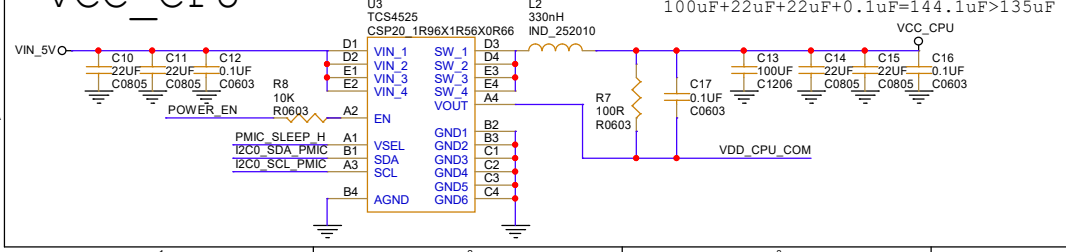


VCC3V3_SYS



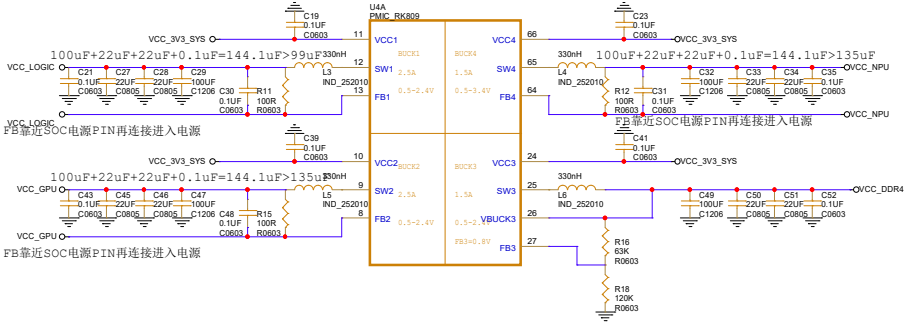


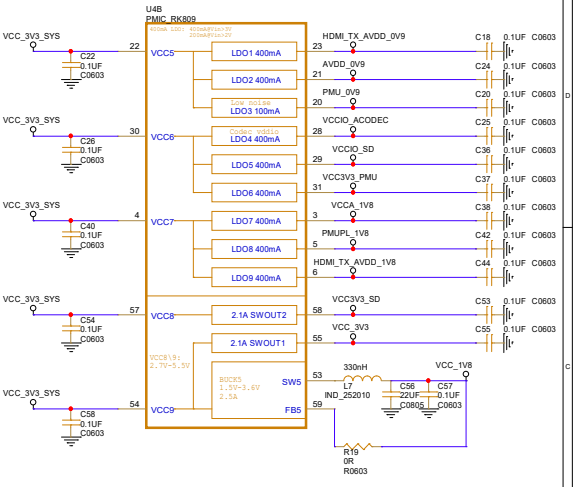
VCC_CPU

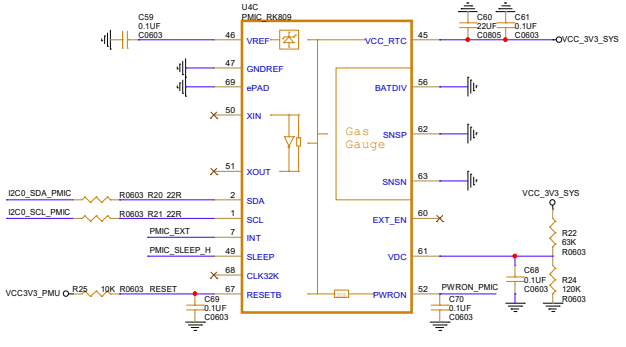


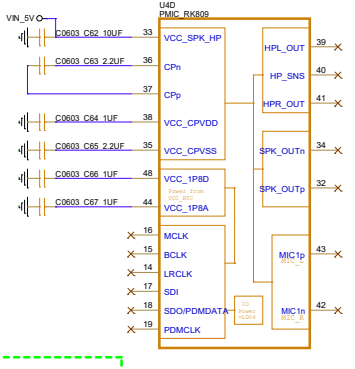
项目名称	<Title>		
电路名称	01.POWER_IN		
纸张大小	A4	作者	TZH
绘制时间	Saturday, June 22, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	7

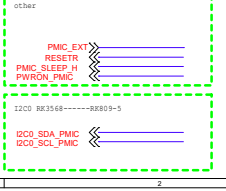
PMIC RK809-5





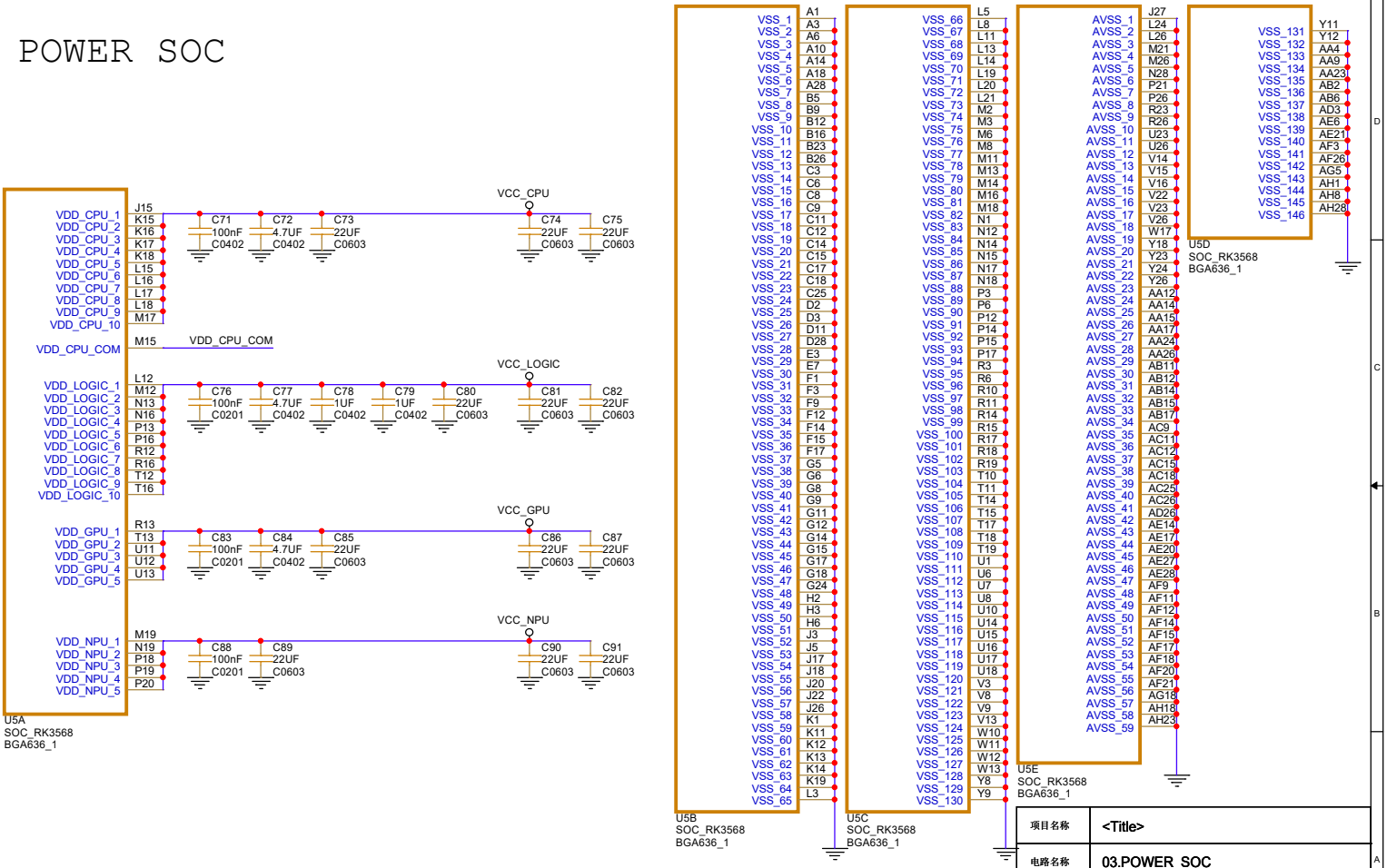






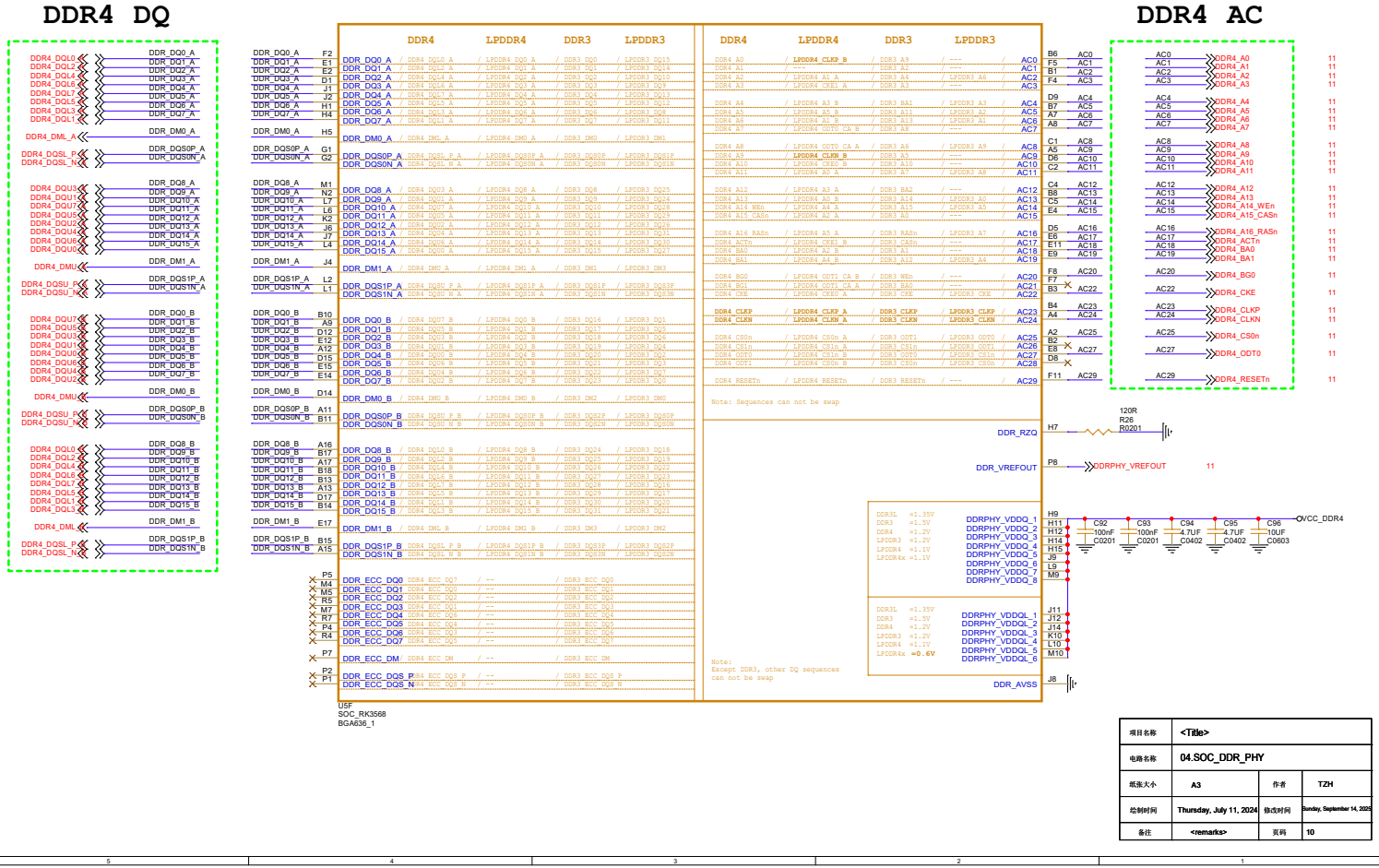
项目名称	<Title>		
电路名称	02.POWER_PMIC		
纸张大小	A3	作者	TZH
绘制时间	Tuesday, July 09, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	8

POWER SOC



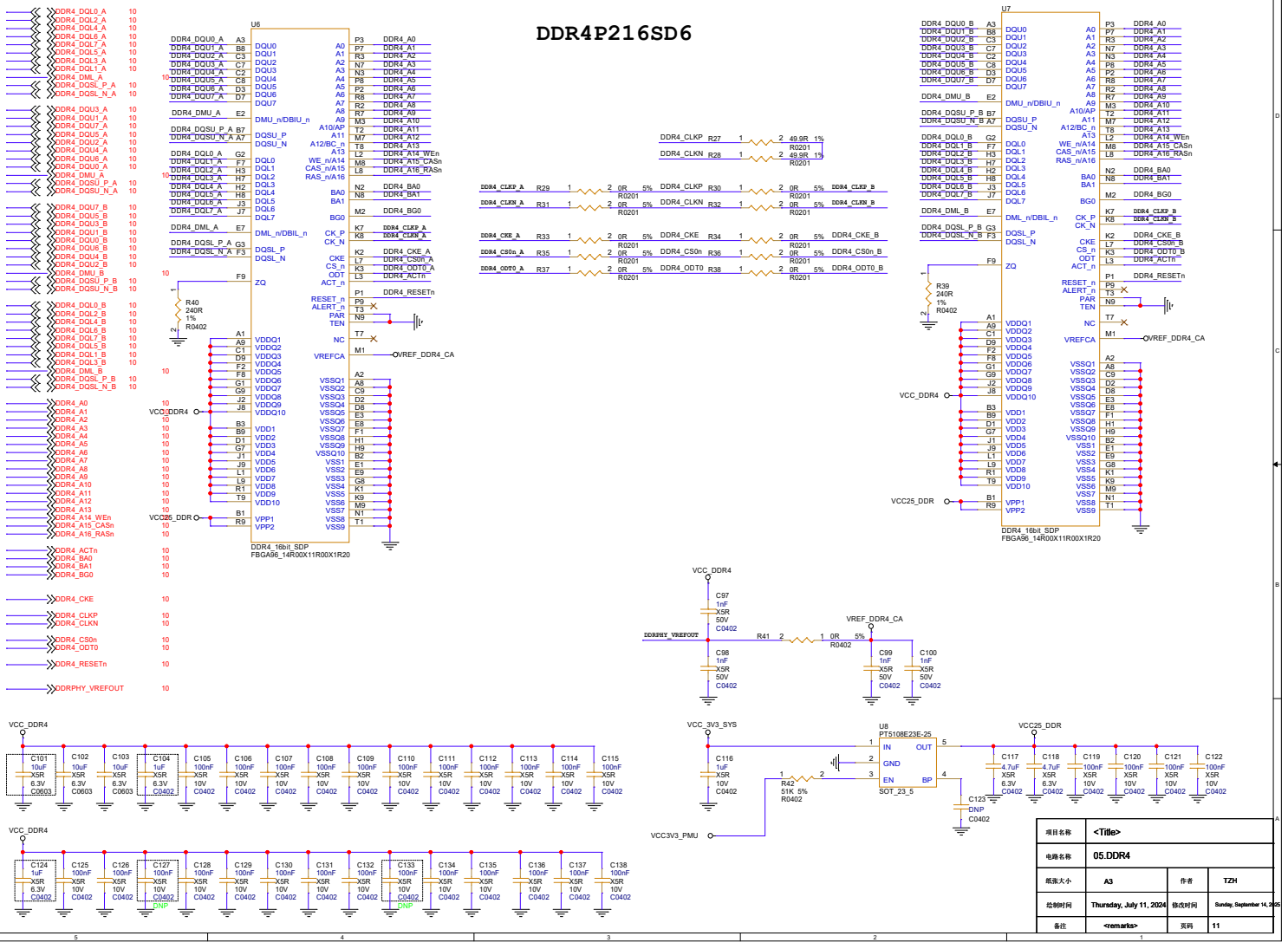
项目名称	<Title>		
电路名称	03.POWER_SOC		
纸张大小	A4	作者	TZH
绘制时间	Thursday, July 11, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	9

SOC DDR PHY



项目名称	<Title>		
电路名称	04.SOC_DDR_PHY		
纸张大小	A3	作者	TZH
绘制时间	Thursday, July 11, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	10

DDR4P216SD6



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电路名称	05.DDR4		
纸张大小	A3	作者	TZH
绘制时间	Thursday, July 11, 2024	修改时间	Sunday, September 14, 2025
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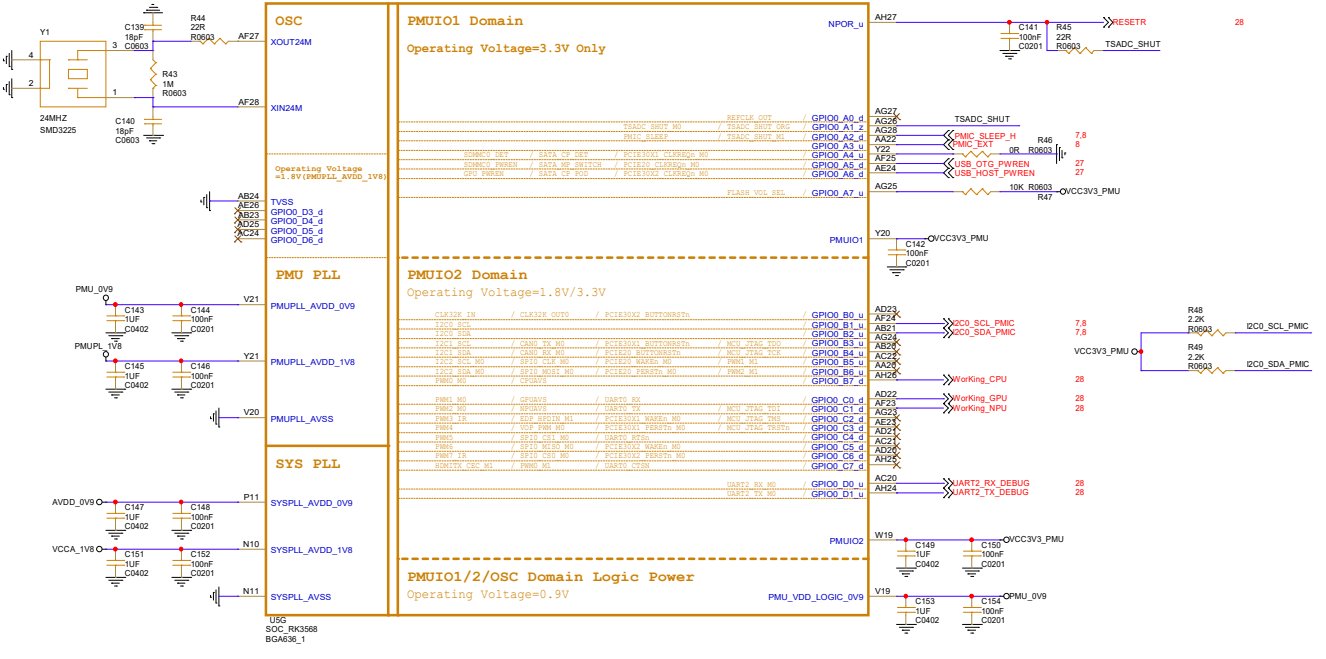

项目名称	<Title>		
电路名称	06.SOC_OSC/PMU/SYSPLL		
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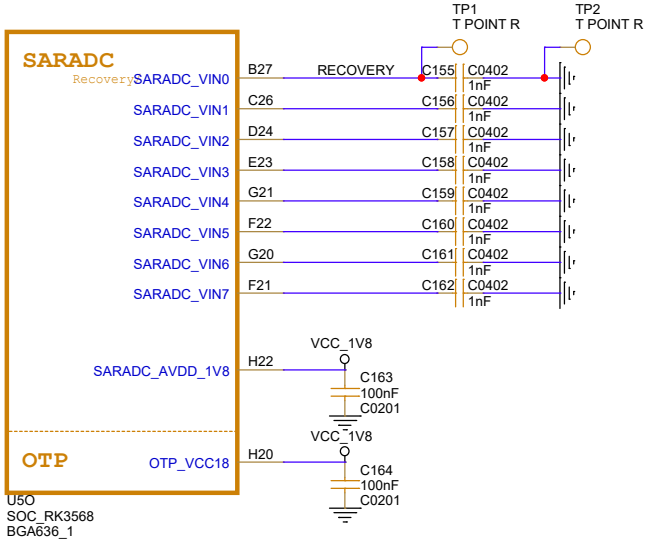
备注	<remarks>	页码	12



项目名称	<Title>		
电路名称	07.SOC_OTP_IO		
纸张大小	A	作者	TZH
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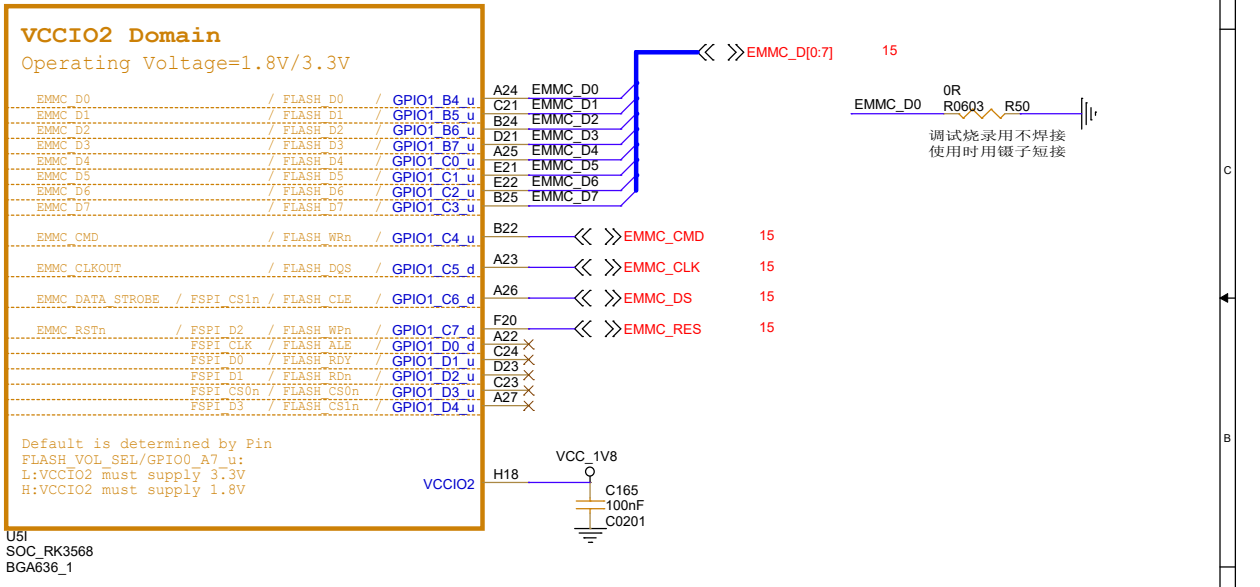
备注	<remarks>	页码	13



项目名称	<Title>		
电路名称	08.SOC_EMMC/Flash_IO		
纸张大小	A	作者	TZH
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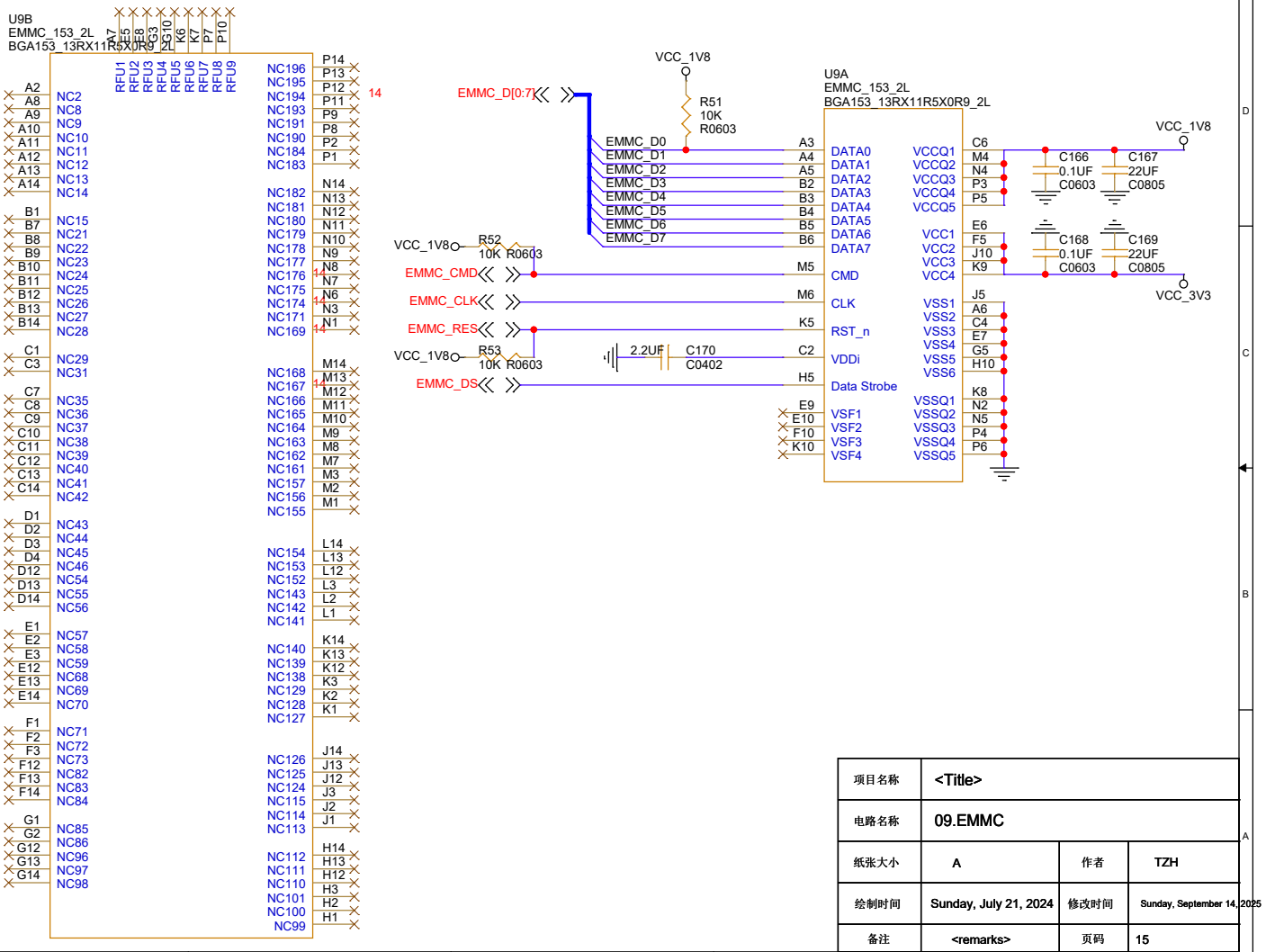

项目名称	<Title>		
电路名称	09.EMMC		
纸张大小	A	作者	TZH
绘制时间	Sunday, July 21, 2024	修改时间	Sunday, September 14, 2025
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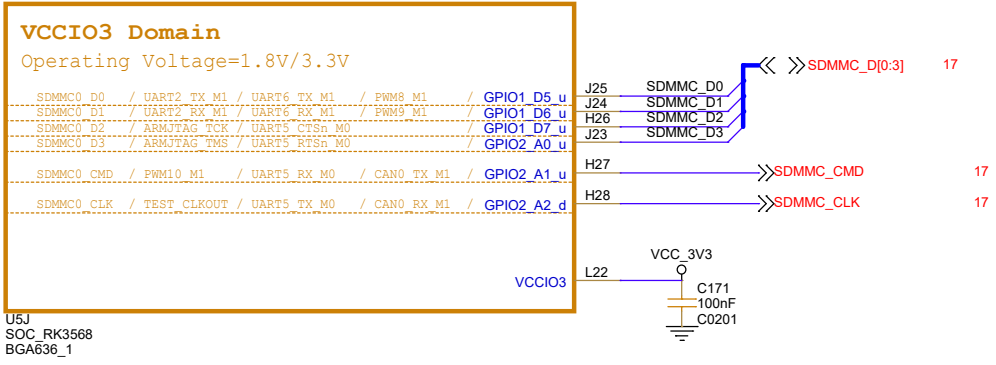
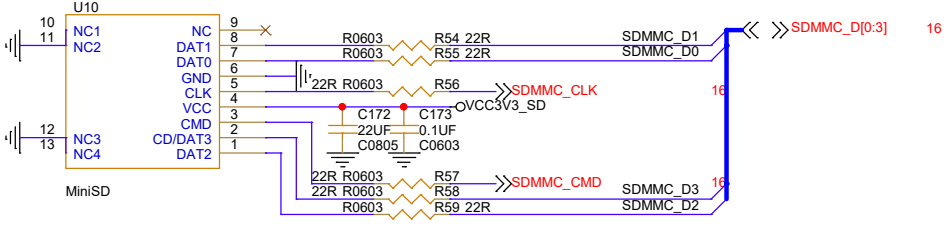
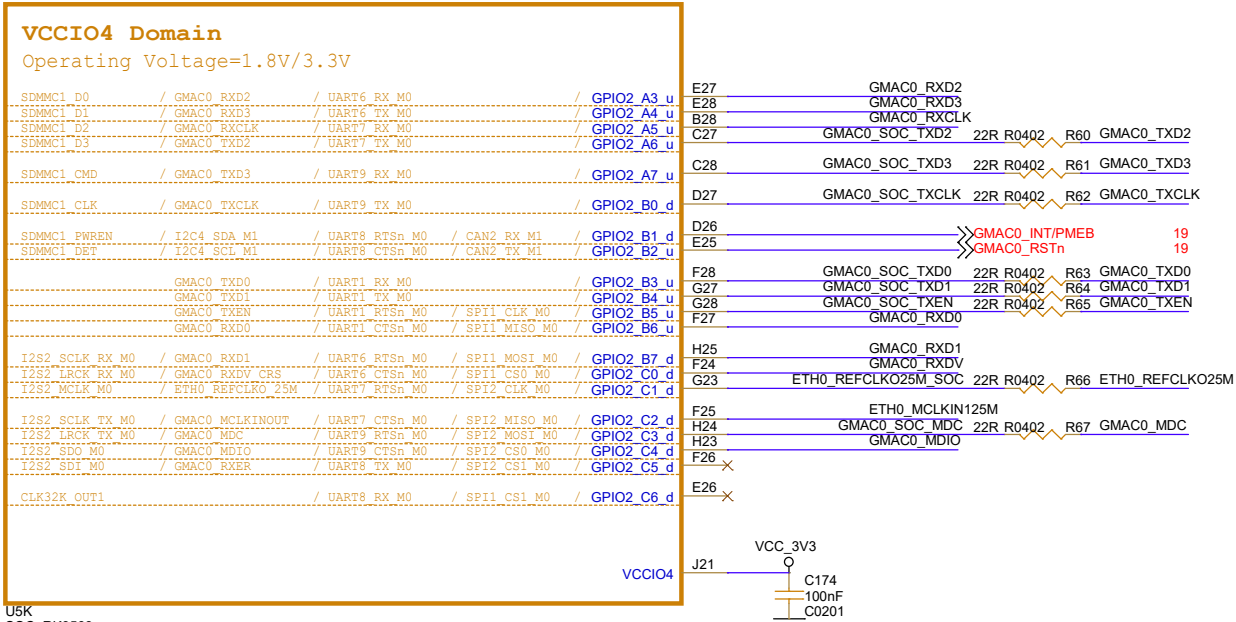
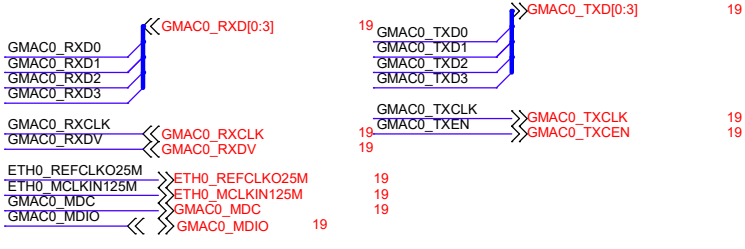


项目名称	<Title>		
电路名称	10.SOC_SDMMC_IO		
纸张大小	A	作者	TZH
绘制时间	Friday, July 12, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	16

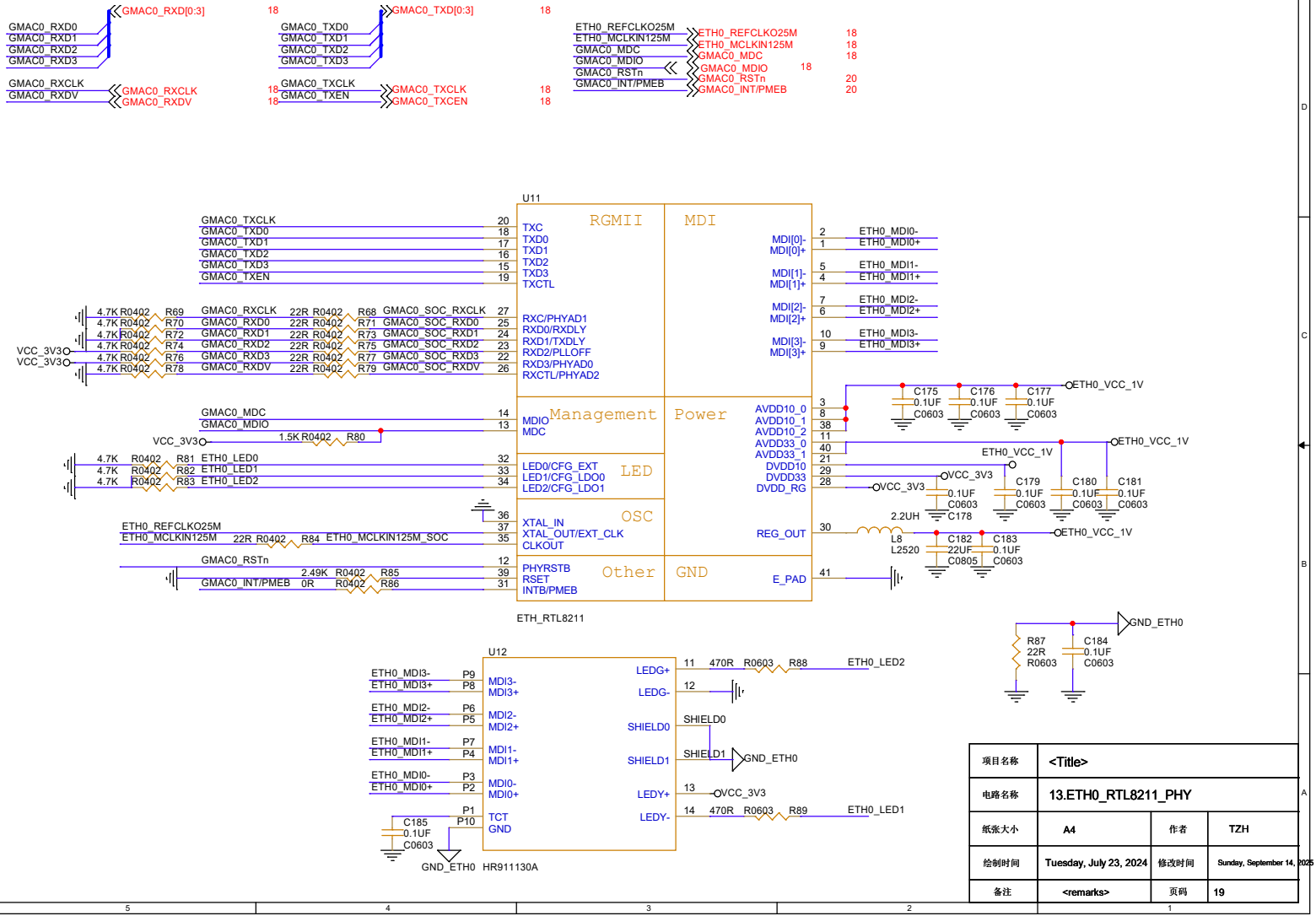


项目名称	<Title>		
电路名称	11.SD_Card		
纸张大小	A	作者	TZH
绘制时间	Monday, July 22, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	17





项目名称	<Title>		
电路名称	12.SOC_ETH0_IO		
纸张大小	A	作者	TZH
绘制时间	Monday, July 22, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	18



项目名称	<Title>		
电路名称	13.ETH0_RTL8211_PHY		
纸张大小	A4	作者	TZH
绘制时间	Tuesday, July 23, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	19

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0 / VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d	AG6
LCDC_D1 / VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d	AD7
LCDC_D2 / VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d	AC8
LCDC_D3 / VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d	AC7
LCDC_D4 / VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d	AF5
LCDC_D5 / VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d	AF6
LCDC_D6 / VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d	AD6
LCDC_D7 / VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d	AH5
LCDC_CLK / VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d	AH4
LCDC_D8 / VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d	AB8
LCDC_D9 / VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d	AE5
LCDC_D10 / VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d	AG4
LCDC_D11 / VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d	AF4
LCDC_D12 / VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d	AH3
LCDC_D13 / VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d	AG3
LCDC_D14 / VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d	AH2
LCDC_D15 / VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d	AG2
LCDC_D16 / VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d	AG1
LCDC_D17 / VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d	AF2
LCDC_D18 / VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d	AF1
LCDC_D19 / VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d	AE1
LCDC_D20 / VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d	AE2
LCDC_D21 / VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d	AE3
LCDC_D22 / PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d	AD4
LCDC_D23 / PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d	AD2
LCDC_HSYNC / VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d	AD1
LCDC_VSYNC / VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d	AA7
LCDC_DEN / VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d	AC4
PWM14_M0 / VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d	AC3
PWM15_IR_M0 / SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d	AC2

VCCIO5_1 V10
VCCIO5_2 V11

VCC_3V3
C186 100nF C0201
C187 100nF C0201

GMAC1_SOC_TXD2 22R R0402 R90 GMAC1_TXD2
GMAC1_SOC_TXD3 22R R0402 R91 GMAC1_TXD3
GMAC1_RXD2
GMAC1_RXD3
GMAC1_SOC_TXCLK 22R R0402 R92 GMAC1_TXCLK
GMAC1_RXCLK
ETH1_REFCLKO25M_SOC 22R R0402 R93 ETH1_REFCLKO25M
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXDV
GMAC1_SOC_TXD0 22R R0402 R94 GMAC1_TXD0
GMAC1_SOC_TXD1 22R R0402 R95 GMAC1_TXD1
GMAC1_SOC_TXEN 22R R0402 R96 GMAC1_TXEN
ETH1_MCLKIN125M
GMAC1_INT/PMEB 21
GMAC1_RSTn 21
GMAC1_SOC_MDC 22R R0402 R97 GMAC1_MDC
GMAC1_MDIO

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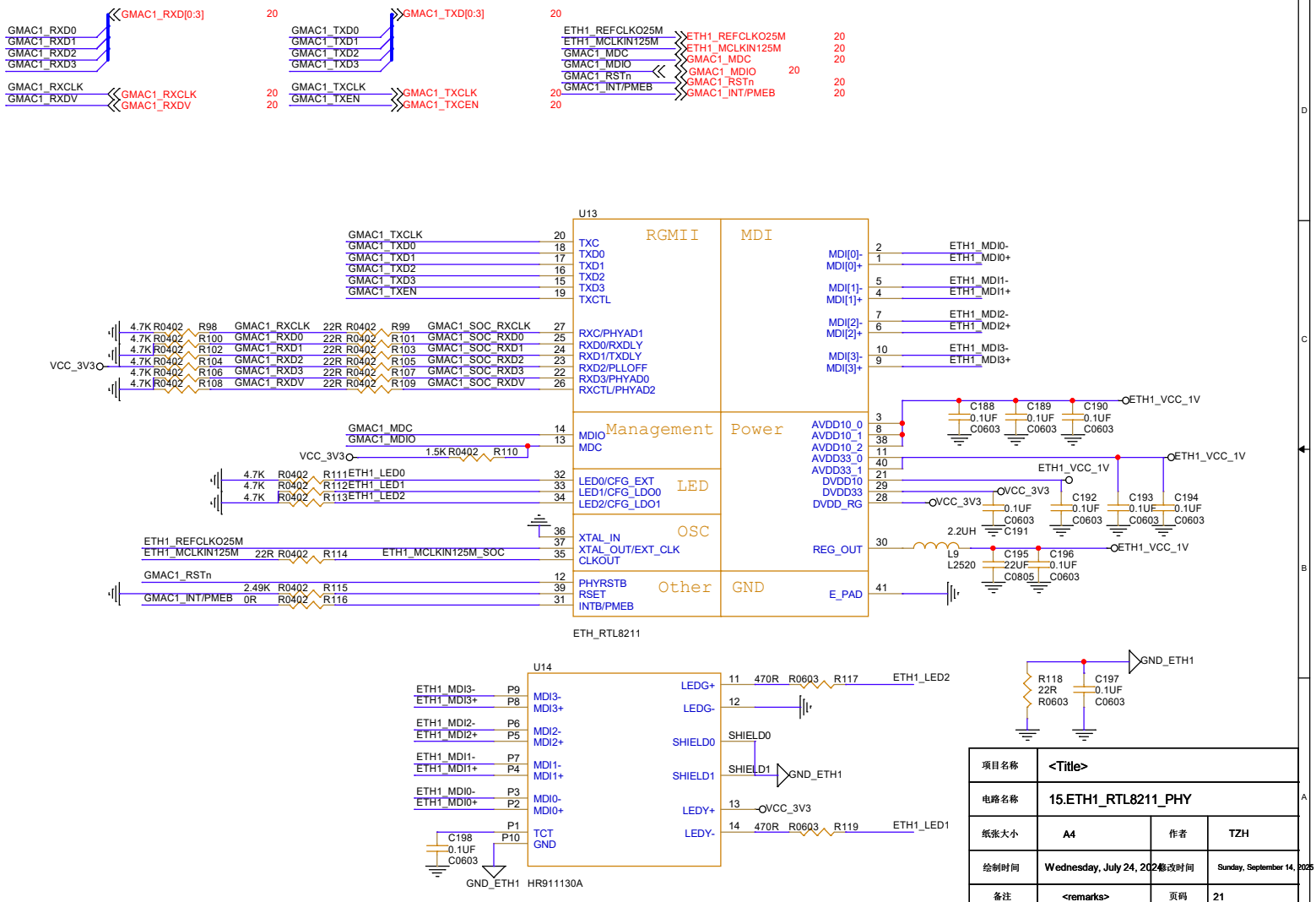
GMAC1_RXD[0:3] 21
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_RXCLK
GMAC1_RXDV
GMAC1_RXCLK 21
GMAC1_RXDV 21

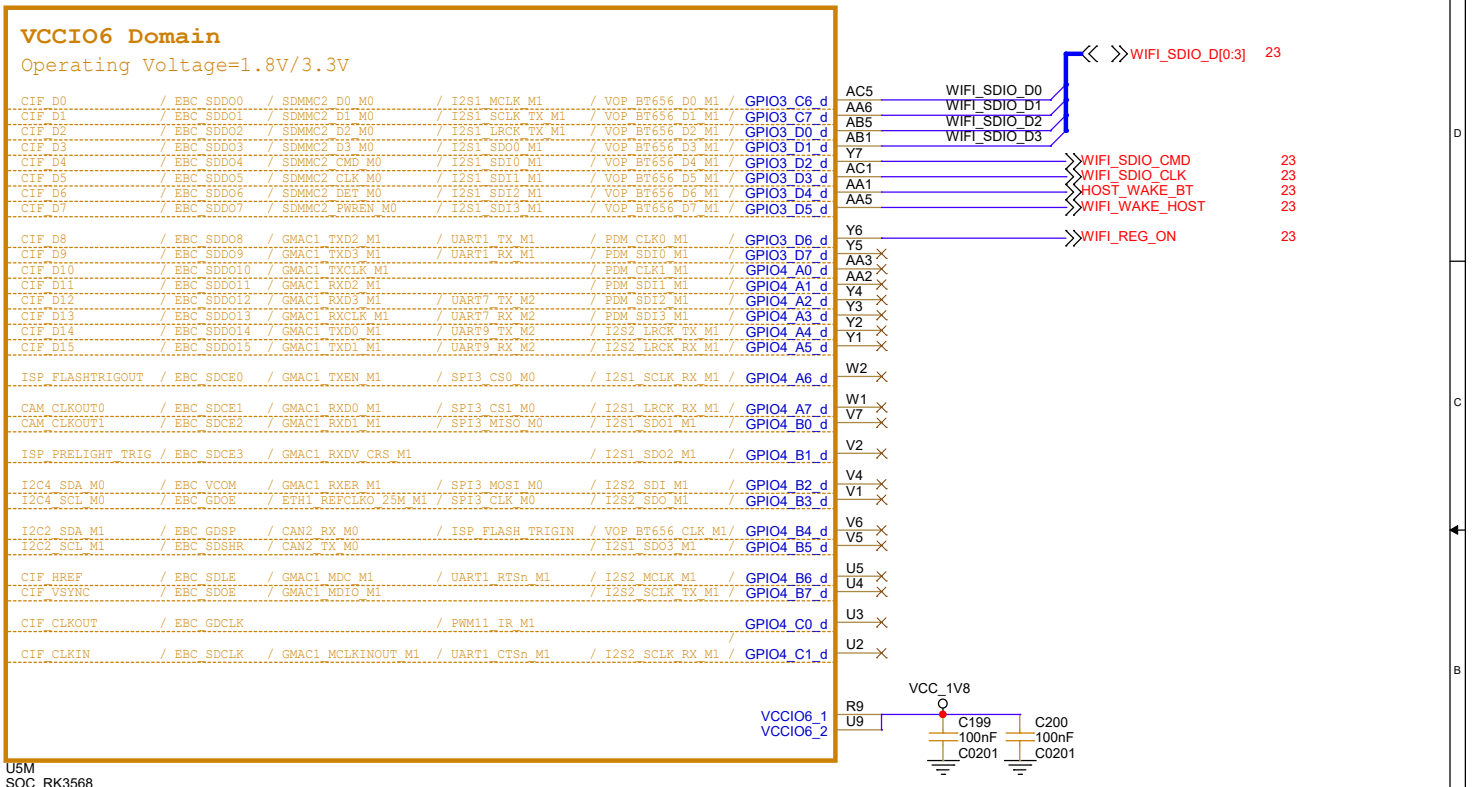
GMAC1_TXD[0:3] 21
GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_TXCLK
GMAC1_TXEN
GMAC1_TXCLK 21
GMAC1_TXCEN 21

ETH1_REFCLKO25M
ETH1_MCLKIN125M
GMAC1_MDC
GMAC1_MDIO
ETH1_REFCLKO25M 21
ETH1_MCLKIN125M 21
GMAC1_MDC 21
GMAC1_MDIO 21

项目名称	<Title>		
电路名称	14.SOC_ETH1_IO		
纸张大小	A	作者	TZH
绘制时间	Tuesday, July 23, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	20



项目名称	<Title>		
电路名称	15.ETH1_RTL8211_PHY		
纸张大小	A4	作者	TZH
绘制时间	Wednesday, July 24, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	21



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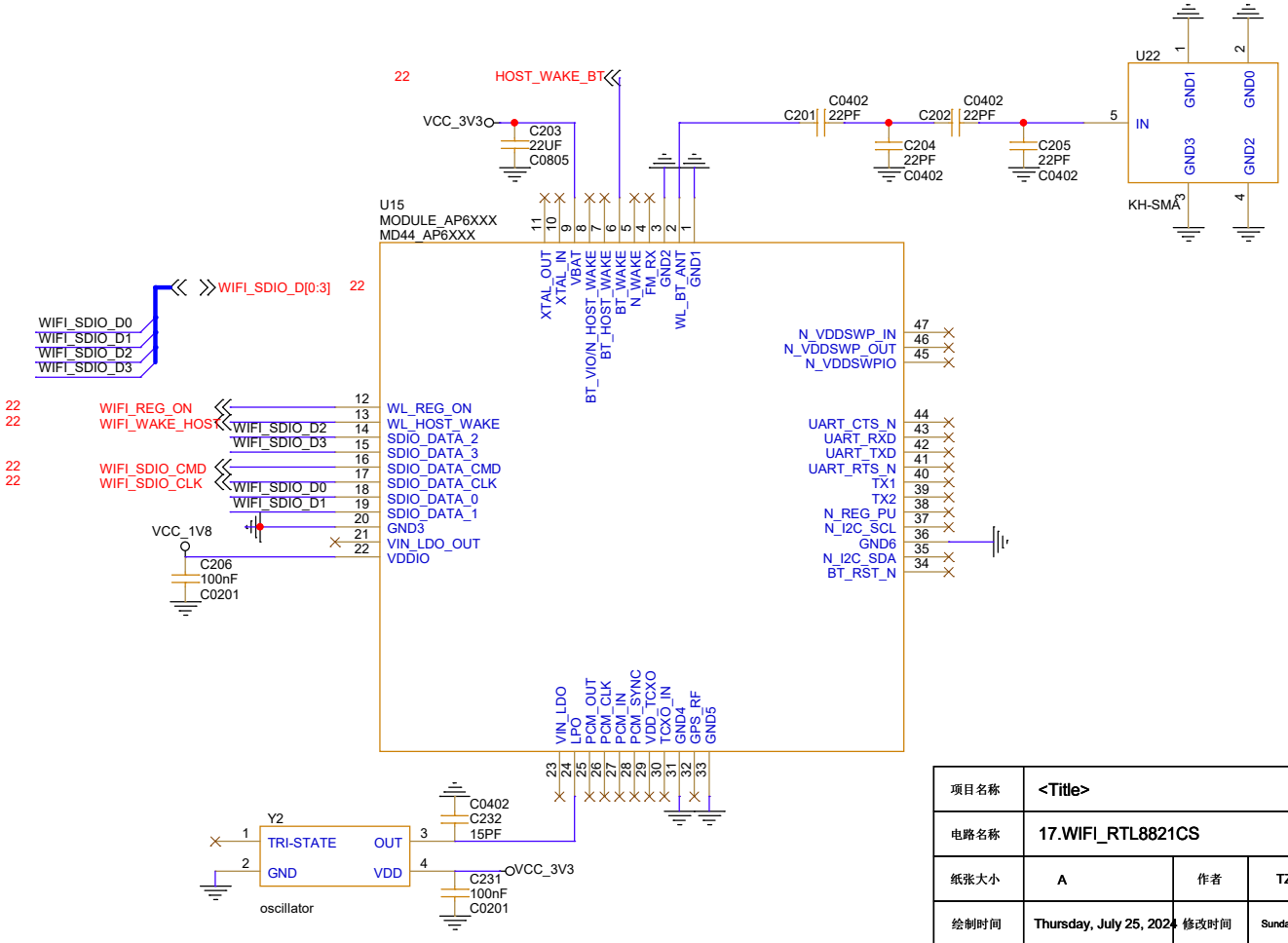
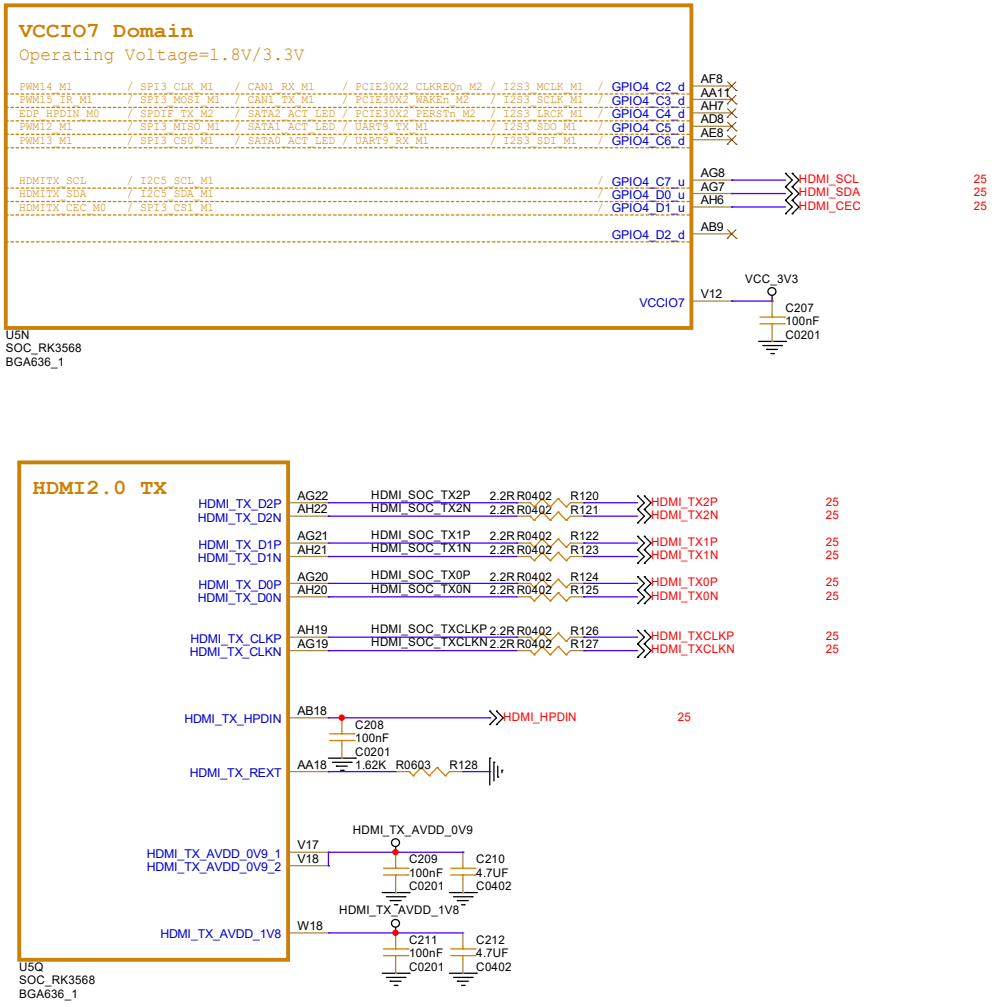
SOC_RK3568
BGA636_1

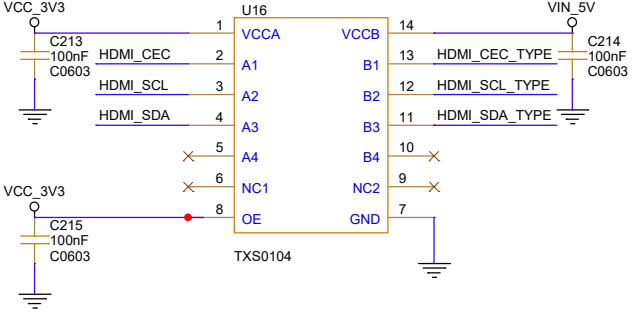
项目名称	<Title>		
电路名称	16.SOC_SDIO_WiFi_IO		
纸张大小	A	作者	TZH
绘制时间	Wednesday, July 24, 202	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	22

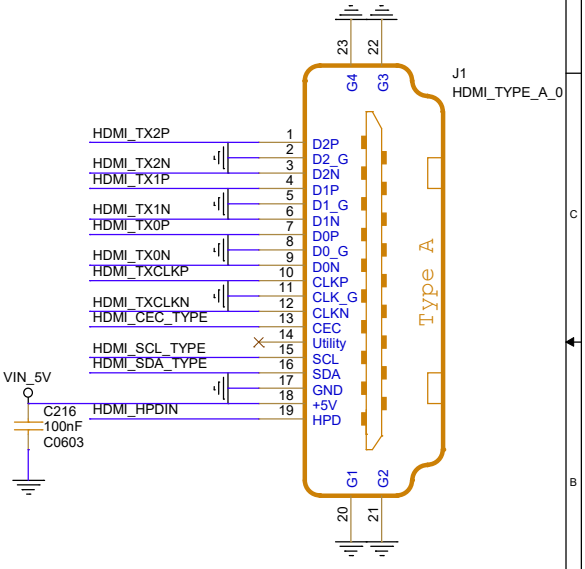


项目名称	<Title>		
电路名称	17.WIFI_RTL8821CS		
纸张大小	A	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	23

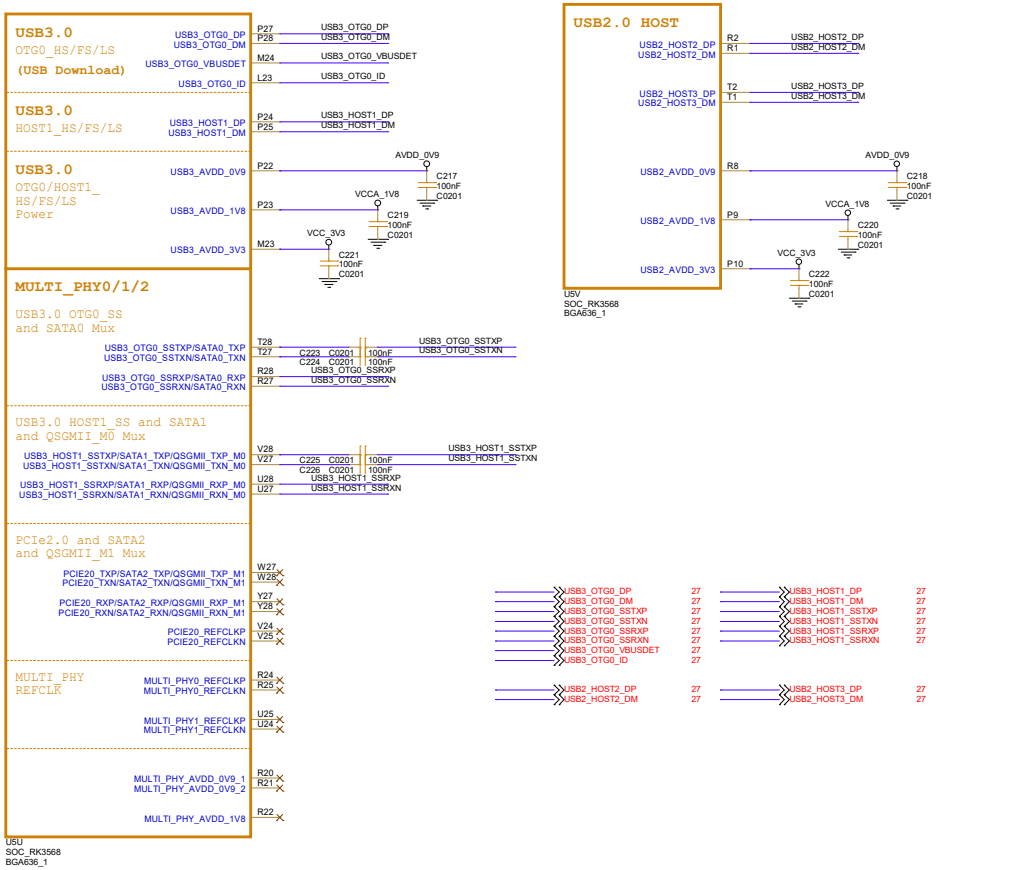


项目名称	<Title>		
电路名称	18.SOC_HDMI_IO		
纸张大小	A4	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	24

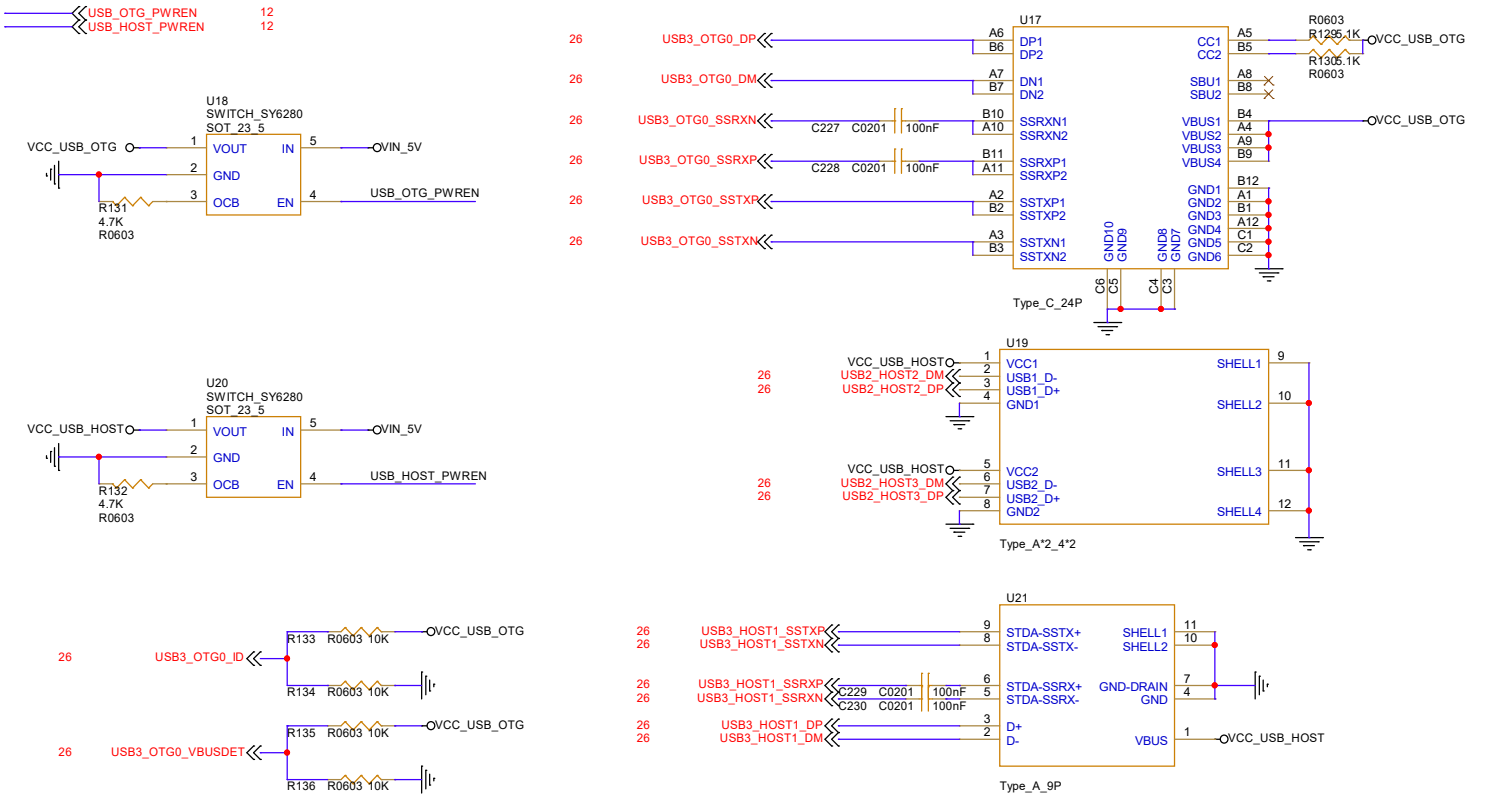




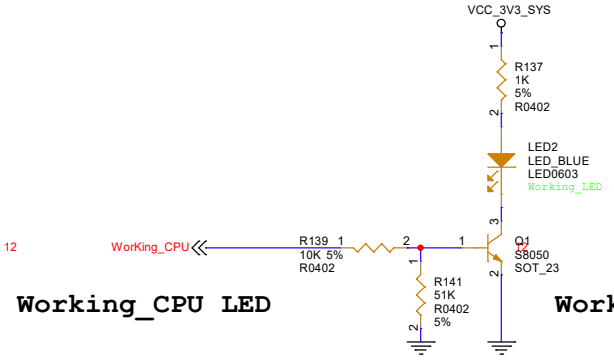
项目名称	<Title>		
电路名称	19.HDMI_TX_PHY		
纸张大小	A	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	25



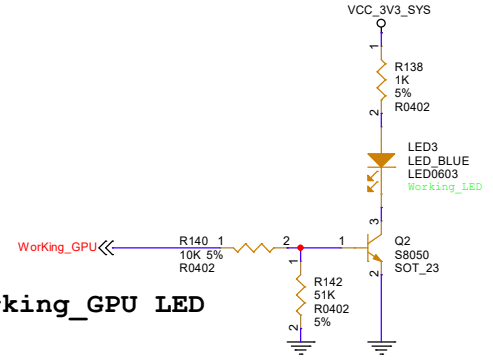
项目名称	<Title>		
电路名称	20.SOC_USB_IO		
纸张大小	Custom	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	26



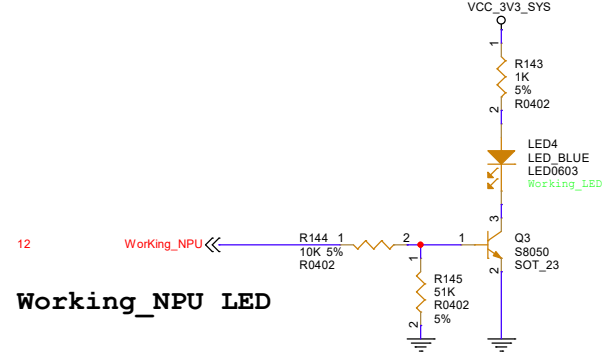
项目名称	<Title>		
电路名称	21.USB2/3_PHY		
纸张大小	A4	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	27



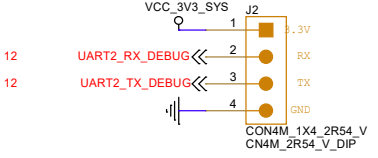
Working_CPU LED

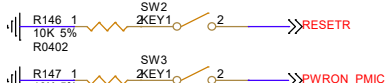


Working_GPU LED

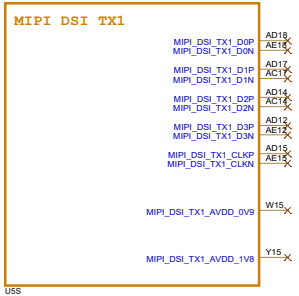


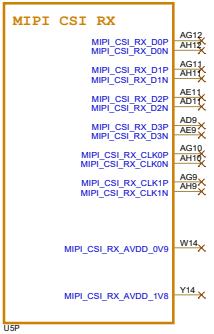
Working_NPU LED

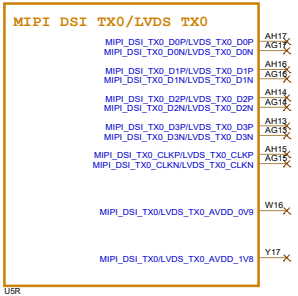


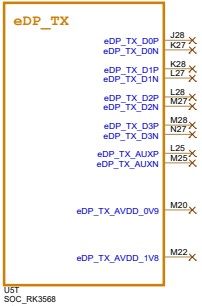


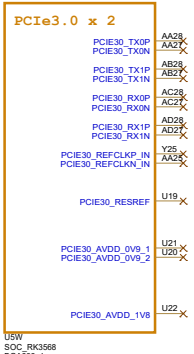
项目名称	<Title>		
电路名称	22.UART/LED/Key_PHY		
纸张大小	A4	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	28

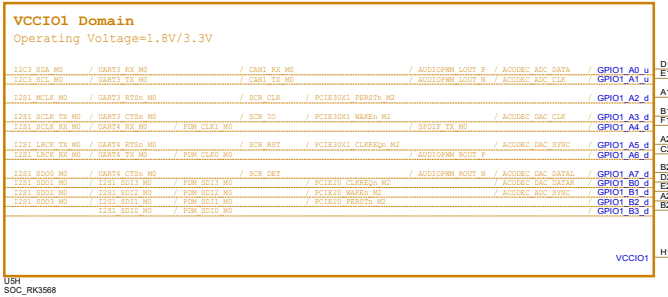












项目名称	<Title>		
电路名称	23.NOT_IO		
纸张大小	A3	作者	TZH
绘制时间	Thursday, July 25, 2024	修改时间	Sunday, September 14, 2025
备注	<remarks>	页码	29