RTD2166-CG

DISPLAYPORT™ TO VGA CONVERTER

PRODUCT BRIEF

(CONFIDENTIAL: Development Partners Only)

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REVISION HISTORY

Revision	Release Date	Summary
1.0	2015/10/02	First release
1.1	2016/12/15	Add 1. Support external monitor 256-byte EDID 2. Smart correction of EDID header and checksum

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1. General Description

The Realtek RTD2166 DisplayPort to VGA converter combines a DisplayPort input interface and an analog RGB DAC output. The embedded MCU is based on an industrial standard 8051 core.

The RTD2166 is suitable for multiple market segments and display applications, such as laptop, motherboard, desktop, dongle, and docking system.

2. Features

General

- 2-lane VESA DisplayPort™ v1.3 compliant receiver
- VGA output interface, DAC speed up to 210-MHz, 8-bit
- Max. resolution up to 1920x1200x60 (RB, reduced blanking) with 24-bit color depth, 1920x1440x60 (RB, reduced blanking) with 18-bit color depth, or 2048x1152x60 (RB, reduced blanking) with 24-bit color depth, or 2048x1536x60 (RB, reduced blanking) with 18-bit color depth.
- Embedded oscillator and there's no need for the external crystal
- Embedded linear dropout regulator (LDO)
- Embedded MCU
- Embedded EDID (RTD2166 will response EDID if terminal device doesn't have it)
- Support external monitor 256-byte EDID
- Smart correction of EDID header and checksum
- Embedded V-sync/H-sync 5V buffer
- Support EEPROM Free mode by using the internal pre-blew ROM
- Programmable internal low-voltage-reset (LVR)
- QFN32 4x4 package

DisplayPort™ Digital Input

- Support 2-lane digital input, speed up to RBR(1.62-Gbps) / HBR (2.7-Gbps)
- VESA DisplayPort™ v1.3 compliant
  - Built-in high performance adaptive equalizer
  - Support 1-MHz AUX channel
  - Support HPD

VGA Output Interface

- Triple 8-bit DAC (Digital-to-Analog Converter) with clock up to 210-MHz
- Support up to 1920x1200x60 (reduced blanking), 1920x1440x60 (reduced blanking), 2048x1152x60 (reduced blanking), and 2048x1536x60 (reduced blanking)
- Embedded V-sync/ H-sync 5V buffer
- HBM 8-KV for VGA connector pins
- VESA VSIS v1r2 compliant

Embedded MCU

- Industrial standard 8051 core
- Support I^2C Master and Slave up to 400-KHz.

Power & Technology

- 3.3V system voltage
- 5V Option for V-sync/ H-sync 5V buffer
- Ultra low standby power < 100uW
- HBM 8-KV for connector pins, and 4.0-KV for the rest pins

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3. System Applications

- Display System on laptop, motherboard, and desktop
- Display System for dongle and docking system

4. Block Diagram

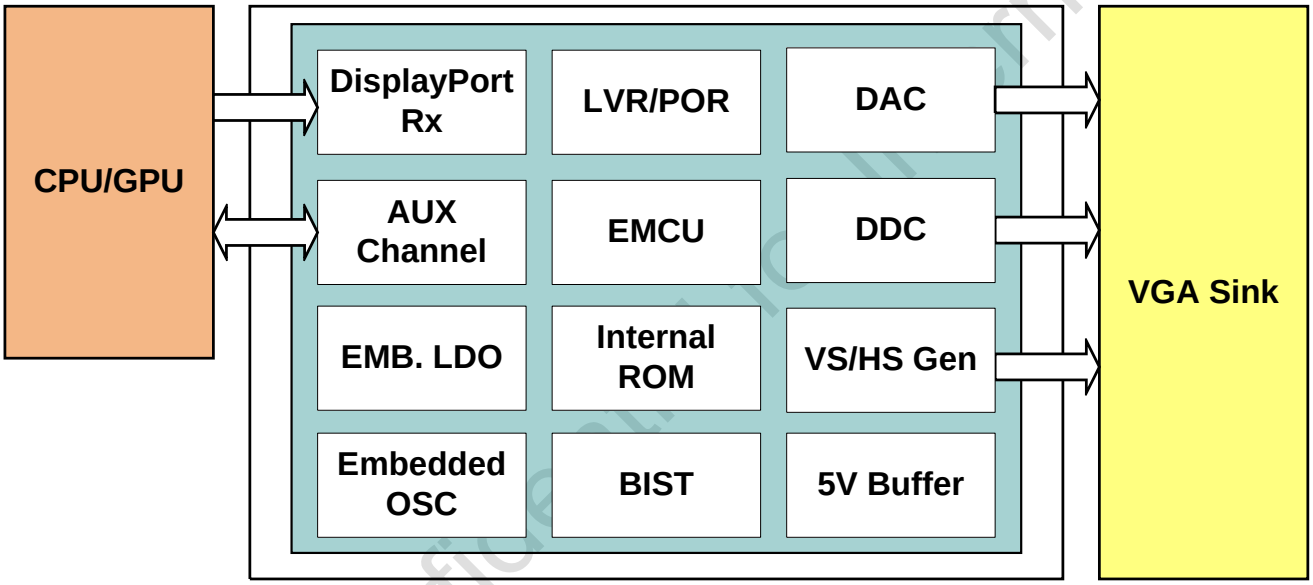

Figure 1. Block Diagram

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5. Pin Assignments

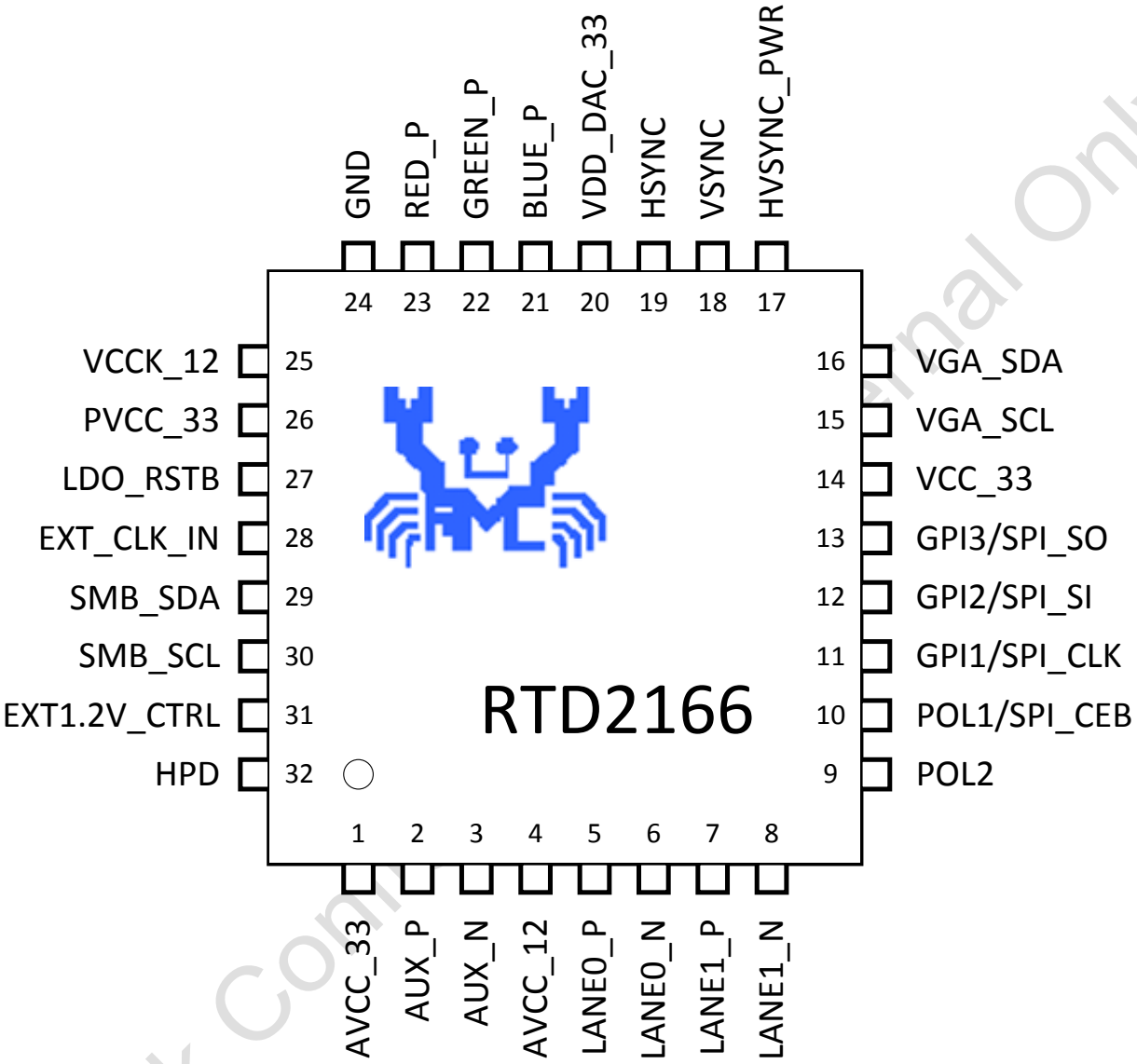

Figure 2. Pin Assignments

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6. Pin Assignments Table

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Table 1 Pin Definition

Pin#	Description	Type	Note
1	AVCC_33	P	Analog power at 3.3V
2	AUX_P	AIO	DP AUX channel positive
3	AUX_N	AIO	DP AUX channel negative
4	AVCC_12	P	Analog power at 1.2V
5	LANE0_P	AI	DP Rx lane0 positive
6	LANE0_N	AI	DP Rx lane0 negative
7	LANE1_P	AI	DP Rx lane1 positive
8	LANE1_N	AI	DP Rx lane1 negative
9	POL2	I	Power on latch selection
10	POL1/SPI_CEB	I/O	Power on latch selection or SPI_CEB (flash mode)
11	GPI1/SPI_CLK	I/O	GPI_1 (ROM mode) or SPI_CLK (flash mode)
12	GPI2/SPI_SI	I/O	GPI_2 (ROM mode) or SPI_SI (flash mode)
13	GPI3/SPI_SO	I/O	GPI_3 (ROM mode) or SPI_SO (flash mode)
14	VCC_33	P	Digital power at 3.3V
15	VGA_SCL	O	VGA DDC clock, 5V tolerance (open-drain)
16	VGA_SDA	O	VGA DDC data, 5V tolerance (open-drain)
17	HVSYNC_PWR	P	Power for embedded H/Vsync buffer (3.3V or 5V optional)
18	VSYNC	O	VGA vertical sync output (3.3V or 5V output)
19	HSYNC	O	VGA horizontal sync output (3.3V or 5V output)
20	VDD_DAC_33	P	Analog power at 3.3V
21	BLUE_P	AO	VGA blue channel output
22	GREEN_P	AO	VGA green channel output
23	RED_P	AO	VGA red channel output
24	GND	G	Ground
25	VCCK_12	P	Analog power at 1.2V
26	PVCC_33	P	LDO power source at 1.2V
27	LDO_RSTB	I	Embedded LDO selection
28	EXT_CLK_IN	I	external reference clock (optional)
29	SMB_SDA	I/O	I2C salve data, 5V tolerance (open-drain)
30	SMB_SCL	I/O	I2C salve clock, 5V tolerance (open-drain)
31	EXT1.2V_CTRL	O	External LDO control for low power mode
32	HPD	O	DP hot plug detection, 5V tolerance

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7. Interfaces and Capability

7.1 DisplayPort™ Input

As a standard DisplayPort™ receiver, RTD2166 consists of two-lane Main Link differential pair, one AUX channel differential pair, and one HPD signal.

1- Main Link

Two lanes differential pair capable of operating HBR (2.7-Gbps) and RBR (1.62-Gbps) data rates for high definition uncompressed video transmission. The main link is fully compliant with the DisplayPort™ v1.3 specification.

2- AUX Channel

A differential half-duplex bi-directional channel used for side-band communication between the DisplayPort™ source and sink devices. The bandwidth of this link is up to 1-Mbps.

3- Hot Plug Detect (HPD)

The HPD signal is fully compliant with the DisplayPort™ v1.3. This includes all input voltage requirements and generation of hot plug and IRQ_HPD events.

7.2 Analog VGA output

RTD2166 integrates triple 8bit-210MHz-DAC (Digital-to-Analog Converters), with each DAC assigned for each color, R (red), G (green), and B (blue). The Analog VGA interface of RTD2166 is compliant with the VESA VSIS v1r2. Real-time Hot plug detection mechanism is also integrated into RTD2166.

The most popular video formats supported by RTD2166 are shown in the following Table 2. However the formats supported by RTD2166 are not limited to this table. Those formats with (a) the data transmission bandwidth lower than the maximal bandwidth of 2-lane DisplayPort™ HBR main-link and (b) the pixel frequency slower than the maximal DAC speed 210-MHz can also be supported by RTD2166.

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Table 2 Supported Popular Timing/ Resolution

Resolution	Refresh Rate (Hz)	Horizontal Freq. (KHz)	Pixel Freq. (MHz)	Standard Type	Ori. Document	Date
640 x 350	85	37.9	31.500	VESA Standard	VDMTPROP	3/1/96
640 x 400	85	37.9	31.500	VESA Standard	VDMTPROP	3/1/96
720 x 400	85	37.9	31.500	VESA Standard	VDMTPROP	3/1/96
640 x 480	60	31.5	25.175	Industry Standard		
	72	37.9	31.500	VESA Standard	VS901101	12/2/92
	75	37.5	31.500	VESA Standard	VDMT75HZ	10/4/93
	85	43.3	36.000	VESA Standard	VDMTPROP	3/1/96
800 x 600	56	35.2	36.000	VESA Guidelines	VG900601	8/6/90
	60	37.9	40.000	VESA Guidelines	VG900602	8/6/90
	72	48.1	50.000	VESA Standard	VS900603A	8/6/90
	75	46.9	49.500	VESA Standard	VDMT75HZ	10/4/93
	85	53.7	56.250	VESA Standard	VDMTPROP	3/1/96
848 x 480	60	31.0	33.750	VESA Standard	AddDMT	3/4/03
1024 x 768	43 (Int.)	35.5	44.900	Industry Standard		
	60	48.4	65.000	VESA Guidelines	VG901101A	9/10/91
	70	56.5	75.000	VESA Standard	VS910801-2	8/9/91
	75	60.0	78.750	VESA Standard	VDMT75HZ	10/4/93
	85	68.7	94.500	VESA Standard	VDMTPROP	3/1/96
1152 x 864	75	67.5	108.000	VESA Standard	VDMTPROP	3/1/ 96
1280 x 720	60	45.0	74.250	CEA Standard	CEA -861	
1280 x 768	60 (RB)	47.4	68.250	CVT Red. Blanking	AddDMT	3/4/03
	60	47.8	79.500	CVT	AddDMT	3/4/03
	75	60.3	102.250	CVT	AddDMT	3/4/03
	85	68.6	117.500	CVT	AddDMT	3/4/03
1280 x 800	60 (RB)	49.3	71.000	CVT Red. Blanking	CVT1.0 2MA-R	5/1/ 07
	60	49.7	83.500	CVT	CVT 1.02MA	5/1/07
	75	62.8	106.500	CVT	CVT 1.02MA	5/1/07
	85	71.6	122.500	CVT	CVT 1.02MA	5/1/07
1280 x 960	60	60.0	108.000	VESA Standard	VDMTPROP	3/1/ 96
	85	85.9	148.500	VESA Standard	VDMTPROP	3/1/ 96
1280 x 1024	60	64.0	108.000	VESA Standard	VDMTREV	12/18/96
	75	80.0	135.000	VESA Standard	VDMT75HZ	10/4/93
	85	91.1	157.500	VESA Standard	VDMTPROP	3/1/96
1360x768	60 (RB)	48.0	72.000	VESA Standard	DMT Update	11/30/07
	60	47.7	85.500	VESA Standard	AddDMT	3/4/03
	60	47.7	85.500	VESA Standard	DMT Update	11/30/07
1400 x 1050	60 (RB)	64.7	101.000	CVT Red. Blanking	AddDMT	5/13/03
	60	65.3	121.750	CVT	AddDMT	3/4/03
	75	82.3	156.000	CVT	AddDMT	3/4/03
	85	93.9	179.500	CVT	AddDMT	3/4/03
1440 x 900	60 (RB)	55.5	88.750	CVT Red. Blanking	CVT1.30MA-R	7/14/04
	60	55.9	106.500	CVT	CVT1.30MA-R	7/14/04
	75	70.6	136.750	CVT	CVT1.30MA-R	7/14/04
	85	80.4	157.000	CVT	CVT1.30MA-R	7/14/04
1600 x 900	60 (RB)	60.0	108.000	VESA Standard	VDMTREV	11/17/08
1600 x 1200	60	75.0	162.000	VESA Standard	VDMTREV	12/18/96
	65	81.3	175.500	VESA Standard	VDMTREV	12/18/96
	70	87.5	189.000	VESA Standard	VDMTREV	12/18/96
	75	93.75	202.5	VESA Standard	VDMTREV	12/18/96
1680 x 1050	60 (RB)	64.7	119.000	CVT Red. Blanking	CVT1.76MA-R	7/14 /04
	60	65.3	146.250	CVT	CVT1.76MA-R	7/14 /04
	75	82.3	187.000	CVT	CVT1.76MA-R	7/14 /04
1920 x 1080	60	67.5	148.500	CEA Standard	CEA -861	-
1920 x 1200	60 (RB)	74.0	154.000	CVT Red. Blanking	AddDMT	3/4/03
	60	74.6	193.250	CVT	AddDMT	3/4/03
1920 x 1440	60 (RB)	88.822	184.750	CVT Red. Blanking	CVT2.76M3-R	-
2048 x 1152	60 (RB)	70.992	156.750	CVT Red. Blanking	VDMT REV	11/17 /08
2048 x 1536	60 (RB)	94.769	209.250	CVT Red. Blanking	CVT3.15M3-R	-
2560 x 1080	60 (RB)	66.636	181.250	Cinema 21:9 Aspect Ratio	N/A	N/A

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8. Electrical Specifications

8.1. Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Voltage on Input (5V tolerant)	V_{IN}	-1	-	5	V
	HVSYNC_PWR (5V Input)	4.75	5	5.25	V
	HVSYNC_PWR (3.3V Input)	3.0	3.3	3.6	V
Supply Voltage	VCC_33	3.0	3.3	3.6	V
	PVCC_33	3.0	3.3	3.6	V
	AVCC_33	3.0	3.3	3.6	V
	VDD_DAC_33	3.0	3.3	3.6	V
	AVCC_12	1.14	1.2	1.26	V
	VCCK_12	1.14	1.2	1.26	V
Output High Voltage	V_{OH}	2.4	-	-	V
Output Low Voltage	V_{OL}	GND	-	0.4	V
Input High Voltage	V_{IH}	2.0	-	-	V
Input Low Voltage	V_{IL}	-	-	0.8	V
Input Leakage Cur.(Vin=Vcc/GND)	I_{LI}	-10	-	+10	μA
Ambient Operating Temperature	T_A	0	-	70	ºC
Storage temperature (plastic)	T_{STG}	-55	-	125	ºC
Thermal Resistance (Junction to case thermal resistance)	θ_{JC}	-	21.2	-	ºC/W
Thermal Resistance (Junction to Air)	θ_{JA}	-	39.5	-	ºC/W
Junction Acceptable Temperature	T_j	-	-	125	ºC

8.2. Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage temperature (plastic)	T_{STG}	-	150	ºC
Junction Temperature	T_j	-	150	ºC
Electrostatic Discharge (Internal Pin)	V_{ESD}		±4	kV
Electrostatic Discharge (External Pin)	V_{ESD}		±8	kV
Latch-Up	I_{LA}		±100	mA

Note: Long term operation at absolute maximum ratings will affect device reliability and cause permanent damage.

8.3. AC Characteristic

The DisplayPort™ receiver of RTD2166, as a standard DP v1.3 complaint Rx, follows the AC specification of DisplayPort™ v1.3 Standard. The related AC parameters are shown in the following two tables.

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Table 5 DisplayPort™ Main Link AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
UI_HBR	Unit interval for HBR(2.7-Gbps)	-	370	-	ps
UI_RBR	Unit interval for RBR(1.62-Gbps)	-	617	-	ps
Down_Spread_Amp.	Link clock down spreading	0	-	0.5	%
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage at RX package pins for HBR (2.7-Gbps)	120	-	-	mV
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage at RX package pins for RBR (1.62-Gbps)	40	-	-	mV
T_{RX-EYE_CHIP}	Minimum receiver eye width at Rx package pins for HBR (2.7-Gbps)	0.47	-	-	UI
T_{RX-EYE_CHIP}	Minimum receiver eye width at Rx package pins for RBR (1.62-Gbps)	0.22	-	-	UI
$T_{RX-MEDIAN-to-MAX-JITTER}$	Max time between the jitter median and max. deviation from the median at Rx package pins for HBR (2.7-Gbps)	-	-	0.265	UI
$T_{RX-MEDIAN-to-MAX-JITTER}$	Max. time between the jitter median and max. deviation from the median at Rx package pins for RBR (1.62-Gbps)	-	-	0.39	UI
$V_{RX-DC-CM}$	RX DC Common Mode Voltage	0	-	2.0	V
$I_{RX-SHORT}$	RX Short Circuit Current Limit	-	-	50	mA

Table 6 DisplayPort™ AUX-CH AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
UI_{MAN}	AUX (Manchester transaction) unit interval	0.4	0.5	0.6	us
Pre-charge	Number of pre-charge pulses	10	-	16	-
$T_{AUX-BUS-PARK}$	AUX CH bus park time	10	-	-	ns
$T_{cycle-to-cycle}$ jitter	Max. allowable UI variation within a single transaction at connector pins of a Rx	-	-	0.05	UI
$V_{AUX-DIFFp-p}$	AUX peak-to-peak voltage at a receiving device	0.32	-	1.36	V
$V_{AUX\_TERM\_R}$	AUX CH termination DC resistance	-	100	-	Ω
$V_{AUX-DC-CM}$	AUX DC common mode voltage	0	-	2.0	V
$V_{AUX-TURN-CM}$	AUX turn around common mode voltage	-	-	0.3	V
I_{AUX_SHORT}	AUX short circuit current	-	-	90	mA
C_{AUX}	AUX AC coupling capacitor	75	-	200	nF

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8.4. Power Sequence

This section describes the power sequencing requirements for RTD2166.

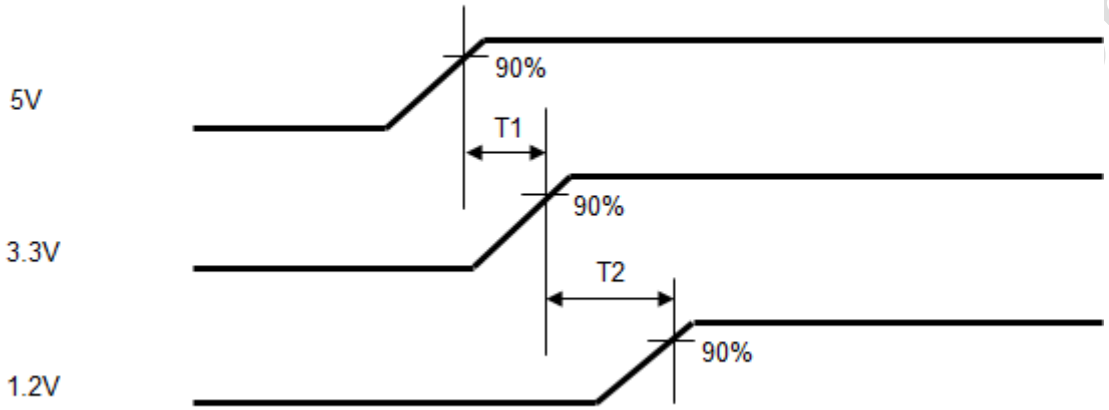

Figure 3. Power Sequence

Table 7 Power Sequencing Requirements

Operating Mode	Parameter	Min	Max	Unit
External 1.2V mode	T1	0	-	ms
	T2	-10	10	ms
Embedded LDO Mode	T1	0	-	ms
	T2	-	-	ms

Note 1: T2 is specified only when 1.2V comes from external power source.

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8.5. Power Consumption

Different applications would result in different power consumptions of RTD2166. For example, whether to the embedded LDO, whether to adopt the embedded oscillator, and how fast of the video clock frequency are all definitely the key factors of the power consumption of RTD2166. The following tables show the reference power consumption of RTD2166 in several different application conditions

Table 8 Power Consumption by Using External 1.2V, External Clock Source, and 3.3V HVSYNC_PWR

Active Resolution / Standby	DP Config.	Min	Typ	Max	Unit
1024x768x60 (74.25-MHz)	1-Lane	-	275	-	mW
1600x900x60 (103-MHz)	1-Lane	-	285	-	mW
1920x1080x60 (148-MHz)	2-Lane	-	315	-	mW
Stand-by mode	-	-	-	100	uW

Table 9 Power Consumption by Using Embedded LDO, Embedded Clock Source, and 5V HVSYNC_PWR

Active Resolution / Standby	DP Config.	Min	Typ	Max	Unit
1024x768x60 (74.25-MHz)	1-Lane	-	435	-	mW
1600x900x60 (103-MHz)	1-Lane	-	455	-	mW
1920x1080x60 (148-MHz)	2-Lane	-	550	-	mW
Stand-by mode	-	-	-	100	uW

Note: In practice, the measured power consumption might be slightly different from the tables above due to the different video content and the different measurement equipment

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9. Mechanical Specifications

Plastic Quad Flat No-Lead Package 32 Leads 4x4mm^2 Outline

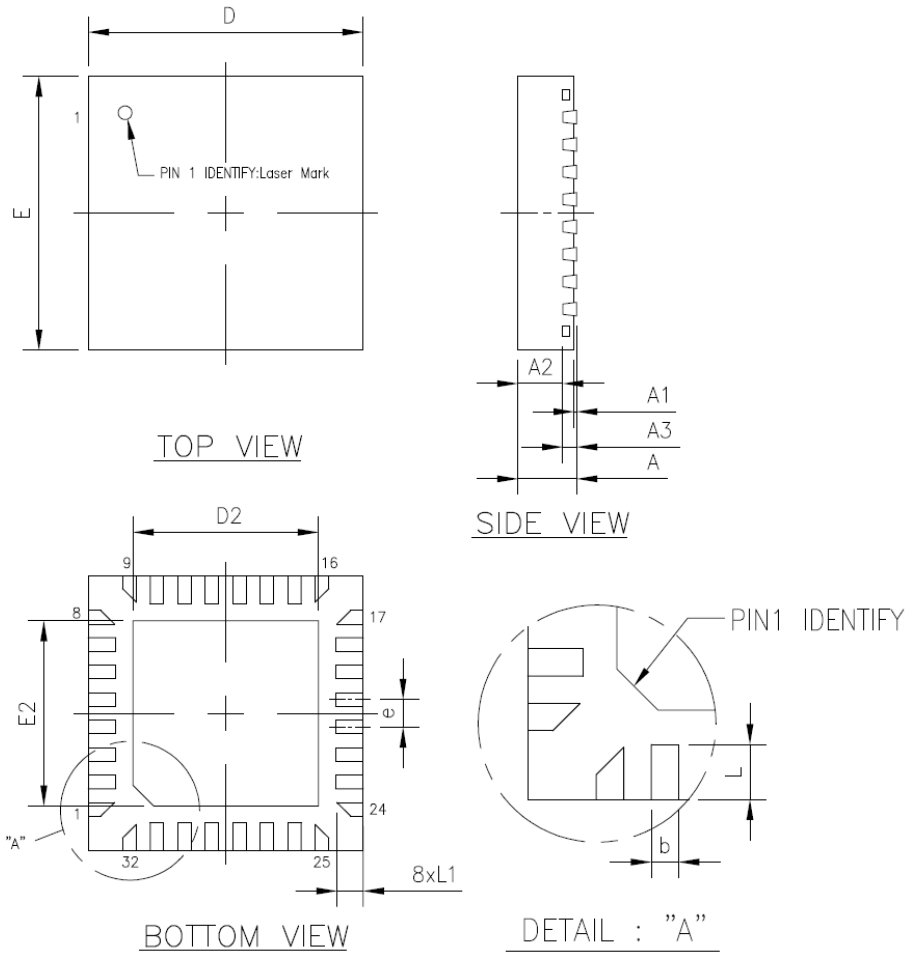

Table 10 Dimensions

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.65	0.70	—	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.080	0.010
D/E	4.00 BSC			0.157 BSC		
D2/E2	2.55	2.70	2.85	0.096	0.106	0.116
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.282	0.382	0.482	0.011	0.015	0.019

Notes：

1. *CONTROLLING DIMENSION：MILLIMETER(mm).*
2. *REFERENCE DOCUMENTL：JEDEC MO-220.*

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10. Ordering Information

Table 11 **Ordering Information**

Part Number	Package	Status
RTD2166-CG	32 Pin (QFN)	MP

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