Τμήμα Μηχανικών Η/Υ και Πληροφορικής, Πανεπιστήμιο Ιωαννίνων

Introduction to low-power microprocessor design - Motivation

Vasileios Tenentes

University of Ioannina

E-mail: tenentes@cse.uoi.gr

ARM® University Worldwide Education Program

Outline

1: Overview of microprocessors manufacturing process

2: Motivation: Why to care about power efficient microrprocessors?

3: Performance of microprocessors

4: Dynamic power and dynamic power reduction design techniques

5: Static power and static power reduction techniques

6: The future, Introduction to IoT applications!!!

Physical applications of microprocessors

How a chip is made: Intel’s 22 nm process

source: https://www.youtube.com/watch?v=d9SWNLZvA8g

How a chip is made: Intel's 22 nm process

source: https://www.youtube.com/watch?v=d9SWNLZvA8g

Its all clear now!

diegofloor 3 months ago

It's all clear now! First you slice the weird garlic, then clean it with blue liquid, Take some pictures with a jigsaw puzzle, look at it with a magnifying glass, spray it with dettol power (it kills 99.9% of all bacteria), then you take a kitchen sponge and dissolve the upper part until it resembles a tennis court. From here on I admit it got a little confusing. I might need more sponges than I anticipated.

(Forgive my silliness. This is a cool video :)

Show less

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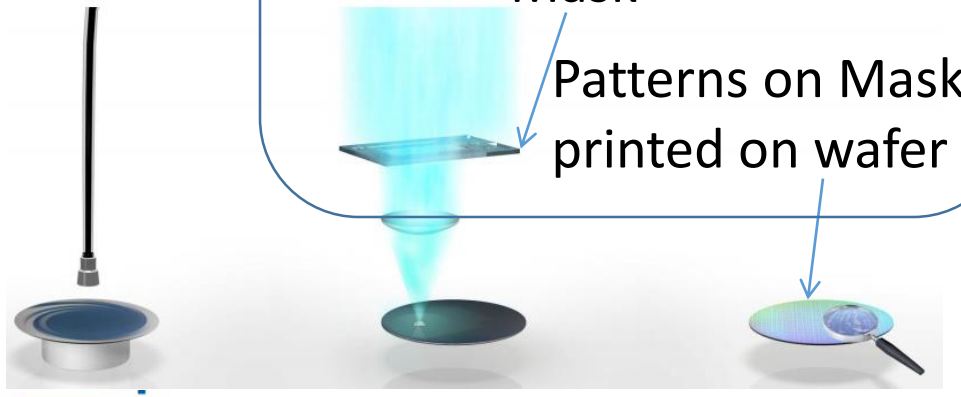
Manufacturing Process: From Sand to Wafer

Wafer is the base for building Integrated Circuits (ICs)

Manufacturing Process

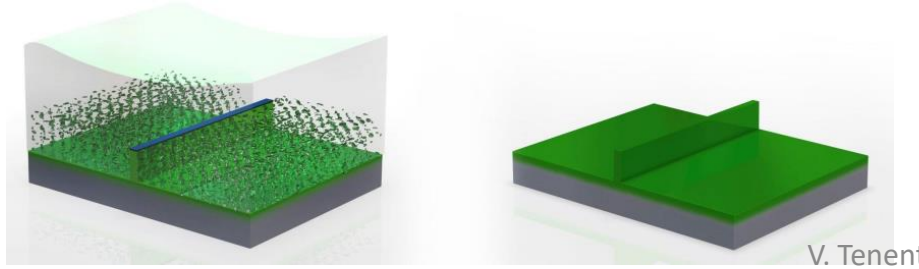
This mask is
the physical product of the design and is required for the manufacturing!

Photolithography
Photoresistivity,
Exposure and Removal

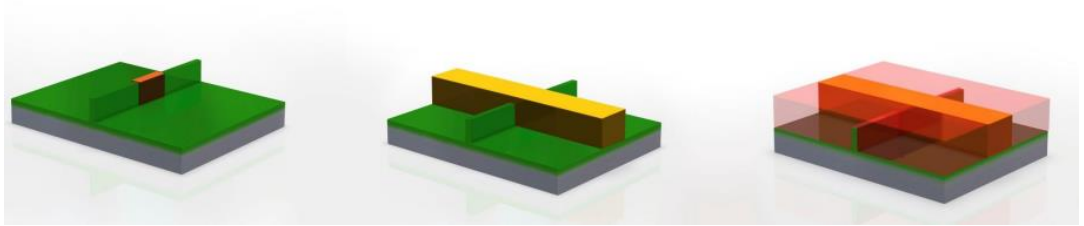


Ion Implantation

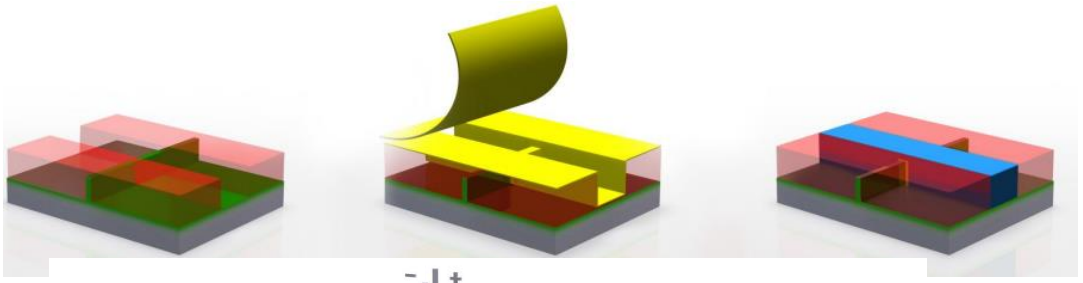
Etching:
Removing unwanted regions



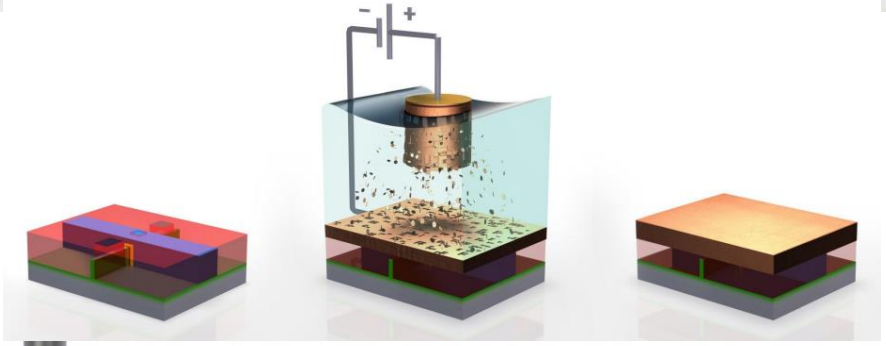
Manufacturing Process



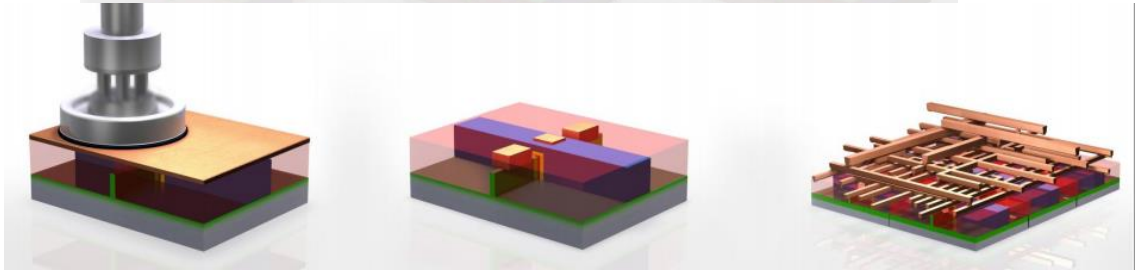
Gate Dielectric,
Gate Electrode & Insulator



Etching, and High-k Metal Gate



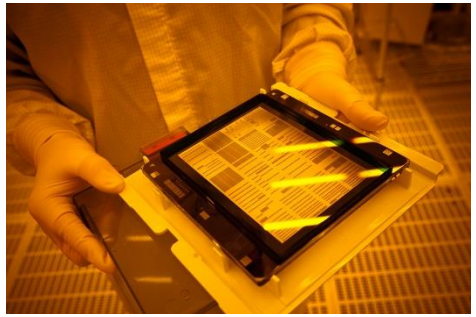
Transistor, Electroplating, Copper thin layer on Wafer Surface

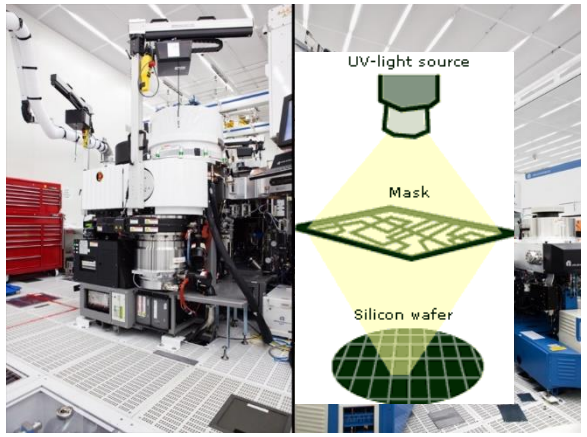


Polishing and Interconnections

Shortly: Mask – Deposit – Etch - Repeat

Any design of SoCs based on CMOS becomes eventually a lithography mask





Applied Materials' Maydan Technology Center,
a state-of-the-art clean room in Santa Clara, California

So why we don't design at the physical level directly?

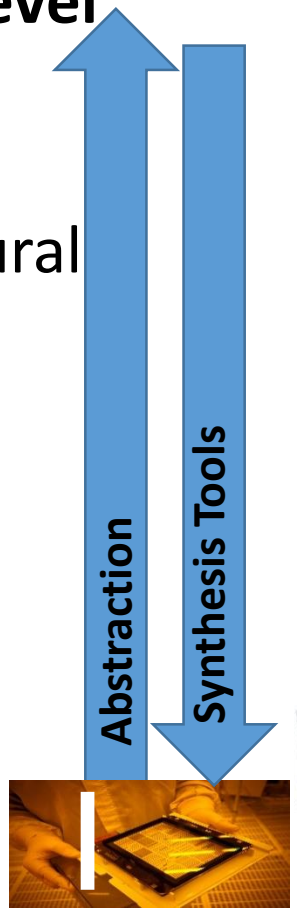
System Architecture Level

Register-Transfer Level (behavioral and structural description)

Logic Level (gates)

Transistor Level

Physical Level (lithography mask)

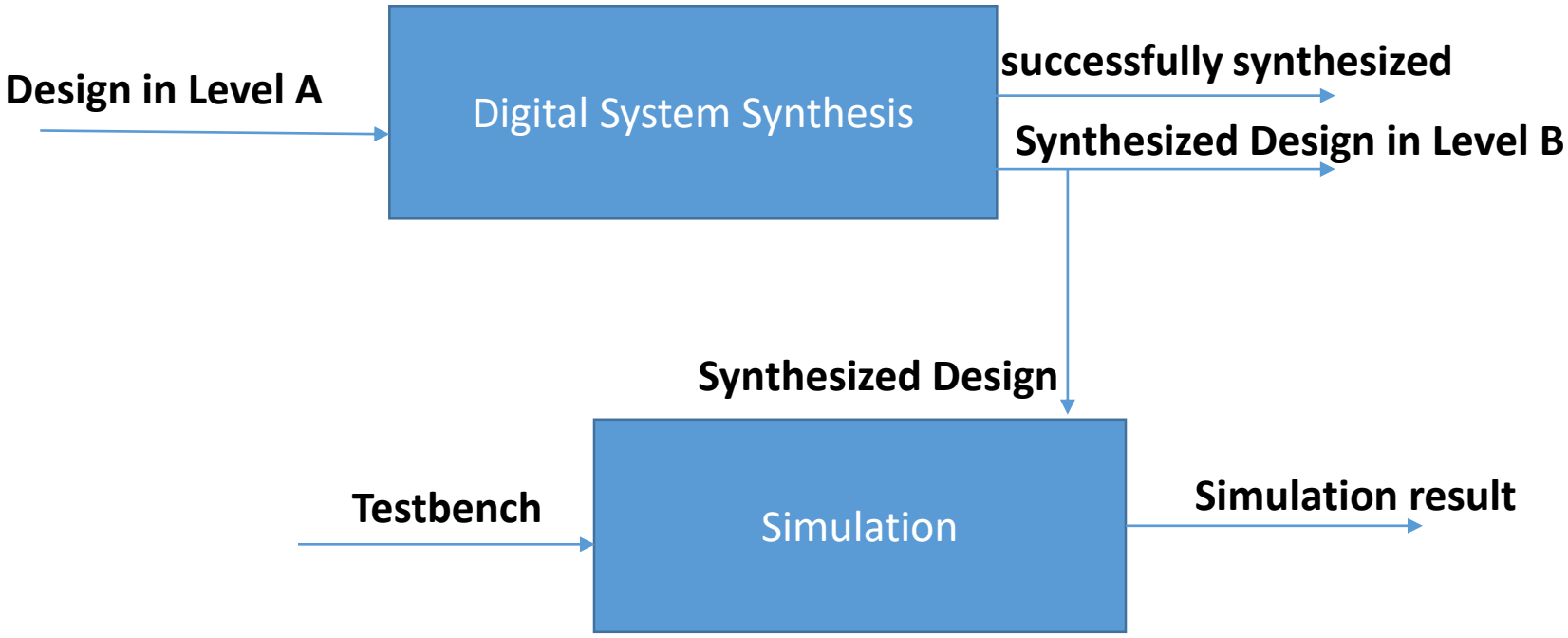


We need **abstraction** of the designing process through **synthesis tools**. It leads to:

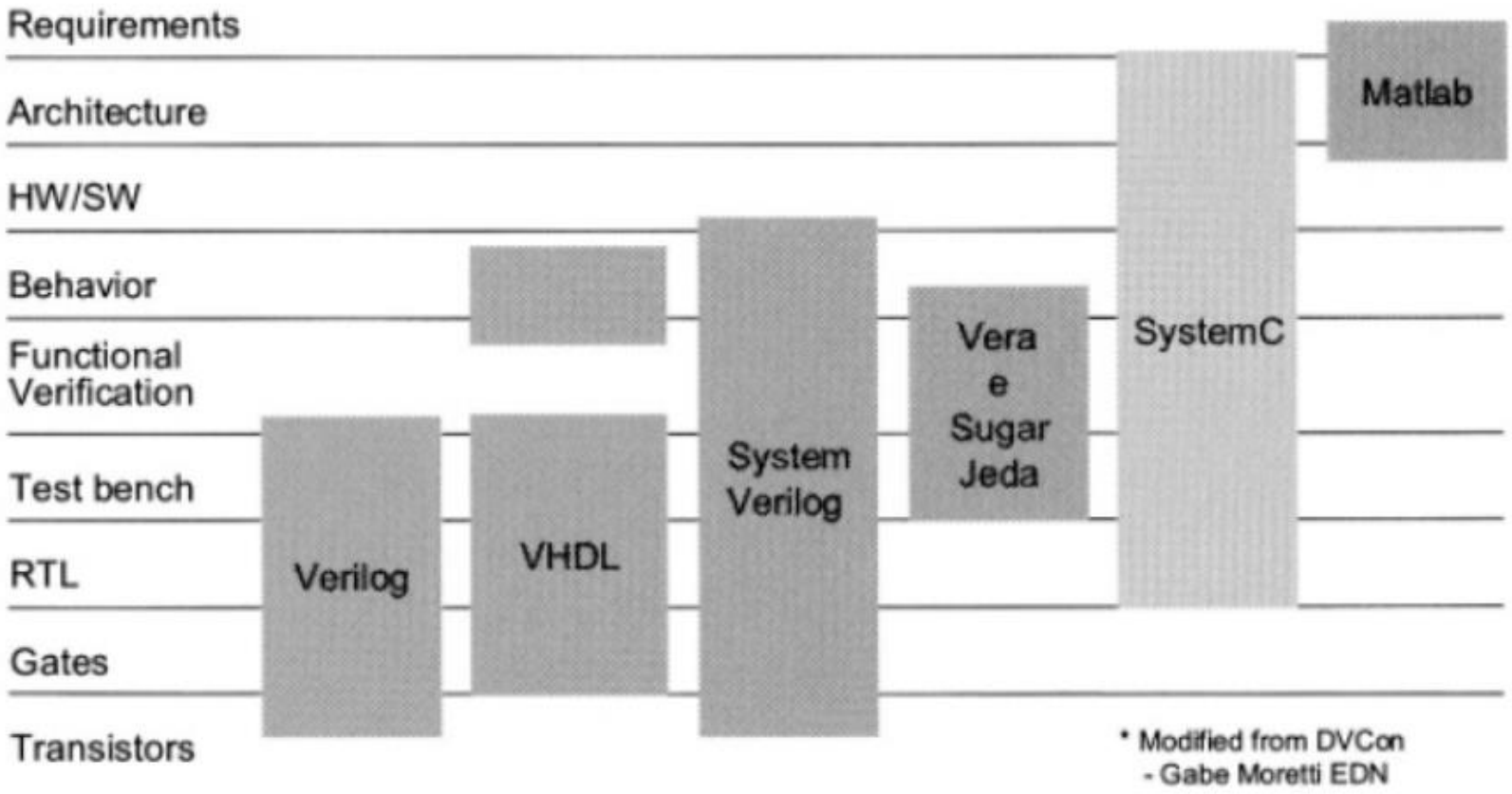
- Faster and cheaper design/manufacturing cycle
- More functionality
- Reusable designs
- !! provides control of specification requirements!
- Applications diversity

V. Tenentes

Synthesis is implementing abstraction



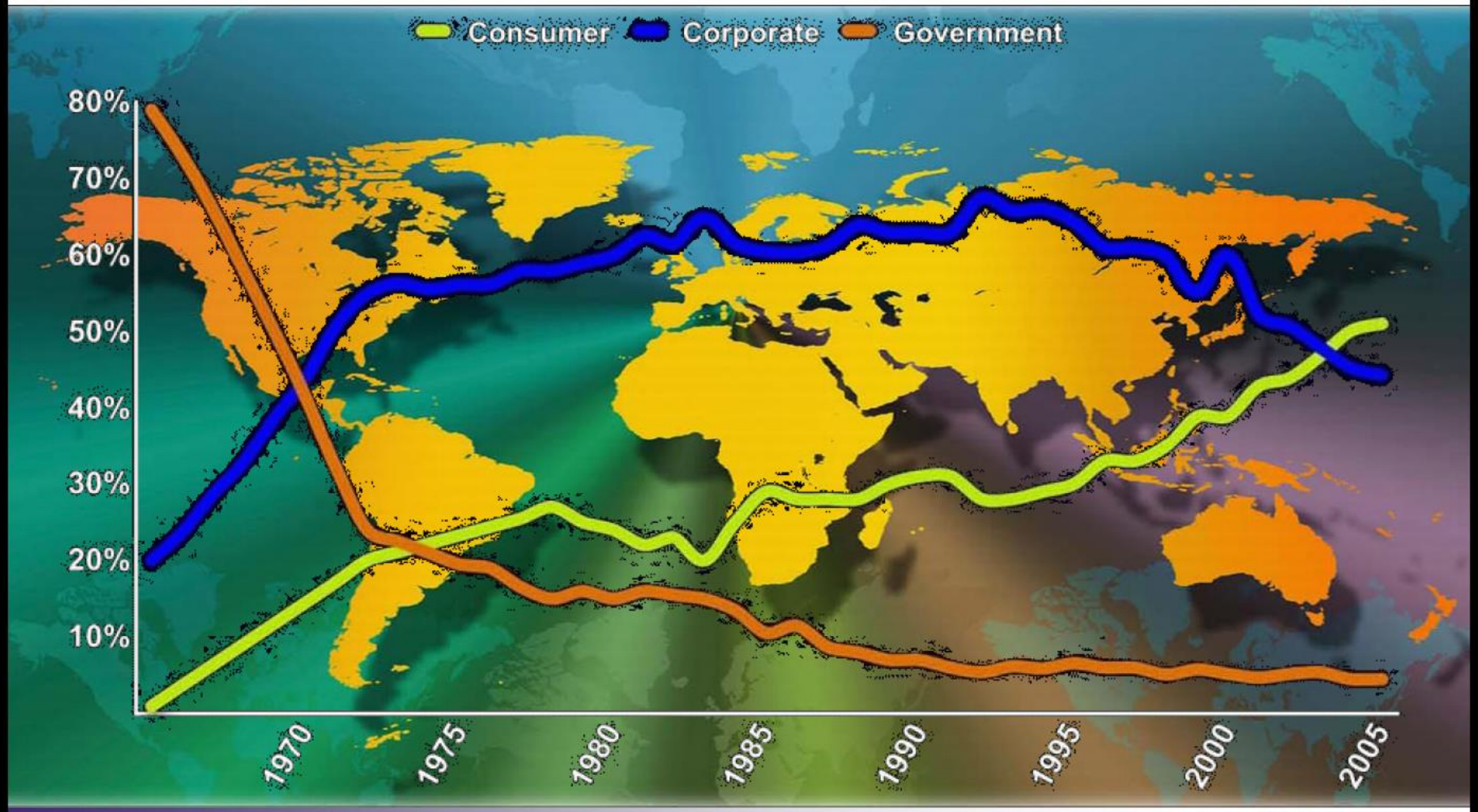
Example of tools/languages used in low-power design



Motivation: Why to care about power efficient microrprocessors?

The Era Of The Consumer is it over?

Households, Semiconductor Industry's #1 Customer

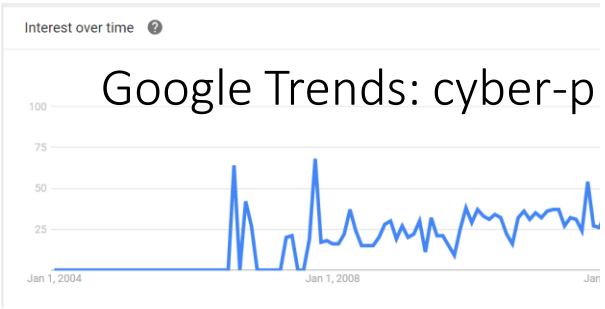


Source: J.-H. Huang, SIA 2004

Smart applications of embedded systems (Cyber-Physical Systems and Internet of Things (IoT))

1926 Nikola Tesla

"When wireless is perfec
converted into a huge br
instruments through wh
be amazingly simple con
A man will be able to car



Source: everything 4.0? Sabina Jesch
2013, invited talk Wuppertal

Back to: The earth converted into a huge "brain"... (Tesla 1926)

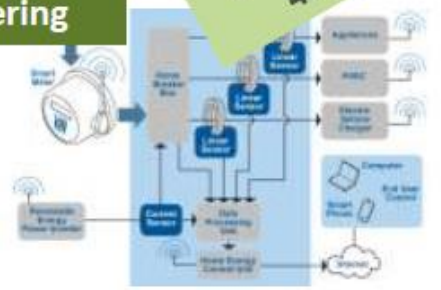
Integrating complex information from multiple heterogenous sources opens multiple possibilities of optimization: e.g. energy consumption, security services, rescue services as well as increasing the quality of life

Building automation

„house 4.0"

Smart metering

„metering 4.0"



Smart grid

„power grid 4.0"

Room automation

„room 4.0"

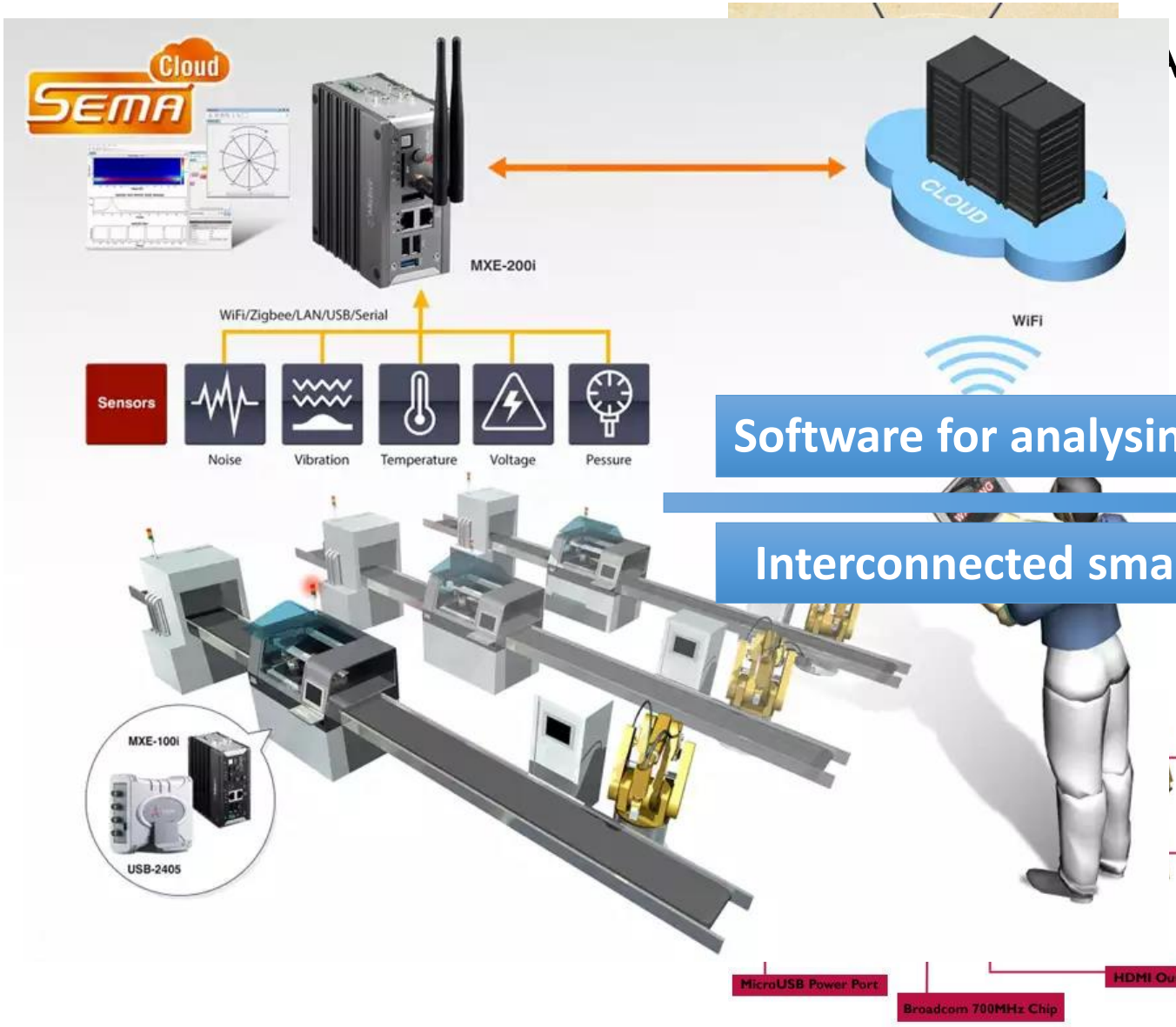
Smart environment

„mobility 4.0"

„...th 4.0"

... and more

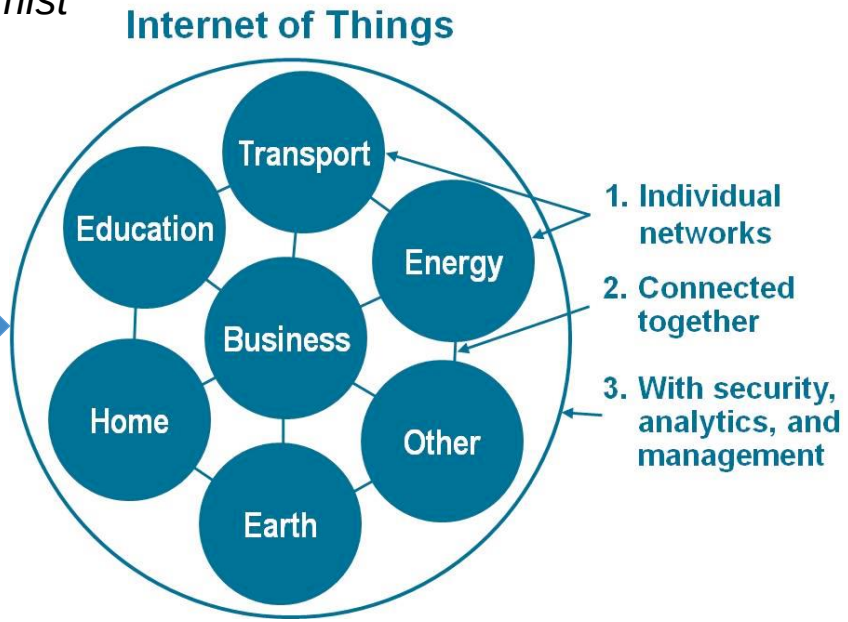
Drivers for CPS/IoT applications



Holy Cow!
A cow generates …
200 MB a year
Source: Augmented business, economist

Software for analysing big data

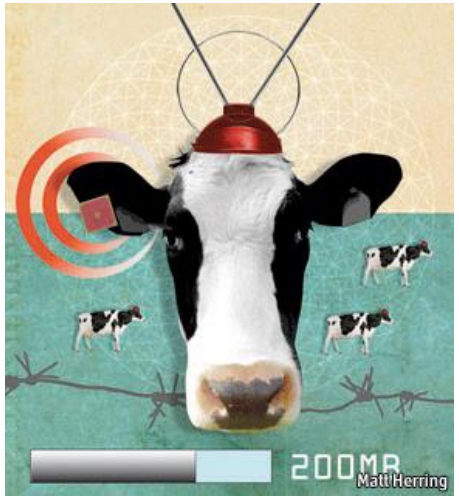
Interconnected small devices

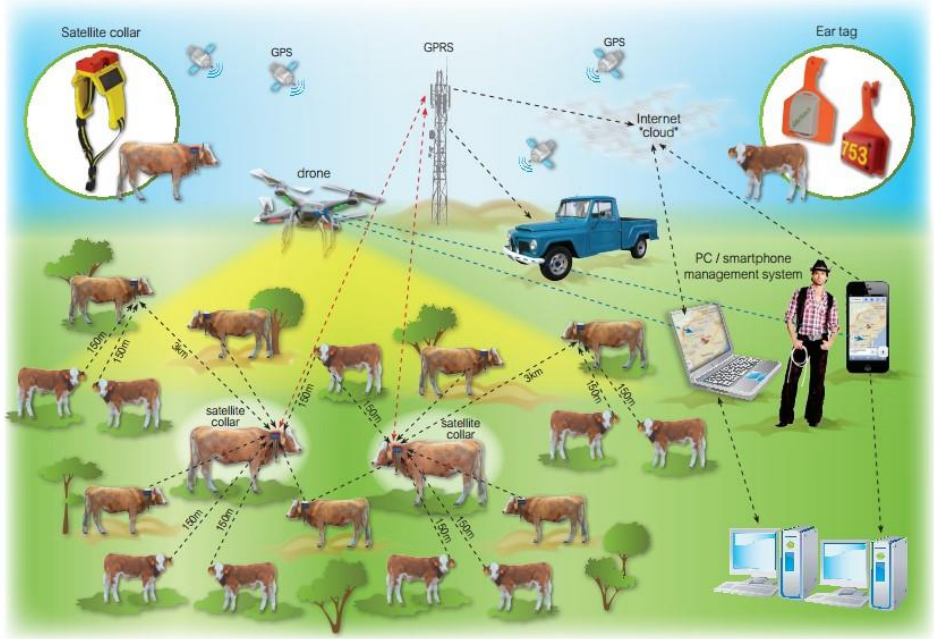


Wearable embedded systems on cattle

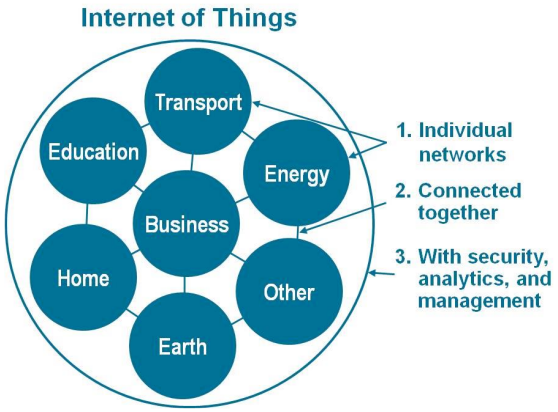
For monitoring their position and status…

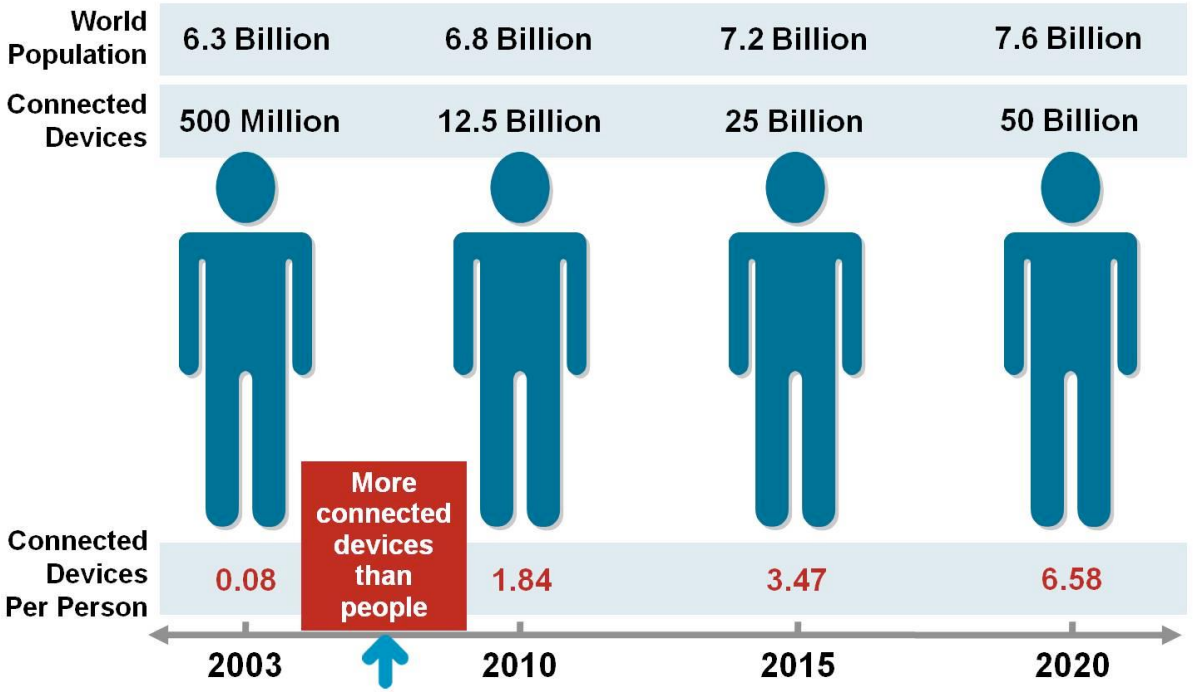
Holy Cow!
A cow generates …
200 MB a year
Source: Augmented business, economist





Energy efficiency: the bottleneck for the Internet-of-Things (IoT)





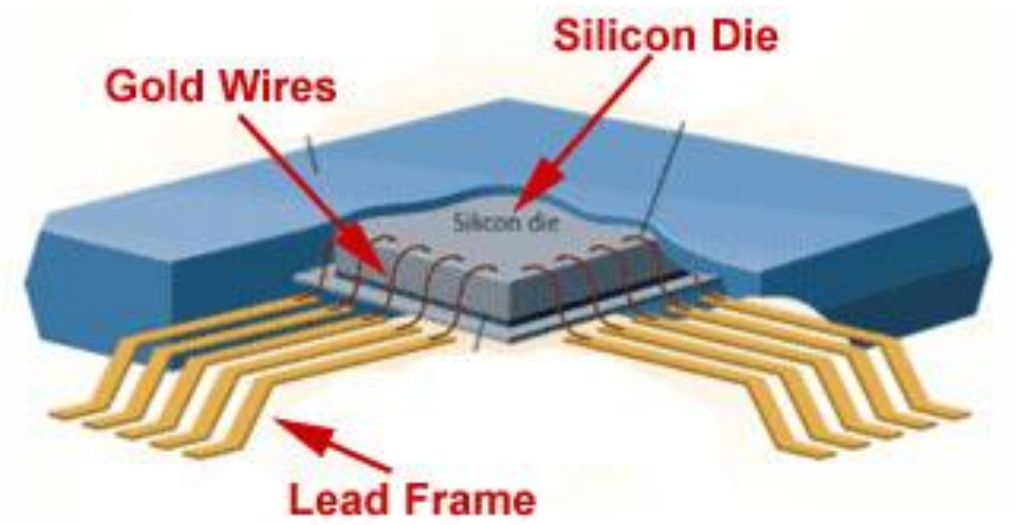
- There is an exponential growth of the demand for connected devices
- There is a bound of 50 Billion connected devices due to **energy constraints** at the networking infrastructure (ARM white paper)
  - Low power digital hardware is required especially for IoT networking stacking (see mbed SoCs) **https://www.openfogconsortium.org**

D. Evans, "The internet of things: How the next evolution of the internet is changing everything," CISCO White paper, vol. 1, p. 14, 2011.
"The Intelligent Flexible Cloud," https://community.arm.com/docs/ DOC-9981, ARM Ltd, White Paper, 2015.
"Intelligent Flexible IoT Nodes," https://community.arm.com/docs/ DOC-10861, ARM Ltd, White Paper, 2015.

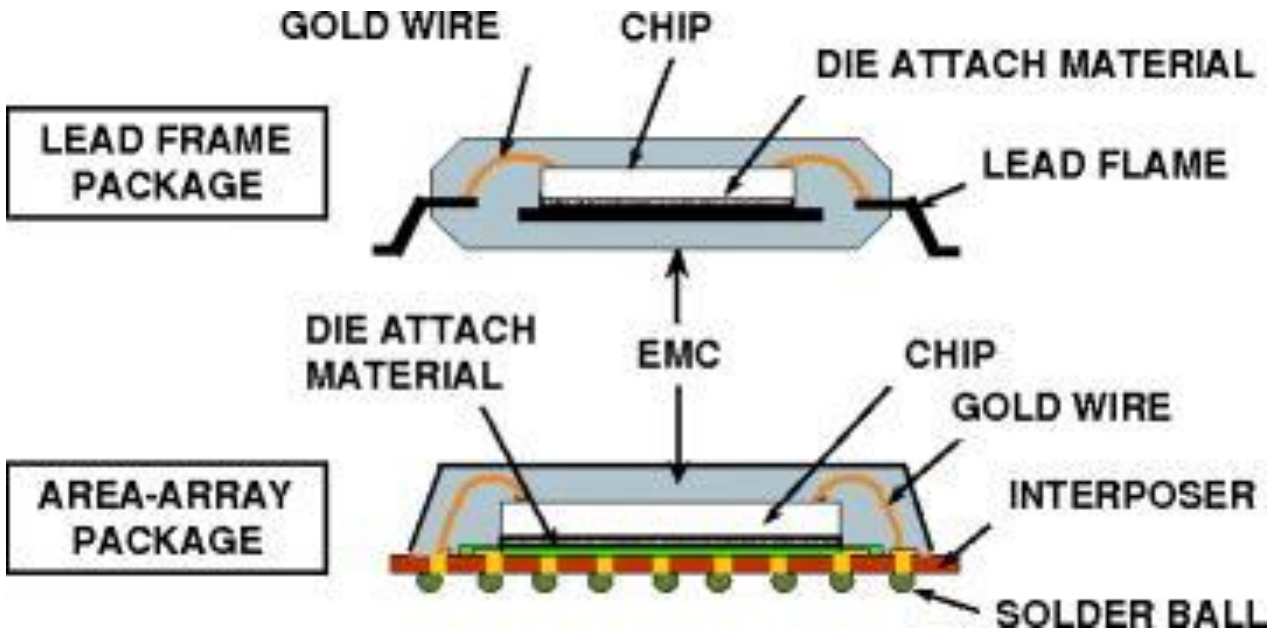
Power density problems that arise

Drivers/Motivation for tackling the power density problem

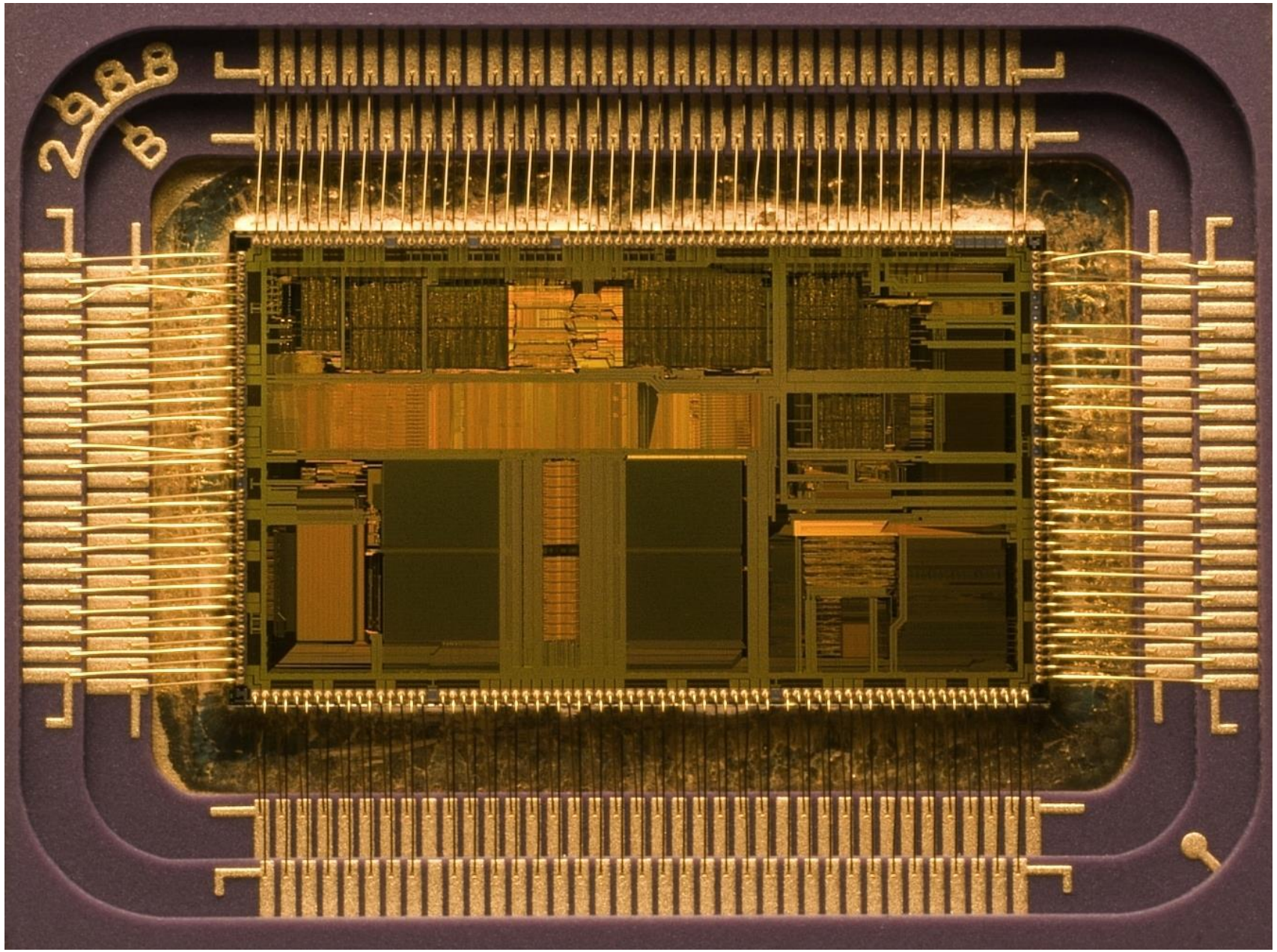
1. Extension of battery life for mobile and IoT applications
2. Reduce cooling costs in enterprise servers
3. Improve system reliability (high power density is causing reliability issues!!!)



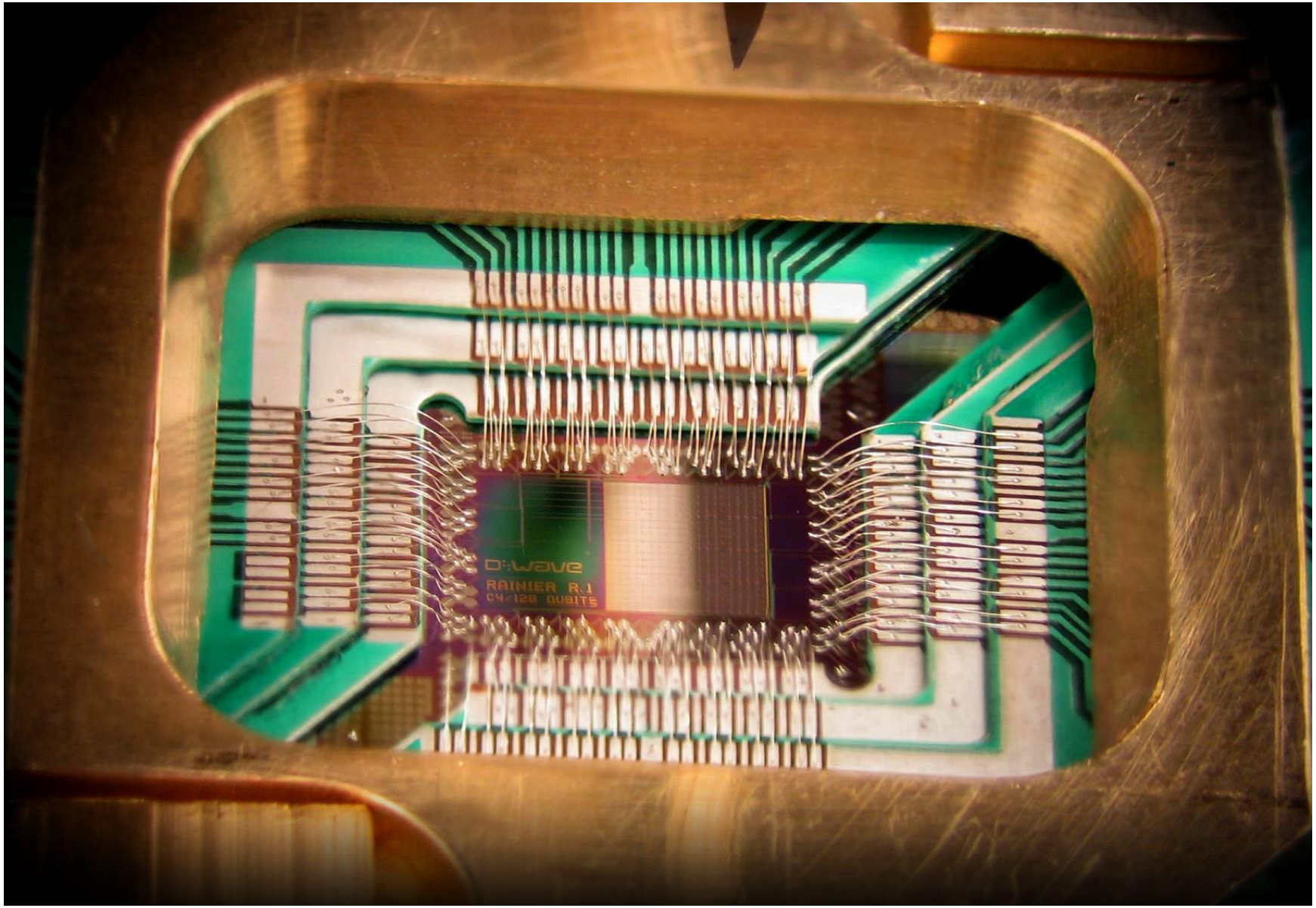
Many packaging technologies



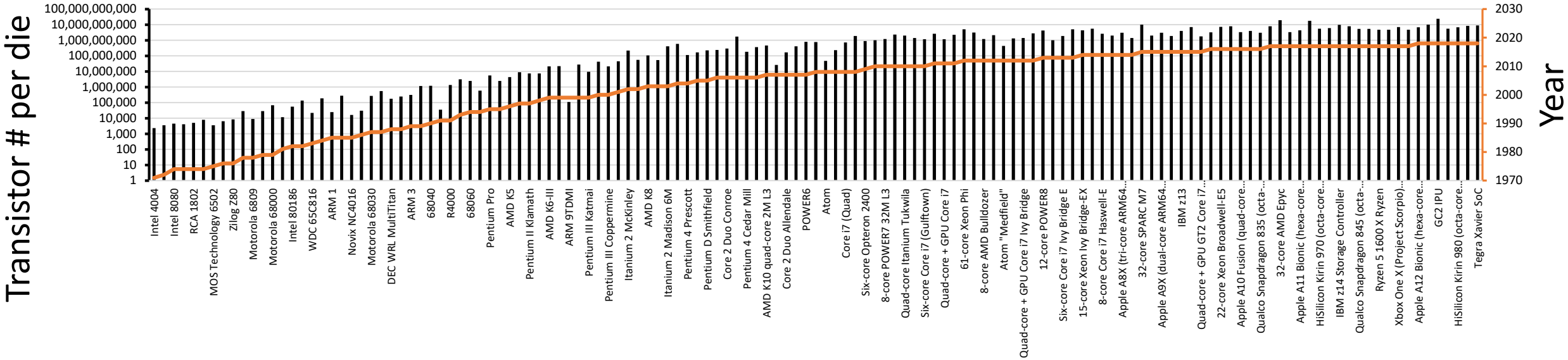
Intel 80486DX2 **CPU**



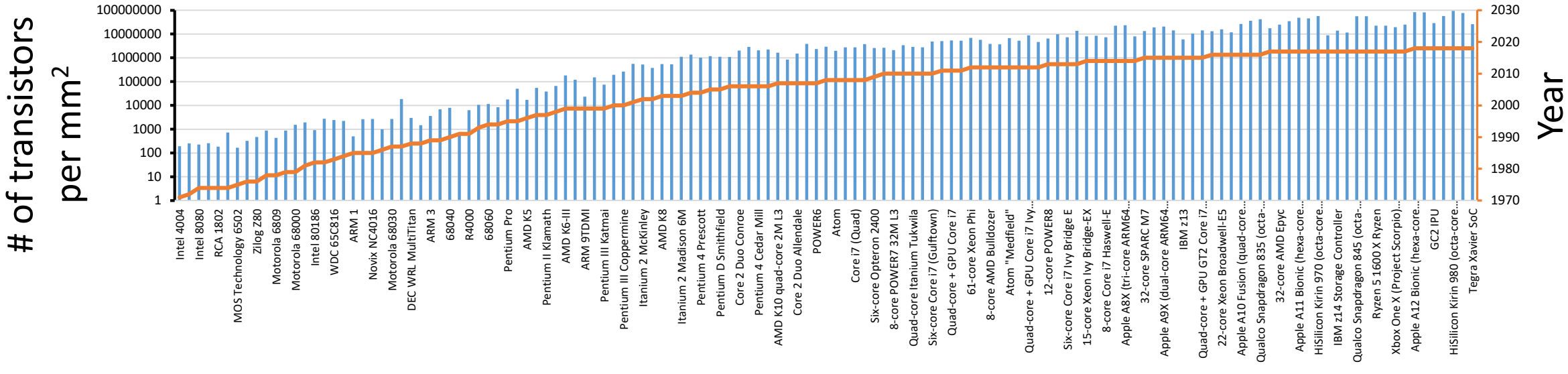
D-Wave Systems Inc., designed to operate as a 128-qubit superconducting adiabatic quantum optimization processor



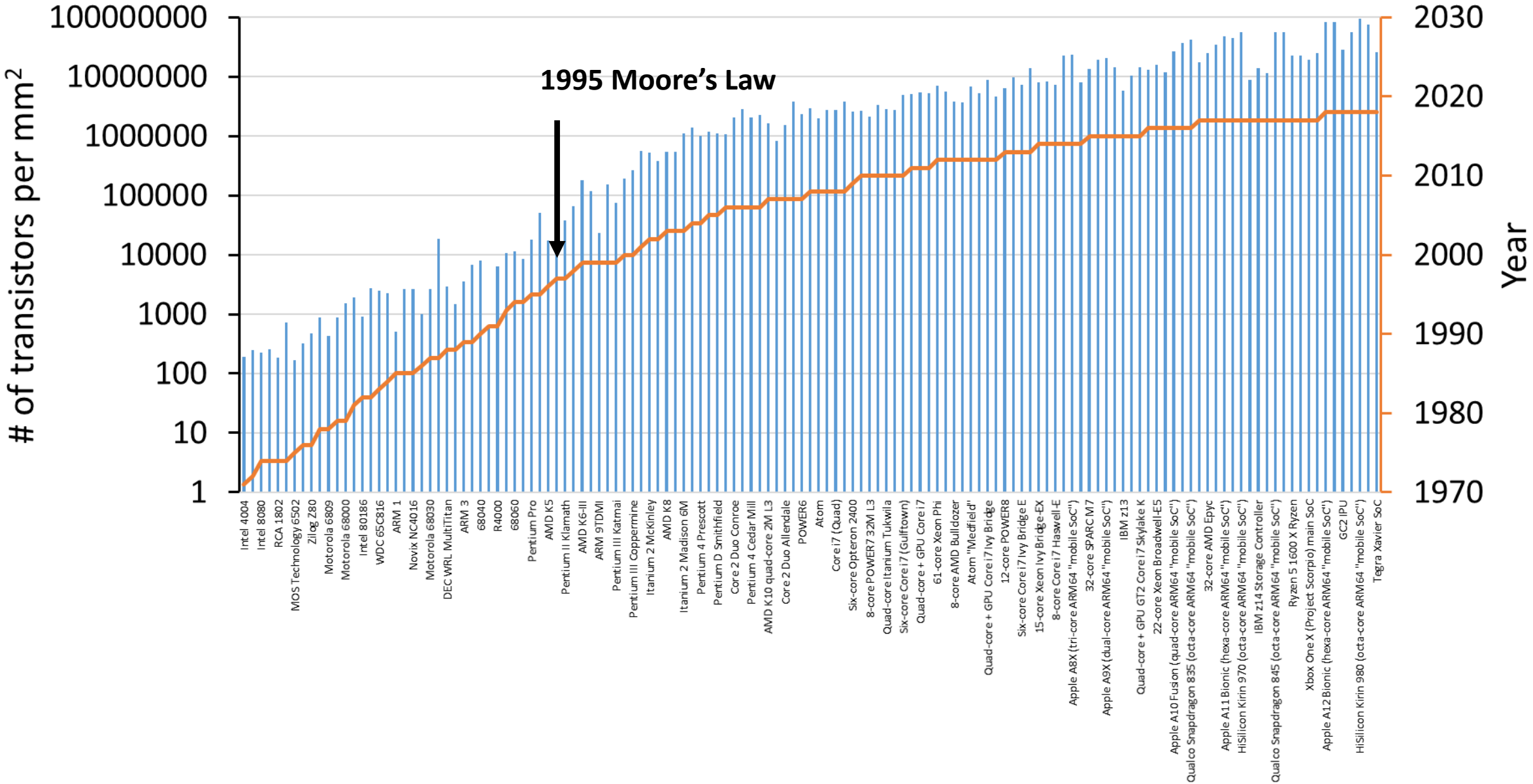
Transistor density = (# of transistors per die)



Transistor density = (# of transistors) / on one square mm



Transistor density = (# of transistors) / on one square mm



Transistor Density aspect of Moore's Law is holding well