```
`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:      02:15:27 09/19/2015
// Design Name:      BCDadder
// Module Name:      G:/12Labs/Lab1/process of    Lab1/Proj1/BCDadder_test.v
// Project Name:    Proj1
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: BCDadder
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module BCDadder_test;

	// Inputs
	reg [3:0] A;
	reg [3:0] B;
	reg Cin;


	reg CinM;


	// Outputs
```

```
  wire [3:0] sM;
  wire CoutM;
 wire Couts;
  // Instantiate the Unit Under Test (UUT)
  BCDadder uut (
        .A(A),
        .B(B),
        .Cin(Cin),
        .sM(sM),
        .CoutM(CoutM),
        .CinM(CinM),

        .Couts(Couts)
  );


  //initial
    // begin
  //$monitor($time, " A= %b, B= %b, Cin= %b, --- Couts = %b, SUM = %b\n", A, B,
Cin, Couts, SM);
     //end

  initial begin
        // Initialize Inputs
        A = 0;
        B = 0;
        Cin = 0;

        CinM = 0;


        // Wait 100 ns for global reset to finish
        #100;

        // Add stimulus here
        #50    A = 4'd0;    B = 4'd0;    Cin=1'b0;
        #50    A = 4'd3;    B=    4'd4;
        #50    A = 4'd2;    B = 4'd5;
```

```
        #50    A = 4'd9;    B = 4'd9;
      #50    A = 4'd8;    B = 4'd8;
        #50    A = 4'd5; B = 4'd6;    Cin=1'b1;


        end

endmodule
```