

```

module FullAdder_test;

    // Inputs
    reg a;
    reg b;
    reg cin;

    // Outputs
    wire s;
    wire cout;

    // Instantiate the Unit Under Test (UUT)
    FullAdder uut (
        .a(a),
        .b(b),
        .cin(cin),
        .s(s),
        .cout(cout)
    );

    initial begin
        // Initialize Inputs
        a = 0;
        b = 0;
        cin = 0;

        // Wait 100 ns for global reset to finish
        #100;

        // Add stimulus here
        #100 a=0; b=0; cin=0;
        #100 a=0; b=0; cin=1;
        #100 a=0; b=1; cin=0;
        #100 a=0; b=1; cin=1;
        #100 a=1; b=0; cin=0;
        #100 a=1; b=0; cin=1;
        #100 a=1; b=1; cin=0;
    end

```

```
        #100 a=1; b=1; cin=1;  
    end
```

```
endmodule
```