```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:        00:29:09 09/27/2015
// Design Name:
// Module Name:        FullAdder
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module FullAdder(

        input [2:0] switch,
        output sum,
        output c_out,
        output    reg [1:0] result
        );

      wire s1,c1,c2;
         reg a;
         reg b;
         reg c_in;

  always@(switch)

  begin
```

```
 a=switch[2];
 b=switch[1];
 c_in=switch[0];

      result[1]=c_out;
    result[0]=sum;

 end

    xor E10(s1,    a,      b);
    and A10(c1,    a,      b);
    xor E20(sum, s1, c_in);
    and A20(c2, s1,    c_in);
      or    O10(c_out, c2, c1);




endmodule
```