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High Frequency Satellite Communication Transmitter

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1 Abstract

The aim of this project is to design and demonstrate a prototype of a high frequency transmitter for satellite communication with a wide bandwidth. We designed the system on two separate PCBs using a "LEGO-like" technology that we borrowed from X-microwave. The PCBs contain the PLL and the Upconverter and are interconnected through unique high frequency connectors that were used by X-microwave for similar purposes.

Such transmitters are relatively new in the space industry, and they bring new communications capabilities and very high data rate links for maritime vessels and more applications. The main issue with transmission in high frequencies is that the signal in these frequencies is much more vulnerable to the weather and physical obstacles in the wireless channel. While there are no physical obstacles in space-to-earth communication, the weather is a real issue in this case and the solution is usually a combination of high frequencies and low frequencies capabilities on the same transmitter.

In the scope of our project, we focused only on the high frequency band, known as the Ka-Band, to comply with the demands of the project. Since this band is more sensitive to noise, due to the higher frequency, we designed the transmitter to be as robust as possible, under the limitations of an academic project.

1.1 Main challenges

- System Design – Design of such a highly complex system imposes many tradeoffs between conflicting requirements of the system. The need for a versatile design to support various applications comes at the expense of designing a system that is more suitable to a specific application (in terms of noise, Form Factor, power and cost). Within the scope of our project, such tradeoffs include the need for many filters to mitigate the noise, while limiting the Form Factor (FoM) of the PCBs.

- Integration – The module we aim to build is based on a LEGO-like board design of "X-microwave". This technology is first time used in the Communication Lab. Moreover, the components in high frequencies that we used are rare and there is an extremely limited selection of modules that meet these requirements for the PLL, Upconverter, Power Amplifiers, etc.

- Noise – The high frequency and wide bandwidth induce various noise and distortion artifacts. Among them are phase noise, white noise and intermodulation harmonic distortion. Our goal is to reduce to a minimum these unwanted artifacts and demonstrate transmission with low signal loss.

- Unfamiliar fields of study – RF Systems, Digital Communications for Satellite Systems, System Design, Board Design. All these disciplines are unknown territories for us and require us to study them thoroughly on our own to gain essential expertise to design our desired system.

- Work with new design tools to model the overall system:

  - Block Diagrams – VISIO, Draw.io
  - Schematic Design – OrCAD Capture
  - Layout Design – PCB Editor
  - PLL Analysis – ADIsimPLL Simulator

1.2 Main features

- Frequency range within K-band – 25.5-27 [GHz].
- Carrier frequency at RF output – 26.25 [GHz].
- Analog Devices IQ modulator (upconverter) with integrated x4 (quadruple) of the Local Oscillator.
- Analog Devices PLL frequency synthesizer generates – Local Oscillator output at 6.5625 [GHz].
- Two RF PCBs of a LEGO like X-microwave technology - the IQ Modulator and the PLL modules.
- SPI-Controlled IQ Modulator with variable attenuator.
- SPI-Controlled PLL with variable LO frequency with Fractional-N divider.
- Crystal Oscillator frequency source - 100 [MHz]
- Overall low noise system – with robustness to phase noise and white noise by differential signaling and meticulous filtering design of PCBs.

2 Full System High Level Block Diagram

The high-level block diagram of the full system is depicted in Figure 1 below.

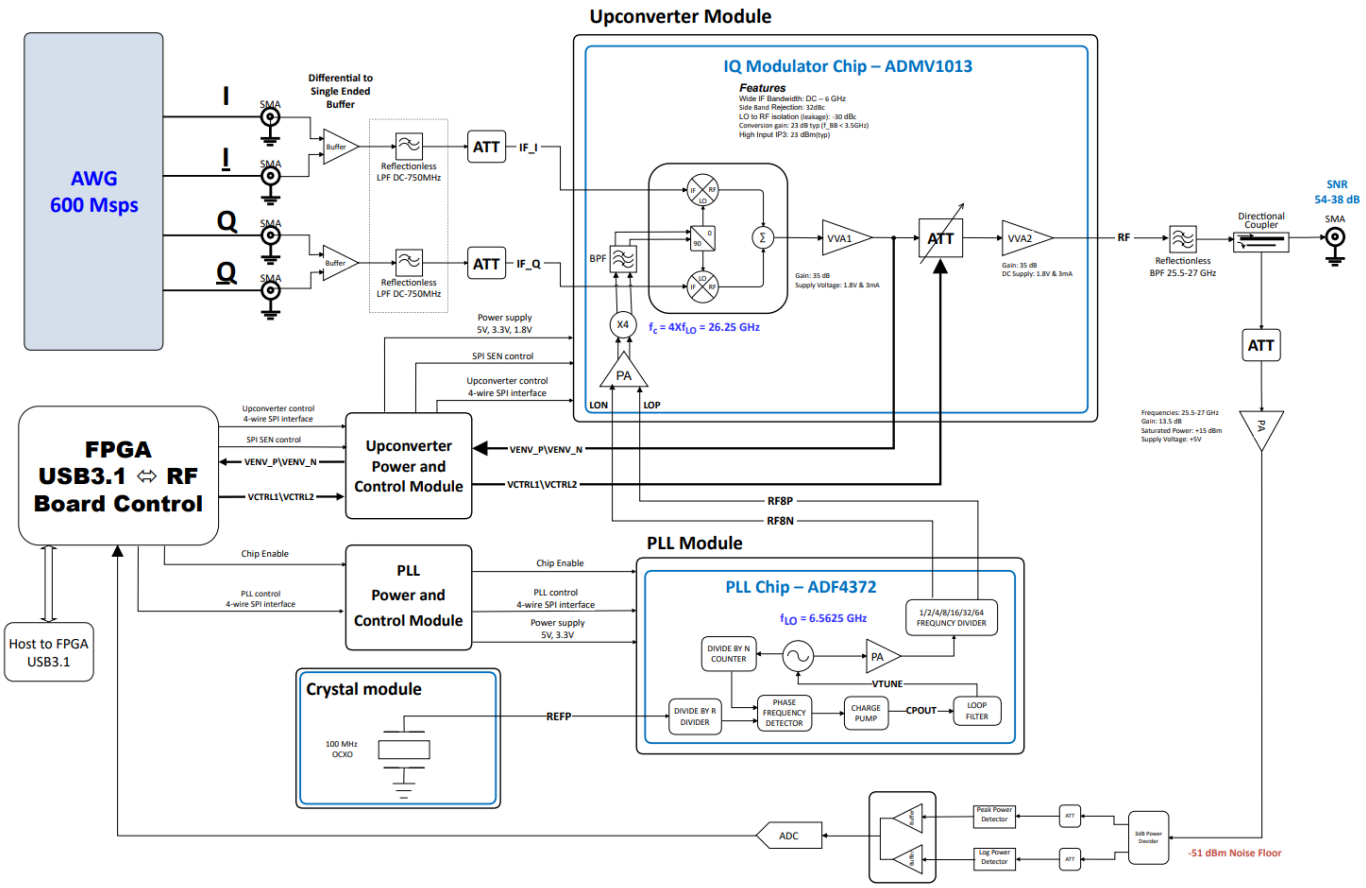


Figure 1 Full system high level block diagram

The core of the system architecture is comprised of the three primary subsystems:

- Upconverter module
- PLL Module
- Crystal Oscillator module

To enable the functionality of the overall system, our implementation includes additional subsystems and interconnections which handle the configuration control and power supply. These subsystems include:

- Upconverter Power and Control module
- PLL Power and Control module
- FPGA-to-RF Board Control
- AWG signal Generator

Within the scope of our project, we focused primarily on the PLL module and the Upconverter module and their meticulous integration. The remaining subsystems in the full system block-diagram are left as reference and presented here for the completeness of the system architecture.

3 Theory

3.1 Frequency synthesizer

Frequency synthesizer is a device that generates an output signal in a desired frequency from a given input frequency source, commonly implemented by a *Crystal Oscillator*.
A variety of methods to synthesize frequency are described in literature and one of the most promising and accurate methods is based on the *Phase-Locked Loop (PLL)*.
This system can create a great variety of high frequency outputs from a single frequency source in a relatively low frequency.
In its most basic form, a PLL is comprised of a *Phase Detector (PD)*, *Voltage Controlled Oscillator (VCO)* and a *Loop Filter (LF)*. The overall constructed system yields a negative feedback control loop that produces a signal at a desired frequency from a given input frequency source.

In the succeeding sections of this chapter, we describe the PLL based frequency synthesis method in great length. We begin from a conceptual model of a PLL and continue to a detailed analysis of its behavior in both *Time Domain (TD)* and *Frequency Domain (FD)*.

3.1.1 Conceptual Model of Phase-Locked Loops

We begin our discussion by providing a conceptual model for the *Phase-Locked Loop (PLL)* and describe its primary attributes.

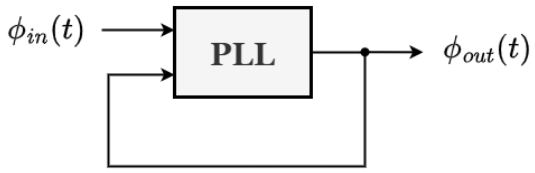


Figure 2 Conceptual model of a PLL with its output tracking its input.

In its most fundamental form, a PLL is a negative feedback control loop which keeps the *phase difference* between its input and output constant over time

$$\phi_{out}(t) - \phi_{in}(t) = const. \tag{1}$$

We say the PLL is in a *locked* state when equation (1) is satisfied. This state ensures that the output phase *tracks* the phase of the PLL input.

A principal and unique consequence of the *phase locking* property is that the frequencies of the input and output of the PLL are **exactly** equal.

This critical attribute of PLLs is derived by the renowned relationship of the *angular frequency* as the time derivative of the *phase*

$$\omega = \frac{d\phi}{dt} \tag{2}$$

By performing time differentiation to equation (1) we arrive at the following relation

$$\frac{d\phi_{out}}{dt} = \frac{d\phi_{in}}{dt} \tag{3}$$

Hence, combining equations (2) and (3) yields the aforementioned key property of a PLL, *i.e.*, when the loop is "locked" the frequencies at the PLL input and output are equal

$$\omega_{out} = \omega_{in} \tag{4}$$

We deduce that if the phases at a PLL output and input differ by a constant for every time instance then their corresponding frequencies are naturally the same.

3.1.2 Basic PLL Model

We move on to a short introduction of the subsystems that construct a basic Phase-Locked Loop (PLL). We shall discuss the properties of each of these subsystems at length further on in this chapter.

The block diagram of a basic PLL is depicted in Figure *3* below.

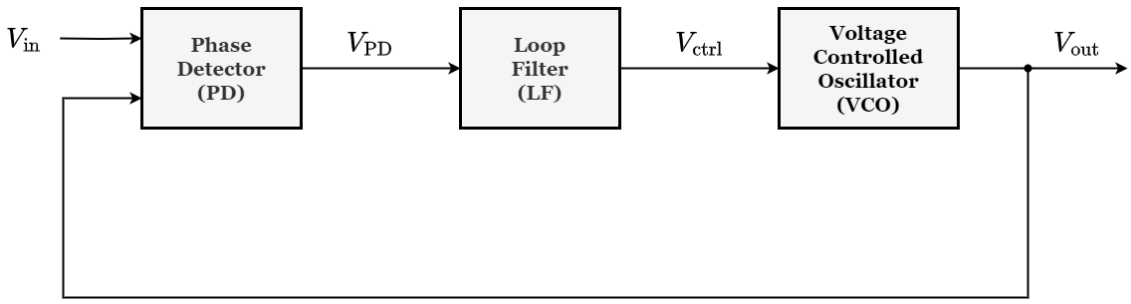


Figure 3 Block diagram of a basic PLL.

The structure of a basic PLL has three subsystems and a unit-gain feedback that, collectively, constitute a closed-loop control system.

The last subsystem in the loop is the *Voltage Controlled Oscillator (VCO)*.
A VCO is a device that *tunes* its output frequency according to the control voltage level at its input. It is common to define the input/output characteristic of a VCO according to following relation

$$\omega_{out} = \omega_0 + K_{\text{VCO}} V_{\text{ctrl}} \tag{5}$$

Where ω_{out} is measured in $[\text{rad/sec}]$ and V_{ctrl} is the control voltage at the VCO input. Hence, we can say that the *frequency deviation*, denoted by $\Delta\omega$, at the VCO output is proportional to the control voltage at its input

$$\Delta\omega = K_{\text{VCO}} V_{\text{ctrl}} \tag{6}$$

Where the proportion factor K_{VCO} is called the *VCO gain* with units of $[\text{rad/sec} \cdot \text{V}]$.

The first subsystem in the loop is the *Phase Detector (PD)*.
A PD is a device that senses two periodic inputs and produces an output whose *average value* is proportional to the phase difference between the two inputs.
A common characterization of the PD input/output relation is given by

$$\overline{V_{\mathrm{PD}}} = K_{\mathrm{PD}}(\phi_{in} - \phi_{out}) \tag{7}$$

Where $\overline{V_{\mathrm{PD}}}$ is the average value at the PD output which is measured in $[\mathrm{Volts}]$ and K_{PD} is called the *phase detector gain*, with units of $[\mathrm{volts/rad}]$. We refer to the phase difference expression $(\phi_{in} - \phi_{out})$ as the *phase error*, denoted by ϕ_{err}.

A naive implementation of a PD may be based on an *exclusive-OR* (*XOR*) gate. In this implementation, the PD generates an output waveform that consists of a periodic series of narrow pulses whose *width* is equal to the phase error ϕ_{err}.

The remaining subsystem is that of the *Loop Filter (LF)*.
A LF is required to close the loop and is introduced between the PD and the VCO, so as to control the overall behavior of the PLL loop.

In its most simplistic version, the LF acts as Lowpass Filter (LPF), thus reducing the high bandwidth that stems from the periodic pulses waveform at the PD output. In this version, the effect of the LF can be regarded as *smoothing* of the transient response of the PD output. This in return, yields a significant relaxation in the fluctuation of the control voltage at the VCO input, which provides more stability to the overall loop.

We shall see further on in this chapter that the LF is commonly designed with added complexity, inspired from control theory *PID controllers*. This results in a device that actively controls the overall performance of the loop, according to the properties of the specific structure of the LF.

We mention in passing that the design of the LF is generally left to be determined by the designer of the PLL (unlike the PD and VCO which are usually quite limited in their variety). This degree of freedom to determine the LF structure is paramount to the overall desired performance of the loop and must be handled very carefully. Since it may prove difficult to derive an optimal structure for the LF of a given PLL, various simulation tools exist to design a LF to comply with the requirements of a specific PLL.

3.1.3 Analysis of a Linear Model for PLLs

PLLs are nonlinear systems by nature. Nevertheless, we may approximate their behavior by "linearizing" the system at a desired operating point. A common approach states that when the phase error is sufficiently small, *i.e.,* $\phi_{err} \approx 0$, the PLL may be approximated as a linear system.

In ordinary electrical devices, the input/output characteristic or the system *Transfer Function (TF),* relates the voltage or current signals at the system's input with those at its output. In PLLs, however, the input/output characteristic of interest is that which relates the phases of the input and output signals, leading to a well-known analysis approach of PLLs in the *phase equivalent representation*.

Consequently, the transfer functions considered herein relate the phase modulation of the PLL input signal with the phase modulation response at its output.

We now consider a general **linear** model of a PLL in its phase equivalent representation and derive the transfer functions of its subsystems in both the *Time Domain (TD)* and the *Frequency Domain (FD)*. We base our analysis on the block diagrams depicted in Figure *4*.

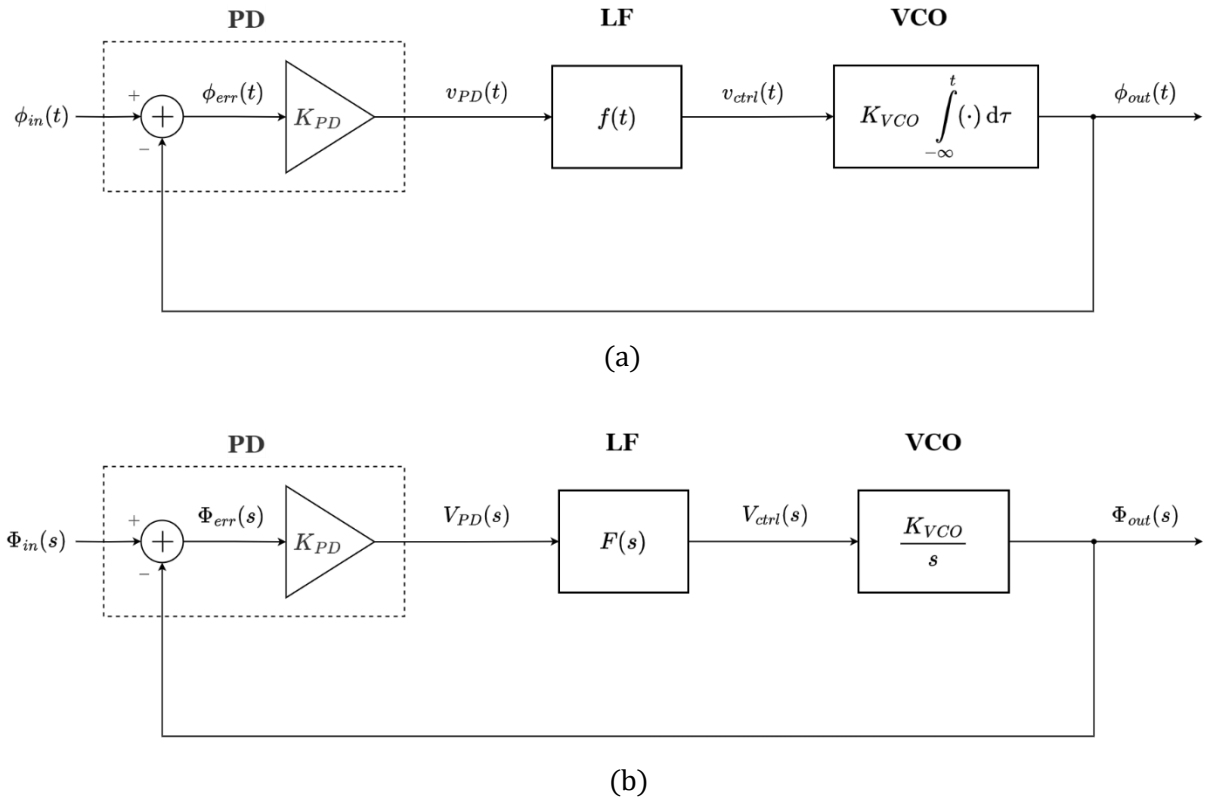


Figure 4 Linear model of a PLL in the equivalent phase representation for (a) Time Domain signals , (b) Frequency Domain signals.

We denote the phase at the PLL input, *i.e.* the reference phase, as $\phi_{in}(t)$ and the phase at the VCO output as $\phi_{out}(t)$, both in [rad].
We assume hereon that the loop is in a *locked* state and that the phase detector is **linear**.

3.1.3.1 Phase Detector (PD)

The phase detector output voltage is given by

$$v_{PD}(t) = K_{PD}\big(\phi_{in}(t) - \phi_{out}(t)\big) \tag{8}$$

Where K_{PD} is called the *phase detector gain*, with units of $[\text{volts/rad}]$.

It may be instructive to define the *phase error* as the difference between the input and output phases as

$$\phi_{err}(t) \triangleq \phi_{in}(t) - \phi_{out}(t) \tag{9}$$

Which leads to rewriting equation (8) as $v_{PD}(t) = K_{PD}\phi_{err}(t)$.

Since here we consider the PD as a **linear** system, we may analyze it in the Frequency Domain by applying the *Laplace Transform (LT)*, denoted by $\mathcal{L}\{\cdot\}$.
Hence, the corresponding output of the PD in Frequency Domain is given by

$$V_{PD}(s) = \mathcal{L}\{v_{PD}(t)\}(s) = K_{PD}\big(\Phi_{in}(s) - \Phi_{out}(s)\big) = K_{PD}\Phi_{err}(s) \tag{10}$$

3.1.3.2 Loop Filter (LF)

In the most general case, the loop filter (LF) may be described as a *Linear Time Invariant (LTI)* system, whose purpose is to **control** the dynamic performance of the overall PLL loop. This subsystem not only filters out high frequency components and noise but rather determines the dynamic behavior of the control voltage at the VCO input, thus **tuning** the output frequency of the VCO.

We mention in passing that the LF functionality is key to the overall loop dynamics. We shall elaborate on this matter later on, while addressing the process of determining the LF structure.

In the most general case, the LF relates its input, denoted by $v_{PD}(t)$, to its output, *i.e.* the VCO control voltage, denoted by $v_{ctrl}(t)$ according to the well-known LTI relation given by

$$v_{ctrl}(t) = v_{PD}(t) * f(t) = \int_{-\infty}^{\infty} v_{PD}(\tau) f(t-\tau)\,\mathrm{d}\tau \tag{11}$$

In the Frequency Domain this corresponds to a simple multiplication

$$V_{ctrl}(s) = V_{PD}(s) \cdot F(s) \tag{12}$$

3.1.3.3 Voltage Controlled Oscillator (VCO)

The deviation in frequency at the VCO output is related to its input control voltage, v_{ctrl}, according to the following relation

$$\Delta\omega = K_{VCO} v_{ctrl} \tag{13}$$

Where $\Delta\omega$ is measured in $[\mathrm{rad/sec}]$ and K_{VCO} is the *VCO gain* factor with units of $[\,\mathrm{rad/sec \cdot V}]$.

To describe the VCO output as a *phase* attribute rather than in terms of the *instantaneous angular frequency*, ω, we exploit the well-known relationship between the two.
We know that the instantaneous angular frequency is nothing but the derivative of the *phase, i.e.* $\omega = d\phi/dt$. Conversely, we may describe the phase as an integral of the instantaneous angular frequency, yielding

$$\phi(t) = \int_{-\infty}^{t} \omega(\tau)\, \mathrm{d}\tau \tag{14}$$

We deduce from equations (13) and (14) that the VCO output phase is given by

$$\phi_{out}(t) = K_{VCO} \int_{-\infty}^{t} v_{ctrl}(\tau)\, \mathrm{d}\tau \tag{15}$$

Hence, the phase of the VCO output is proportional to the integral of the control voltage $v_{ctrl}(t)$. In Frequency Domain this relation corresponds to a factor of $1/s$, *i.e.* an ideal integrator, yielding the following relation

$$\Phi_{out}(s) = V_{ctrl}(s) \cdot \frac{K_{VCO}}{s} \tag{16}$$

3.1.3.4 Overall System Transfer Functions

It can be shown (with some Laplace domain simple algebra) that the following overall loop transfer functions hold:

- Open loop transfer function:

$$G(s) = \frac{\Phi_{out}(s)}{\Phi_{err}(s)} = \frac{K_{PD} K_{VCO} F(s)}{s} \tag{17}$$

- System (closed loop) transfer function:

$$H(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{G(s)}{1 + G(s)} = \frac{K_{PD} K_{VCO} F(s)}{s + K_{PD} K_{VCO} F(s)} \tag{18}$$

- Error transfer function:

$$E(s) = \frac{\Phi_{err}(s)}{\Phi_{in}(s)} = \frac{1}{1 + G(s)} = \frac{s}{s + K_{PD}K_{VCO}F(s)} \tag{19}$$

3.1.3.5 Loop Filter Characteristics for Second-Order PLLs

At this point we need to determine the desirable Loop Filter (LF) characteristic for our overall negative feedback control system which constitutes the PLL.

For simplicity we limit our discussion to the scope of *second-order* PLLs, *i.e.* control loops which contain precisely two poles. The *order* of the PLL stems from the degree of the polynomial in the denominator of the system transfer function $H(s)$.

We mention here that the vast majority of practical PLLs are either second order or are designed by approximating their behavior to a second order loop while neglecting higher order effects. Also, second order control loops have a particularly rich theoretical foundation and are therefore instrumental in describing the main tradeoffs in the design of the control system.

It is instructive to distinguish between the notion of the PLL order and its *type*, where the latter refers to the number of *integrators* which are incorporated in the loop.

A very common choice for second-order PLLs is that of the *proportional-plus-integrator (P+I)* loop filter, which is given by

$$F_{PI}(s) = K_1 + \frac{K_2}{s} \tag{20}$$

We mention that the P+I loop filter contains a single integrator with a gain of K_2. Because of the inherent integration in the VCO, this specific configuration has a total of two integrators, thus producing a *type 2* (commonly referred to as type-II) PLL.

By inserting equation (20) into the general system transfer function given by equation (18) we obtain the system transfer function for the P+I loop filter configuration

$$H_{PI}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{K_{PD}K_{VCO}K_1 s + K_{PD}K_{VCO}K_2}{s^2 + K_{PD}K_{VCO}K_1 s + K_{PD}K_{VCO}K_2} \tag{21}$$

Which may be expressed in the familiar control theory form

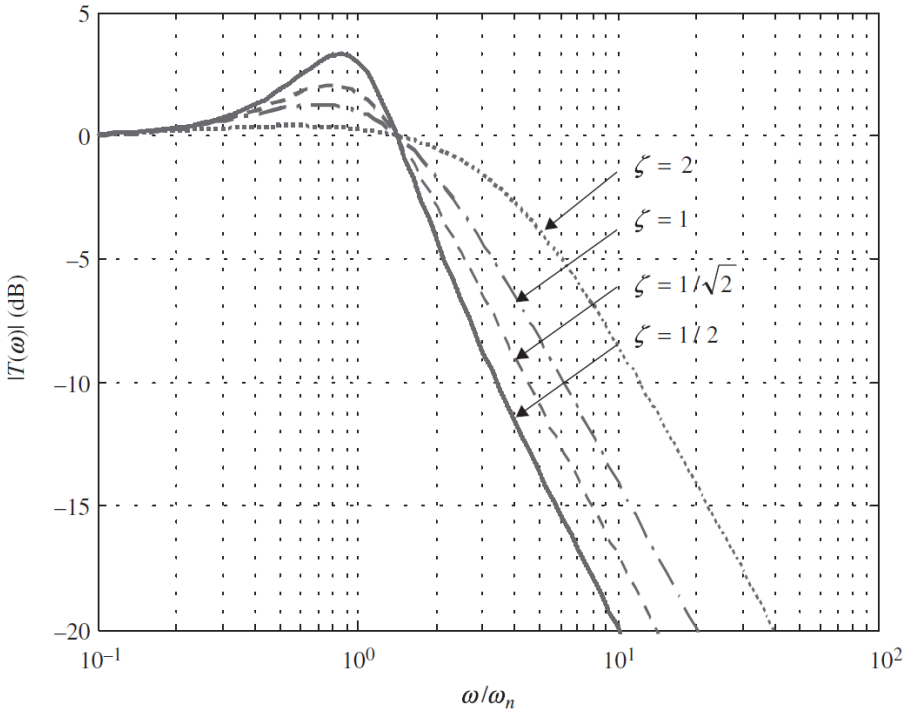
$$H_{PI}(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{22}$$

Where in this case, the *natural frequency* ω_n and the *damping factor* ξ are given by the following

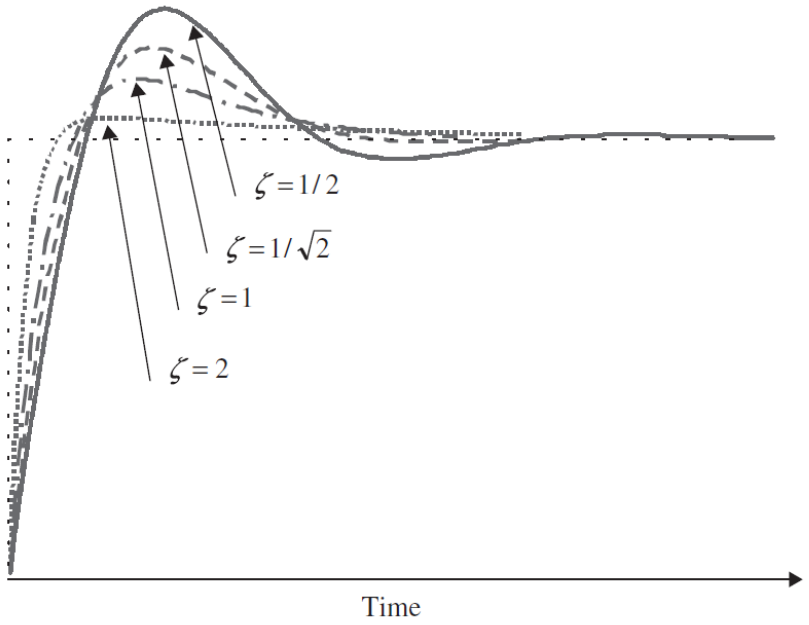
$$\xi = \frac{K_1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{K_2}} \tag{23}$$

$$\omega_n = \sqrt{K_{PD}K_{VCO}K_2} \tag{24}$$

Depicted in Figure *5* below are examples of the effect of different values of ξ and ω_n on second-order PLLs in both the system frequency response and its step response (figures are taken from [2]).



(a)



(b)

Figure 5 Effect of the damping factor ξ and the natural frequency ω_n on (a) the frequency response of a second-order PLL , (b) the step response of a second-order PLL.

3.1.4 PLL Based Frequency Synthesizers

As a final step of our discussion, we move on to discuss an extremely useful property of PLLs which deals with *frequency multiplication*. By a small modification to the PLL scheme that was discussed extensively before, we can generate an output frequency ω_{out} that is a multiple of the input (reference) frequency ω_{in}.

As depicted in Figure 6, the output frequency of a PLL can be divided before being fed back to the phase detector. The $\div N$ device is nothing but a counter that generates one output pulse for every N pulses at its input. When the loop is in the locked state, $\omega_{\text{div}} = \omega_{\text{in}}$, thus yielding a frequency at the overall system output of

$$\omega_{\text{out}} = N\omega_{\text{in}} \tag{25}$$

We call the divide ratio, N, the modulus.

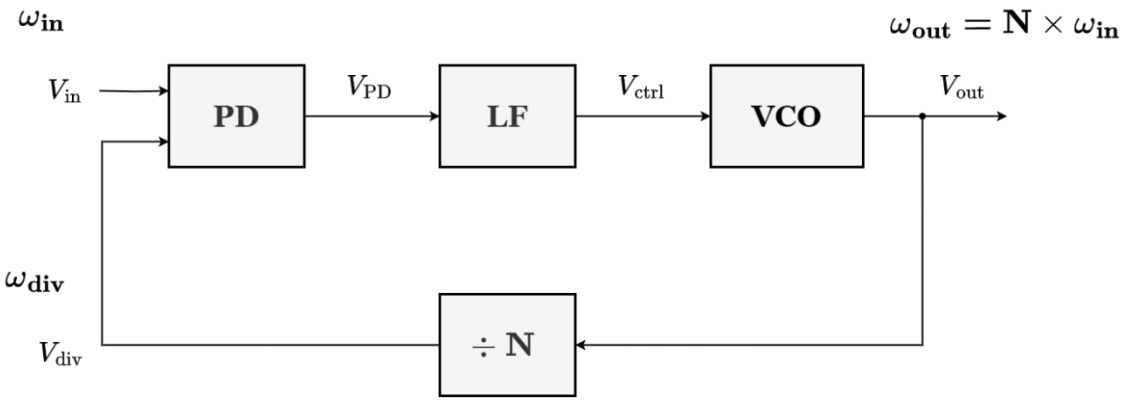


Figure 6 PLL based frequency synthesizer utilizing frequency multiplication.

The configuration depicted in Figure 6, can essentially *synthesize* any desired output frequency, by setting the proper value for N, which may be an integer or a fraction. We mention in passing that there are two major classes of *frequency synthesizers*, both stem from the frequency multiplication property described above.

The first class are the *Integer-N frequency synthesizers*, where N is an integer value, yielding an output frequency which is an integer multiple of the input.

The second class are the *Fractional-N frequency synthesizers*, in which N has both an integer and a fractional part, often denoted as $N.F$. In this case the output frequency may take *any* non-integer multiple of the input, yielding an output frequency which is exclusively controlled by the value of the divide ratio $N.F$, regardless of the input frequency value.

The two classes of frequency synthesizers are described extensively in literature and emerge in countless applications. In the scope of our discussion, they are of interest for the role they play as the frequency source that feeds the *IQ Modulator* for the purpose of *upconversion* to passband (RF). This is done by frequency multiplication of a *frequency source* (crystal oscillator) in a considerably low frequency in MHz which is then converted to a few GHz.

3.2 IQ Modulator

An *IQ Modulator* is a system that takes two real signals (data streams) which are completely independent and performs *upconversion* to a single *passband* signal in RF frequency, which represents a combination of the two original real signals.
This combination is uniquely defined, such that the two original real signals will not interfere with one another once upconverted to passband (RF). This pivotal property of IQ Modulators enables high *Spectral Efficiency* in comparison with other upconversion methods, which is highly desired since the *available spectrum* is a limited resource.

A discussion regarding the IQ modulator functionality and its major advantages usually begins with the introduction of a few key concepts concerning passband (RF) signals and their corresponding *baseband* representations.

We define a *band-limited* (*narrowband*) signal in passband $x(t)$, as a signal whose double-sided bandwidth W is much smaller than the *carrier frequency* f_c of the upconverter, *i.e.*, a passband signal for which the following relation holds: $f_c \gg W$.

Any passband signal $x(t)$ which is both real and band-limited (narrowband) may be represented in terms of its corresponding baseband signal $x_{BB}(t)$. Another common terminology for $x_{BB}(t)$ is the *Complex Envelope* (*CE*) of $x(t)$.
The representation of $x(t)$ in terms of its corresponding baseband signal x_{BB}(t) is given by

$$x(t) = \sqrt{2}\,\Re\mathrm{e}\{x_{BB}(t)e^{j2\pi f_c t}\} \tag{26}$$

Where $x(t) \in \mathbb{R}$ is a band-limited passband signal but the baseband signal $x_{BB}(t) \in \mathbb{C}$.

Since the baseband signal is complex it may be written in the following form

$$x_{BB}(t) = x_I(t) + jx_Q(t) \tag{27}$$

Where here both $x_I(t) \in \mathbb{R}$ and $x_Q(t) \in \mathbb{R}$.

Substituting equation (27) for $x_{BB}(t)$ in equation (26) and utilizing *Euler's formula* yields the well-known representation for the passband signal in terms of its *In-phase* and *Quadrature* components:

$$\begin{aligned} x(t) &= \sqrt{2}\,\Re\mathrm{e}\left\{\left(x_I(t) + jx_Q(t)\right)e^{j2\pi f_c t}\right\} \\ &= \sqrt{2}\,\Re\mathrm{e}\left\{\left(x_I(t) + jx_Q(t)\right)\cdot\left(\cos(2\pi f_c t) + j\sin(2\pi f_c t)\right)\right\} \\ &= x_I(t)\sqrt{2}\cos(2\pi f_c t) - x_Q(t)\sqrt{2}\sin(2\pi f_c t) \end{aligned} \tag{28}$$

Where we define $x_I(t)$ as the In-phase component of the passband signal $x(t)$ and $x_Q(t)$ as its Quadrature component.

A schematic block diagram of the IQ Modulator is depicted in Figure 7.

An important aspect of IQ modulation is that the $\cos(\cdot)$ and $\sin(\cdot)$ functions are *orthogonal* to one another. This is made evident by their inner product over a single period $T = \frac{1}{f_c}$ which amounts to zero

$$\langle \cos(2\pi f_c t)\,, \sin(2\pi f_c t)\rangle = \int_0^T \cos(2\pi f_c t)\sin(2\pi f_c t)\,\mathrm{d}t = 0 \tag{29}$$

The orthogonality of the trigonometric functions leads to a valuable property of IQ Modulators; the In-phase and Quadrature components of the passband signal $x(t)$ are orthogonal and lead to two independent channels in passband (RF) that do not interfere one another.

The In-phase and Quadrature components form two independent channels, while sharing the same bandwidth in passband within the available spectrum.
From a different perspective, we say that the IQ Modulator takes advantage of the redundancy that stems from the fact that the passband signal $x(t)$ is real and therefore has a *Fourier Transform* that is symmetric w.r.t. DC.

For comparison, the *Double-Sideband* (*DSB*) *Modulator* occupies a bandwidth that is **double** the bandwidth occupied by an IQ Modulator conveying the same *data rate*.
Conversely, we deduce that the Spectral Efficiency of the IQ Modulator is **twice** the Spectral Efficiency of the DSB Modulator.

This property is highly desirable as it leads to better utilization of the available spectrum, which is an extremely limited resource. In other words, higher Spectral Efficiency means we achieve higher data rates for a given bandwidth or pack more bits per second in a bandwidth of 1 $[Hz]$.

We mention in passing that modern Digital Communication systems often employ *Quadrature Amplitude Modulation (QAM)* to achieve high data rates.
QAM is well-suited for implementation using the IQ Modulator and therefore this modulation method is very common and may be found in most practical applications for modern communication links.

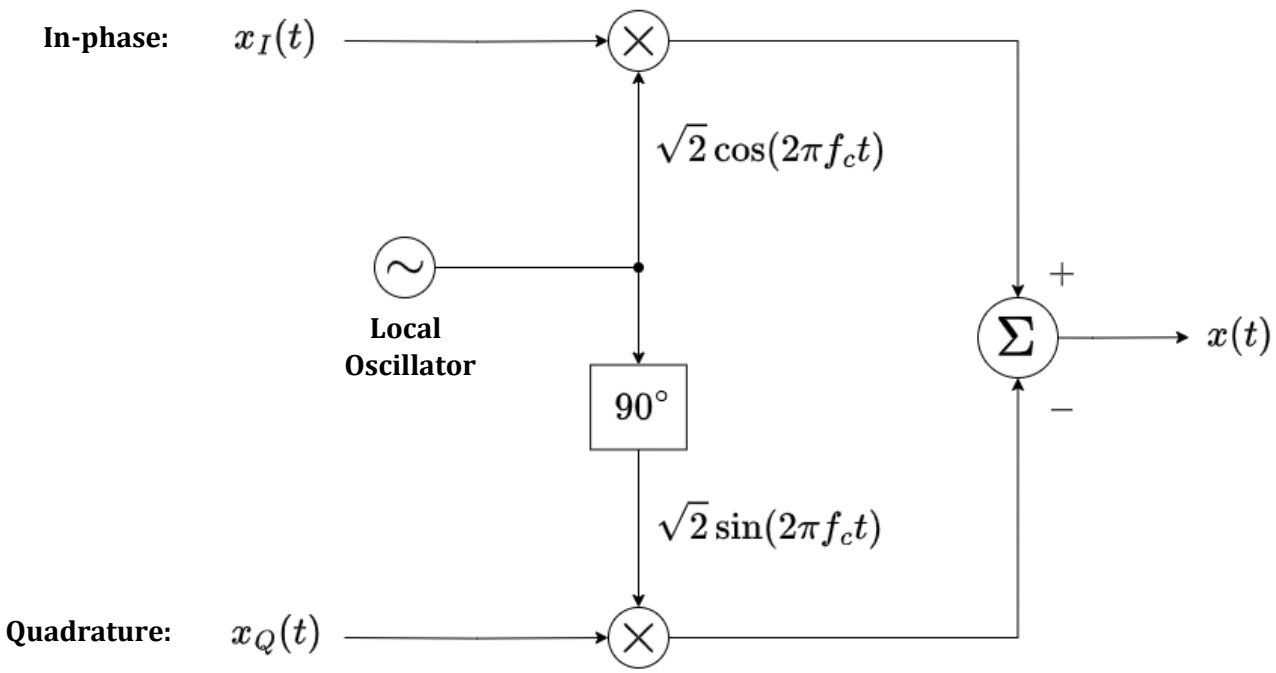


Figure 7 Block diagram of an IQ Modulator.

3.3 Frequency Source

For any communication system there is a need for a frequency source, usually in communication systems and clocks a Crystal oscillator is used, in Crystal oscillator there is a piezoelectric resonator that determine the frequency by its parameters and as a result of a voltage applied to its electrodes, this is very common frequency source in applications with demand for high accuracy frequency, the piezoelectric resonator have much better Q factor than other frequency sources such as RLC circuits, and it is more durable.

4 Components selection

4.1 Upconverter

We chose the ADMV1013 Upconverter with IQ-modulator of Analog Devices, with a range between 24GHz to 44GHz.
During the search and choice of the modulator we took into account a few considerations:

- Low value noise figure – [15db, 20db] in our desired frequency range 25.5-27 [GHz]
- The reliability and life expectancy of the product
- The temperature range that fits the space temperature [-40C, 85C]
- The programing capabilities and flexibility of the modulator for tests and adjust after production.

We looked for an upconverter that our carrier frequency lay in the middle of its RF frequency range.

Out of the products available in the market we found only the ADMV1013 upconverter that meets this requirement – RF frequency range [24GHz, 44GHz].

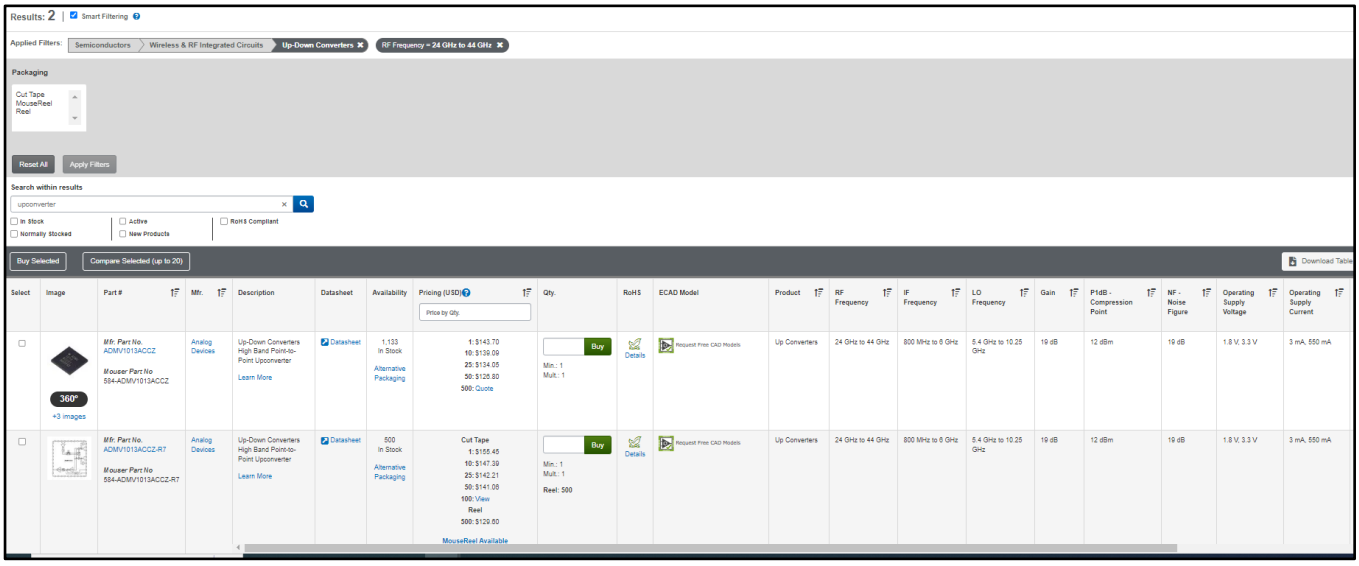
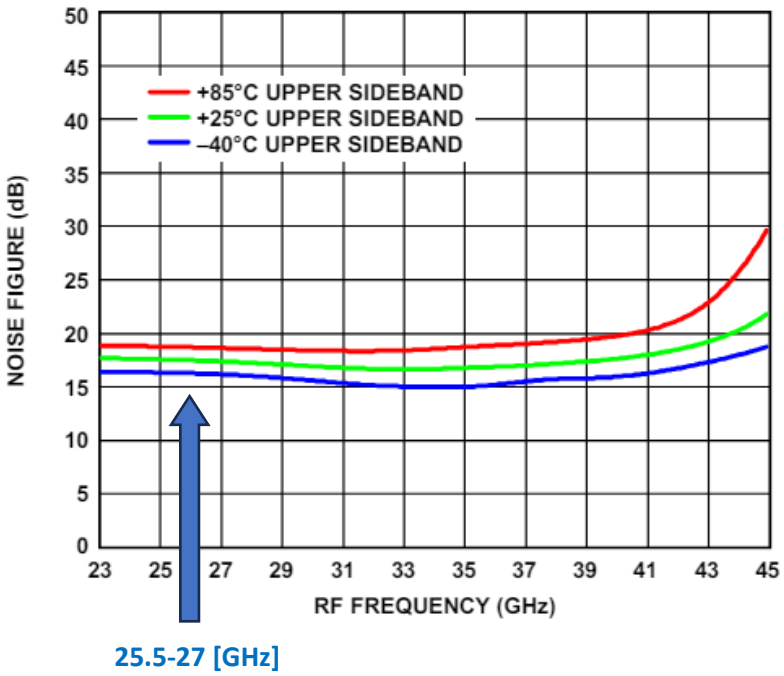


Figure 8 List of suitable upconverters from Mauser search engine.



25.5-27 [GHz]

Figure 9 ADMV1013 Noise Figure characteristic in the frequency range of 25.5-27 GHz.

4.2 PLL

We chose the ADF4372 PLL of Analog Devices, with an internal VCO and tuning range between 62.5MHz to 16GHz and high resolution 39bit.
Our main consideration for choosing this PLL was that it was recommended by Analog Devices to be paired with the ADMV1013 upconverter.

This PLL has one of the highest RF frequency range, which can enable further experiments at higher frequency with our upconverter, this was a side consideration for this PLL as well.

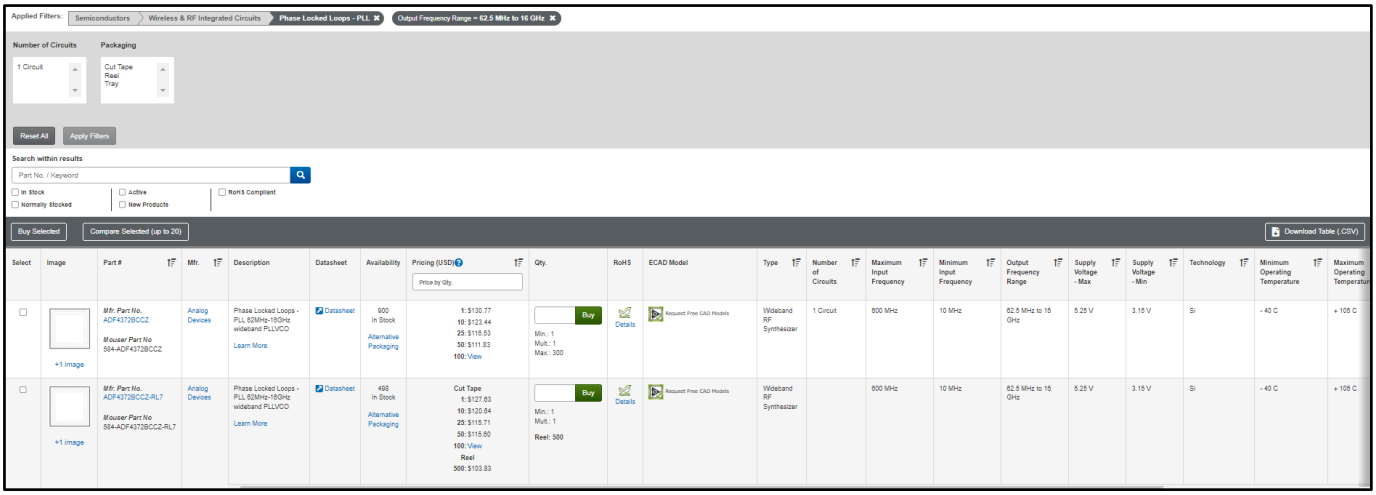


Figure 10 List of suitable PLLs from Mauser search engine.

4.3 Crystal Oscillator

We are going to use a 100 MHz crystal oscillator that is widely used in the communication lab, and we already have it in store, the 100 MHz Crystal is standard in a lot of applications, and it will be easier and chipper to use it and replace it.

5 Design

5.1 System-Level Block Diagram Design

The diagram design is the fundamental of any HW and SW system design. This diagram is the first step and the highest level of design of a system and therefore one of the most important parts of the project.
Depicted in Figure *11* is our system level block diagram. In the diagram we decided the basic method that the system will work and we had to consider the variables challenges and goals for our system in every decision and method we use, and we had to consider also the impact of one part of the system on another and to compromise between our system goals.
We met with Denis, our project supervisor, and understood with him what the main components are, and how we approach a high frequency transmitter design.
We started diagram build, using the Visio and Draw.IO tools, and after some "ping pong" process with Denis and a lot of materials reading we had our basic project Diagram. During the design phase we updated this diagram with the new components and distinctive designs and methods.

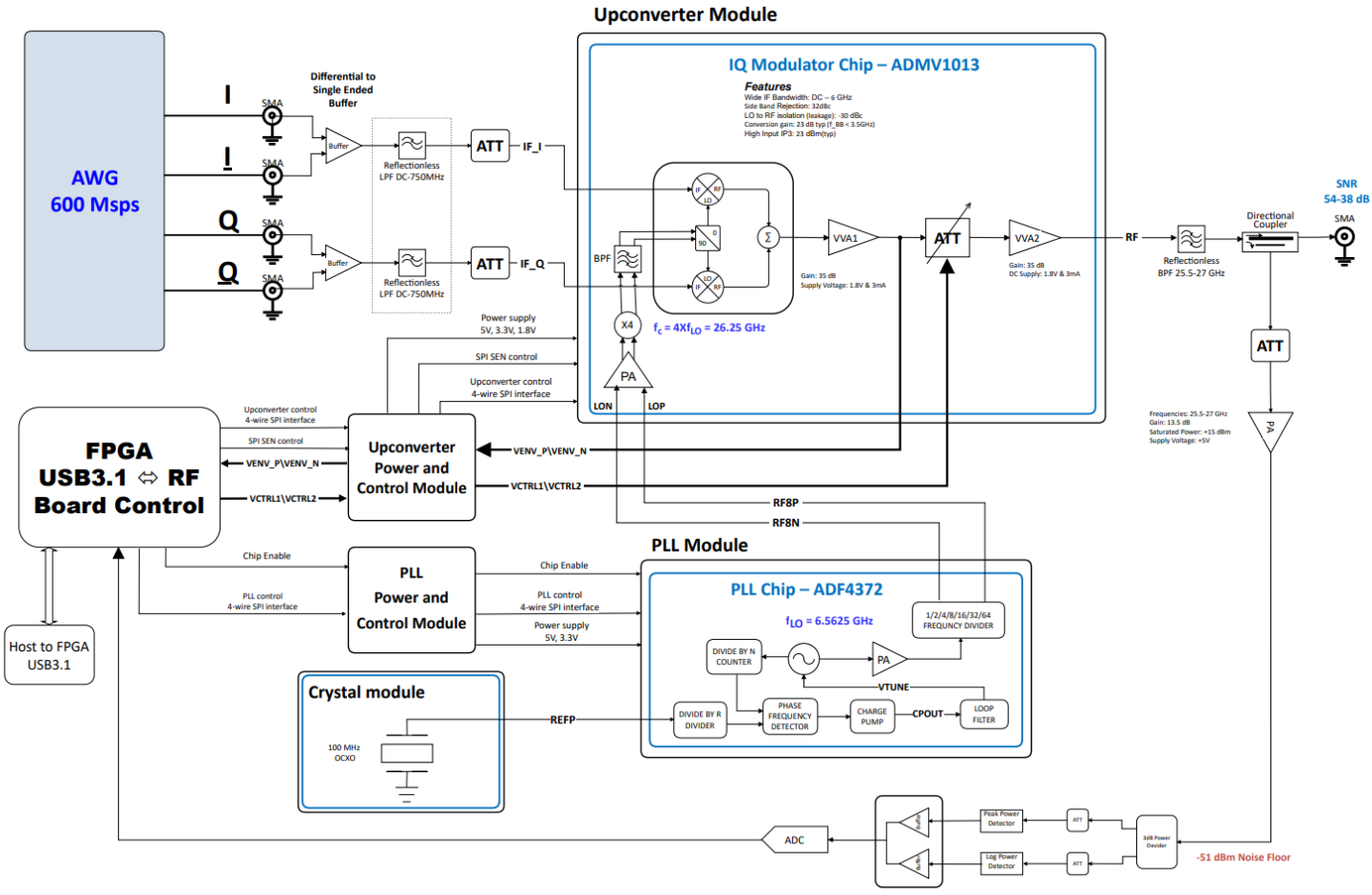


Figure 11 Full system high level block diagram

5.2 PCB Design Study

5.2.1 Schematic Design

We learned how to design an electrical schematic on the OrCAD Capture Cis tool on the lab computers, we got help from Denis, Ela and Menashe, some Capture guide docs, and a lot of learning materials on websites and on YouTube.

5.2.2 Board Design

We sat to learn how layout design is made in OrCAD PCB Designer, we learned from Denis Ela and from the internet.
The idea of learning layout design was to understand the layout designer work – Ela and then Menashe, and to be able to affect the important design feature and fix the layout design during the designer work.
Ela did the two Bords pretty quick and after three and a half versions we finished the rejects and closed the layout design.
Later when the PLL chip was obsolete, and we had to choose another PLL chip we worked with Menashe and redesign the PLL layout.

5.3 PLL Design

5.3.1 PLL Analysis Using ADIsimPLL Simulator

We used Analog Devices' recommended simulation tool for PLL Analysis, called **ADIsimPLL™**, to get a better understanding of the overall performance of our selected PLL.
We used the simulation to determine the topology of the Loop Filter and for setting the values of its resistors and capacitors.

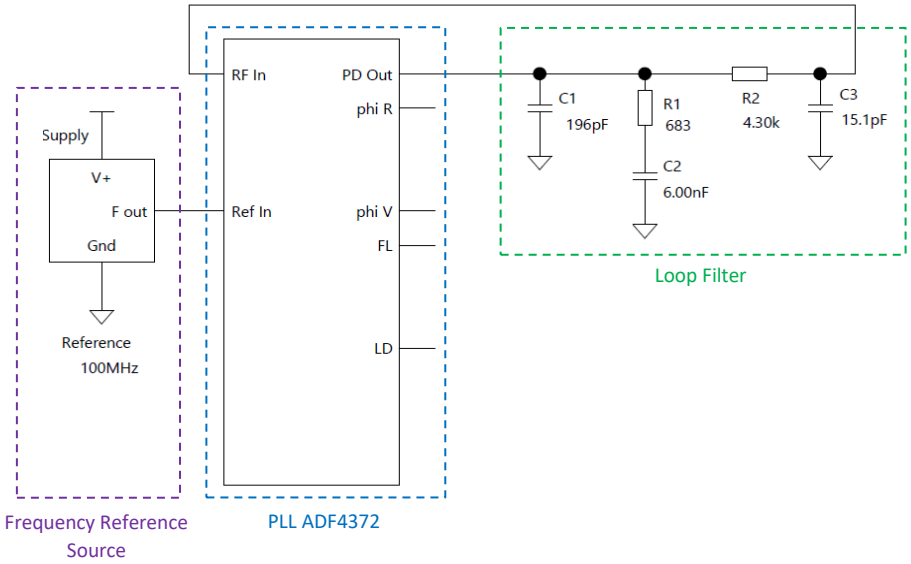
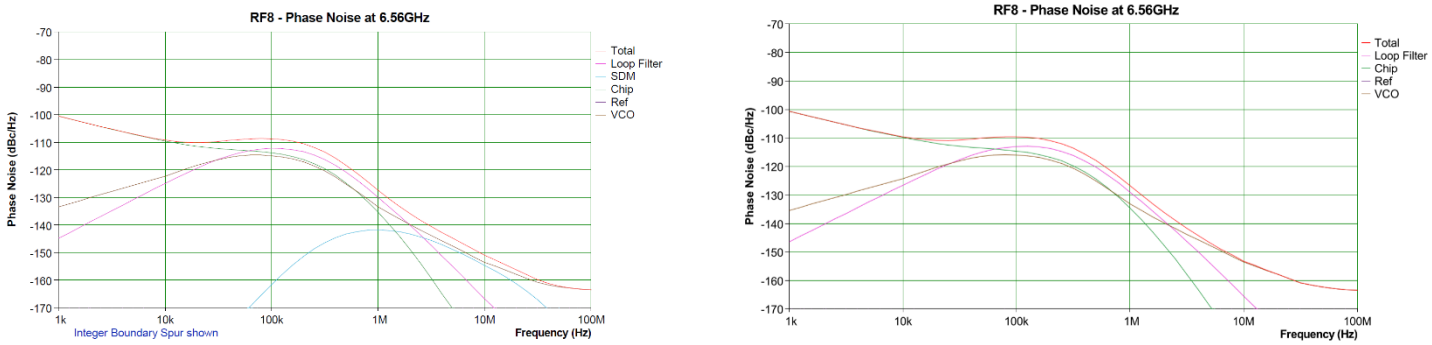


Figure 12 ADIsimPLL simulation model

Our simulation model, depicted in Figure *12*, holds the following properties:

- **Frequency Reference Source** – the ADIsimPLL tool determines the simulation structure by a few parameters, one of the most important is the frequency reference, at the beginning we determined the frequency reference to be such that, by multiplying it by some integer, we would get the desired output frequency at $f_{LO} = 6.56125\ [GHz\ ]$.
  This design decision would have generated the desired output frequency while bypassing the "fractional-N" frequency divider sub-system within the ADF4372 PLL, thus reducing the overall phase noise.
  The frequency reference that met this requirement was $f_{REF}^{(1)} = 104.66\ [MHz]$.
  After showing the results to Denis and consulting with him we decided to choose a frequency reference that would be compatible to an existing off-the-shelf Crystal Oscillator that exists in the lab. This design decision was justified by the fact that the phase noise induced due to the fractional-N divider was relatively minor.
  Therefore, we made another simulation in ADIsimPLL with the new frequency reference at $f_{REF}^{(2)} = 100\ [MHz]$, with the use of the fractional-N divider this time.
  See also Figure *13*, for a comparison of the overall phase noise, with and without the use of the fractional-N divider.

- **Signals:**
  - **"Ref in"** – signal is the Frequency Reference source input, which provides the PLL with its reference input to create the desired frequency output which is higher.
  - **"RF in"** – the output of the loop filter, which is used as a DC voltage input to determine the VCO (voltage-controlled oscillator) output frequency.
  - **"PD Out"** – Phase Detector output is the error signal that is derived from the phase difference between the VCO output and the frequency reference input. This error signal feeds the loop filter and tunes the voltage of the input to the VCO.
- **Loop Filter Topology:** The ADIsimPLL tool provides several possibilities for design of a loop filter topology. These topologies span from a very simple filter structure which results in significant phase noise, to highly complex loop filters which have a substantial form factor and would be much more expensive.
  We considered these two trade-offs and consulted with Denis and ultimately chose a relatively simple loop filter topology. As can be seen in the rightmost block of Figure 12, *i.e.* the Loop Filter, there are not many components in the Loop Filter and no amplifiers in it. This choice proved sufficient for our needs.
- **Loop Filter Component Values:** After we chose the loop filter structure, we selected the desired local oscillator output frequency to be $f_{LO} = 6.56125\ [GHz\ ]$ and then ran the simulation.
  The simulator automatically determined the resistance and capacitance of all of the loop filter components, to achieve the best overall phase noise behavior of our PLL.



(a) (b)

Figure 13 PLL Phase Noise (a) with fractional-N subsystem, (b) without Fractional-N subsystem.

5.3.2 PLL Schematic Design

We learned about PLL and read the datasheet of our component, then we looked at some references from various sources, including – evaluation board from Analog Devices, X-microwave board design and the Datasheet of course.
And then we consulted with Denis and used a simulation tool of Analog Devices (ADIsimPLL – as described in the chapter above) to determine the components and values we need to combine on the schematic for the best performance and lowest noises.

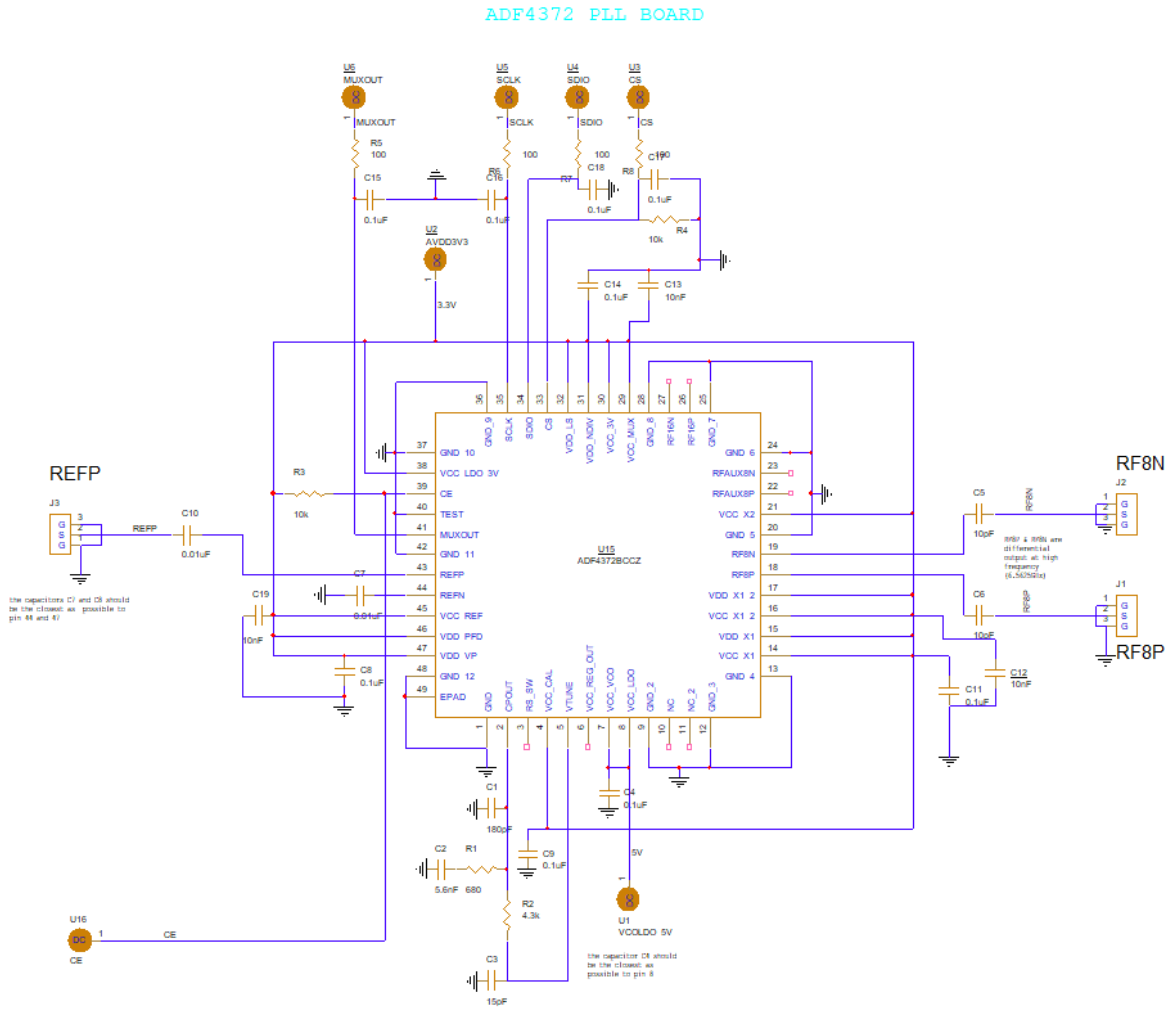


Figure 14 PLL schematic.

- **PLL RF Output, Versatility VS Performance** - we considered to design the PLL module with 16 [GHz] RF output for greater output frequency range, that could help in further test and experiments of the prototype in the Communication Lab, however that would degrade the performance of the system in the desired frequency [6.5625 [GHz].
  on the other hand designing the PLL Module with 8 [GHz] RF output will result in the best performance for our desired system frequency but without the versatility for higher frequency. Finally, we chose the 8 [GHz] design, with an option to produce the 16 [GHz] version board in the future, based on the same schematic design with a minor change.

- **Loop Filter Components Value** – the Loop Filter is the most affective component design in the PLL to control the performance of the output RF signal. To understand how we design this Loop Filter look at the PLL Analysis ADIsimPLL chapter above.

- **Differential Signaling output** – differential signaling is the best method for overcoming a white noise (thermal noise, crosstalk, external electromagnetic field etc.). In our case the RF signals are in high frequency, what make them vulnerable to any noise, mainly for crosstalk and thermal noise, the decision to design the RF signals as differential signals was in the core of our initial design.

- **DC filtering on the RF wires** – in the PLL we blocked any DC input and output on the RF signals, by implementing small capacitors on the relevant wires. This will pass only the high frequency signal as for the DC signal is a short. It is important to block the DC additive of the signal to not harm the processing inside the chip.

- **Power pins AC decoupling** – we put two capacitors of 0.1 [uF] on the power wires coupling to the ground, on each side of chip, as close as possible to the power input pins. That will prevent high frequency signals from entering the chip on the DC power signals. As described in electronic circuits theory the Capacitive Reactance of the capacitor to a given frequency signal is given by the equation:

$$X_c = \frac{1}{2\pi f_C C} \ [\Omega] \tag{30}$$

where X_c is the Capacitive Reactance, f_c is the frequency of the signal and C is the Capacity of the Capacitor. The Capacitive Reactance of the capacitor is like the resistance of it to AC signals. In our case $X_c = \frac{1}{2\pi f_C 10^{-7}} = 16 \cdot \frac{10^9}{f_c}[\Omega]$ that means it pass only the high frequency signals to the ground [MHz] and above.

- **SPI RC (LPF) filtering** – the same goes here only that with the RC filter we can determine the frequency that filtered to the ground more precisely.
the RC filter equation is:

$$V_C = \frac{1}{1 + RC_S} V_{in} \tag{31}$$

The $RC_s = \tau$ parameter depends on the signal frequency and determines the cutoff frequency for the Low Pass Filter and below this frequency all the signals will be blocked. In our case we determined the parameter to be - $\tau = RC_s = 100[\Omega] \cdot 10^{-7}[F] = 10^{-5}[sec]$ which is a typical value for SPI signals filtering that runs in [MHz].

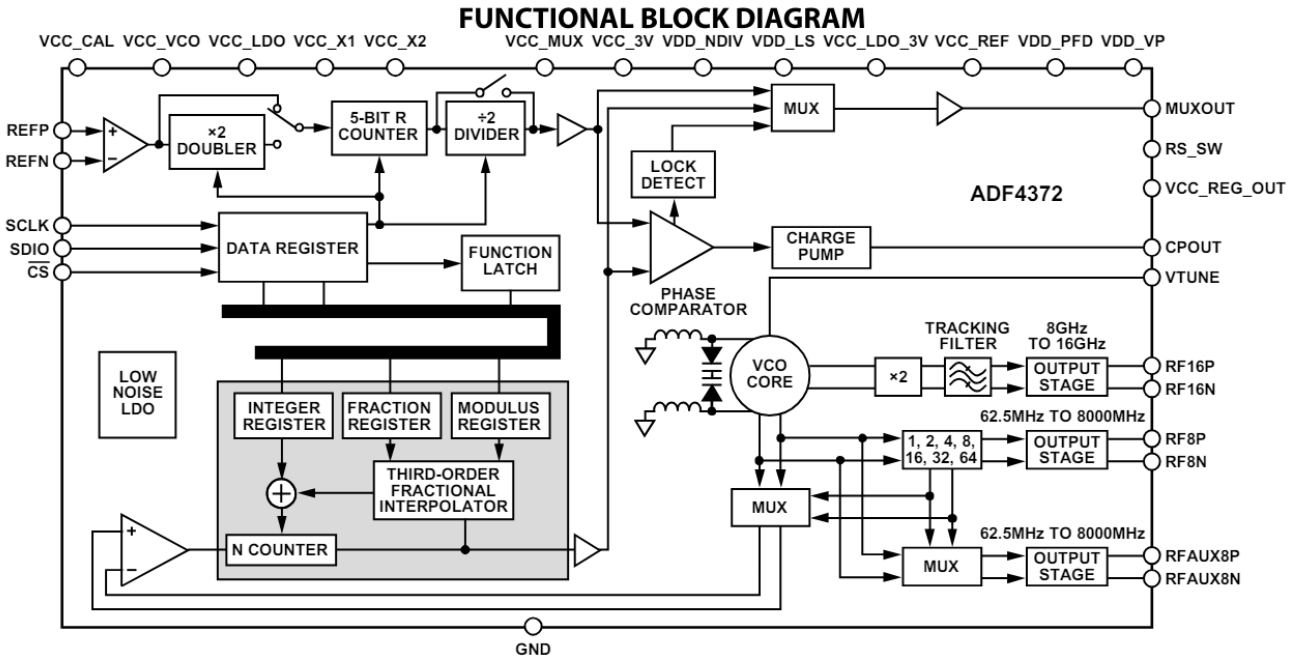


Figure 15 The ADF4372 Internal Architecture.

5.3.2 PLL Layout Design

- **4 layers Board – Top, Ground, Power, Bottom** – the PLL board is an RF board that usually made with few layers, this board is only 4-layers board, almost all the wiring is happening in the top layer and the power layer contains only the power plain and one wiring. The other two layers are the ground layer which separates the top layer from the power layer and the bottom layer which connects the control and power Vias to the power and control board (that is yet to be designed).
- **Resources –** Menashe and Denis ☺, a lot of ping pong with Denis which taught us a lot from his experience and knowledge in RF board design.
- **Design stages by priority –** RF first! We learned that the smartest thing to do is to prioritize our system goals through design stages, that means to design the most important part on the board (RF) first, which more vulnerable to noise and more delicate, and then design the less important and delicate parts of the system – SPI wires, power wires etc.
- **Differential Signaling –** the length of a differential signaling must be the same and it is much better that the shape of the wires will be the same too. It because of the effect of the noise we want to cancel on both wire (N/P) must be the same.
- **RF wiring and Connectors build with Ground "fence" –** the ground fence is to create the same effect as a Farraday Cage, only from three sides (under the wire and from both sides). This design blocks most of the noise coming from the chip and the other wires.
- **Curved RF wires for better transition –** that curved wire design is much less noisy in RF signals, because the signal has less return from the wire angular shape. That can be seen in electronic fields domain, when analyzing the return wave of a wire shape and there are also simulators that analyze this phenomenon.

- **Loop Filter –** we tried to put the Loop Filter components as close as possible to each other to create a Lumped Circuit. That is important because the bigger the distance between two components, the bigger the effect they have on each other, that effect also have second and third order effects and thus the overall behavior of the circuit is less predictable and will be less accurate.
- **Power pins AC filtering –** we tried to put the filtering capacitors as close as possible to the chip entrance pins. Because the board is small and there is a limited space, it was not easy.
this is important because the closer the filter to the pin, the more effective the filter because it filter more of the wire and less wire is enter the chip unfiltered.
- **Constraint to X-microwave Form Factor and Grid –** the board is small! 3x2 [cm] and the all the vias should be on a grid crosses specified by X-microwave, that caused us a lot of headache and design limits.
- **Vias on the Grid for the Power and Control Board –** we tried to put all the vias on the grid crosses unsuccessfully. We left with two vias that are not on the grid crosses – the 3.3V and the CE wires that connected to pins number 38 and 39, for those vias we will need to do (hand) Back Drilling, to disconnect them from the power and control board ground bottom layer, that will be attached to this board.

5.3.2.1 Top Plan

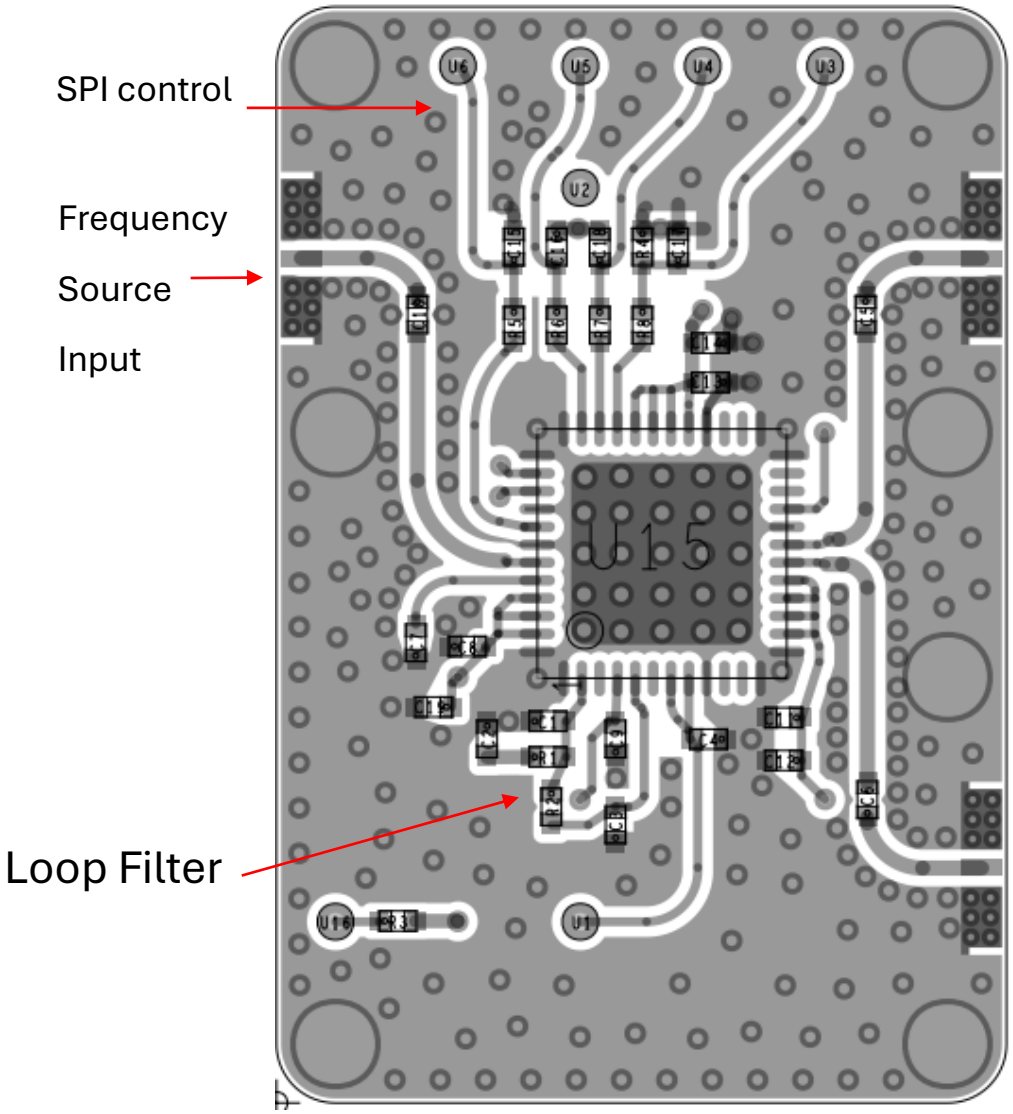


Figure 16 PLL layout top layer.

5.3.2.2 Ground Plan

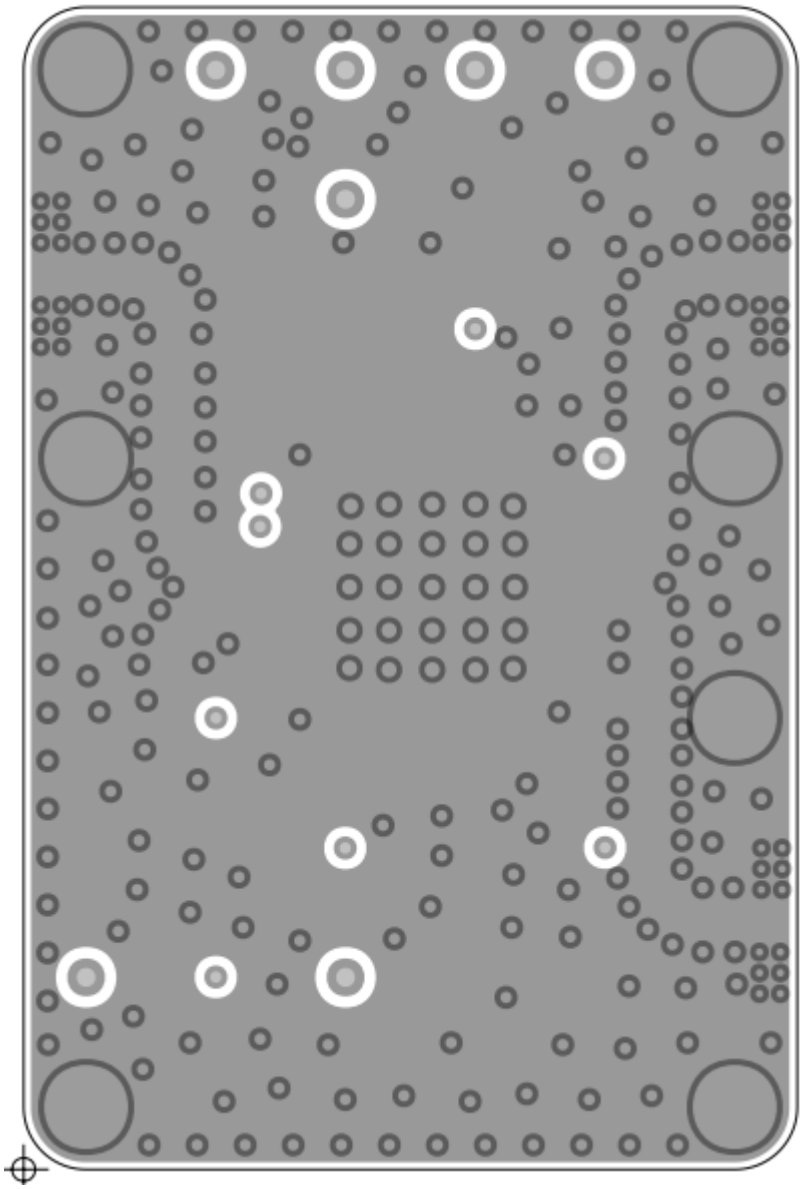


Figure 17 PLL layout ground layer.

5.3.2.3 Power Plan

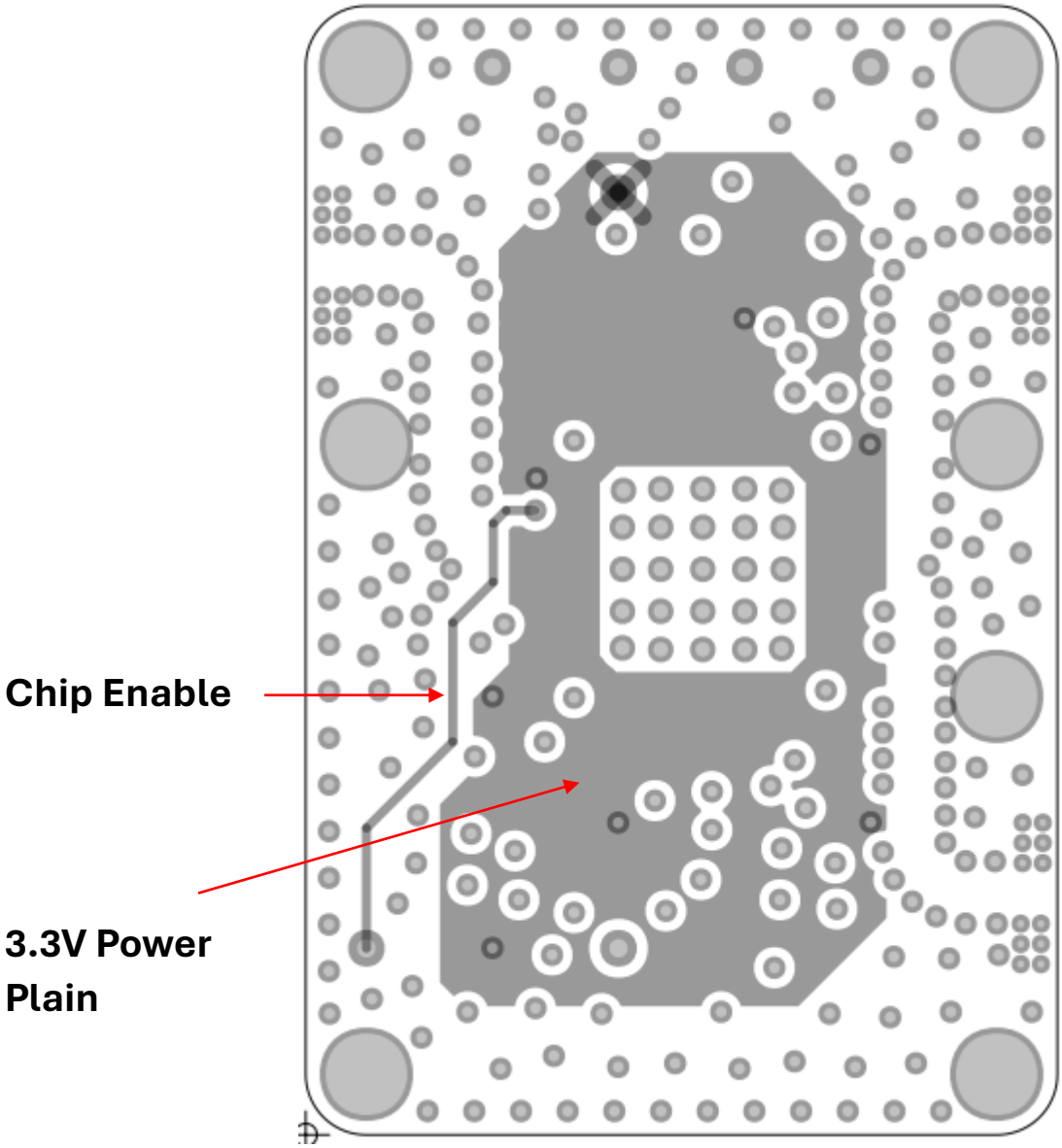


Figure 18 PLL power layer.

5.3.2.4 Bottom Plan

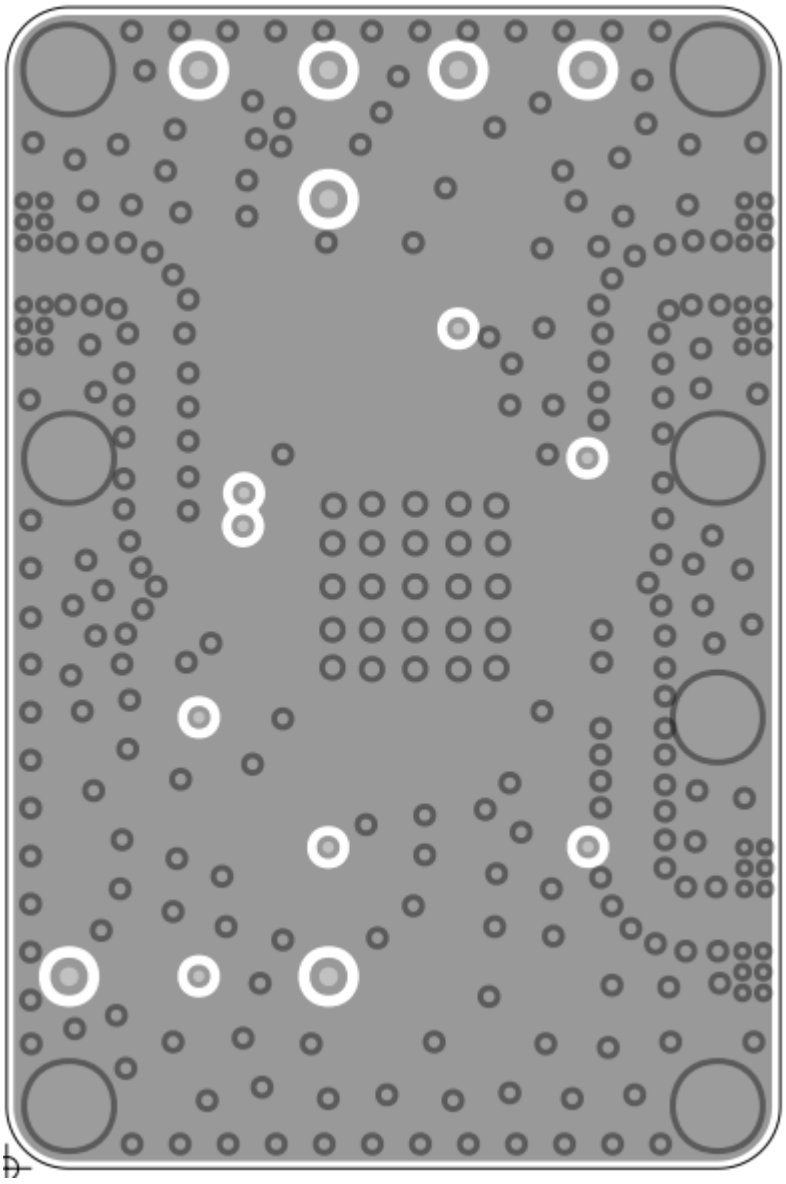


Figure 19 PLL bottom layer.

5.3 Upconverter Design

5.3.1 Upconverter Schematic Design

First, we learned about modulation and IQ-modulation, and then we read the Datasheet of the IQ modulator chip from Analog Devices, we learned the basic functions of the chip, what every pin stands for and what are the inputs and outputs of it.
Then we looked in some design references from the Evaluation Board of Analog Devices and the X-microwave design, and summarized our understanding and implemented it to the components and connections on the electrical scheme.

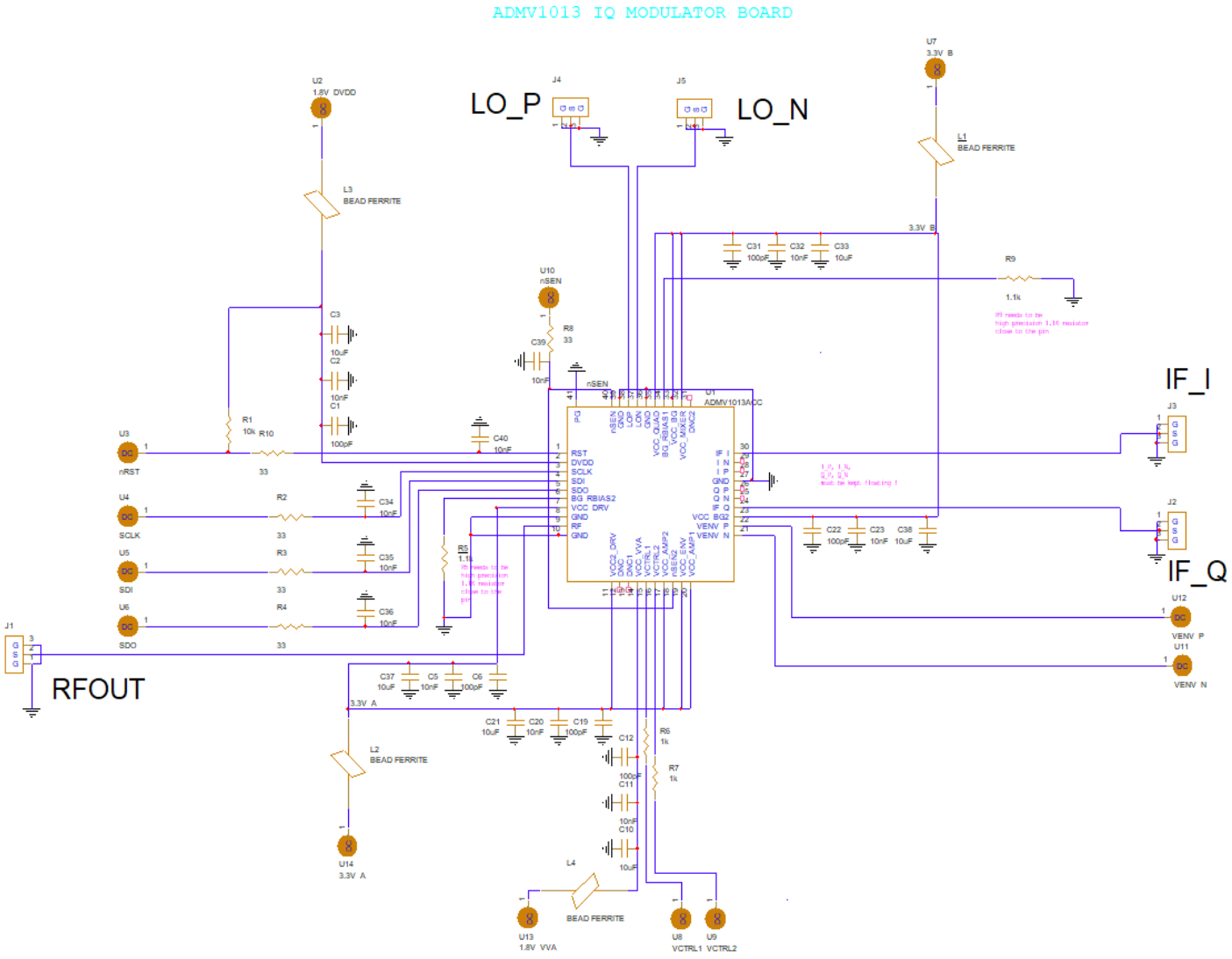


Figure 20 Upconverter schematic.

Main considerations:

- **Differential Signaling output** – in this board we have the Local Oscillator differential signals that comes from the PLL, and we also have the VENV_P/N as a differential signaling, those wires are the power detector output of the RF output from the chip, so it is also connected to highest frequency signal of the system.
- **Power pins AC decoupling** – we put three capacitors of $10[\mu F], 10[nF], 100[pF]$ on the power wires coupling to the ground, on each side of chip, as close as possible to the power input pins.
  As described in equation (30) in the PLL schematic design chapter, the capacitive reactance in these capacitors are:
  $X_{10[\mu F]} = \frac{1}{2\pi f_c 10^{-5}} = 16 \cdot \frac{10^7}{f_c}[\Omega],$
  $X_{10[nF]} = 16 \cdot \frac{10^{10}}{f_c}[\Omega],$
  $X_{100[pF]} = 16 \cdot \frac{10^{12}}{f_c}[\Omega]$

  This filter is more wide band and more robust the PLL power pins filter and it pass more high frequency signals to the ground.
- **SPI RC (LPF) filtering** – the same as in the PLL goes here. In the Upconverter we determined the parameter to be - $\tau = RC_s = 33[\Omega] \cdot 10^{-8}[F] = 33 \cdot 10^{-8}[sec]$ which is also typical value for SPI signals filtering that runs in [MHz].
- **VENV_P/N for RF out Amplitude Power Detection –** in the ADMV1013 we have the Voltage Envelope Positive and Negative pins, those pins routed to the Power and Control board via vias to be read by the FPGA board and the host that connected to it.
- **VCTRL1/2 for Attenuator Variation According to VENV detection –** the Voltage Control 1/2 pins control the attenuation of the RF output signal and they are routed as well to the FPGA to be controlled according to the VENV values.

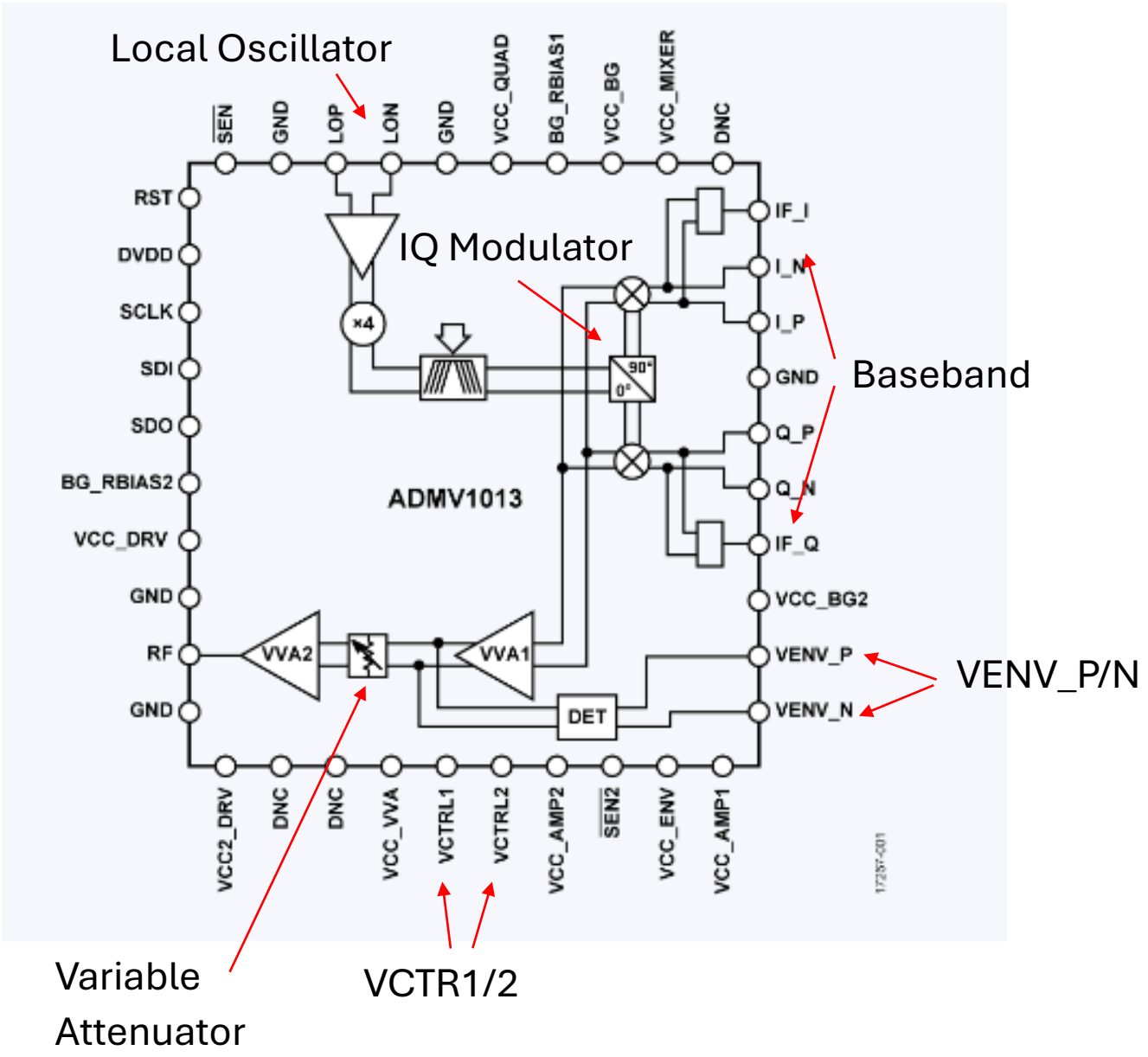


Figure 21 The ADMV1013 Internal Architecture.

5.3.2 Upconverter Layout Design

- **A lot of the RF design considerations are the same as in the PLL**
- **4 layers Board – Top, Ground, Power, Bottom** – as in the PLL board we have in the Upconverter only 4-layers board, almost all the wiring is happening in the top layer and the power layer contains only the power plain and three wiring. The other two layers are the ground layer which separates the top layer from the power layer and the bottom layer which connects the control and power Vias to the power and control board (that is yet to be designed).
- **Resources –** same here Menashe and Denis ☺
- **Design stages by priority –** here too RF first!
- **Differential Signaling –** here too the length and the shape of the differential wires are the same.
- **RF wiring and Connectors build with Ground "fence" –** the same as in the PLL.
- **Curved RF wires for better transition –** the same as in the PLL
- **Power pins AC filtering –** here we have a little more capacitors, but the considerations and the design are basically the same.
- **Constraint to X-microwave Form Factor and Grid –** the board here is also small! 3x3 [cm] and relative to the number of components it was harder than the PLL to put all the capacitors and other components in their place (close to the pins).
- **Vias on the Grid for the Power and Control Board –** here too we tried to put all the vias on the grid crosses unsuccessfully. We left with four vias that are not on the grid crosses – the VENV_P/N on the pins 21 and 22 and the 3.3VA on pin 7 and the nSEN on pin 18, for those vias we will need to do (hand) Back Drilling, to disconnect them from the power and control board ground bottom layer, that will be attached to this board.

5.3.2.1 Top Plan

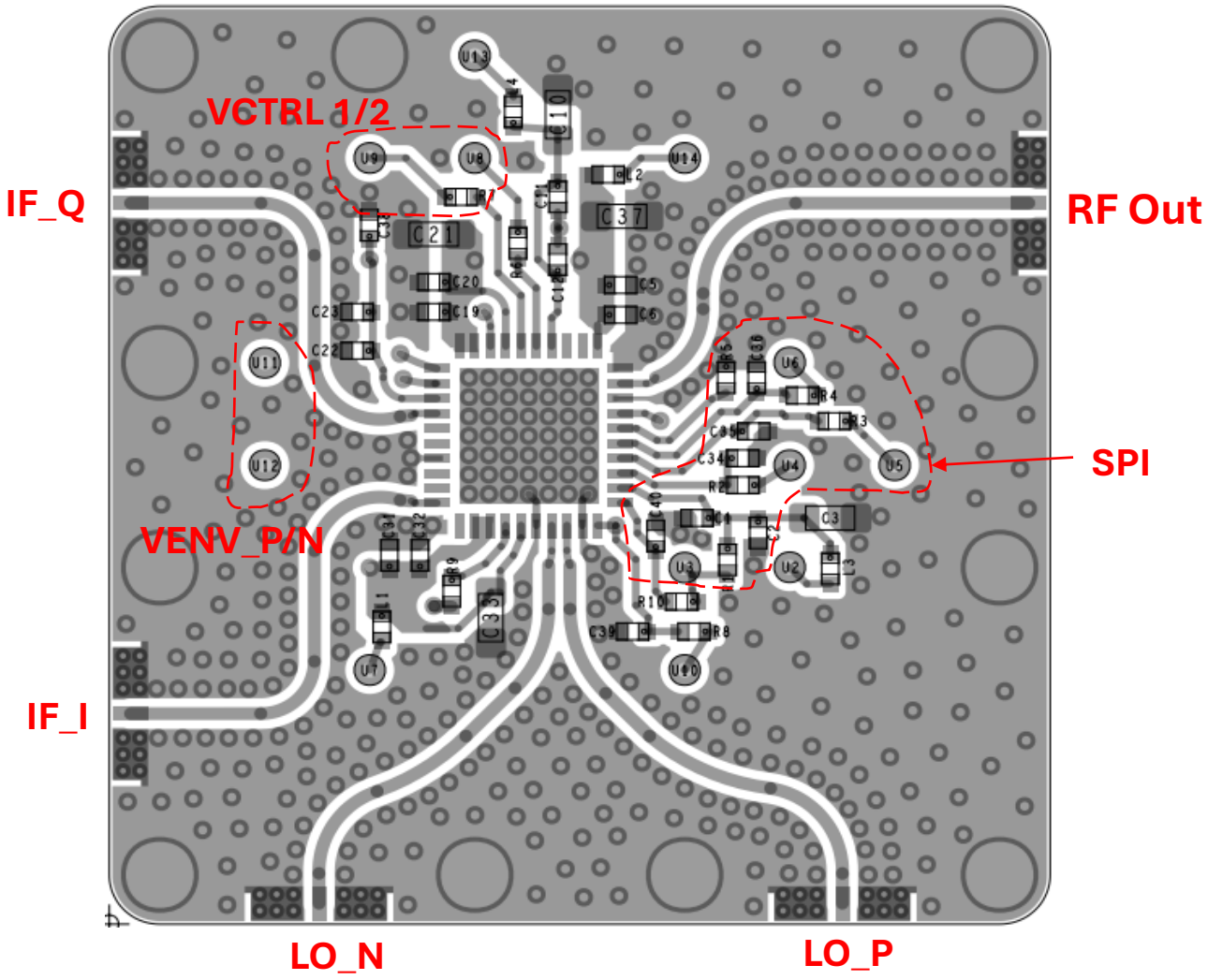


Figure 22 Upconverter layout top layer.

5.3.2.2 Ground Plan

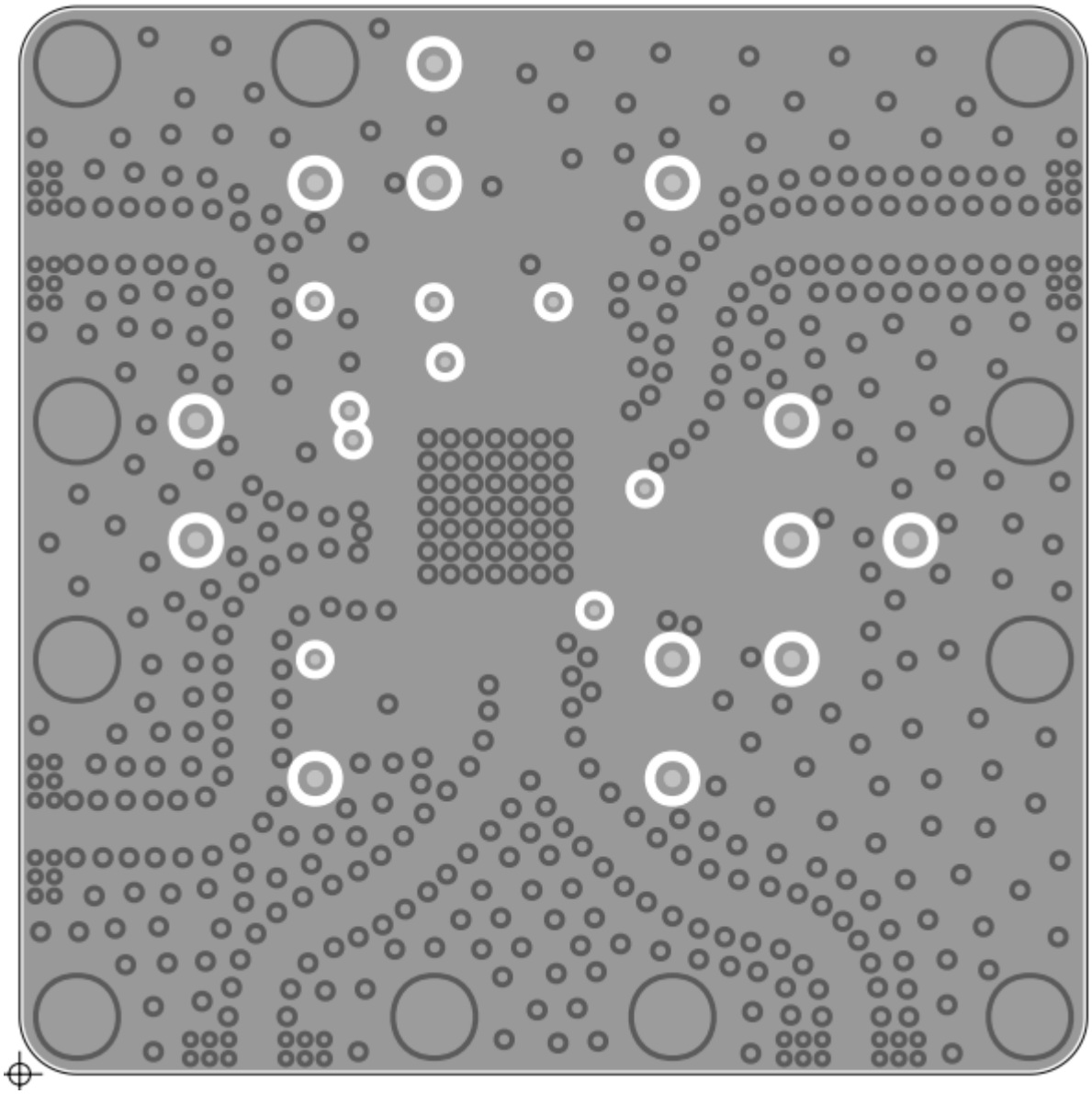


Figure 23 Upconverter layout ground layer.

5.3.2.3 Power Plan

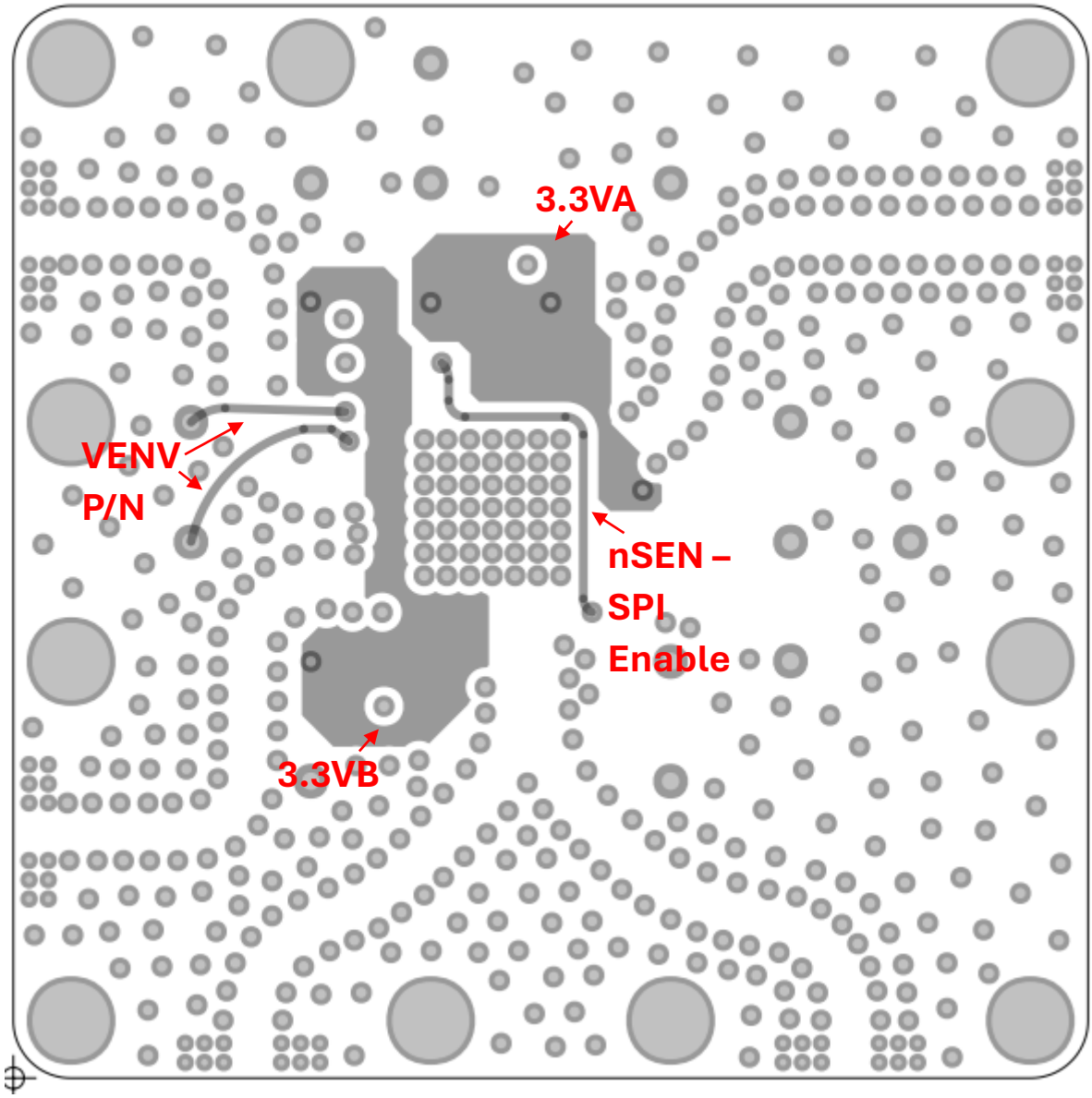


Figure 24 Upconverter layout power layer.

5.3.2.4 Bottom Plan

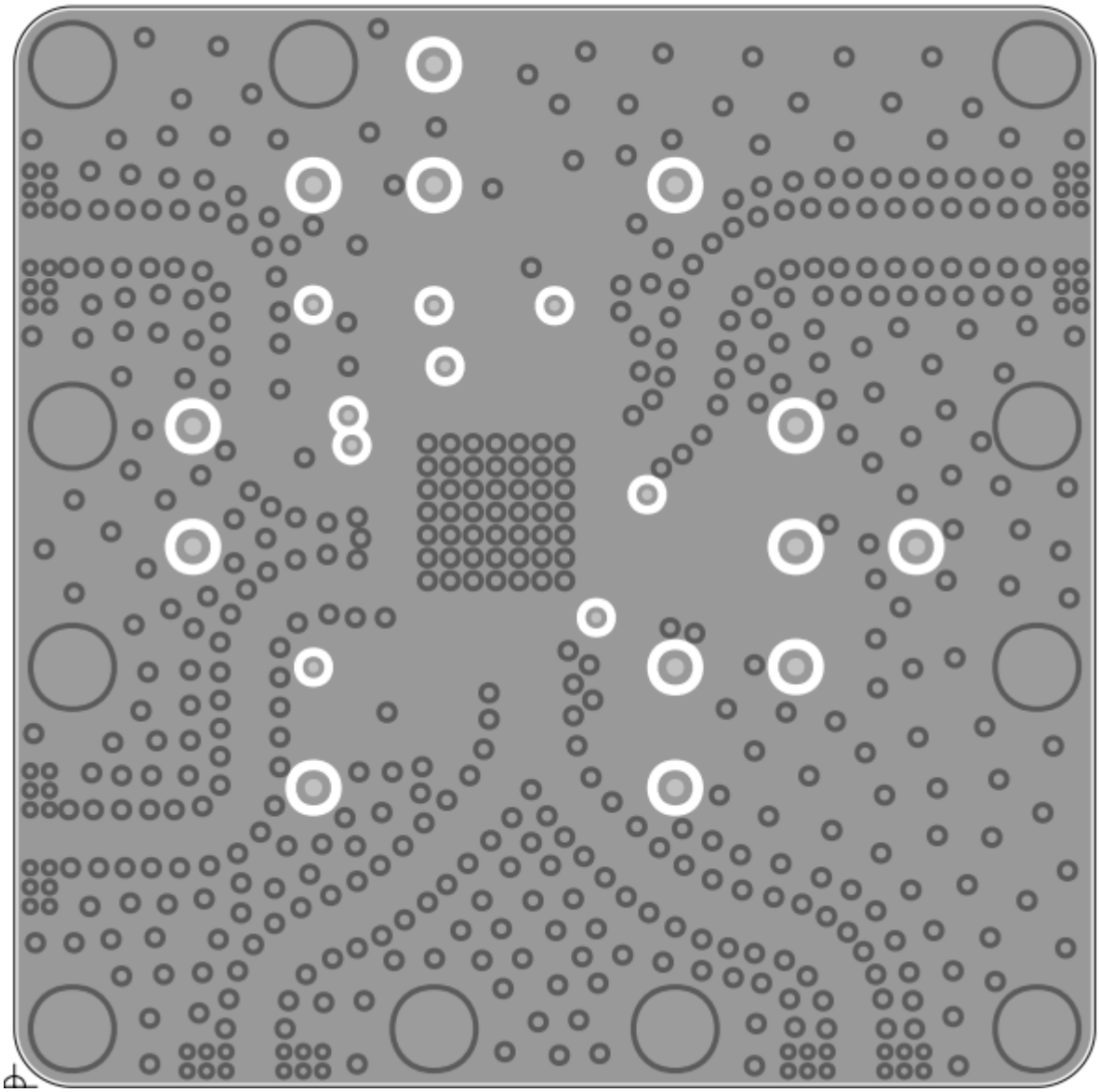


Figure 25 Upconverter layout bottom layer.

6 Conclusions

- **Results and testing** – system has not been tested de-facto yet and remaining stages of the design should be carried out by future projects in order to complete the full system. Power and control boards corresponding to the PLL and the IQ Modulator are required to complete the functionality of the system.
- **Hardware projects** – making a complex hardware system become a reality is quite challenging. There is a long way to go from the starting point of an abstract high level block diagram and all the way to an operating hardware system.
  Following through on such a demanding process is rewarding and we gained a lot of useful experience.
- **RF systems** – the main considerations are minimizing the noise and proper integration of the different subsystems. We have great faith in our design and believe it will demonstrate exceptional robustness to noise once the modules are manufactured.
- **System design** – experience, experience, experience…
- **Theoretical foundation** – it is extremely important to start at this stage and dig deep. Our conclusion regarding the necessary theoretical foundation is that is essential to invest sufficient time to ramp-up on theory before “jumping” to the actual design stage.
- **Board Design** – learning curve can only be achieved by trial and error (ping-pong with Denis and Menashe). There is a great deal of know-how when it comes to board design.
- **Teamwork** – Makes the dream work!
  We believe that our positive collaboration helped us follow through with this challenging project. Each teammate contributed from his past experience and expertise in a way that emphasized our strengths. Our past experience and areas of knowledge complemented each other very well.
- **Experience** – consult with experienced and knowledgeable figures (like Denis and Menashe) whenever in doubt.
- **Documentation and backups** – very important for efficiency and future reference.

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7.1 PLL

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