SHORT RANGE

NINA-B1 series

Stand-alone Bluetooth low energy modules

System Integration Manual

Abstract

This document describes the system integration of NINA-B1 series stand-alone Bluetooth® low energy modules. With embedded Bluetooth low energy stack and u-blox connectivity software, these modules are tailored for OEMs who wish to have the shortest time-to-market. The OEMs can also embed their own application on top of the integrated Bluetooth low energy stack using Nordic SDK or Arm® Mbed™ integrated development environment (IDE).

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Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Initial Production	Early Prod. Information	Data from product verification. Revised and supplementary data may be published later.
Mass Production / End of Life	Production Information	Final product specification.

This document applies to the following products:

Product name	Type number	u-blox connectivity software version	PCN reference	Product status
NINA-B111	NINA-B111-00B-00	1.0.0	N/A	Mass Production
	NINA-B111-01B-00	2.0.0	N/A	Mass Production
	NINA-B111-02B-00	3.0.1	N/A	Initial Production
NINA-B112	NINA-B112-00B-00	1.0.0	N/A	Mass Production
	NINA-B112-01B-00	2.0.0	N/A	Mass Production
	NINA-B112-02B-00	3.0.1	N/A	Initial Production

Contents

1 System description

1.1 Overview and applications

The NINA-B1 series modules are small stand-alone Bluetooth low energy modules featuring Bluetooth 5, a powerful Arm® Cortex®-M4 with FPU, and state-of-the-art power performance. The embedded low power crystal in NINA-B1 minimizes power consumption, thus extending the battery life.

The NINA-B1 is delivered with u-blox connectivity software that provides support for u-blox Bluetooth low energy Serial Port Service, GATT client and server, beacons, NFC™, and simultaneous peripheral and central roles – all configurable from a host by using AT commands.

NINA-B1 offers full flexibility for customers who prefer to add their application to run on the built-in Cortex-M4 with FPU. With 512 kB flash and 64 kB RAM, it offers the best-in-class capacity for customer applications running on top of the Bluetooth low energy stack using SDK from Nordic Semiconductor or Arm® Mbed™. Additionally, NFC and interfaces such as SPI, I²C, and I²S are available, and features like Bluetooth Mesh, AirFuel, and Apple HomeKit are also supported. In combination with Wirepas Connectivity stack, NINA-B1 can form large scale industrial mesh networks for several applications, such as lighting, asset tracking, and metering.

NINA-B112 comes with an internal antenna and NINA-B111 has a pin for use with an external antenna. The internal PIFA antenna is specifically designed for the small NINA-B1 form factor and provides an extensive range of more than 300 m, independent of ground plane and component placement.

The module is globally certified for use with the internal antenna or a range of external antennas. This reduces time and effort for customers integrating NINA-B1 in their designs.

Model		Radio						Interfaces				Power				Features								Grade		
	Software application	Bluetooth® qualification	Bluetooth profiles	NFC for "Touch to Pair"	Maximum radiated output power (EIRP) [dBm]	Maximum range [m]	Antenna type	UART	SPI and I²C	GPIO pins	AD converters (ADC)	Power supply: 1.7- 3.6 VDC	Current consumption, sleep [µA]	Current consumption, idle [µA]	Current consumption, Tx @ 0 dBm [mA]	u-blox Low Energy Serial Port Service	GATT server and GATT client	Throughput [Mbps]	AT command support	IPv6	Mesh networking	Max simultaneous connections	Over-the-air firmware update	Standard	Professional	Automotive
NINA-B111	uCS[1]	v4.2	G	•	7	350	P	•				•	0.3	2	5	•	•	0.7	•			8				
	Open CPU[2]	v5.0	G	•	7	350	P	•	•	19	8	•	0.3	2	5		•	1.4		•	•	20	•			
NINA-B112	uCS[1]	v4.2	G	•	6	300	I	•				•	0.3	2	5	•	•	0.7	•			8				
	Open CPU[2]	v5.0	G	•	6	300	I	•	•	19	8	•	0.3	2	5		•	1.4		•	•	20	•			

1 = u-blox connectivity software
2 = open CPU for embedded customer developed applications using Nordic SDK, Arm® Mbed™ or Wirepas SDK
P = antenna pin
I = internal antenna
G = GATT

Table 1: NINA-B1 series main features summary

1.1.1 Module architecture

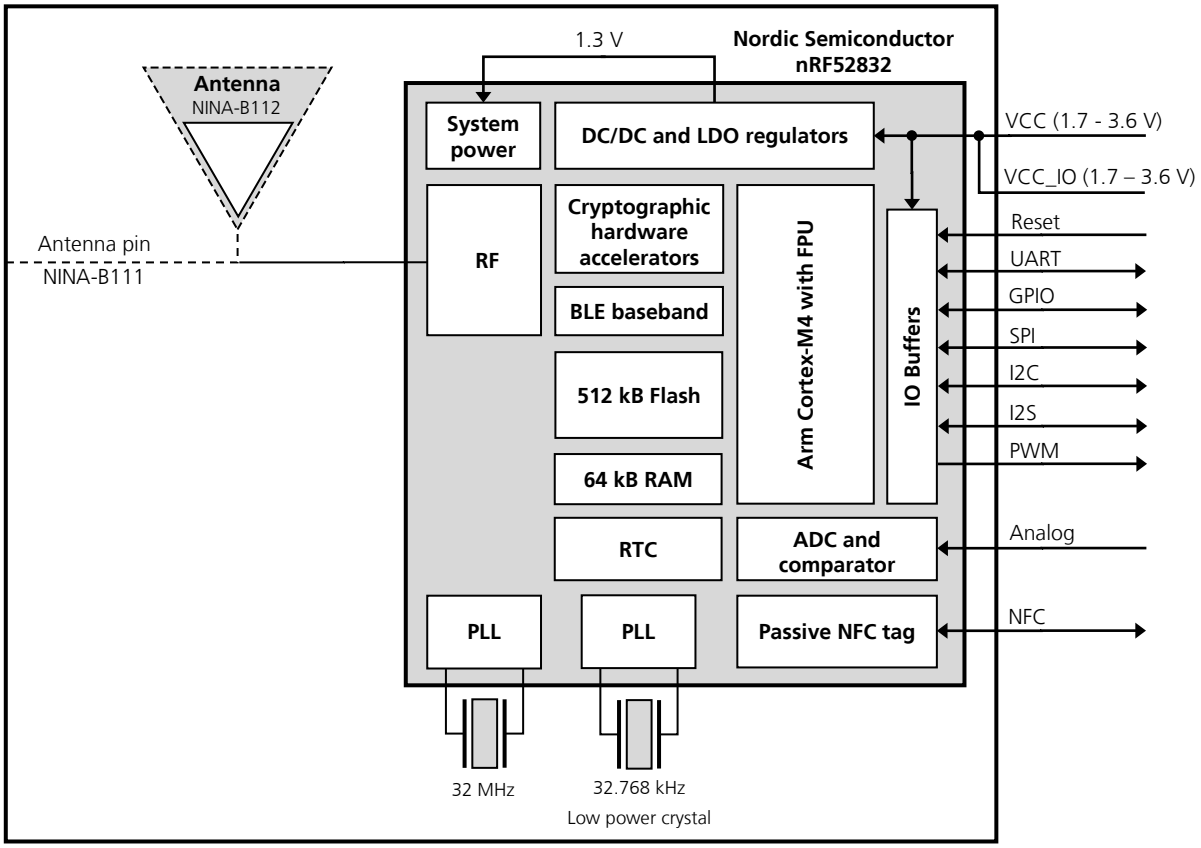


Figure 1: Block diagram of NINA-B1 series

1.1.2 Hardware options

The NINA-B1 series modules use an identical hardware configuration except for the different PCB sizes and antenna solutions. An on board 32.768 kHz low power crystal is always included and an integrated DC/DC converter for higher efficiency under heavy load situations.

1.1.3 Software options

The NINA-B1 series module can be used either together with the pre-flashed u-blox connectivity software or as an Open CPU module where you can run your own application developed with either Arm Mbed, Nordic SDK or Wirepas development environment inside the NINA-B1 module. The different software options are described in more detail in section 2.

1.2 Pin configuration and function

1.2.1 Pin attributes

1. **FUNCTION:** Pin function
2. **PIN NAME:** The name of the package pin or terminal
3. **PIN NUMBER:** Package pin numbers associated with each signal
4. **POWER:** The voltage domain that powers the pin
5. **TYPE:** Signal type description:
   - I = Input
   - O = Output
   - I/O = Input and Output
   - D = Open drain

- DS = Differential
- PWR = Power
- GND = Ground
- PU = Internal Pull-Up
- PD = Internal Pull-Down
- H = High-Impedance pin
- RF = Radio interface

6. **SIGNAL NAME:** The signal name for that pin in the mode being used
7. **REMARKS:** Pin description and notes.

1.2.2 Pin description

The pin-out described in Figure 2 is an example pin-out that demonstrates the most commonly used interfaces.

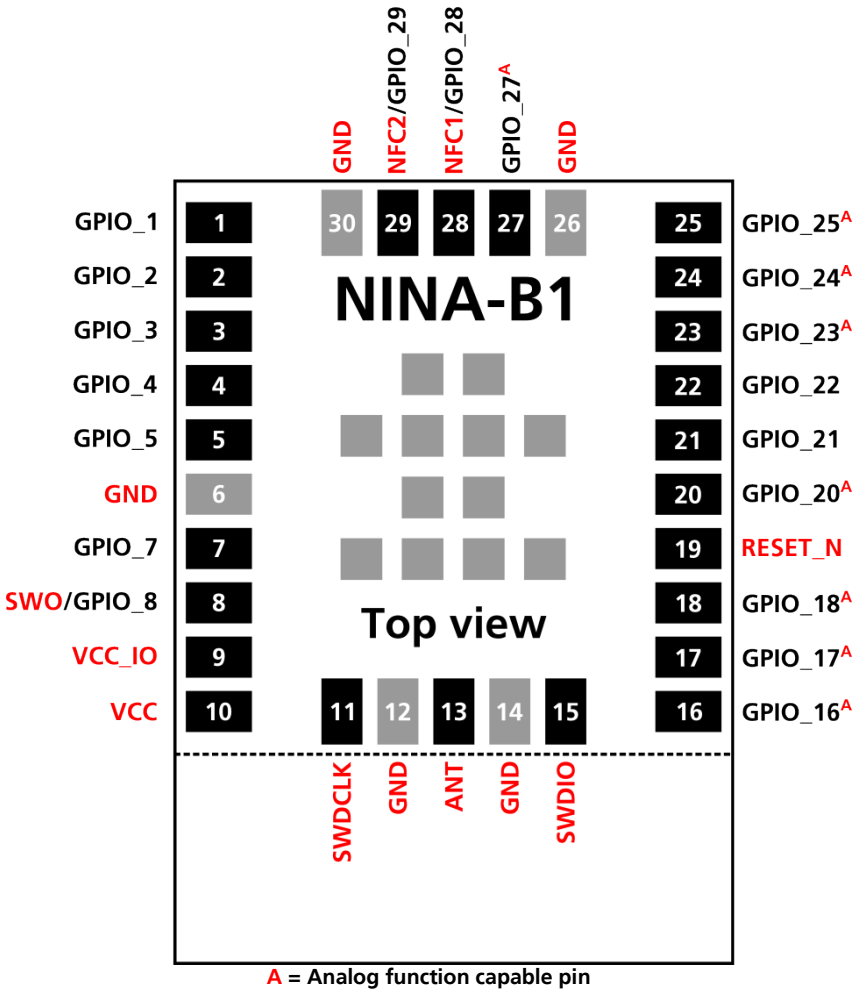


Figure 2: NINA-B1 series pin assignment (top view)

The grey pins in the center of the modules are GND pins. The outline of NINA-B111 ends at the dotted line as shown in Figure 2, where the antenna area of NINA-B112 begins.

☞ All digital or analog functions described in this manual can be freely assigned to any GPIO pin. Analog functions are limited to analog capable pins. Signals marked red in Figure 2 are not freely assignable but locked to a specific pin.

☞ The GPIO pins 16, 17, 18, and 20 are connected to pins located close to the radio part of the RF chip. It is recommended to avoid using these pins for high speed digital interfaces or sinking/sourcing large currents through them. Doing so, can affect the RF performance.

Do not apply an NFC field to the NFC pins when they are configured as GPIOs. Doing so may cause permanent damage to the module. When driving different logic levels on these pins in GPIO mode, a small current leakage will occur, make sure they are set to the same logic level before entering into any power saving modes.

Function	Pin Name	Pin No.	nR52 pin	Type	Description	u-blox connectivity software
Power	**VCC**	10		PWR	Module supply input 1.7-3.6V range	
	VCC_IO	9		PWR	IO Voltage supply input Must be connected to VCC on NINA-B1	
	GND	6, 12, 14, 26, 30		GND	Module ground	
	EGP	-		GND	The exposed pads in the center of the module should be connected to the GND	
GPIO	**GPIO_1**	1	P0.08	I/O	General purpose I/O	RED: System status signal
	GPIO_2	2	P0.11	I/O	General purpose I/O	
	GPIO_3	3	P0.12	I/O	General purpose I/O	
	GPIO_4	4	P0.13	I/O	General purpose I/O	
	GPIO_5	5	P0.14	I/O	General purpose I/O	
	GPIO_7	7	P0.16	I/O	General purpose I/O	GREEN/SWITCH_1: This signal is multiplexed: GREEN: System status signal. SWITCH_1: • Grounding SWITCH_1 and SWITCH_2 during a reset will make the module enter the bootloader. • Grounding SWITCH_1 and SWITCH_2 during a reset and holding it low for 10s will make the module restore all factory settings.
	GPIO_16	16	P0.28	I/O	General purpose I/O Pin is analog capable	UART_DTR: Can be used to indicate system mode
	GPIO_17	17	P0.29	I/O	General purpose I/O Pin is analog capable	UART_DSR: Can be used to set system mode
	GPIO_18	18	P0.30	I/O	General purpose I/O Pin is analog capable	SWITCH_2: • Grounding SWITCH_1 and SWITCH_2 during reset will make the module enter the bootloader. • Grounding SWITCH_1 and SWITCH_2 during a reset and holding it low for 10s will make the module restore all factory settings. • Grounding SWITCH_2 during reset will reset the UART serial settings. • Can be use as external connect or to enable parable mode. See *u-blox Short Range Modules AT Commands Manual [4]* for more details.
	GPIO_20	20	P0.31	I/O	General purpose I/O Pin is analog capable	UART_RTS: UART request to send control signal
	GPIO_21	21	P0.07	I/O	General purpose I/O	UART_CTS: UART clear to send control signal
	GPIO_22	22	P0.06	I/O	General purpose I/O	UART_TXD UART data output

Function	Pin Name	Pin No.	nR52 pin	Type	Description	u-blox connectivity software
	GPIO_23	23	P0.05	I/O	General purpose I/O Pin is analog capable	UART_RXD: UART data input
	GPIO_24	24	P0.02	I/O	General purpose I/O Pin is analog capable	
	GPIO_25	25	P0.03	I/O	General purpose I/O Pin is analog capable	
	GPIO_27	27	P0.04	I/O	General purpose I/O Pin is analog capable	
Control	**RESET_N**	19	P0.21	I	System reset input Active low	
Radio	**ANT**	13		I/O	Tx/Rx antenna interface Used with NINA-B111 modules	
	NFC1/GPIO_28	28	P0.09	I/O	NFC antenna pin 1 May be used as a GPIO	
	NFC2/GPIO_29	29	P0.10	I/O	NFC antenna pin 2 May be used as a GPIO	
Other	**SWO/GPIO_8**	8	P0.18	I/O	Serial Wire debug trace data output May be used as a GPIO	BLUE: System status signal
	SWDCLK	11		I	Serial Wire Debug port clock signal	
	SWDIO	15		I/O	Serial Wire Debug port data signal	

Table 2: NINA-B1 pin description

⚠ **Do not apply any Voltage to Digital, Control and Radio signal groups while in Non-powered mode to avoid damaging the module.**

1.3 Supply interfaces

1.3.1 Main supply input

The NINA-B1 series uses an integrated DC/DC converter to transform the supply voltage presented at the **VCC** pin into a stable system core voltage. Due to this, the NINA-B1 modules are compatible for use in battery powered designs.

While using NINA-B1 with a battery, it is important that the battery type can handle the peak power of the module. In case of battery supply, consider adding extra capacitance on the supply line to avoid capacity degradation. See the *NINA-B1 series Data Sheet [2]* for information about voltage supply requirement and current consumption.

Rail	Voltage requirement	Current requirement (peak)
VCC	1.7 V – 3.6 V	15 mA

Table 3: Summary of voltage supply requirements

☞ The current requirement in Table 3 considers using the u-blox connectivity software with UART comunication. But it does not include any aditional I/O current. Any use of external push-buttons, LEDs, or other interfaces will add to the total current consumption of the NINA-B1 module. The peak current consumption of the entire design will have to be taken into account when considering a battery powered solution.

1.3.2 Digital I/O interfaces reference voltage (VCC_IO)

On the NINA-B1 series modules, the I/O voltage level is the same as the supply voltage and **VCC_IO** is internally connected to the supply input **VCC**.

When using NINA-B1 with a battery, the I/O voltage level will vary with the battery output voltage, depending on the charge of the battery. Level shifters might be needed depending on the I/O voltage of the host system.

1.3.3 VCC application circuits

The power for NINA-B1 series modules is provided through the VCC pins, which can be one of the following:

- Switching Mode Power Supply (SMPS)
- Low Drop Out (LDO) regulator
- Battery

The SMPS is the ideal choice when the available primary supply source has higher value than the operating supply voltage of the NINA-B1 series modules. The use of SMPS provides the best power efficiency for the overall application and minimizes current drawn from the main supply source.

⚠ **While selecting SMPS, ensure that AC voltage ripple at switching frequency is kept as low as possible. Layout shall be implemented to minimize impact of high frequency ringing.**

The use of an LDO linear regulator is convenient for a primary supply with a relatively low voltage where the typical 85-90% efficiency of the switching regulator leads to minimal current saving. Linear regulators are not recommended for high voltage step-down as they will dissipate a considerable amount of energy.

DC/DC efficiency should be evaluated as a tradeoff between active and idle duty cycle of the specific application. Although some DC/DC can achieve high efficiency at extremely light loads, a typical DC/DC efficiency quickly degrades as idle current drops below a few mA greatly reducing the battery life.

Due to the low current consumption and wide voltage range of the NINA-B1 series module, a battery can be used as a main supply. The capacity of the battery should be selected to match the application. Care should be taken so that the battery can deliver the peak current required by the module. See the *NINA-B1 series Data Sheet [2]* for electrical specifications.

It is considered as best practice to have decoupling capacitors on the supply rails close to the NINA-B1 series module, although depending on the design of the power routing on the host system, capacitance might not be needed.

1.4 System function interfaces

1.4.1 Module reset

You can reset the NINA-B1 modules by applying a low level on the **RESET_N** input pin, which is normally set high with an internal pull-up. This causes an "external" or "hardware" reset of the module. The current parameter settings are not saved in the non-volatile memory of the module and a proper network detach is not performed.

1.4.2 Internal temperature sensor

The radio chip in the NINA-B1 module contains a temperature sensor used for over temperature and under temperature shutdown.

⚠ **The temperature sensor is located inside the radio chip and should not be used if an accurate temperature reading of the surrounding environment is required.**

1.5 Debug – Serial Wire Debug (SWD)

The primary interface for debug is the SWD interface. The SWD interface can also be used for software upgrade.

The two pins, **SWDIO** and **SWDCLK** should be made accessible on header or test points.

1.6 Serial interfaces

As the NINA B1 module can be used with both the u-blox connectivity software and open CPU based application, based on either the Nordic SDK or the Arm Mbed platform, the available interfaces and the pin mapping can differ. For detailed pin information, see the Pin description section.

1.6.1 Universal Asynchronous Serial Interface (UART)

The NINA-B1 series module provides a Universal Asynchronous Serial Interface (UART) for data communication.

The following UART signals are available:

- Data lines (**RXD** as input, **TXD** as output)
- Hardware flow control lines (**CTS** as input, **RTS** as output)
- **DSR** and **DTS** are used to set and indicate system modes

The UART can be used as both 4 wire UART with hardware flow control and 2-wire UART with only **TXD** and **RXD**. If using the UART in 2-wire mode, **CTS** should be connected to GND on the NINA-B1 module.

Depending on the bootloader used, the UART interface can also be used for software upgrade. See the Software section for more information.

The u-blox connectivity software adds the **DSR** and **DTR** pins to the UART interface. These pins are not used as originally intended, but to control the state of the NINA-B1 module. Depending on the current configuration, the **DSR** can be used to:

- Enter command mode
- Disconnect and/or toggle connectable status
- Enable/disable the rest of the UART interface
- Enter/wake up from the sleep mode

See the *NINA-B1 series Data Sheet [2]* for characteristic information about the UART interface.

Interface	Default configuration
COM port	115200 baud, 8 data bits, no parity, 1 stop bit, hardware flow control

Table 4: Default settings for the COM port while using the u-blox connectivity Software

It is recommended to make the UART available either as test points or connected to a header for software upgrade.

The IO level of the UART will follow the VCC voltage and it can thus be in the range of 1.8 V and 3.6 V. If you are connecting the NINA-B1 module to a host with a different voltage on the UART interface, a level shifter should be used.

1.6.2 Serial Peripheral Interface (SPI)

NINA-B1 supports up to 3 serial peripheral interfaces that can operate in both master and slave modes with a maximum serial clock frequency of 8 MHz in both these modes. The SPI interfaces use the following 4 signals:

- **SCLK**
- **MOSI**
- **MISO**
- **CS**

When using the SPI interface in master mode, it is possible to use GPIOs as additional Chip Select (CS) signals to allow addressing of multiple slaves.

1.6.3 I^2C interface

The Inter-Integrated Circuit (I^2C) interfaces can be used to transfer or receive data on a 2-wire bus network. The NINA-B1 modules can operate as both master and slave on the I^2C bus using both standard (100 kbps) and fast (400 kbps) transmission speeds. The interface uses the **SCL** signal to clock instructions and data on the **SDL** signal.

External pull up resistors are required for the I^2C interface. The value of the pull up resistor should be selected depending on the speed and capacitance of the bus.

1.7 GPIO pins

The NINA-B1 series module can provide up to 19 pins, which can be configured as general purpose input or output. 7 GPIO pins are capable of handling analog functionality. All pins are capable of handling interrupt.

Function	Description	Default NINA-B1 pin	Configurable GPIOs
General purpose input	Digital input with configurable edge detection and interrupt generation.		Any
General purpose output	Digital output with configurable drive strength, pull-up, pull-down, open-source, open-drain and/or slew rate.		Any
Pin disabled	Pin is disconnected from input buffers and output drivers.	All*	Any
Timer/ counter	High precision time measurement between two pulses/ Pulse counting with interrupt/event generation.		Any
Interrupt/ Event trigger	Interrupt/event trigger to the software application/ Wake up event.		Any
ADC input	8/10/12-bit analog to digital converter		Any analog
Analog comparator input	Compare two voltages, capable of generating wake-up events and interrupts		Any analog
PWM output	Output complex pulse width modulation waveforms		Any
Connection status indication	Indicates if a BLE connection is maintained	BLUE**	Any

* = If left unconfigured ** = If using u-blox connectivity software

Table 5: GPIO custom functions configuration

1.7.1 Analog interfaces

8 out of the 19 digital GPIOs can be multiplexed to analog functions. The following analog functions are available for use:

- 1x 8-channel ADC
- 1x Analog comparator*
- 1x Low-power analog comparator*

*Only one of the comparators can be used simultaneously.

1.7.1.1 ADC

The Analog to Digital Converter (ADC) can sample up to 200 kHz using different inputs as sample triggers. Table 6 shows the sample speed in correlation to the maximum source impedance. It supports 8/10/12-bit resolution. Any of the 8 analog inputs can be used both as single-ended inputs and as differential pairs for measuring the voltage across them. The ADC supports full 0 V to VCC input range.

ACQ [us]	Maximum source resistance [kΩ]
3	10
5	40
10	100
15	200
20	400
40	800

Table 6: Acquisition vs source impedance

1.7.1.2 Comparator

The comparator compares voltages from any analog pin with different references as shown in Table 7. It supports full 0 V to VCC input range and can generate different software events to the rest of the system.

1.7.1.3 Low power comparator

The low-power comparator operates in the same way as the normal comparator, with reduced functionality. It can be used during system OFF modes as a wake up source.

1.7.1.4 Analog pin options

The following table shows the supported connections of the analog functions.

☞ An analog pin may not be simultaneously connected to multiple functions.

Analog function	Connects to
ADC single-ended input	Any analog pin or VCC
ADC differential input	Any analog pin or VCC pair
Comparator IN+	Any analog pin
Comparator IN-	Pin 24 or 25, VCC, 1.2 V, 1.8 V, 2.4 V
Low-power comparator IN+	Any analog pin
Low-power comparator IN-	Pin 24 or 25, 1/16 to 15/16 VCC in steps of 1/16 VCC

Table 7: Possible uses of analog pin

1.8 Antenna interfaces

☞ The antenna interface is different for each module variant in the NINA-B1 series.

1.8.1 Antenna pin – NINA-B111

The NINA-B111 is equipped with an RF pin. The RF pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line to allow reception of radio frequency (RF) signals in the 2.4 GHz frequency band.

Choose an antenna with optimal radiating characteristics for the best electrical performance and overall module functionality. An internal antenna, integrated on the application board or an external antenna that is connected to the application board through a proper 50 Ω connector can be used.

While using an external antenna, the PCB-to-RF-cable transition must be implemented using either a suitable 50 Ω connector, or an RF-signal solder pad (including GND) that is optimized for 50 Ω characteristic impedance.

1.8.1.1 Antenna matching

The antenna return loss should be as good as possible across the entire band when the system is operational to provide optimal performance. The enclosure, shields, other components and surrounding environment will

impact the return loss seen at the antenna port. Matching components are often required to re-tune the antenna to bring the return loss within an acceptable range.

It is difficult to predict the actual matching values for the antenna in the final form factor. Therefore, it is a good practice to have a placeholder in the circuit with a "pi" network, with two shunt components and a series component in the middle, to allow maximum flexibility while tuning the matching to the antenna feed.

1.8.1.2 Approved antenna designs

NINA-B1 modules come with a pre-certified design that can be used to save costs and time during the certification process. To take advantage of this service, the customer is required to implement antenna layout according to u-blox reference designs. The reference design is described in *Appendix* B.

The designer integrating a u-blox reference design into an end-product is solely responsible for the unintentional emission levels produced by the end-product.

The module may be integrated with other antennas. In this case, the OEM installer must certify his design with respective regulatory agencies.

1.8.2 Integrated antenna – NINA-B112

The NINA-B112 is equipped with an integrated antenna on the module. This will simplify the integration as there will be no need to do RF trace design on the host PCB. By using the NINA-B112 with integrated antenna, the certification of the NINA-B1 series module can be reused, thus minimizing the effort needed in the test lab.

1.8.3 NFC antenna

The NINA-B1 series modules include a Near Field Communication interface, capable of operating as a 13.56 MHz NFC tag at a bit rate of 106 kbps. As an NFC tag, data can be read from or written to the NINA-B1 modules using an NFC reader; however the NINA-B1 modules are not capable of reading other tags or initiating NFC communications. Two pins are available for connecting to an external NFC antenna: **NFC1** and **NFC2**.

1.9 Reserved pins (RSVD)

Do not connect reserved (**RSVD**) pin. The reserved pins can be allocated for future interfaces and functionality.

1.10 GND pins

Good connection of the module's GND pins with solid ground layer of the host application board is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

See the Module footprint and paste mask and Thermal guidelines sections for information about ground design.

2 Software

The NINA-B1 series module can be used either with the preflashed u-blox connectivity software or as an Open CPU module where you can run your own application developed with either Arm Mbed, Nordic SDK or Wirepas development environment inside the NINA-B1 module.

The software on the NINA-B1 module contains of the following parts:

- SoftDevice S132 is a *Bluetooth*® low energy (BLE) central and peripheral protocol stack solution
- Optional bootloader
- Application

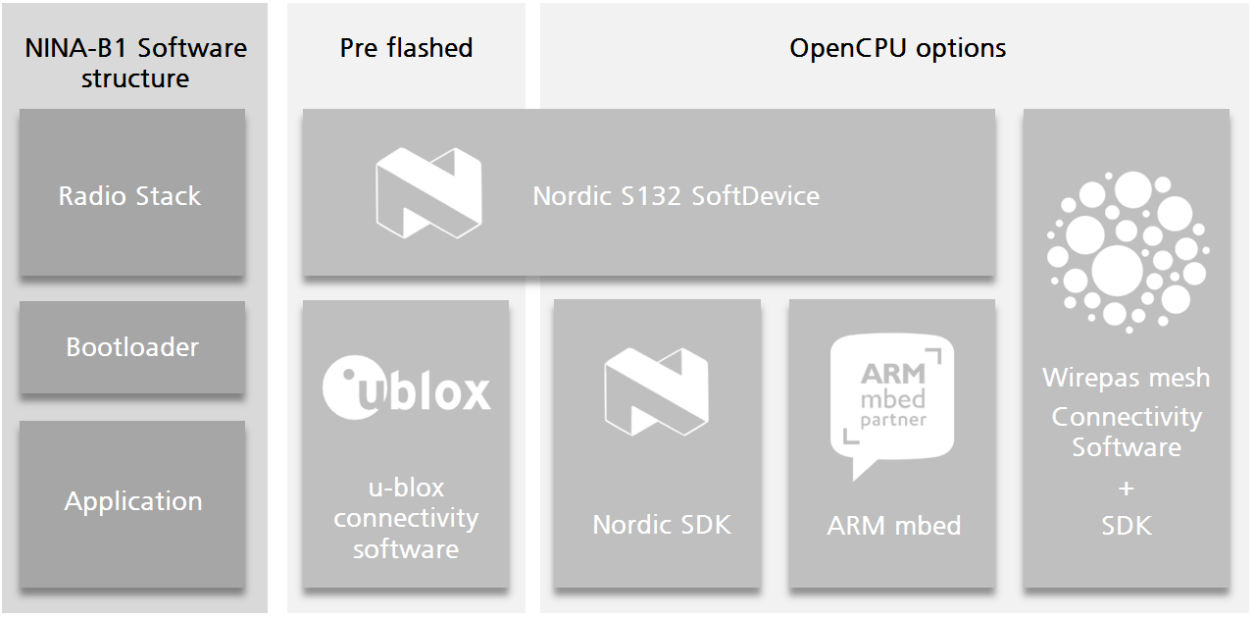


Figure 3: NINA-B1 software structure and available software options

2.1 u-blox connectivity software

The NINA-B1 series module is delivered with the preflashed u-blox connectivity software.

The u-blox connectivity software enables the use of the Bluetooth Low Energy functions, controlled by AT-commands over the UART interface. Examples of supported features are u-blox Low Energy Serial Port Service, GATT server and client, central and peripheral roles and multidrop connections. More information on the features and capabilities of the u-blox connectivity software and how to use it can be found in the *NINA-B1 Getting started guide [3]* and *u-blox Short Range Modules AT Commands Manual [4]*.

2.2 Open CPU

2.2.1 Nordic SDK

The Nordic nRF5 SDK provides a rich developing environment for different devices and applications by including a broad selection of drivers and libraries. The SDK is delivered as a plain .zip-archive, which makes it easy to install. The SDK comes with support for Keil µVision IDE, GCC make files, and IAR support, which gives the freedom to choose the IDE and compiler.

2.2.1.1 Getting started on the Nordic SDK

To work with the Nordic SDK on the NINA-B1 series module, follow the steps mentioned below:

1. Get started with the Nordic Semiconductor toolchain and examples:
    a. Download and install the nRFgo Studio, which includes the nRF Tools package: JLinkARM, JLink CDC, nRFjprog, and mergehex from www.nordicsemi.com. To quickly locate the application package on this website, search for "nRFgo Studio".
    b. Download and install the latest Keil MDK-ARM from www.keil.com.
    c. Download and extract the latest nRF5 SDK found on http://www.nordicsemi.com/eng/Products/Bluetooth-low-energy/nRF5-SDK to the directory that you want to use to work with the nRF5 SDK.
    d. Install the Device Family Pack that is shipped with the SDK, or let Keil install it automatically.

☞ All SDK versions do not include the device family pack and it is preferred to let Keil install it automatically.

    e. Read the information in the SDK Release Notes and check the nRF5 Software Development Kit documentation available at http://infocenter.nordicsemi.com/.

Nordic tools

More information and links to all available tools as well as supported compilers can be found in the Nordic info center.
http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.gs/dita/gs/nordic_tools.html

Support – Nordic development forum

For support on questions related to the development of software using the Nordic SDK, refer to the *Nordic development zone* - https://devzone.nordicsemi.com/

2.2.1.2 Create a custom board for Nordic SDK

The predefined hardware boards included in the Nordic SDK are Nordic development boards only. To add support for a custom board, a custom board support file with the name custom_board.h can be created. This file should be located in the folder …\components\boards\. The custom board can then be selected by adding the define statement #define BOARD_CUSTOM.

The above-mentioned file location is according to the Nordic nRF5 SDK version 12.2.0.

Figure 4 shows an example of how the custom board support file can look like for EVK-NINA-B1.

```
#ifndef BOARD_CUSTOM_H
#define BOARD_CUSTOM_H

#ifdef __cplusplus
extern "C" {
#endif

#include "nrf_gpio.h"

// In this case PIN 16 is used as button SW1, if the green led
// should be used it is possible to defined that one instead.
#define LEDS_NUMBER    2

#define LED_1          8    // Red
#define LED_2          18   // Blue

#define LEDS_ACTIVE_STATE 0

#define LEDS_LIST { LED_1, LED_2 }

#define BSP_LED_0      LED_1
#define BSP_LED_1      LED_2

#define LEDS_INV_MASK  LEDS_MASK

#define BUTTONS_NUMBER 2

#define BUTTON_1       16   // SW1
#define BUTTON_2       30   // SW2
#define BUTTON_PULL    NRF_GPIO_PIN_PULLUP

#define BUTTONS_ACTIVE_STATE 0

#define BUTTONS_LIST { BUTTON_1, BUTTON_2 }

#define BSP_BUTTON_0   BUTTON_1
#define BSP_BUTTON_1   BUTTON_2

#define RX_PIN_NUMBER  5
#define TX_PIN_NUMBER  6
#define CTS_PIN_NUMBER 7
#define RTS_PIN_NUMBER 31
#define HWFC           true

#define SPIS_MISO_PIN   12  // SPI MISO signal.
#define SPIS_CSN_PIN    11  // SPI CSN signal.
#define SPIS_MOSI_PIN   13  // SPI MOSI signal.
#define SPIS_SCK_PIN    14  // SPI SCK signal.

#define SPIM0_SCK_PIN   14  // SPI clock GPIO pin number.
#define SPIM0_MOSI_PIN  13  // SPI Master Out Slave In GPIO pin number.
#define SPIM0_MISO_PIN  12  // SPI Master In Slave Out GPIO pin number.
#define SPIM0_SS_PIN    11  // SPI Slave Select GPIO pin number.

// Low frequency clock source to be used by the SoftDevice
#define NRF_CLOCK_LFCLKSRC      {.source        = NRF_CLOCK_LF_SRC_XTAL,            \
                                 .rc_ctiv       = 0,                                \
                                 .rc_temp_ctiv  = 0,                                \
                                 .xtal_accuracy = NRF_CLOCK_LF_XTAL_ACCURACY_20_PPM}

#ifdef __cplusplus
}
#endif

#endif // BOARD_CUSTOM_H
```

Figure 4: Example of EVK-NINA-B1 custom board support file

2.2.2 Arm Mbed OS

Arm Mbed OS is an open source embedded operating system designed specifically for the "things" in the Internet of Things. It includes all the features to develop a connected product, including security, connectivity, an RTOS, and drivers for sensors and I/O devices. With an RTOS core, based on the widely used open-source CMSIS-RTOS RTX, Arm Mbed OS supports deterministic, multithreaded real time software execution. Arm Mbed OS has native support for building across the Arm Compiler 5, GCC, and IAR compiler toolchains.

2.2.2.1 Getting started with the Arm Mbed OS

A list of prerequisites to getting started with Arm Mbed OS 5 development on EVK-NINA-B1 is provided at https://github.com/ARMmbed/mbed-os-example-ble#getting-started.

Mbed CLI is the name of the Arm Mbed command line tool, which enables the full Mbed workflow such as repositories version control, maintaining dependencies, updating from remotely hosted repositories (GitHub, GitLab and mbed.org), and invoking Arm Mbed's own build system. The document available at https://github.com/ARMmbed/mbed-cli#introduction covers the installation and usage of the Mbed CLI.

For a description on how to create a build target for EVK-NINA-B1, see section 2.2.2.2.3.

Bluetooth low energy examples from Arm Mbed are available at https://github.com/ARMmbed/mbed-os-example-ble.

2.2.2.2 Create a custom target for Arm Mbed

2.2.2.2.1 Add target

Add a new JSON object to the **targets.json** file located in the **"\mbed-os\targets\"** folder. Figure 5 shows an example of the JSON object for EVK-NINA-B1. See *Standard properties [6]* section *[6]*for a list of the properties that are known to the Arm Mbed build system.

☞ The above-mentioned folder location is as per the Arm Mbed OS release 5.2.

```
"EVK_NINA_B1": {
    "supported_form_factors": ["ARDUINO"],
    "inherits": ["MCU_NRF52"],
    "macros_add": [
        "BOARD_PCA10040",
        "NRF52_PAN_12",
        "NRF52_PAN_15",
        "NRF52_PAN_58",
        "NRF52_PAN_55",
        "NRF52_PAN_54",
        "NRF52_PAN_31",
        "NRF52_PAN_30",
        "NRF52_PAN_51",
        "NRF52_PAN_36",
        "NRF52_PAN_53",
        "S132",
        "CONFIG_GPIO_AS_PINRESET",
        "BLE_STACK_SUPPORT_REQD",
        "SWI_DISABLE0",
        "NRF52_PAN_20",
        "NRF52_PAN_64",
        "NRF52_PAN_62",
        "NRF52_PAN_63"],
    "device_has": [
        "ANALOGIN",
        "ERROR_PATTERN",
        "I2C",
        "I2C_ASYNCH",
        "INTERRUPTIN",
        "LOWPOWERTIMER",
        "PORTIN",
        "PORTINOUT",
        "PORTOUT",
        "PWMOUT",
        "RTC",
        "SERIAL",
        "SERIAL_ASYNCH",
        "SLEEP",
        "SPI",
        "SPI_ASYNCH",
        "SPISLAVE"],
    "release_versions": ["2", "5"]
},
```

Figure 5: Example of EVK-NINA-B1 target object

2.2.2.2.2 Pin mapping

Create a folder with the same name as the JSON object created in section 2.2.2.2.1. The folder should be located in **"\mbed-os\targets\TARGET_NORDIC\TARGET_NRF5\TARGET_MCU_NRF52832\"**. For EVK-NINA-B1, the folder will be called **TARGET_EVK_NINA_B1**.

In this new folder, there should be two files, device.h and PinNames.h.

1. **device.h:** This contains the `#include object.h` as shown in Figure 6.

```
#ifndef MBED_DEVICE_H
#define MBED_DEVICE_H

#include "objects.h"

#endif
```

Figure 6: Example code for device.h

2. **PinNames.h:** The PinNames.h file should declare and define a couple of enumerations to configure the custom pin mapping. Figure 6 and Figure 7 show the contents of the PinNames.h file in the case of EVK-NINA-B1.

```
#ifndef MBED_PINNAMES_H
#define MBED_PINNAMES_H

#include "cmsis.h"

#ifdef __cplusplus
extern "C" {
#endif

    typedef enum {
        PIN_INPUT,
        PIN_OUTPUT
    } PinDirection;

#define PORT_SHIFT  3

    typedef enum {
        // nRF52 pin names
        p0 = 0,
        p1 = 1,
        p2 = 2,
        p3 = 3,
        p4 = 4,
        p5 = 5,
        p6 = 6,
        p7 = 7,
        p8 = 8,
        p9 = 9,
        p10 = 10,
        p11 = 11,
        p12 = 12,
        p13 = 13,
        p14 = 14,
        p15 = 15,
        p16 = 16,
        p17 = 17,
        p18 = 18,
        p19 = 19,
        p20 = 20,
        p21 = 21,
        p22 = 22,
        p23 = 23,
        p24 = 24,
        p25 = 25,
        p26 = 26,
        p27 = 27,
        p28 = 28,
        p29 = 29,
        p30 = 30,
        p31 = 31,
        NC = (int)0xFFFFFFFF,     // Not connected
```

Figure 7: PinNames.h - Example code for EVK-NINA-B1

```
//NINA-B1 module pin names
NINA_B1_GPIO_1 = p8,
NINA_B1_GPIO_2 = p11,
NINA_B1_GPIO_3 = p12,
NINA_B1_GPIO_4 = p13,
NINA_B1_GPIO_5 = p14,

NINA_B1_GPIO_7 = p16,
NINA_B1_GPIO_8 = p18,

NINA_B1_GPIO_16 = p28,
NINA_B1_GPIO_17 = p29,
NINA_B1_GPIO_18 = p30,

NINA_B1_GPIO_20 = p31,
NINA_B1_GPIO_21 = p7,
NINA_B1_GPIO_22 = p6,
NINA_B1_GPIO_23 = p5,
NINA_B1_GPIO_24 = p2,
NINA_B1_GPIO_25 = p3,

NINA_B1_GPIO_27 = p4,
NINA_B1_GPIO_28 = p9,
NINA_B1_GPIO_29 = p10,

// EVK-NINA-B1 board
LED1 = NINA_B1_GPIO_1,  // Red
LED2 = NINA_B1_GPIO_7,  // Green/SW1
LED3 = NINA_B1_GPIO_8,  // Blue
LED4 = NC,

SW1 = NINA_B1_GPIO_7,
SW2 = NINA_B1_GPIO_18,

D0 = NINA_B1_GPIO_23,
D1 = NINA_B1_GPIO_22,
D2 = NINA_B1_GPIO_21,
D3 = NINA_B1_GPIO_20,
D4 = NINA_B1_GPIO_8,
D5 = NC,   // SWDIO
D6 = NINA_B1_GPIO_28,
D7 = NINA_B1_GPIO_29,

D8 = NC,   // SWDCLK
D9 = NINA_B1_GPIO_1,
D10 = NINA_B1_GPIO_2,
D11 = NINA_B1_GPIO_4,
D12 = NINA_B1_GPIO_3,
D13 = NINA_B1_GPIO_5,

D14 = NINA_B1_GPIO_24,
D15 = NINA_B1_GPIO_25,

A0 = NINA_B1_GPIO_25,
A1 = NINA_B1_GPIO_24,
A2 = NINA_B1_GPIO_27,
A3 = NINA_B1_GPIO_18,
A4 = NINA_B1_GPIO_17,
A5 = NINA_B1_GPIO_16,


// Nordic SDK pin names
RX_PIN_NUMBER = p5,
TX_PIN_NUMBER = p6,
CTS_PIN_NUMBER = p7,
RTS_PIN_NUMBER = p31,

I2C_SDA0 = p2,
I2C_SCL0 = p3,


// Arm Mbed interface pins
USBTX = TX_PIN_NUMBER,
USBRX = RX_PIN_NUMBER
} PinName;
```

Figure 8: PinNames.h - Example code for EVK-NINA-B1 (Continued)

```
typedef enum {
    PullNone = 0,
    PullDown = 1,
    PullUp = 3,
    PullDefault = PullUp
} PinMode;

#ifdef __cplusplus
}
#endif
#endif
```

Figure 9: PinNames.h - Example code for EVK-NINA-B1 (Continued)

2.2.2.2.3 Build software

In the Arm Mbed CLI, compile software by using the name of the object created in the targets.json file as parameter to the board flag. In the EVK-NINA-B1 example, the build command will be:

`"mbed compile -t GCC_ARM -m EVK_NINA_B1"`.

2.2.3 Wirepas connectivity software

The NINA-B1 series module can also be used together with the Wirepas software stack. This will enable the NINA-B1 module to be used in a big scale true mesh environment.

The Wirepas connectivity software is third party software licensed from Wirepas.

For more information about the Wirepas connectivity software, contact the u-blox support for your area as listed in the Contact section.

2.3 Flashing the NINA-B1 module

It is possible to reflash the NINA-B1 module using either the UART or SWD interface whenever a new version of the u-blox connectivity software is available or when using a custom application.

Flashing of u-blox connectivity software is normally done over UART. If the flash is erased or any other software is flashed on the NINA-B1 module, then the SoftDevice and the u-blox bootloader must be flashed over SWD before the u-blox connectivity software can be flashed again. See section 2.3.2 for more information.

2.3.1 UART flashing

To use the UART interface, the module must have a bootloader that supports flashing over UART. The u-blox connectivity software v2.0.0 and later includes a bootloader that can flash over UART.

NINA-B1 modules with u-blox connectivity software v1.0.0 can be flashed using the SWD interface only and not the UART interface. See section 2.3.2 for flashing instructions.

The u-blox connectivity software for UART flashing contains two separate .zip files:

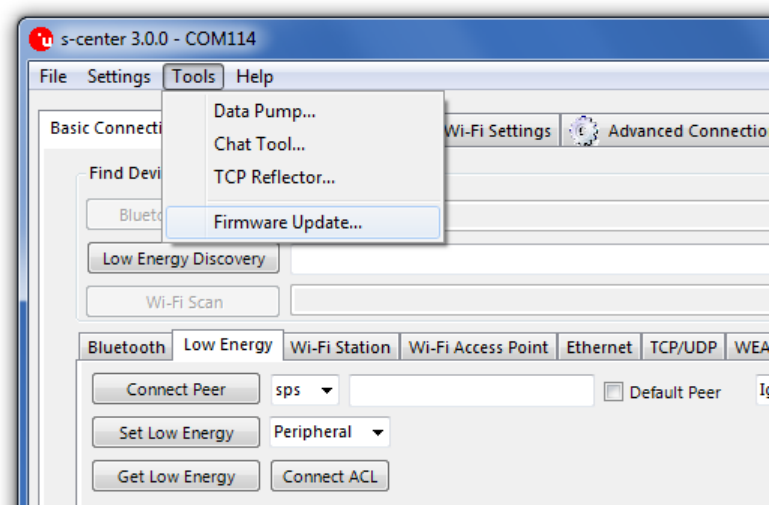
1. One zip file contains the application and
2. Another contains the bootloader and SoftDevice as listed below:
   - Application – NINA-B11X-FWx.x.x.zip
   - Bootloader and SoftDevice – NINA-B11X-BOOTx.x.x_SDx.x.x.zip

It is critical that both the zip files are flashed during an update and that the zip file that contains the bootloader and the SoftDevice is flashed first.

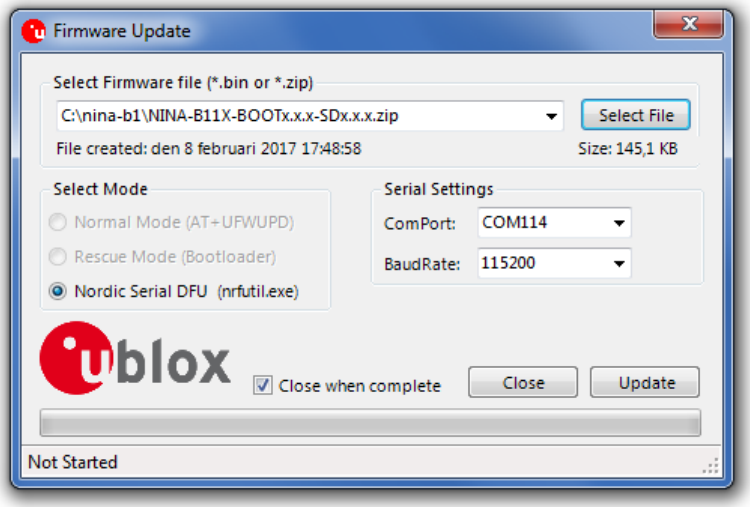
2.3.1.1 s-center

To flash the module using s-center,

1. Select **Tools** > **Firmware Update** as shown in the following screenshot:



2. Select the file that contains the bootloader and SoftDevice.

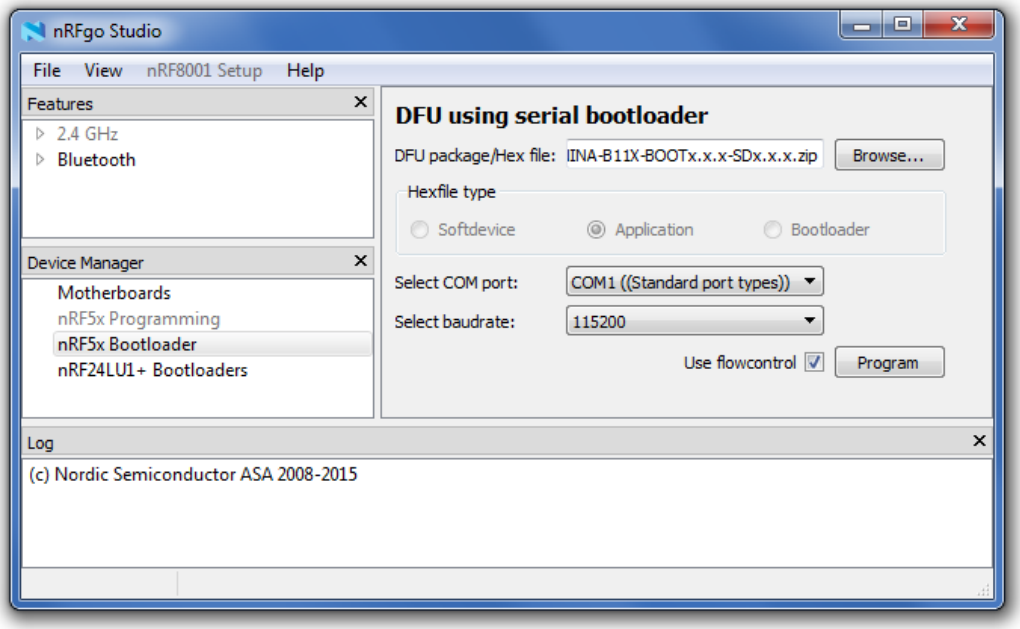


3. Set the correct COM port and the desired speed and click **Update** button.
4. The module will then reboot into the bootloader and the flashing will start. A command prompt will start in the background to run the external program *nrfutil*. When the flashing is done, the command prompt will close by itself.
5. Repeat the above-mentioned steps 1 to 3 with the file that contains the application.

2.3.1.2 nRFgo Studio

The Nordic tool nRFgo Studio can also be used to reflash the NINA-B1 module over UART. See the *Nordic Semiconductor Infocenter [14]* for information about the tool.

1. Start the nRFgo Studio and open the tab called **Device Manager/nRF5x Bootloader**
2. Select the zip file that contains the bootloader and the SoftDevice to flash down to the module.
3. Select the correct COM port and the desired speed (115200, with flow control) and click **Program**.



The nRFgo Studio will then ask you to put the device in the bootloader mode. This is done either by sending the AT command *AT+UFWUPD=0* or by grounding GPIO7/SWITCH1 and GPIO18/SWITCH2 during a reset of the module. Repeat the above-mentioned steps 1 to 3 with the file that contains the application.

Keep in mind that the bootloader will time out and resume the application after 10 seconds. Flashing must have started before the time out and resuming of the application.

2.3.2 SWD flashing

For SWD flashing, an external debugger has to be connected to the SWD interface of the NINA-B1 module. The nRFgo Studio can then be used to flash the software to the module.

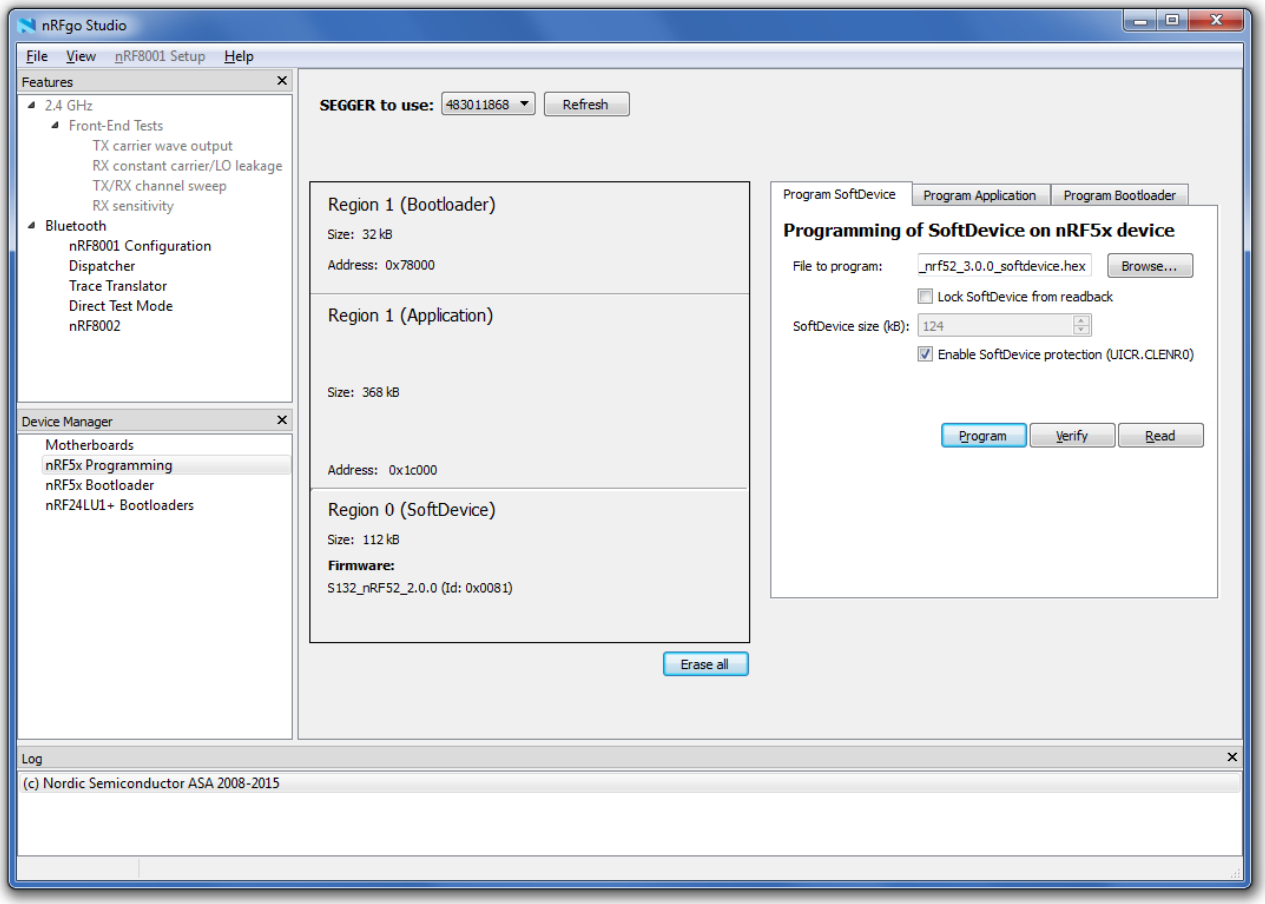
The external debugger SEGGER J-Link BASE has been verified to work with the NINA-B1 modules.

The EVK-NINA-B1 evaluation kit incorporates an onboard debugger and can thus be flashed without any external debugger.

2.3.2.1 Flashing the software

Flashing the software will erase the Bluetooth device address, which must be manually rewritten to the module after flashing. Ensure that you make a note of your Bluetooth device address before continuing with the flashing procedure. See section 2.3.2.2 for additional information.

In the device manager of the nRFgo Studio, select **nRF5x Programming** as shown in the following screenshot:



Go to the respective tabs and flash the following files in the below-mentioned order:

1) SoftDevice
2) Bootloader (if applicable)
3) Application
4) Application validation file (only applicable for u-blox connectivity software)

In the software deliveries on the u-blox webpage, the .hex files for the u-blox connectivity software are available:

- SoftDevice (s132_nrf52_xxx.hex)
- Bootloader (NINA-B11X_BOOT_xxx.hex)
- Application (NINA-B11X_FW_xxx.hex)
- Application validation file (valid_app_xxx.hex)

When developing and flashing applications based on the Nordic SDK, it is recommended to do an **Erase all** to remove the u-blox connectivity software and its stored parameters before flashing down the custom application.

When the new u-blox connectivity software has been flashed, remember to restore the Bluetooth device address as mentioned in section 2.3.2.3.

2.3.2.2 Read the Bluetooth device address

Flashing the software will erase the Bluetooth device address, which must be manually rewritten to the module after flashing. Ensure that you make a note of your Bluetooth device address before continuing with the flashing procedure. There are two ways to access the Bluetooth device address of your module as described in the following subsections:

2.3.2.2.1 Data Matrix barcode

If your device is already erased or not responding, you will have to read out the Bluetooth device address from the Data Matrix barcode that can be found on the module label.

Use a barcode reader capable of handling the data matrix barcodes. Remove the first 3 and the last 4 digits of the code read out, the remaining code is the Bluetooth device address.

Example reading from the Data Matrix barcode (Bluetooth device address is marked in **bold**):

684**D4CA6EB00613**0200

2.3.2.2.2 AT command

If your device is still operational and running u-blox connectivity software, execute the following command to read-out the Bluetooth device address (Bluetooth device address marked in **bold**):

AT+UMLA=1

+UMLA: **D4CA6EB00613**

OK

2.3.2.3 Restoring the Bluetooth device address

When the new u-blox connectivity software is flashed to the module, it is important to restore the Bluetooth device address as well.

Step 1:

To enable writing of the Bluetooth device address, execute the following command and wait for the startup event:

AT+UPROD=1

OK

+STARTUP

Step 2:

To write your Bluetooth device address to the flash memory of the device and reset the device, execute the following commands (Bluetooth device address is marked in **bold** below, replace with your own):

AT+UPRODPW=1,**D4CA6EB00613**

OK

AT+CPWROFF

OK

+STARTUP

Step 3:

Verify that you have successfully written your Bluetooth Device address to the device using the following command:

AT+UMLA=1

+UMLA: D4CA6EB00613

OK

The Bluetooth device address will be permanently stored. The only way to write the Bluetooth device address again in case you do a mistake is to repeat the SWD flashing procedure as mentioned in section 2.3.2.1.

Failing to restore the Bluetooth device address will cause some of the Bluetooth security modes not to work.

3 Design-in

3.1 Overview

For an optimal integration of NINA-B1 series modules in the final application board, it is recommended to follow the design guidelines stated in this chapter. Every application circuit must be properly designed to guarantee the correct functionality of the related interface, however a number of points require high attention during the design of the application device.

The following list provides important points sorted by rank of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **Ant** pad.

   Antenna circuit affects the RF compliance of the device integrating NINA-B1 modules with applicable certification schemes. Follow the recommendations provided in section 3.2 for schematic and layout design.

2. Module supply: **VCC**, **VCC_IO**, and **GND** pins.

   The supply circuit affects the performance of the device integrating NINA-B1 series module. Follow the recommendations provided in section 3.3 for schematic and layout design.

3. Analog signals: GPIO

   Analog signals are sensitive to noise and should be routed away from high frequency signals.

4. High speed interfaces: **UART, SPI** and **SWD** pins.

   High speed interfaces can be a source of radiated noise and can affect compliance with regulatory standards for radiated emissions. Follow the recommendations provided in sections 3.4.1 and 2.4.2 for schematic and layout design.

5. System functions: **RESET_N**, **I2C**, **GPIO** and other **System input and output pins**.

   Accurate design is required to guarantee that the voltage level is well defined during module boot.

6. Other pins:

   Accurate design is required to guarantee proper functionality.

3.2 Antenna interface

As the unit cannot be mounted arbitrary, the placement should be chosen with consideration so that it does not interfere with radio communication. The NINA-B112 with an internal surface mounted antenna cannot be mounted in a metal enclosure. No metal casing or plastics using metal flakes should be used. Avoid metallic based paint or lacquer as well. The NINA-B111 offers more freedom as an external antenna can be mounted further away from the module.

⚠ **According to FCC regulations, the transmission line from the module's antenna pin to the antenna or antenna connector on the host PCB is considered part of the approved antenna design. Therefore, module integrators must either follow exactly one of the antenna reference design used in the module's FCC type approval or certify their own designs.**

3.2.1 RF transmission line design (NINA-B111 only)

RF transmission lines, such as the ones from the **ANT** pad up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω. Figure 10 illustrates the design options and the main parameters to be taken into account when implementing a transmission line on a PCB:

- The micro strip (a track coupled to a single ground plane, separated by dielectric material)
- The coplanar micro strip (a track coupled to ground plane and side conductors, separated by dielectric material)
- The strip line (a track sandwiched between two parallel ground planes, separated by dielectric material).

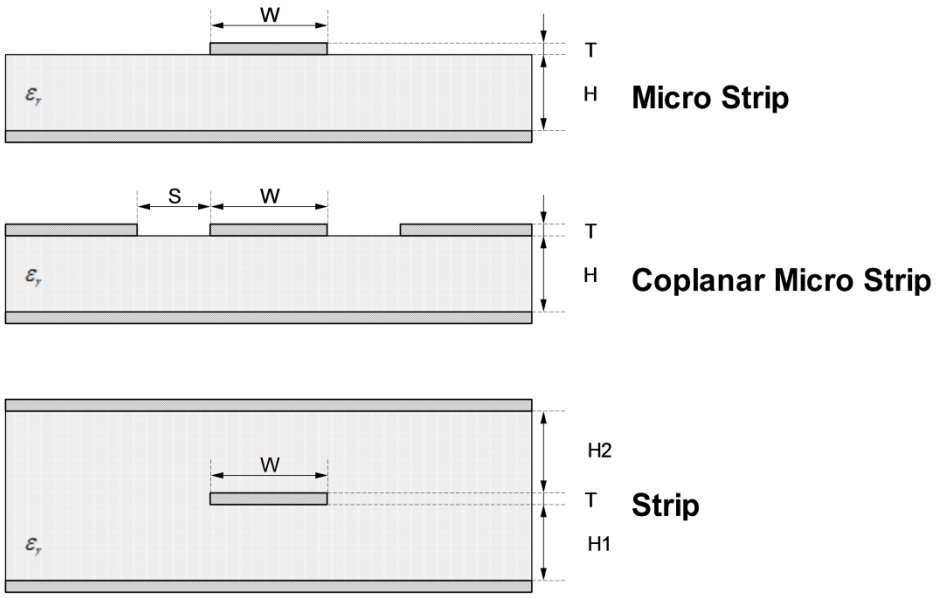


Figure 10: Transmission line trace design

To properly design a 50 Ω transmission line, the following remarks should be taken into account:

- The designer should provide enough clearance from surrounding traces and ground in the same layer; in general, a trace to ground clearance of at least two times the trace width should be considered and the transmission line should be 'guarded' by ground plane area on each side.
- The characteristic impedance can be calculated as first iteration using tools provided by the layout software. It is advisable to ask the PCB manufacturer to provide the final values that are usually calculated using dedicated software and available stack-ups from production. It could also be possible to request an impedance coupon on panel's side to measure the real impedance of the traces.
- FR-4 dielectric material, although its high losses at high frequencies can be considered in RF designs providing that :
    - RF trace length must be minimized to reduce dielectric losses.
    - If traces longer than few centimeters are needed, it is recommended to use a coaxial connector and cable to reduce losses
    - Stack-up should allow for thick 50 Ω traces and at least 200 µm trace width is recommended to assure good impedance control over the PCB manufacturing process.
    - FR-4 material exhibits poor thickness stability and thus less control of impedance over the trace length. Contact the PCB manufacturer for specific tolerance of controlled impedance traces.
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: route RF lines in 45 ° angle or in arcs.
- Add GND stitching vias around transmission lines.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer.
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit to avoid crosstalk between RF traces and Hi-impedance or analog signals.
- Avoid stubs on the transmission lines, any component on the transmission line should be placed with the connected pad over the trace. Also avoid any unnecessary component on RF traces.

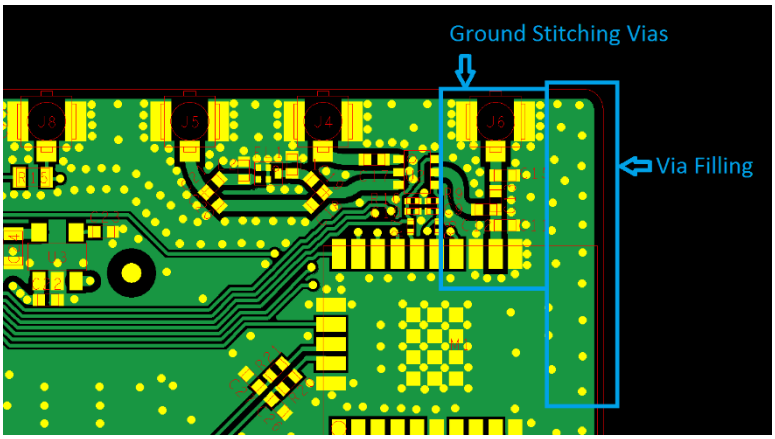


Figure 11: Example of RF trace and ground design from LILY-W1 Evaluation Kit (EVK)

3.2.2 Antenna design (NINA-B111 only)

Designers must take care of the antennas from all perspective at the beginning of the design phase when the physical dimensions of the application board are under analysis/decision as the RF compliance of the device integrating NINA-B1 module with all the applicable required certification schemes heavily depends on the radiating performance of the antennas. The designer is encouraged to consider one of the u-blox suggested antenna part numbers and follow the layout requirements.

- External antennas such as linear monopole:
  - External antennas basically do not imply physical restriction to the design of the PCB where the module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected with minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces radiation performance.
  - A high quality 50 Ω coaxial connector provides proper PCB-to-RF-cable transition.
- Integrated antennas such as patch-like antennas:
  - Internal integrated antennas imply physical restriction to the PCB design:

    Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane related to the antenna element must be considered.

    The RF isolation between antennas in the system has to be as high as possible and the correlation between the 3D radiation patterns of the two antennas has to be as low as possible. In general, an RF separation of at least a quarter wavelength between the two antennas is required to achieve a maximum isolation and low pattern correlation; increased separation should be considered if possible, to maximize the performance and fulfil the requirements in Table 8.

    As numerical example, the physical restriction to the PCB design can be considered as shown below:

    Frequency = 2.4 GHz → Wavelength = 12.5 cm → Quarter wavelength = 3.125 cm[1]
  - Radiation performance depends on the whole product and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.

[1] Wavelength referred to a signal propagating over the air.

Table 8 summarizes the requirements for the antenna RF interface.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** pin.
Frequency Range	2400 - 2500 MHz	Bluetooth low energy.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the primary antenna RF connection matches the 50 Ω characteristic impedance of the **ANT** pin. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT** pin over the operating frequency range thus, maximizing the amount of the power transferred to the antenna.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to the antenna input; the efficiency is a measure of how well an antenna receives or transmits.
Maximum Gain	Refer to Section 5	The maximum antenna gain must not exceed the value specified in type approval documentation to comply with the radiation exposure limits specified by regulatory agencies.

Table 8: Summary of antenna interface (ANT) requirements for NINA-B1

In both the cases, while selecting external or internal antennas, the following recommendations should be observed:

- Select antennas that provide optimal return loss (or VSWR) figure over all the operating frequencies.
- Select antennas that provide optimal efficiency figure over all the operating frequencies.
- Select antennas that provide appropriate gain figure (that is, combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity does not exceed the regulatory limits specified in some countries (for example, by FCC in the United States).

3.2.2.1 RF Connector Design

If an external antenna is required, the designer should consider using a proper RF connector. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

Table 9 suggests some RF connector plugs that can be used by the designers to connect RF coaxial cables based on the declaration of the respective manufacturers. The Hirose U.FL-R-SMT RF receptacles (or similar parts) require a suitable mated RF plug from the same connector series. Due to wide usage of this connector, several manufacturers offer compatible equivalents.

Manufacturer	Series	Remarks
Hirose	U.FL® Ultra Small Surface Mount Coaxial Connector	Recommended
I-PEX	MHF® Micro Coaxial Connector	
Tyco	UMCC® Ultra-Miniature Coax Connector	
Amphenol RF	AMC® Amphenol Micro Coaxial	
Lighthorse Technologies, Inc.	IPX ultra micro-miniature RF connector	

Table 9: U.FL compatible plug connector

Typically, the RF plug is available as a cable assembly. Different types of cable assembly are available; the user should select the cable assembly best suited to the application. The key characteristics are:

- RF plug type: select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: Typically from 0.8 mm to 1.37 mm. Select thicker cables to minimize insertion loss.
- Cable length: Standard length is typically 100 mm or 200 mm; custom lengths may be available on request. Select shorter cables to minimize insertion loss.
- RF connector on the other side of the cable: for example another U.FL (for board-to-board connection) or SMA (for panel mounting)

Consider that SMT connectors are typically rated for a limited number of insertion cycles. In addition, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect U.FL connector to a more robust connector such as SMA fixed on panel.

☞ A de-facto standard for SMA connectors implies the usage of reverse polarity connectors (RP-SMA) on Wi-Fi and Bluetooth end products to increase the difficulty for the end user to replace the antenna with higher gain versions and exceed regulatory limits.

The following recommendations apply for proper layout of the connector:

- Strictly follow the connector manufacturer's recommended layout:
  - SMA Pin-Through-Hole connectors require GND keep-out (that is, clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts.
  - UFL surface mounted connectors require no conductive traces (that is, clearance, a void area) in the area below the connector between the GND land pads.
- If the connector's RF pad size is wider than the micro strip, remove the GND layer beneath the RF connector to minimize the stray capacitance thus keeping the RF line 50 Ω. For example, the active pad of the UF.L connector must have a GND keep-out (that is, clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

3.2.2.2 Integrated antenna design

If integrated antennas are used, the transmission line is terminated by the integrated antennas themselves. The following guidelines should be followed:

- The antenna design process should begin at the start of the whole product design process. Self-made PCBs and antenna assembly are useful in estimating overall efficiency and radiation path of the intended design.
- Use antennas designed by an antenna manufacturer providing the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the related integrated antenna requirements. The ground plane of the application PCB may be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated, however overall antenna efficiency may benefit from larger ground planes.

  Proper placement of the antenna and its surroundings is also critical for antenna performance. Avoid placing the antenna close to conductive or RF-absorbing parts such as metal objects, ferrite sheets and so on as they may absorb part of the radiated power or shift the resonant frequency of the antenna or affect the antenna radiation pattern.
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning/matching to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines and plan the validation activities on the final prototypes like tuning/matching and performance measures (see Table 8).
- RF section may be affected by noise sources like hi-speed digital buses. Avoid placing the antenna close to buses such as DDR or consider taking specific countermeasures like metal shields or ferrite sheets to reduce the interference.

⚠ **Take care of interaction between co-located RF systems like LTE sidebands on 2.4 GHz band. Transmitted power may interact or disturb the performance of NINA-B1 modules.**

3.2.3 On-board antenna design (NINA-B112 only)

Keep a minimum clearance of 5 mm between the antenna and the casing. Keep a minimum of 10 mm free space from the metal around the antenna including the area below the antenna. If a metal enclosure is required, NINA-B111 with antenna pin has to be used.

It is recommended to place the NINA-B112 module so that the internal antenna is in the corner of the host PCB (Pin 15/16 should be in the corner) as shown in Figure 12. The antenna side (short side closest to the antenna), positioned along one side of the host PCB ground plane is the second best option. It is beneficial to have a large ground plane on the host PCB and have a good grounding on the NINA-B1 module.

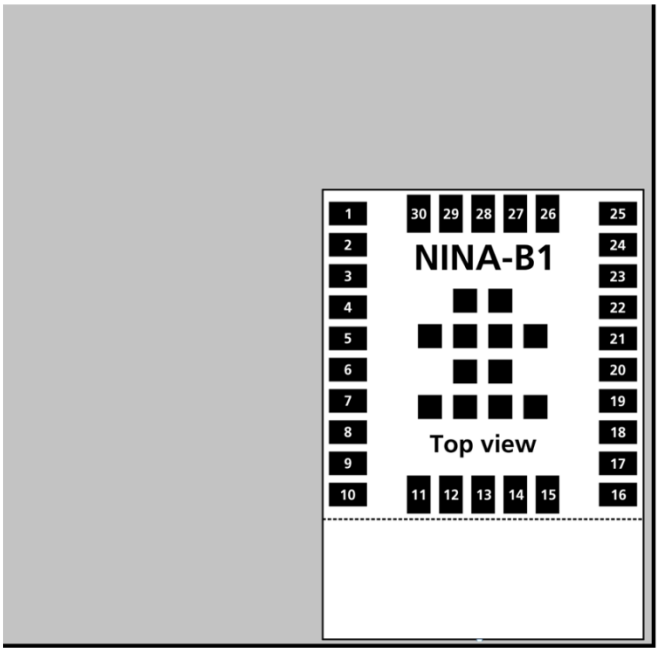


Figure 12: NINA-B112 with internal antenna

Take care when handling the EVK-NINA-B112. Applying force to the NINA-B112 module might damage the internal antenna.

3.3 Supply interfaces

3.3.1 Module supply design

Good connection of the module's VCC pin with DC supply source is required for correct RF performance. The guidelines are summarized below:

- The VCC connection must be as wide and short as possible.
- The VCC connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units. It is a good practice to interpose at least one layer of PCB ground between VCC track and other signal routing.

There is no strict requirement of adding bypass capacitance to the supply net close to the module. But depending on the layout of the supply net and other consumers on the same net, bypass capacitors might still be beneficial. Though the GND pins are internally connected, connect all the available pins to solid ground on the application board, as a good (low impedance) connection to an external ground can minimize power loss and improve RF and thermal performance.

3.4 Data communication interfaces

3.4.1 Asynchronous serial interface (UART) design

The layout of the UART bus should be done so that noise injection and cross talk are avoided.

It is recommended to use the hardware flow control with RTS/CTS to prevent temporary UART buffer overrun.

- If CTS is 1, then the Host/Host Controller is allowed to send.
- If CTS is 0, then the Host/Host Controller is not allowed to send.

3.4.2 Serial peripheral interface (SPI)

The layout of the SPI bus should be done so that noise injection and cross talk are avoided.

3.4.3 I²C interface

The layout of the I²C bus should be done so that noise injection and cross talk are avoided.

3.5 NFC interface

Ensure that the NFC pins are configured correctly. Connecting an NFC antenna to the pins configured as GPIO will damage the module.

The NFC antenna coil must be connected differentially between NFC1 and NFC2 pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz.

The required tuning capacitor value is given by the below equations: An antenna inductance of Lant = 2 µH will give tuning capacitors in the range of 130 pF on each pin. For good performance, match the total capacitance on NFC1 and NFC2.

The NINA-B1 modules have been tested with a 3x3 cm PCB trace antenna, so it is recommended to keep an antenna design close to these measurements. You can still use a smaller or larger antenna as long as it is tuned to resonate at 13.56 MHz. In order to comply with European regulatory demands, the NFC antenna must be placed in such a way that the space between the NINA-B1 module and the remote NFC transmitter is always within 3 meters during transmission.

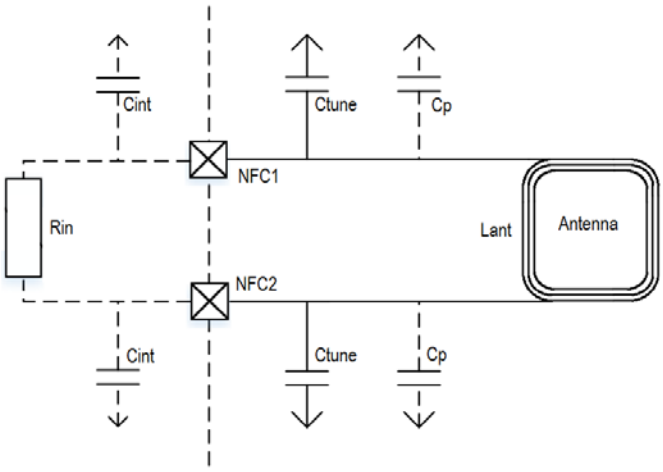


Figure 13: NFC antenna design

$$C'_{tune} = \frac{1}{(2\pi \times 13.56\,MHz)^2 L_{ant}} \quad were\ C'_{tune} = \frac{1}{2} \times \left(C_p + C_{int} + C_{tune}\right)$$

$$C_{tune} = \frac{2}{(2\pi \times 13.56\,MHz)^2 L_{ant}} - C_p - C_{int}$$

3.5.1 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.

3.6 General High Speed layout guidelines

These general design guidelines are considered as best practices and are valid for any bus present in the NINA-B1 series modules; the designer should prioritize the layout of higher speed busses. Low frequency signals are generally not critical for layout.

One exception is represented by High Impedance traces (such as signals driven by weak pull resistors) that may be affected by crosstalk. For those traces, a supplementary isolation of 4w from other busses is recommended.

3.6.1 General considerations for schematic design and PCB floor-planning

- Verify which signal bus requires termination and add series resistor terminations to the schematics.
- Carefully consider the placement of the module with respect to antenna position and host processor.
- Verify with PCB manufacturer allowable stack-ups and controlled impedance dimensioning.
- Verify that the power supply design and power sequence are compliant with NINA-B1 series module specification (refer to section 1.3).

3.6.2 Module placement

- Accessory parts like bypass capacitors should be placed as close as possible to the module to improve filtering capability, prioritizing the placement of the smallest size capacitor close to module pads.

Particular care should be taken not to place components close to the antenna area. The designer should carefully follow the recommendations from the antenna manufacturer about the distance of the antenna vs. other parts of the system. The designer should also maximize the distance of the antenna to Hi-frequency busses like DDRs and related components or consider an optional metal shield to reduce interferences that could be picked up by the antenna thus reducing the module's sensitivity.

- An optimized module placement allows better RF performance. See Antenna interfaces section for more information on antenna consideration during module placement.

3.6.3 Layout and manufacturing

- Avoid stubs on high speed signals. Even through-hole vias may have an impact on signal quality.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length; longer traces will degrade signal performance. Ensure that maximum allowable length for high speed busses is not exceeded.
- Ensure that you track your impedance matched traces. Consult with your PCB manufacturer early in the project for proper stack-up definition.
- RF and digital sections should be clearly separated on the board.
- Ground splitting is not allowed below the module.
- Minimize bus length to reduce potential EMI issues from digital busses.
- All traces (including low speed or DC traces) must couple with a reference plane (GND or power); Hi-speed busses should be referenced to the ground plane. In this case, if the designer needs to change the ground reference, an adequate number of GND vias must be added in the area of transition to provide a low impedance path between the two GND layers for the return current.
- Hi-Speed busses are not allowed to change reference plane. If a reference plane change is unavoidable, some capacitors should be added in the area to provide a low impedance return path through the different reference planes.
- Trace routing should keep a distance greater than 3w from the ground plane routing edge.
- Power planes should keep a distance from the PCB edge sufficient to route a ground ring around the PCB, the ground ring must then be connected to other layers through vias.

3.7 Module footprint and paste mask

The mechanical outline of the NINA-B1 series module can be found in the *NINA-B1 series Data Sheet [2]*. The proposed land pattern layout reflects the pads layout of the module.

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, which implements the solder mask opening 50 µm larger per side than the corresponding copper pad.

The suggested paste mask layout for the NINA-B1 series modules is to follow the copper mask layout as described in *NINA-B1 series Data Sheet [2]*.

These are recommendations only and not specifications. The exact mask geometries, distances, and stencil thicknesses must be adapted to the specific production processes of the customer.

3.8 Thermal guidelines

The NINA-B1 series modules have been successfully tested in -40 °C to +85 °C. The NINA-B1 series module is a low power device and will generate only a small amount of heat during operation. A good grounding should still be observed for temperature relief during high ambient temperature.

3.9 ESD guidelines

The immunity of devices integrating NINA-B1 modules to Electro-Static Discharge (ESD) is part of the Electro-Magnetic Compatibility (EMC) conformity, which is required for products bearing the CE marking, compliant with the R&TTE Directive (99/5/EC), the EMC Directive (89/336/EEC) and the Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with these directives implies conformity to the following European Norms for device ESD immunity: ESD testing standard *CENELEC EN 61000-4-2* and the radio equipment standards *ETSI EN 301 489-1*, *ETSI EN 301 489-7*, *ETSI EN 301 489-24*, the requirements of which are summarized in Table 10.

The ESD immunity test is performed at the enclosure port, defined by *ETSI EN 301 489-1* as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is seen as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

The applicability of ESD immunity test to the whole device depends on the device classification as defined by *ETSI EN 301 489-1*. Applicability of ESD immunity test to the related device ports or the related interconnecting cables to auxiliary equipment, depends on device accessible interfaces and manufacturer requirements, as defined by *ETSI EN 301 489-1*.

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in *CENELEC EN 61000-4-2*.

For the definition of integral antenna, removable antenna, antenna port, device classification refer to the *ETSI EN 301 489-1*. For the contact and air discharges definitions refer to *CENELEC EN 61000-4-2*.

Application	Category	Immunity Level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration	Indirect Contact Discharge	±8 kV

Table 10: Electro-Magnetic Compatibility ESD immunity requirements as defined by CENELEC EN 61000-4-2, ETSI EN 301 489-1, ETSI EN 301 489-7, ETSI EN 301 489-24

NINA-B1 is manufactured taking into account specific standards to minimize the occurrence of ESD events; the highly automated process complies with IEC61340-5-1 (STM5.2-1999 Class M1 devices) standard thus the designer should implement proper measures to protect from ESD events, any pin that may be exposed to the end user.

Compliance with standard protection level specified in EN61000-4-2 can be achieved by including ESD protections in parallel to the line, close to areas accessible by the end user.

4 Handling and soldering

☞ No natural rubbers, hygroscopic materials or materials containing asbestos are employed.

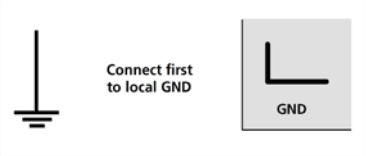
4.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels, tapes or trays, moisture sensitivity levels (MSL), shipment and storage, as well as drying for preconditioning refer to *NINA-B1 series Data Sheet [2]* and *u-blox Package Information Guide [1]*.

4.2 Handling

The NINA-B1 series modules are Electro-Static Discharge (ESD) sensitive devices and require special precautions during handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device
- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10 pF, coax cable ~50-80 pF/m, soldering iron, …)
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).



4.3 Soldering

4.3.1 Reflow soldering process

The NINA-B1 series modules are surface mount modules supplied on a FR4-type PCB with gold plated connection pads and produced in a lead-free process with a lead-free soldering paste. The bow and twist of the PCB is maximum 0.75% according to IPC-A-610E. The thickness of solder resist between the host PCB top side and the bottom side of the NINA-B1 series module must be considered for the soldering process.

The module is compatible with industrial reflow profile for RoHS solders. Use of "No Clean" soldering paste is strongly recommended.

The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. The optimal soldering profile used has to be trimmed for each case depending on the specific process and PCB layout.

Process parameter		Unit	Target
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	T_{SMIN}	°C	150
	T_{SMAX}	°C	200
	t_S (from 25 °C)	s	150
	t_S (Pre-heat)	s	110
Peak	T_L	°C	217
	t_L (time above T_L)	s	90
	T_P (absolute max)	°C	260
	t_P (time above T_P -5 °C)	s	40
Cooling	Ramp-down from T_L	K/s	6
General	$T_{to\ peak}$	s	300
	Allowed soldering cycles	-	1

Table 11: Recommended reflow profile

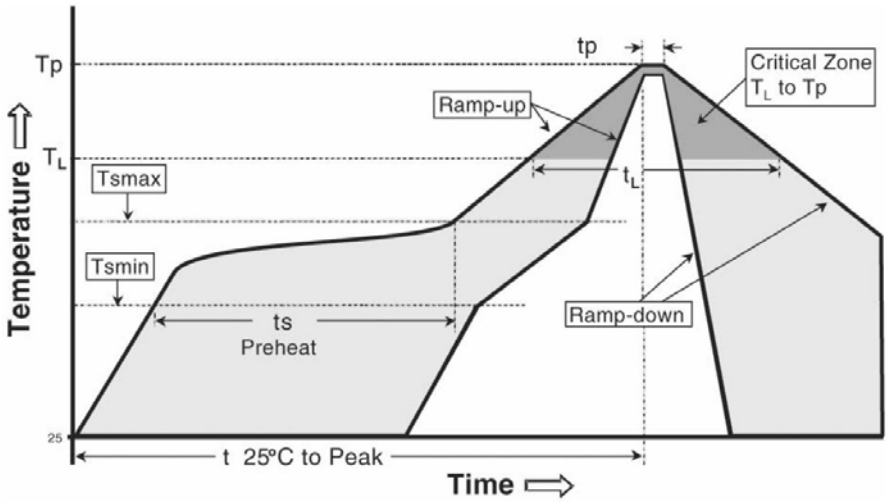


Figure 14: Reflow profile

Lower value of T_P and slower ramp down rate (2 – 3 °C/sec) is preferred.

After reflow soldering, optical inspection of the modules is recommended to verify proper alignment.

Target values in Table 11 should be taken as general guidelines for a Pb-free process. Refer to JEDEC J-STD-020C [7] standard for further information.

4.3.2 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.

- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the crystal oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering process.

4.3.3 Other remarks

- Only a single reflow soldering process is allowed for boards with a module populated on it.
- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices may require wave soldering to solder the THT components. Only a single wave soldering process is allowed for boards populated with the modules. *Miniature Wave Selective Solder* process is preferred over traditional wave soldering process.
- Hand soldering is not recommended.
- Rework is not recommended.
- Conformal coating may affect the performance of the module, it is important to prevent the liquid from flowing into the module. The RF shields do not provide protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating. Conformal coating of the module will void the warranty.
- Grounding metal covers: attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk and will void module's warranty. The numerous ground pins are adequate to provide optimal immunity to interferences.
- The module contains components that are sensitive to Ultrasonic Waves. Use of any ultrasonic processes such as cleaning, welding etc., may damage the module. Use of ultrasonic processes on an end product integrating this module will void the warranty.

5 Qualifications and approvals

For regulatory information, see the *NINA-B1 series Datasheet [2].*

6 Product testing

6.1 u-blox In-Series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically in production line. Stringent quality control process has been implemented in the production line. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment (ATE) in production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. Figure 15 illustrates typical automatic test equipment (ATE) in a production line.

The following tests are performed as part of the production tests:

- Digital self-test (software download, MAC address programming)
- Measurement of currents
- Functional tests
- Digital I/O tests
- Measurement of RF characteristics in all supported bands (such as receiver sensitivity, transmitter power levels and so on.)

Figure 15: Automatic test equipment for module test

6.2 OEM manufacturer production test

As the testing is already done by u-blox, an OEM manufacturer does not need to repeat software tests or measurement of the module's RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damage the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified state can detect a short circuit if compared with a "Golden Device" result.

The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and to perform basic RF performance tests.

6.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test compares the signal quality with a "Golden Device" in a location with known signal quality. This test can be performed after establishing a connection with an external device.

A very simple test can be performed by just scanning for a known Bluetooth low energy device and checking the signal level (Received Signal Strength Indicator (RSSI)).

☞ These kinds of test may be useful as a "go/no go" test but not for RF performance measurements.

This test is suitable to check the functionality of the communication with the host controller and the power supply. It is also a means to verify if components are well soldered.

A basic RF functional test of the device including the antenna can be performed with standard Bluetooth low energy devices as remote stations. The device containing the NINA-B1 series module and the antennas should be arranged in a fixed position inside an RF shield box to prevent interferences from other possible radio devices to get stable test results.

Appendix

A Glossary

Name	Definition
ADC	Analog to Digital Converter
ATE	Automatic Test Equipment
BLE	Bluetooth Low Energy
CLI	Command Line Interface
CTS	Clear To Send
DDR	Dual-Data Rate
EMC	Electro-Magnetic Compatibility
EMI	Electro Magnetic Interference
ESD	Electro Static Discharge
EVK	Evaluation Kit
FCC	Federal Communications Commission
GATT	Generic ATTribute profile
GND	Ground
GPIO	General Purpose Input/Output
IC	Industry Canada
I^2C	Inter-Integrated Circuit
JSON	JavaScript Object Notation
LDO	Low Drop Out
LED	Light-Emitting Diode
MAC	Media Access Control
MSL	Moisture Sensitivity Level
NSMD	Non Solder Mask Defined
PCB	Printed Circuit Board
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Received Signal Strength Indicator
RTS	Request to Send
RXD	Receive Data
SCL	Signal Clock
SDL	Specification and Description Language
SMA	SubMiniature version A
SMD	Solder Mask Defined
SMPS	Switching Mode Power Supply
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
THT	Through-Hole Technology
TXD	Transmit Data
UART	Universal Asynchronous Receiver/Transmitter
VCC	IC power-supply pin

Table 12: Explanation of abbreviations used

B Antenna reference designs

Designers can take full advantage of NINA-B1's *Single-Modular Transmitter certification approval* by integrating the u-blox reference design into their products. This approach requires compliance with the following rules:

- Only listed antennas can be used. Refer to *NINA-B1 series Data sheet [2]* for the listed antennas.
- Schematics and parts used in the design must be identical to u-blox. RF components may show different behavior at the frequencies of interest due to different construction and parasitic, use u-blox's validated parts for antenna matching.
- PCB layout must be identical to the one provided by u-blox, please implement one of the reference designs included in this section or contact u-blox.
- The designer must use the stack-up provided by u-blox. RF traces on the carrier PCB are part of the certified design.

The available designs are presented in this section.

B.1 Reference design for external antennas (U.FL connector)

When using the NINA-B111 together with this antenna reference design, the circuit trace layout must be made in strict compliance with the instructions below.

All the components placed on each RF trace must be kept as indicated in the reference design. The reference design uses a micro coaxial connector that is connected to the external antenna via a 50 Ω pigtail.

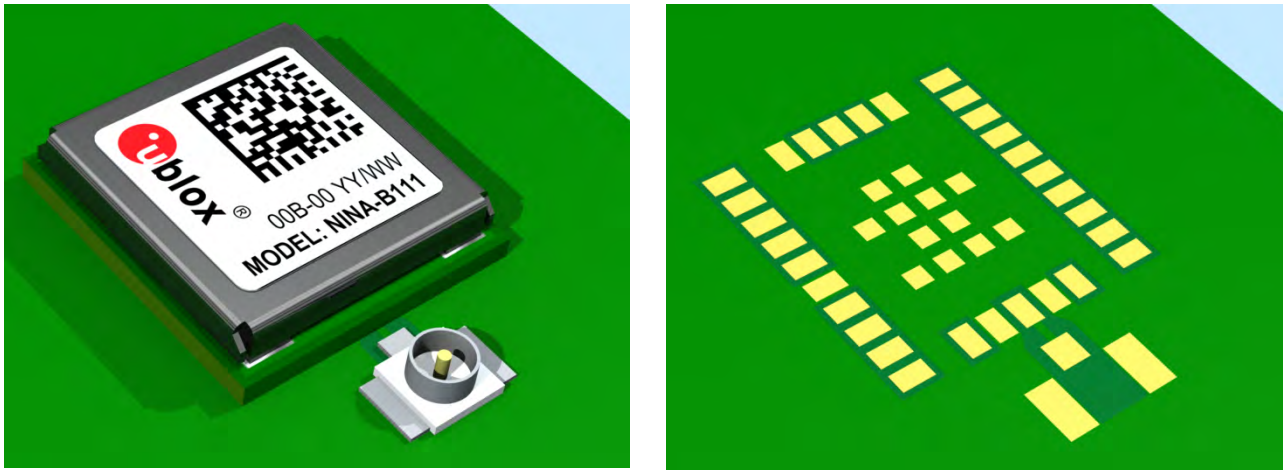


Figure 16: Antenna reference design embedded on a host carrier PCB

B.1.1 Floor plan

This section describes where the critical components and copper traces are positioned on the reference design.

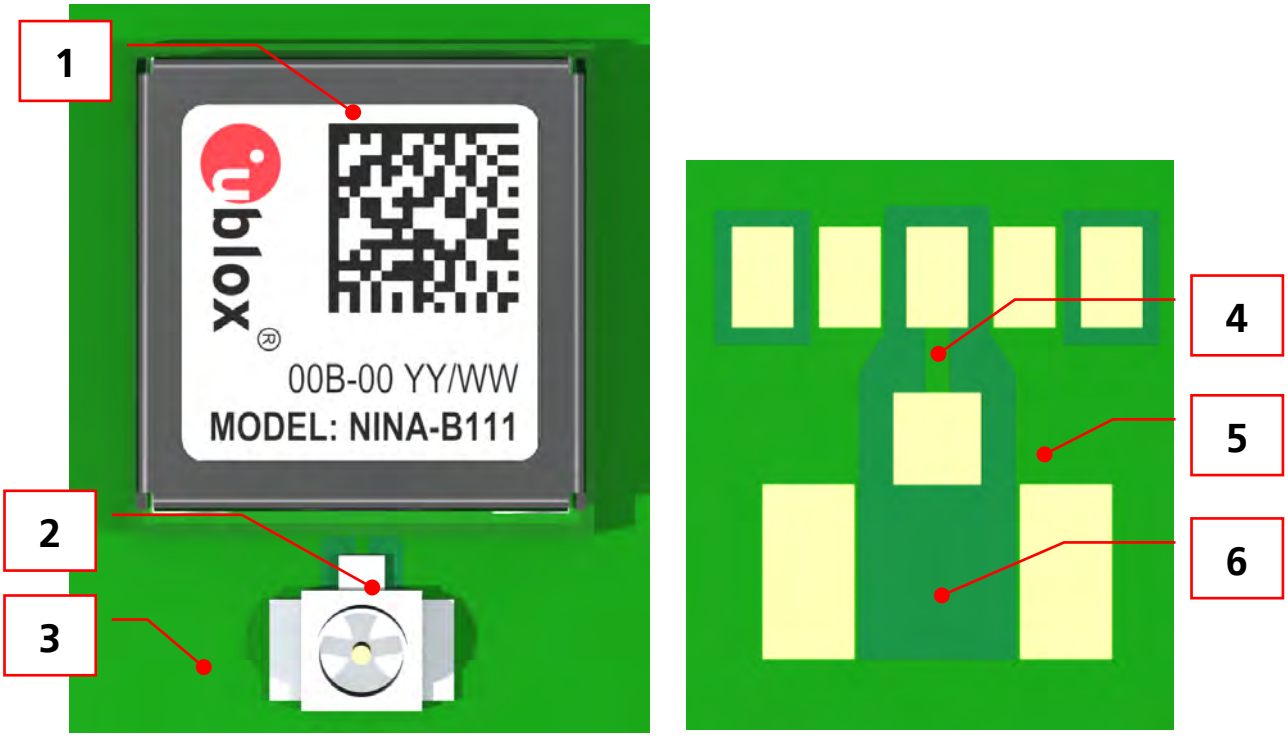


Figure 17: NINA-B111 antenna reference design

Reference	Part	Manufacturer	Description
1	NINA-B111	u-blox	NINA-B111 module
2	U.FL-R-SMT-1(10)	Hirose	Coaxial Connector, 0 – 6 GHz, for external antenna
3	Carrier PCB		Should have a solid GND inner layer under and around the RF components (vias and small openings are allowed).
4	RF trace		Antenna coplanar microstrip, matched to 50 Ω
5	GND trace		(Green) Minimum required top layer GND-trace.
6	Copper keep out		(Dark green) Keep this area free from any copper on the top layer.

Table 13: Included parts in the antenna connector reference design

B.1.2 RF trace specification

The 50 Ω coplanar micro-strip dimensions used in the reference design are stated in Figure 18 and Table 14. The GND plane beneath the RF trace must be intact.

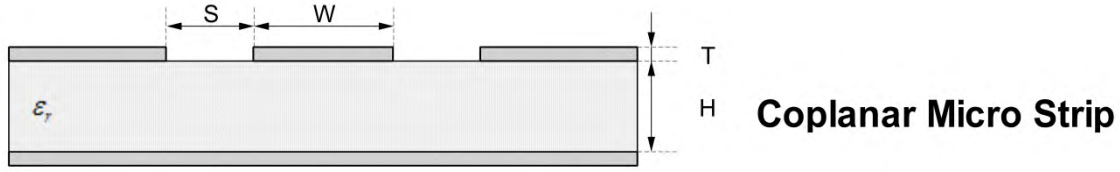


Figure 18: Coplanar micro-strip dimension specification

Item	Value
S	See Figure 19
W	280 µm
T	Soldermask: 20 +/- 10 µm Copper film and plating/surface coating: 35 +/- 15 µm
H	150 +/- 20 µm
ε_r	3.77 +/- 0.5

Table 14: Coplanar micro-strip specification

Figure 19 displays the minimum required GND trace required around the RF trace and pins. GND stitching vias should be used around the RF trace to ensure a proper GND connection. No other components are allowed within this area.

The solid GND layer beneath the 'top layer' shall surround at least the entire RF trace and connector. No signal traces are allowed to be routed on the GND layer within this area but vias and small openings are allowed.

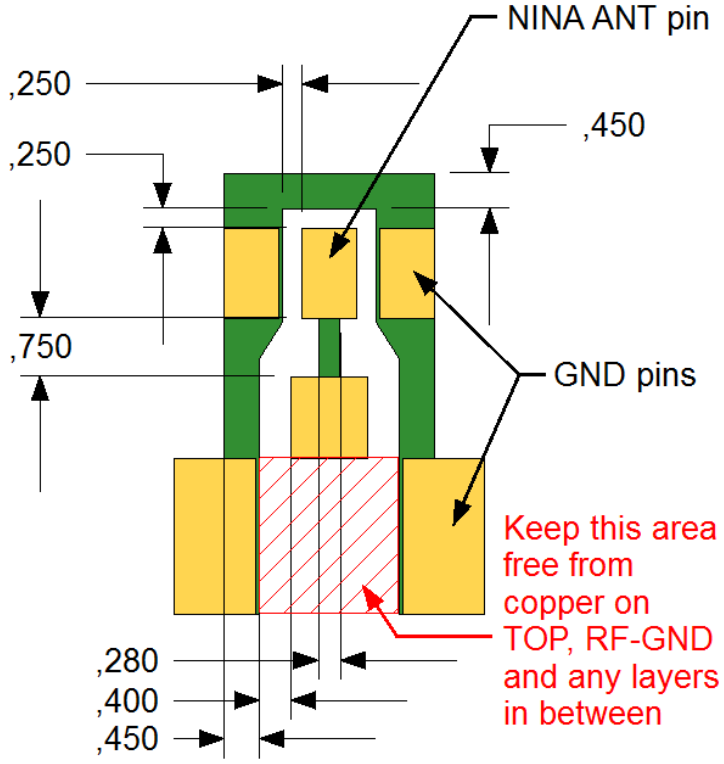


Figure 19: RF trace and minimum required GND trace of the NINA-B111 external antenna reference design

Related documents

[1] u-blox Package Information Guide, document number UBX-14001652

[2] NINA-B1 series Data sheet, document number UBX-15019243

[3] NINA-B1 Getting Started guide, document number UBX-16009942

[4] u-blox Short Range Modules AT Commands Manual, Document No. UBX-14044127

[5] Adding and configuring Mbed targets - https://docs.mbed.com/docs/mbedmicro-api/en/latest/api/md_docs_mbed_targets.html

[6] JEDEC J-STD-020C - Moisture/Reflow Sensitivity Classification for Non Hermetic Solid State Surface Mount Devices.

[7] IEC EN 61000-4-2 - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test

[8] ETSI EN 301 489-1 - Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements

[9] IEC61340-5-1 - Protection of electronic devices from electrostatic phenomena – General requirements

[10] ETSI EN 60950-1:2006 - Information technology equipment – Safety – Part 1: General requirements

[11] FCC Regulatory Information, Title 47 – Telecommunication

[12] JESD51 – Overview of methodology for thermal testing of single semiconductor devices

[13] Nordic Semiconductor Infocenter - http://infocenter.nordicsemi.com/index.jsp

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our website (http://www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	22-Feb-2016	fbro, ajoh, kgom	Initial release.
R02	19-May-2016	fbro	Updated information about reflashing the modules.
R03	15-Jun-2016	fbro, kgom	Updated main feature summary (Table 1). Updated pin-out information (section 1.2.2). Updated flash instructions (section 1.1). Added information about NFC (section 1.8.3 and section 3.5).
R04	8-Sep-2016	fbro, ajoh, kgom	Changed the document status to Early Production Information. Included section 2: Software and Appendix B. Updated section 5. Removed section 1.5.
R05	3-Mar-2017	fbro, apet, mhan, kgom	On page 2, added type numbers for u-blox connectivity software v2.0.0; also replaced Document status with Disclosure restriction. Updated Overview and applications section according to the new features provided with u-blox connectivity software v2.0.0. Added more information in the Software section.
R06	9-Mar-2017	apet, mhan, kgom	Updated the flashing instructions (section 2.3).
R07	16-May-2017	kgom	Minor updates.
R08	29-Jun-2017	fbro, ajoh, kgom	Included support for u-blox connectivity software version 3.0.1. Updated Table 1. Added information about NFC antenna in chapter 3.5. Added more information in the Block Diagram Figure 1). Increased the number of analog capable pins to 8 (previously 7); the new pin was previously intended for another use. Updated the product status to Mass Production. Replaced firmware with software.
R09	24-Nov-2017	lalb, mhan, kgom,	Updated section 1.1 and made a few minor changes in section 6.1. Also updated this document based on the latest brand guidelines of Arm Mbed.

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