Post Lab 2

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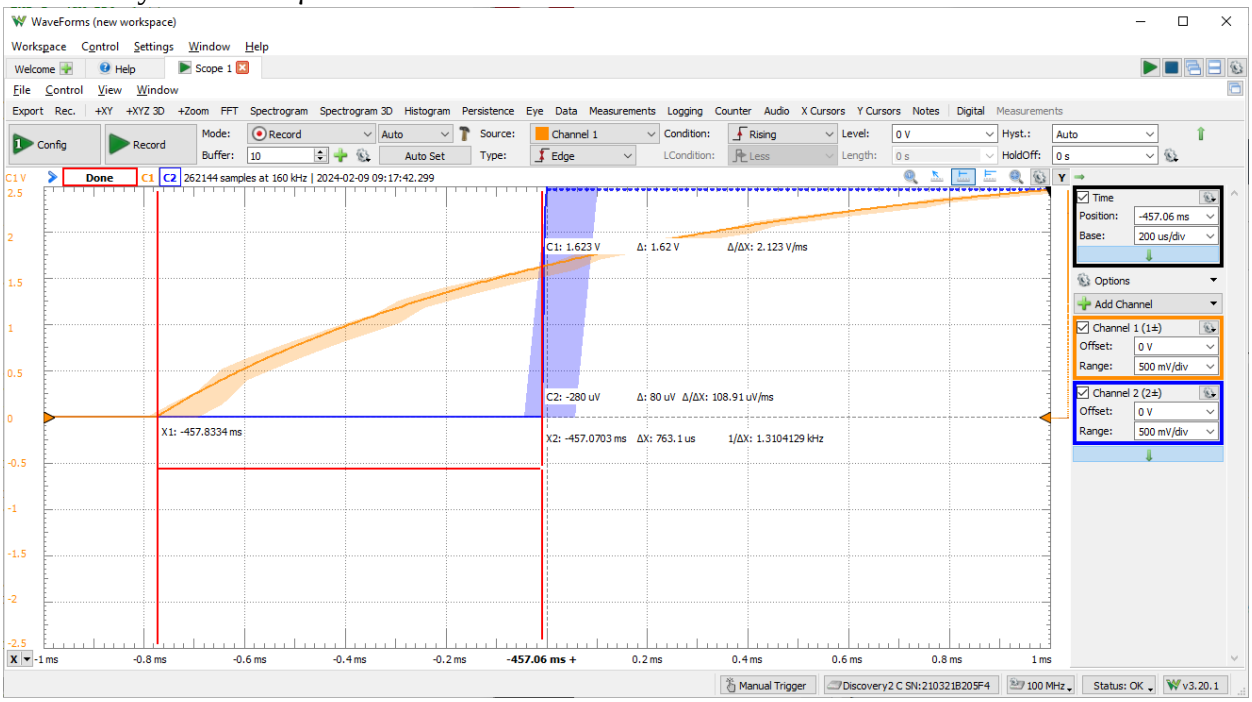
https://github.com/u1252010/ECE-6780-u1252010

1. Because PA0 and PC0 are connected to EXTI0 through the same SYSCFG multiplexer. I would say you can use both pins at the same time, however, both pins will trigger the SAME interrupt and not two different ones.
2. Level 0 is the highest priority and level 3 is the lowest priority.
3. NVIC reserves 8 bits for each interrupt. It only uses 2 of the bits, specifically bits [7:6] in each group, with bits [5:0] being unused.
4. The latency was 763.1 μs



5. Because the status flag indicates when an interrupt is triggered and needs servicing. Without disabling this flag, the processor with think the triggered interrupt needs servicing over and over again ad infinitum.