National Chiao Tung University
Institute of Electronic Engineering

NCTU Mixed-Signal Electronic Design Automation Lab. 2018

CAD HW4 - Modeling Mixed-Signal System and Simulating with AMS

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Date: December 13, 2021

Lab: ED-413

Outline

- Introduction to AMS
- AMS Simulation Setup
  - Analog Simulation with Verilog-A Model
  - Mixed-Signal Behavioral Model Simulation
    - Lab1: Analog Model Simulation with AMS
    - Lab2: Mixed-Signal Model Simulation with AMS
    - Lab3: Modeling Ideal Circuit with Verilog-A

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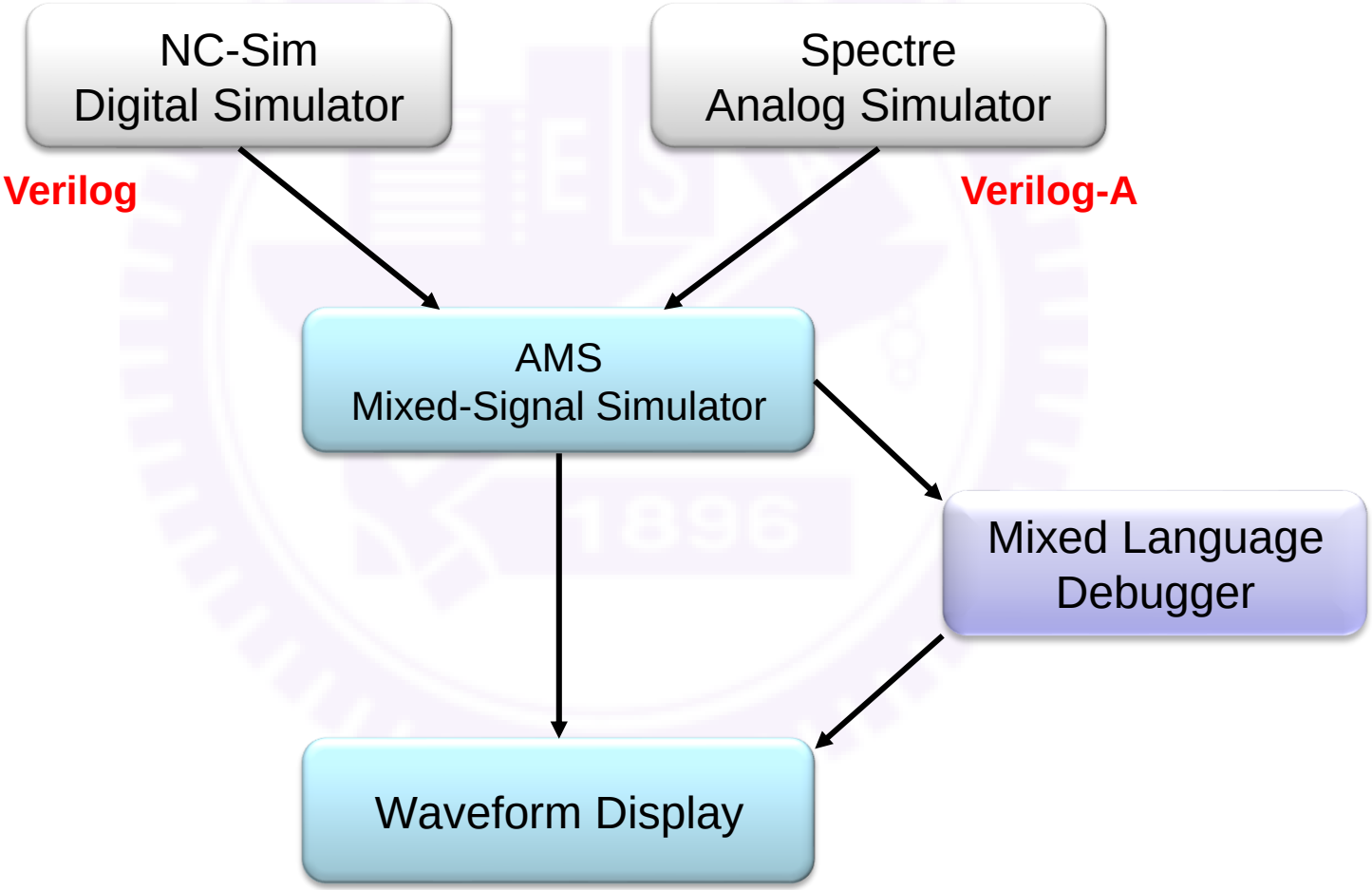
What is AMS Designer

- Top-down system-on-chip simulation for complex mixed-signal designs
- A single executable simulator incorporating the fastest in digital and most flexible analog simulation capability
  - Digital: NC-Sim
  - Analog: Spectre
- Simulation of complex designs incorporating any and all of the following:
  - Verilog, VHDL
  - Verilog-A, Verilog-AMS, VHDL-AMS
  - Spectre
  - SPICE
  - Composer schematics

What is AMS Designer(cont.)



Mixed-Signal Simulation with Model

- The mixed-signal behavioral model simulation can verify:
  - System behavior is correct or not?
  - System requirement is met or not?
  - System performance is satisfied or not?
- Weaknesses:
  - Only time domain information can be obtained directly
    - All behavioral model should be converted into time domain
    - Other characteristics might be calculated from time domain data

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Environment Setting

- NC-Verilog / Verilog-XL
  - e.g > source /usr/cad/cadence/CIC/incisiv.cshrc
- Spectre
  - e.g > source /usr/cad/cadence/CIC/mmsim.cshrc
- Composer / Virtuoso
  - e.g > source /usr/cad/cadence/CIC/ic_06.17.709.cshrc

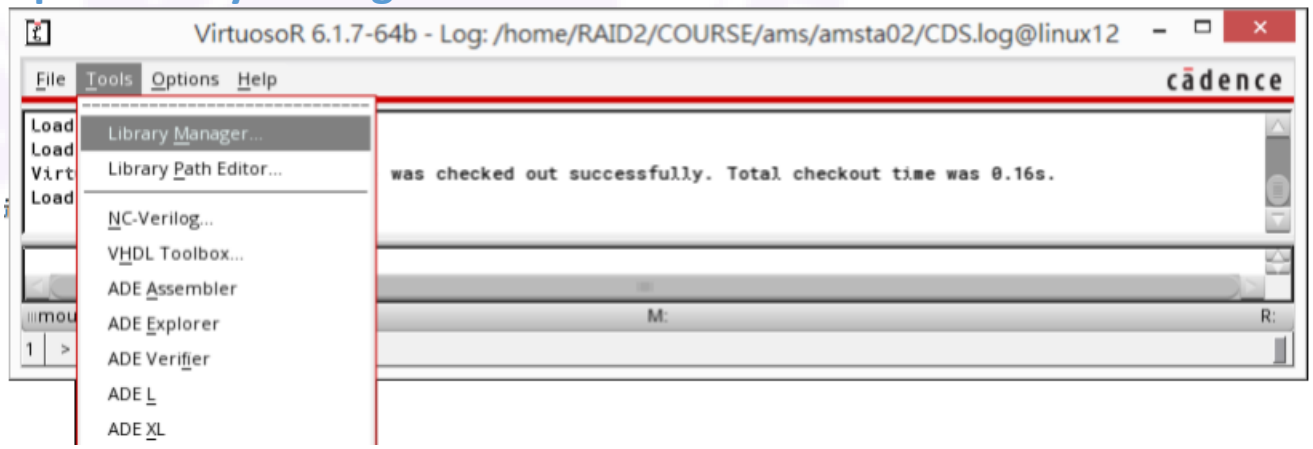
Simulation Flow

Step 1. > virtuoso &

Step 2. Open library manager

- Create library
- Create cell view & symbol
  - Verilog-A models
  - Verilog models
  - Schematic
  - Config
- Set ADE

Open library manager



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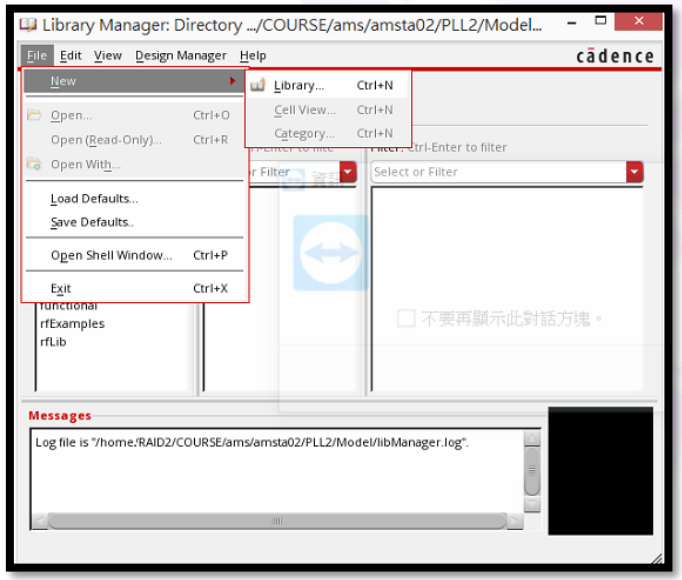
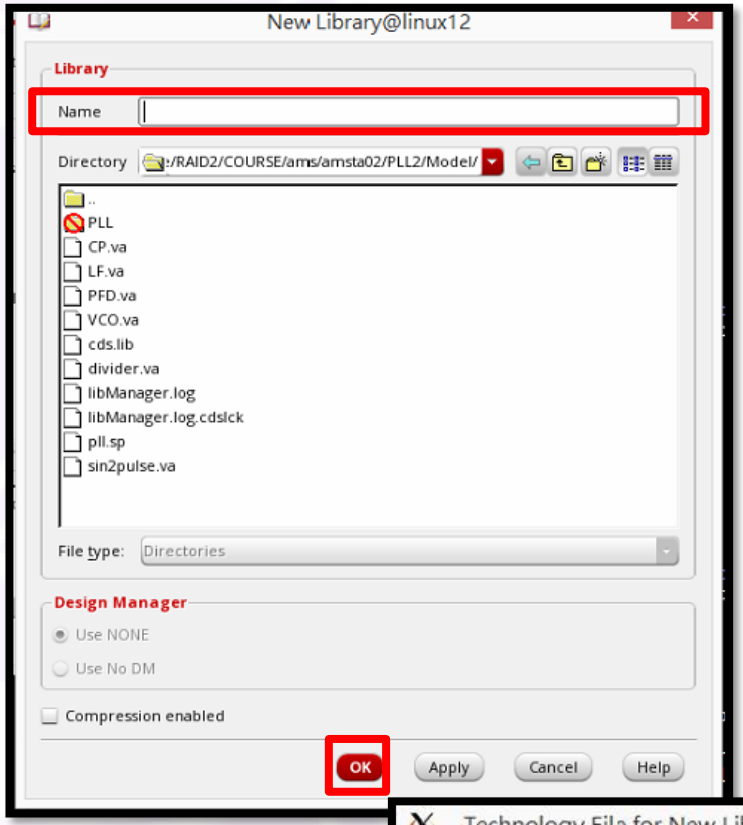
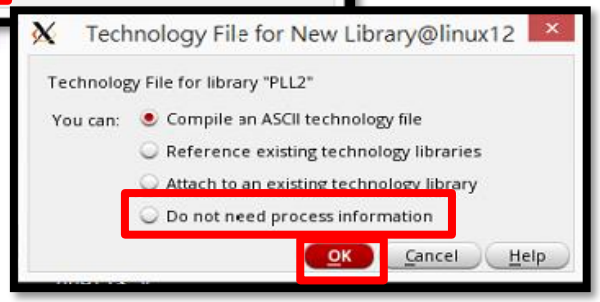


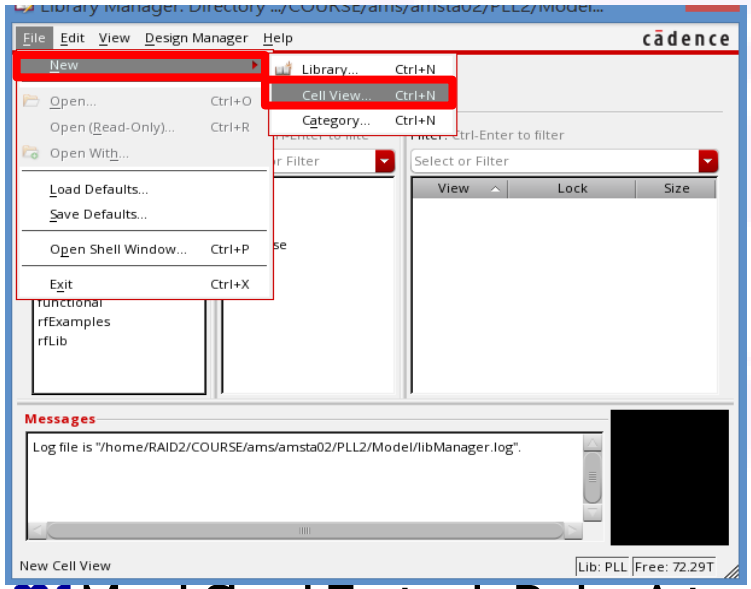


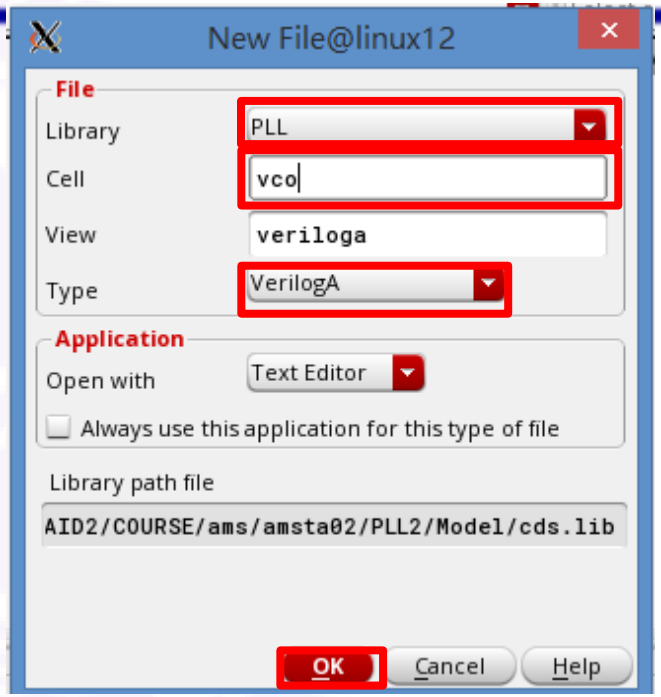


Create Verilog-A Cells

- Create library
- Create cell view & symbol
  - Verilog-A models
  - Verilog models
  - Schematic
  - Config
- Set ADE

Create a new cell view



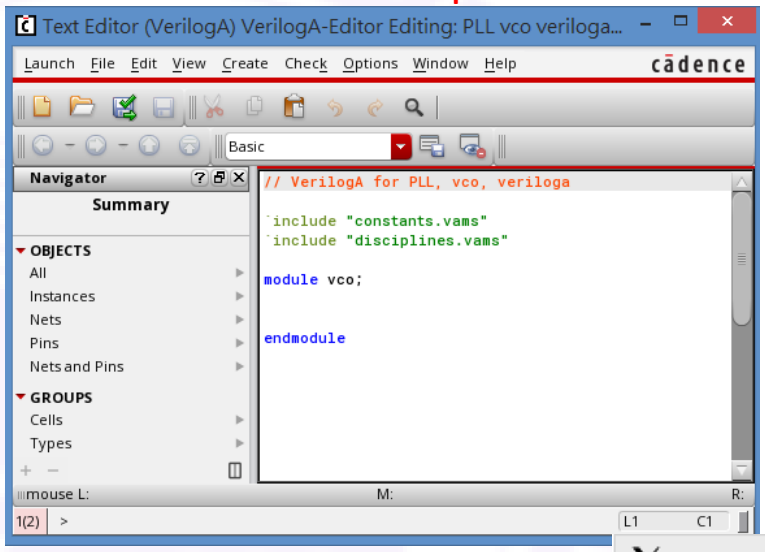


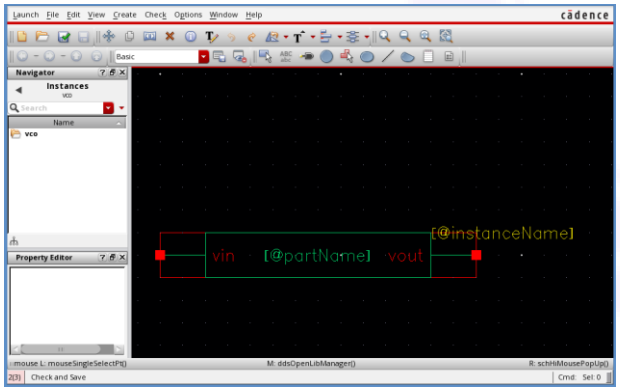
1. Choose your library
2. Input the name on the Cell Name column
3. Choose the **VerilogA** type for Analog model
4. OK

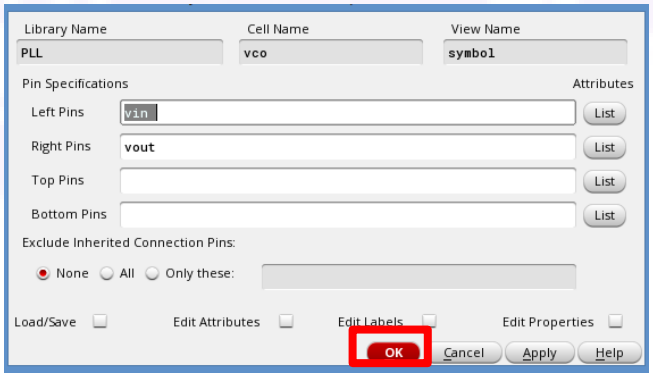
Designing with Verilog-A

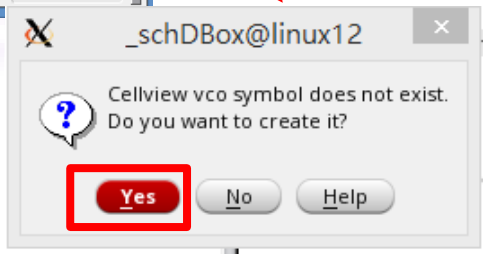
- Create library
- Create cell view & symbol
  - Verilog-A models
  - Verilog models
  - Schematic
  - Config
- Set ADE

Enter behavioral description





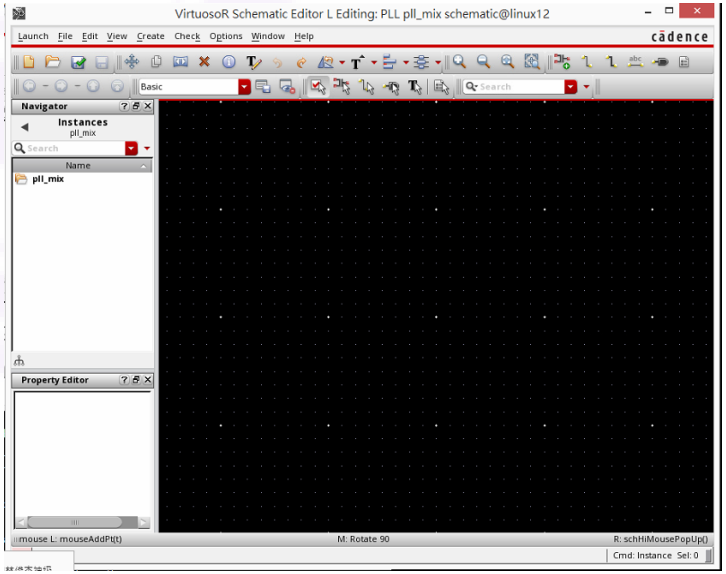




Create Top Cell - Schematic

- Create library
- Create cell view & symbol
  - Verilog-A models
  - Verilog models
  - Schematic
  - Config
- Set ADE

Input the name on the Cell Name column and choose the Schematic



Create Top Cell - Schematic

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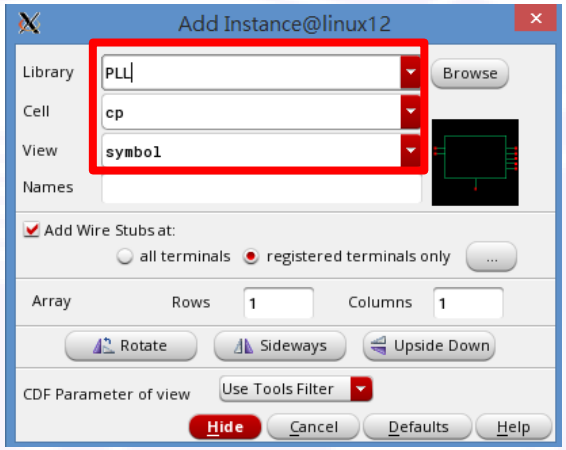
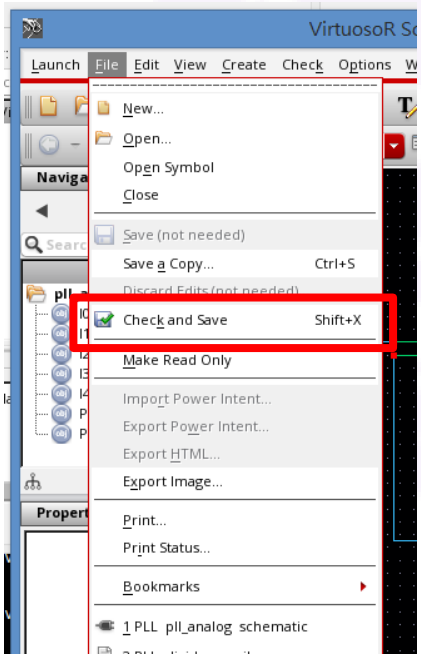
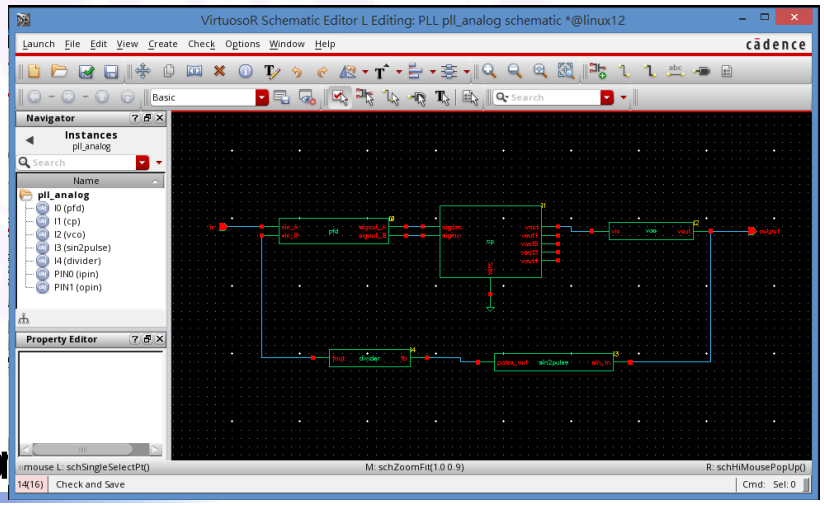
Add Instance: Create→instance (i)



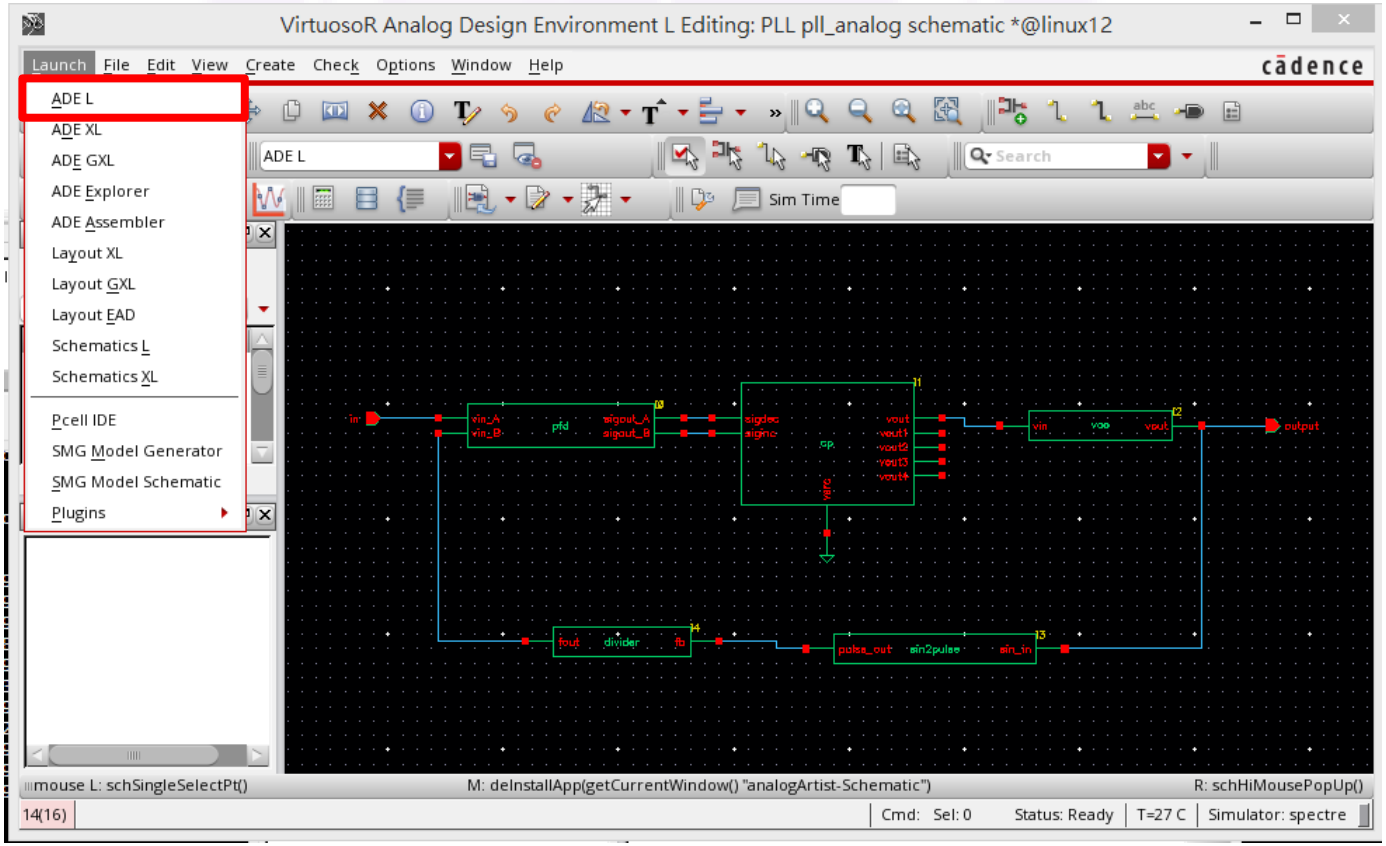


Add connection: Create → wire (w)
Add input/output: Create → pin (p)

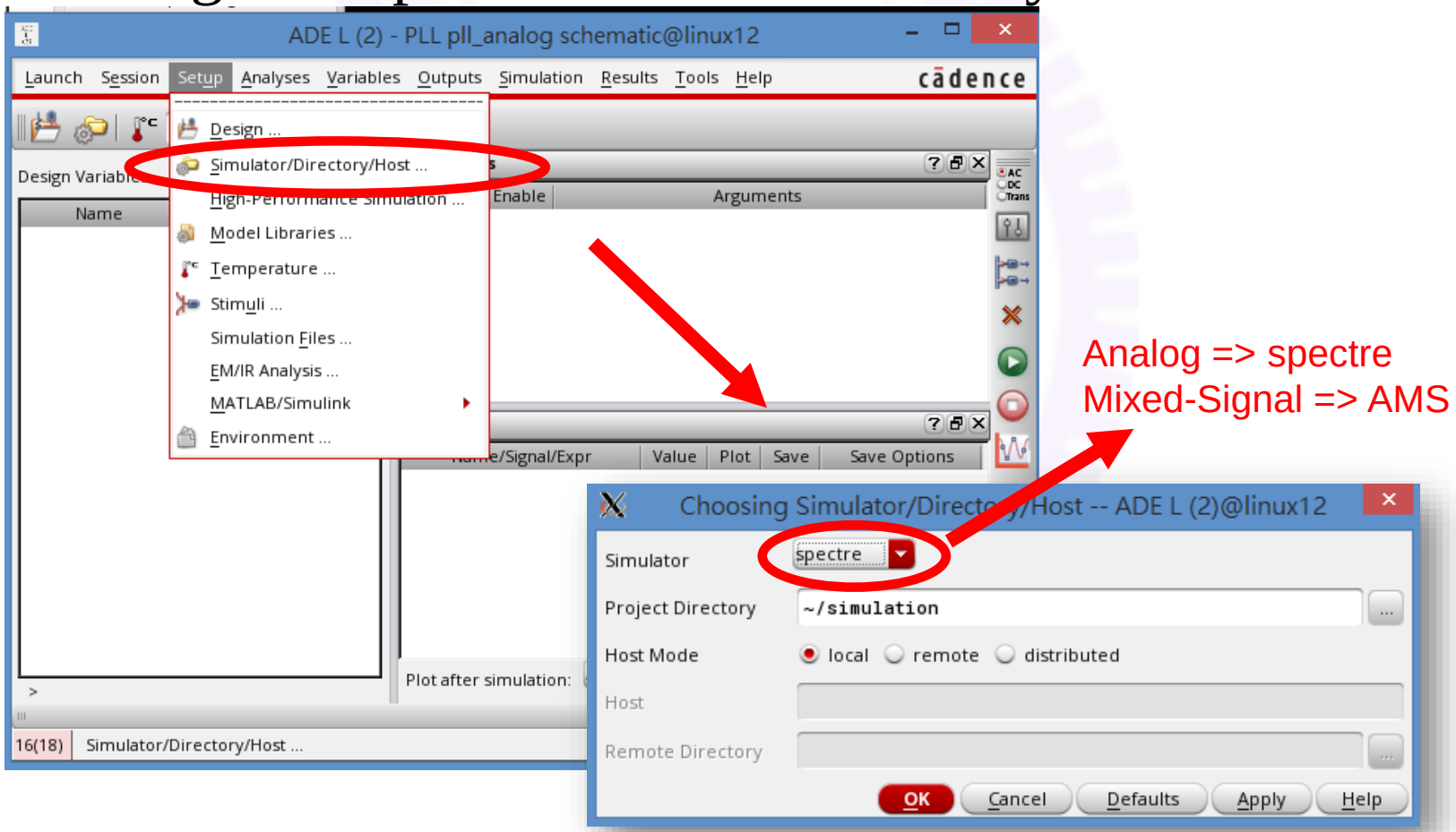


Simulation Environment

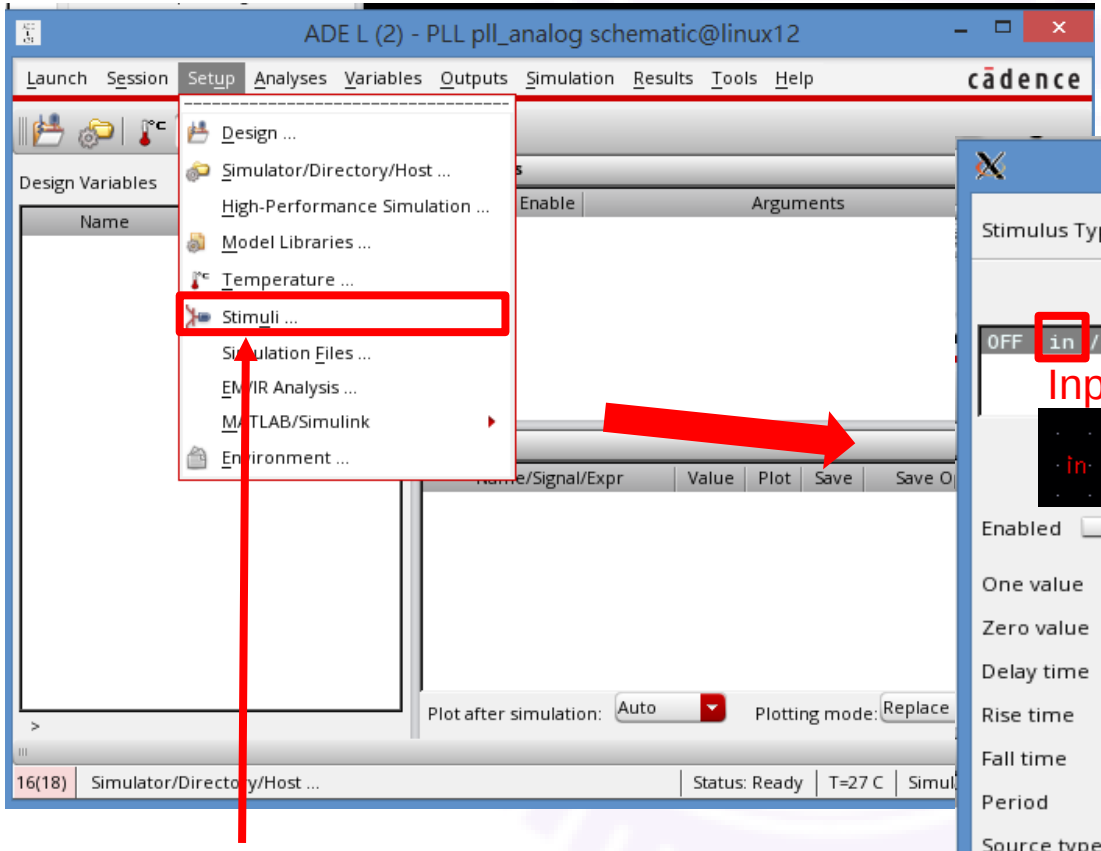
- Open Analog Design Environment (ADE) in schematic editing window

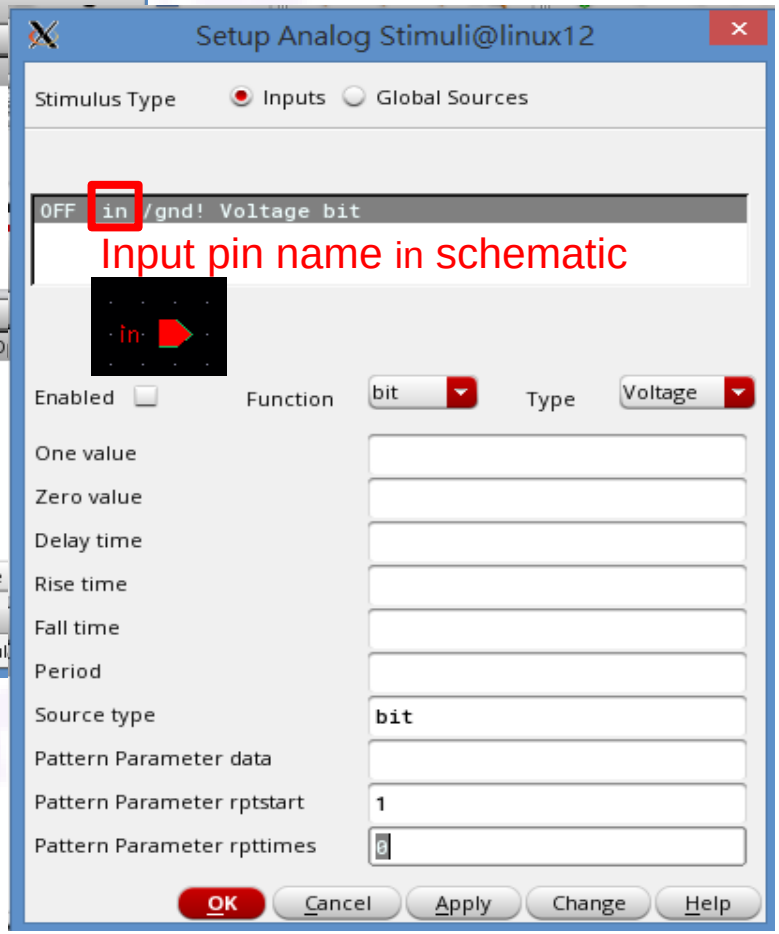


- Through Setup -> Simulator/Directory/Host



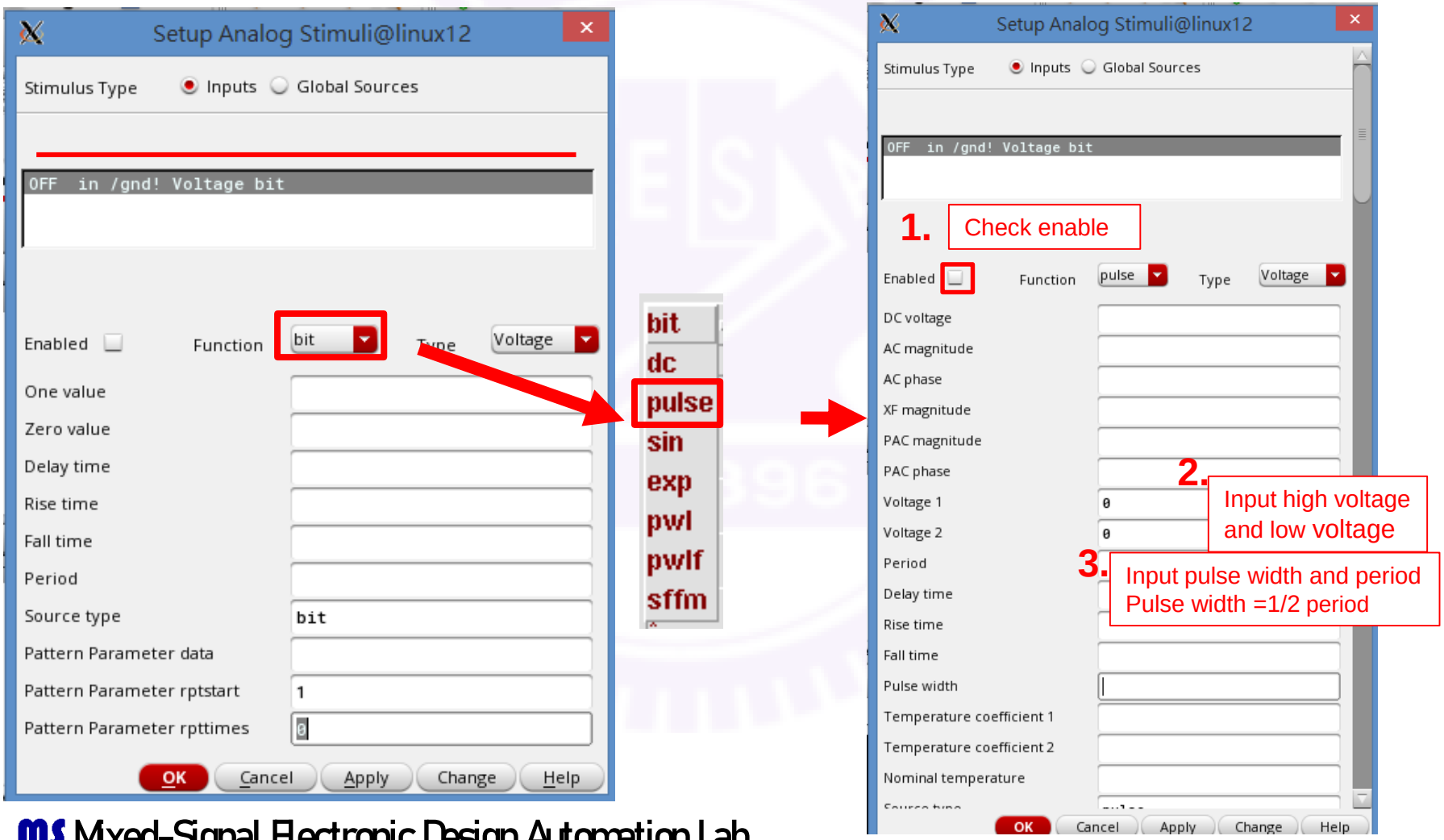
Give input information(1/2)



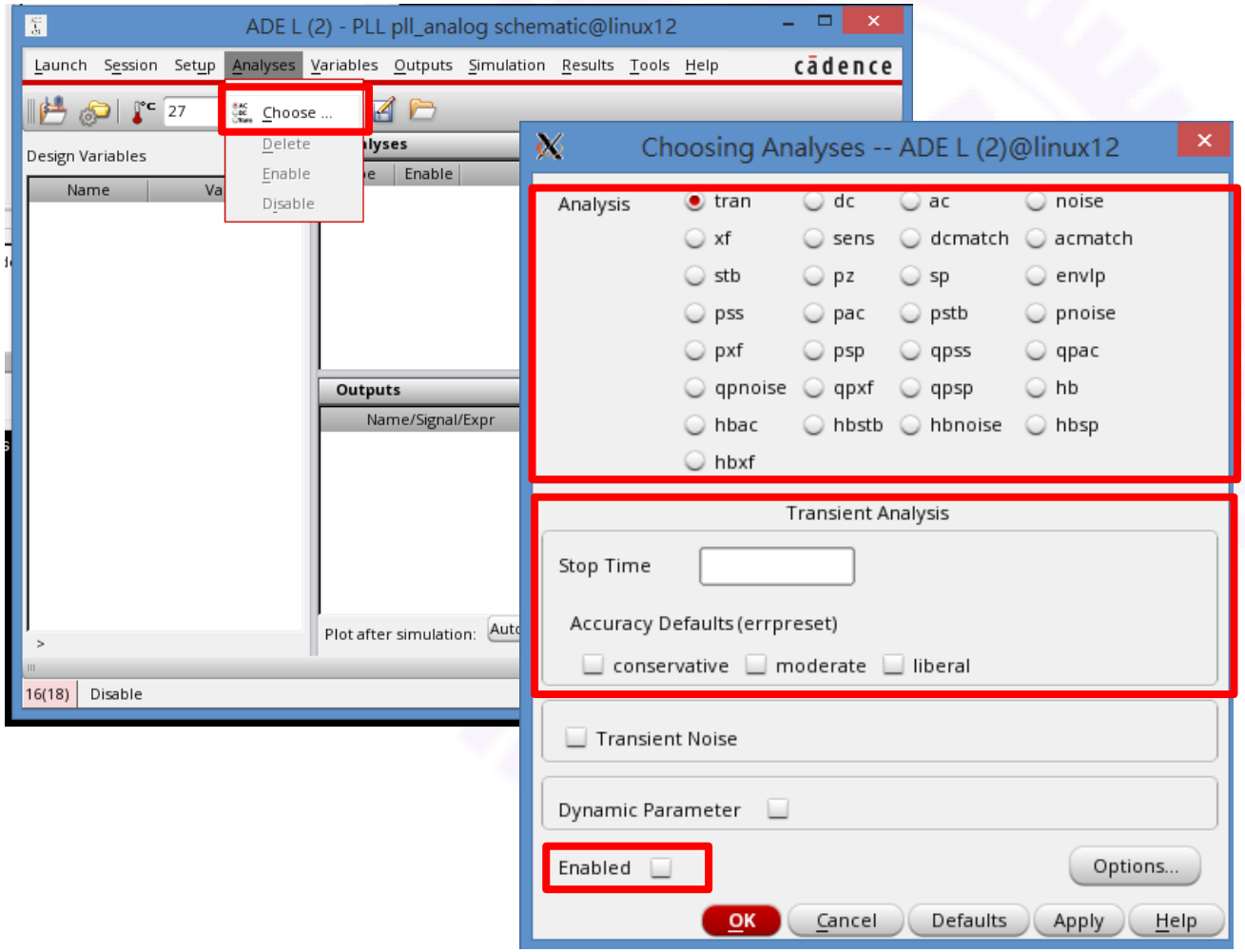


If choose spectre as simulator, there only has stimuli

Give input information(2/2)



Choose Analysis Type

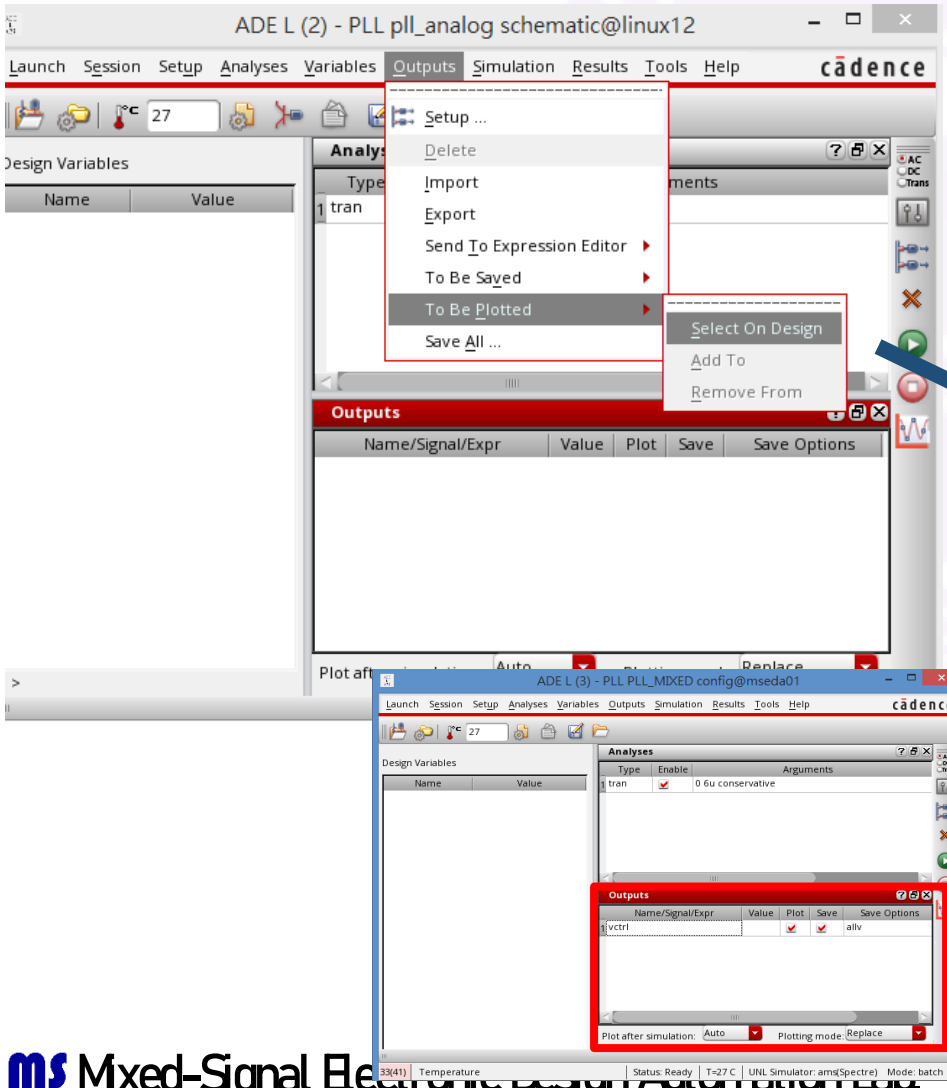


Choose tran analysis

Set the simulation time and the accuracy flag

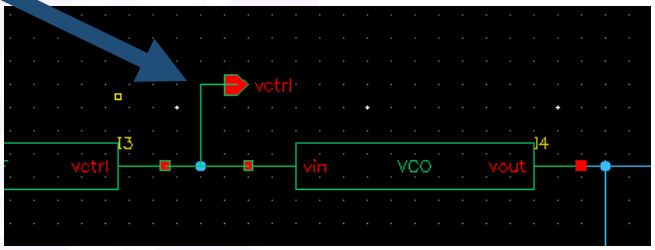
Check enable to simulati

Save Output Nodes



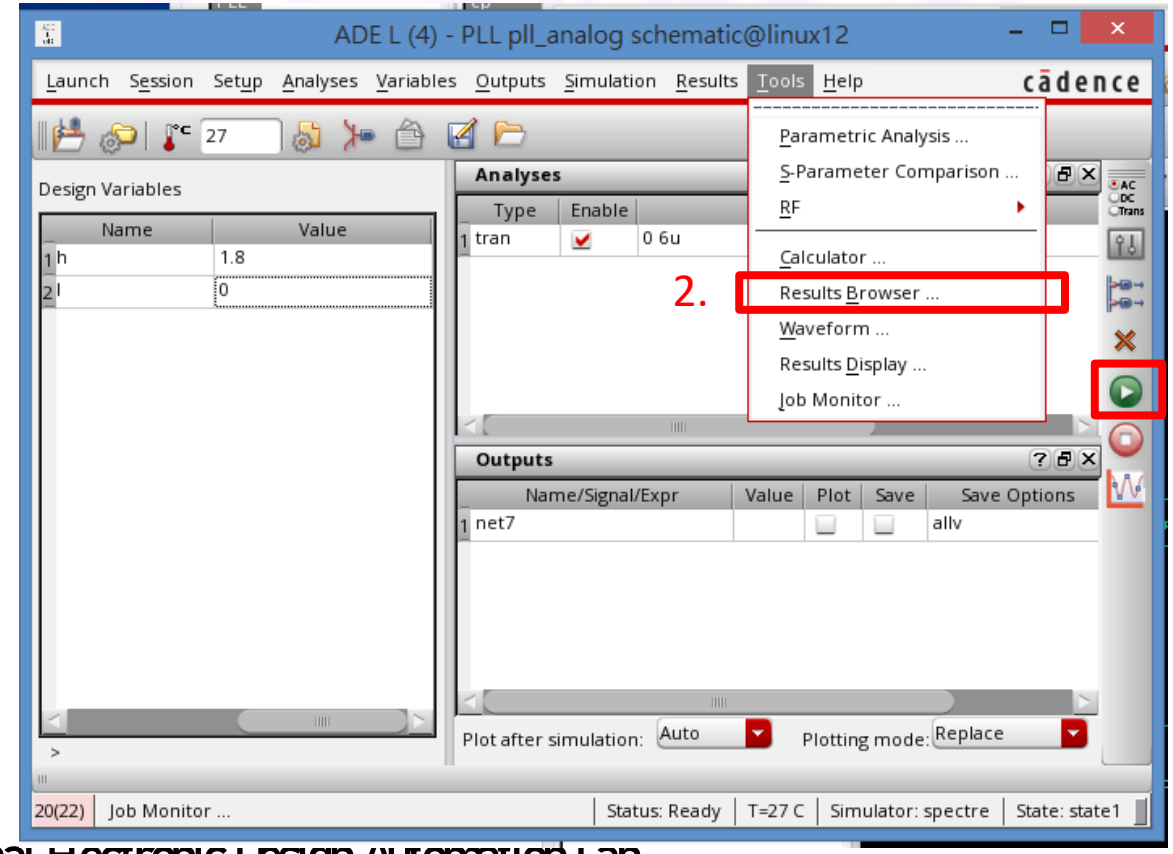
To Be Plotted:

- Select on **line or node**
- Press **Esc** to cancel



Submit the Simulation

- Execute the simulation job with Run
- Tools → Results Brower



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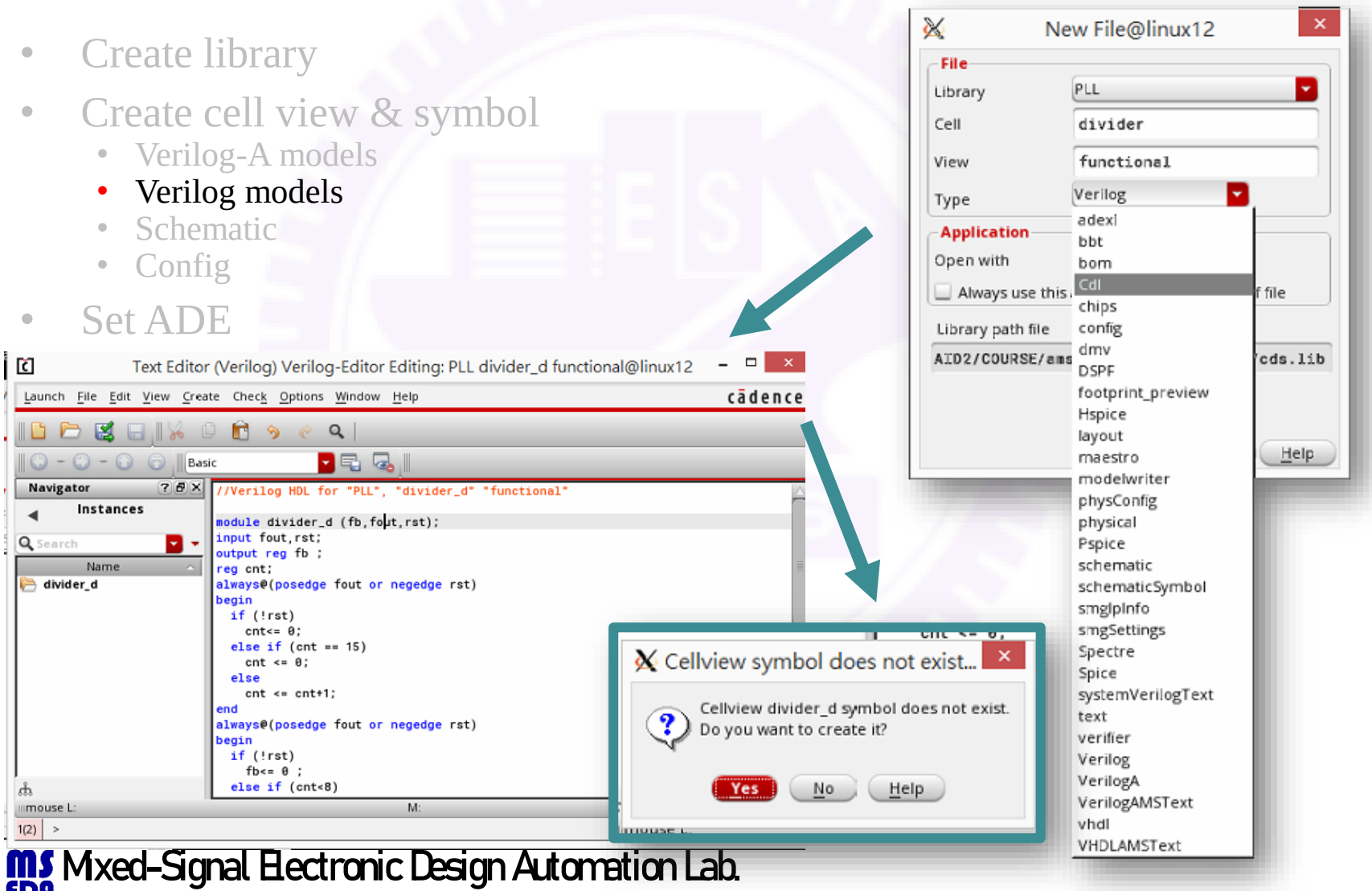
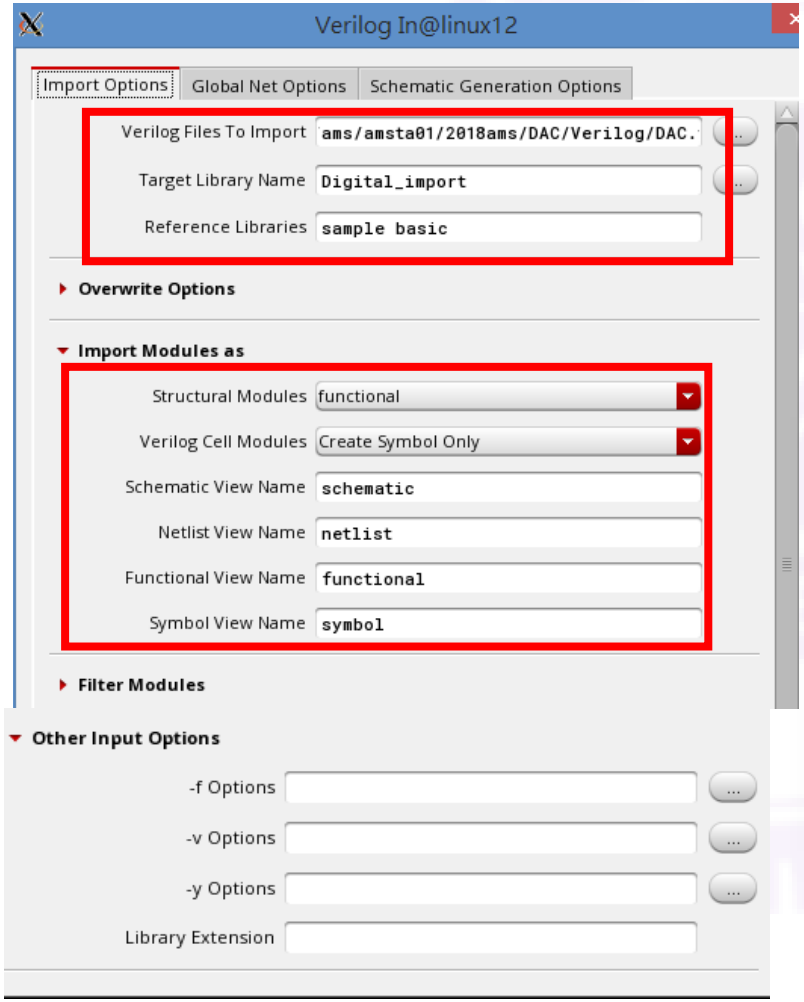
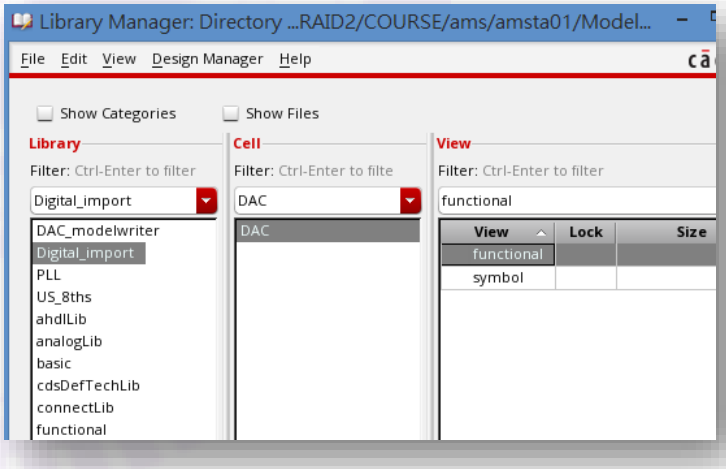


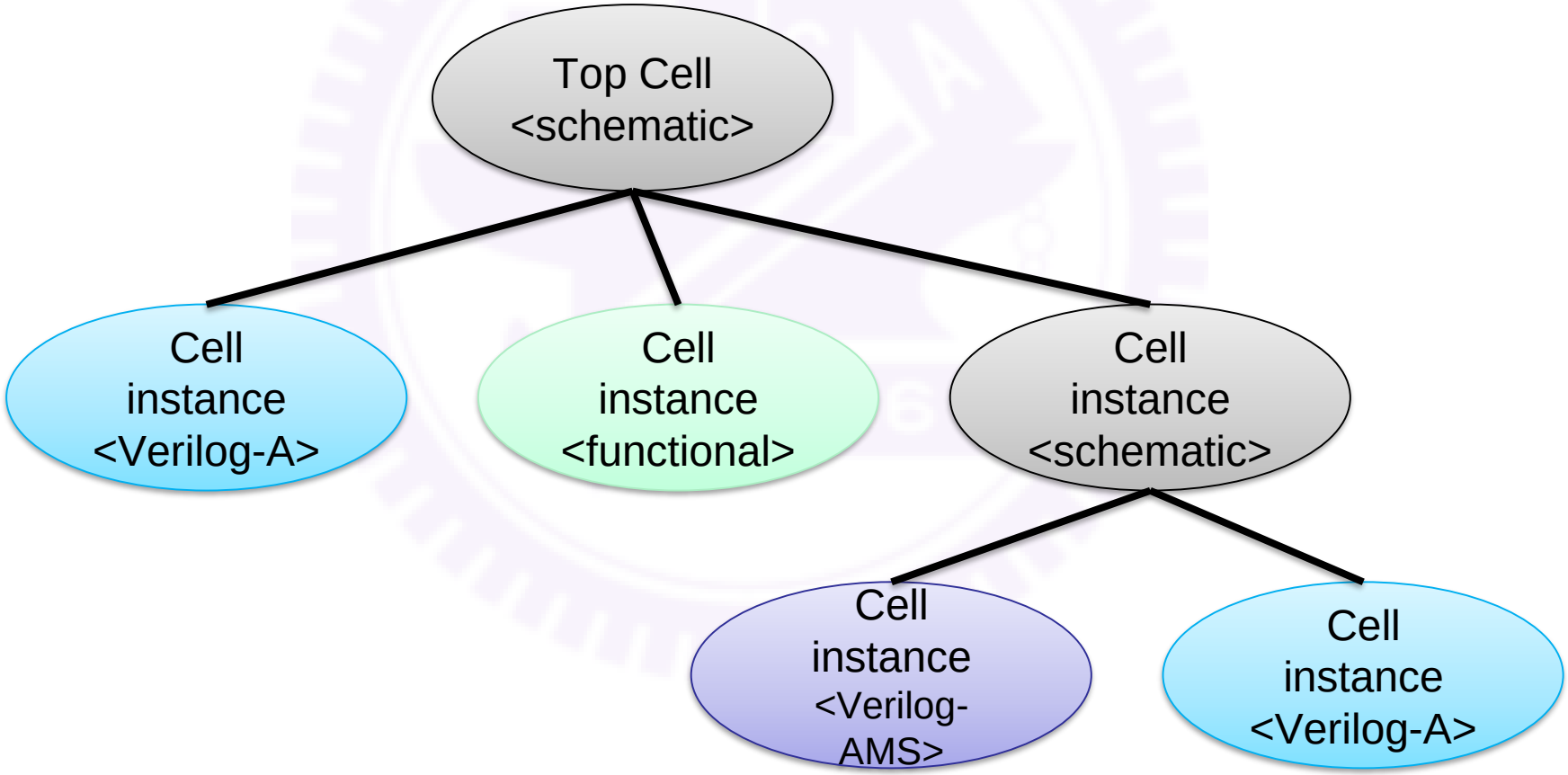
Import Digital Design





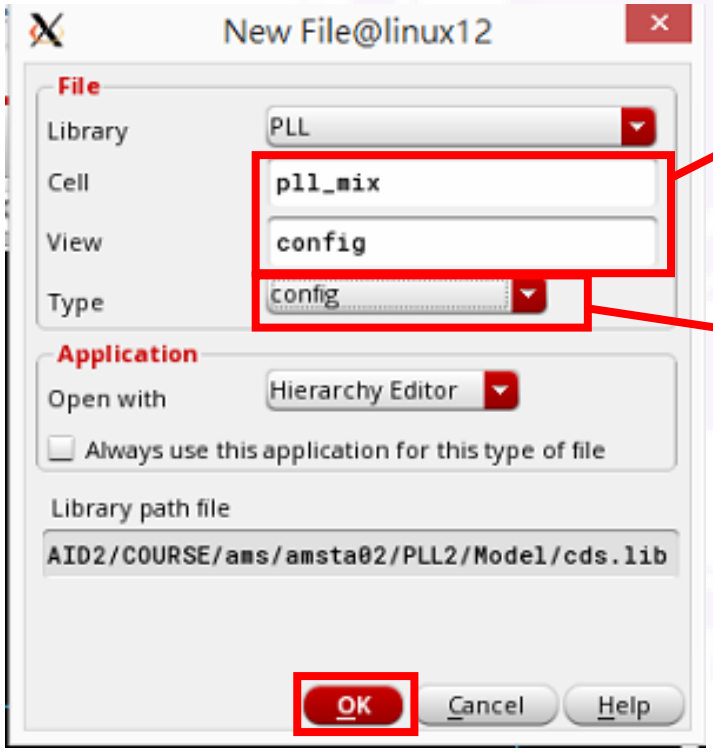
Design Hierarchy – AMS

- Before creating the top schematic cell (add instance and connection), creating a config view for AMS simulation



Create Config View for Simulation

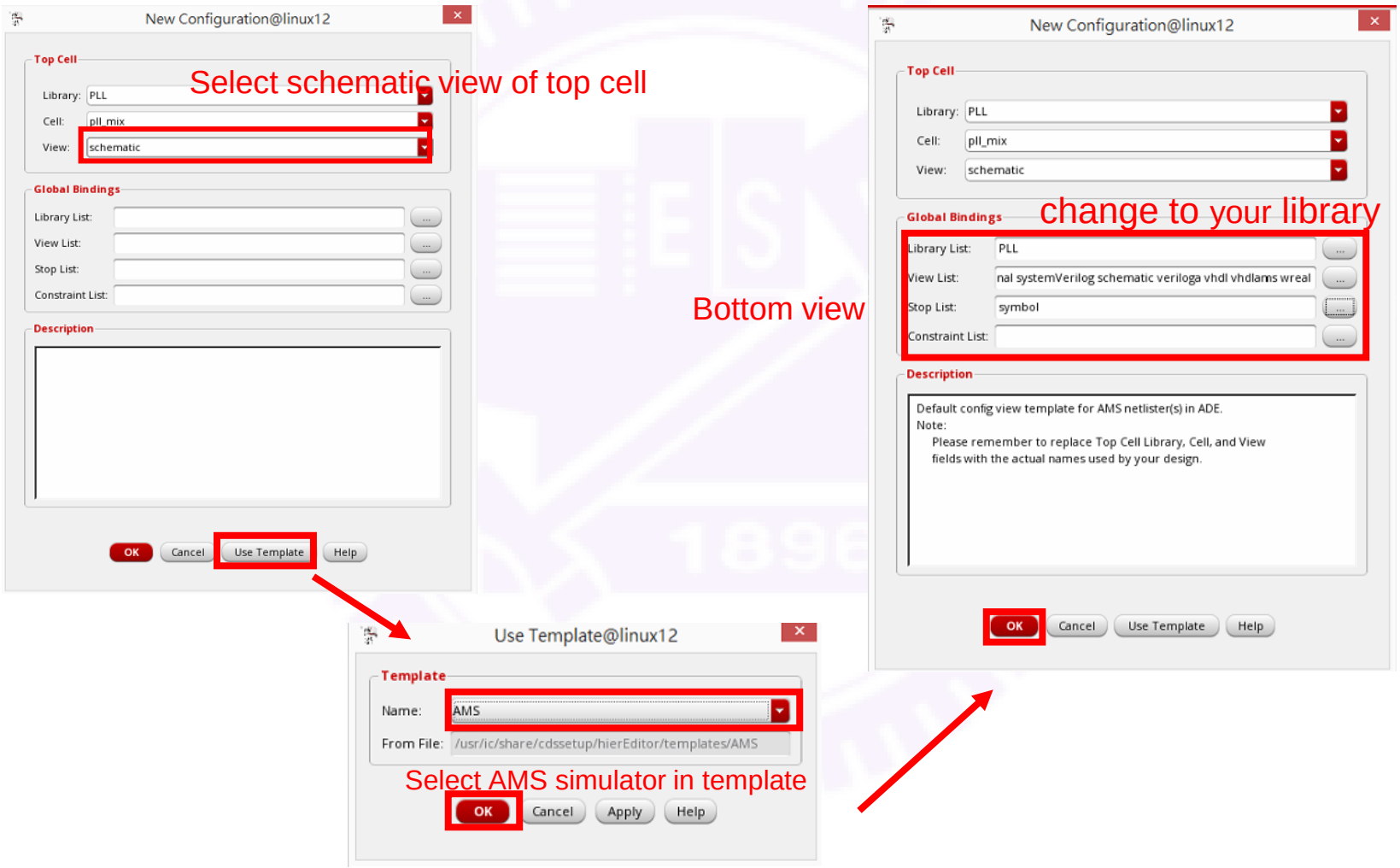
- The mixed-signal simulation hierarchy is controlled by **Hierarchy-Editor**
  - It must have to be defined in the **config** cell view.



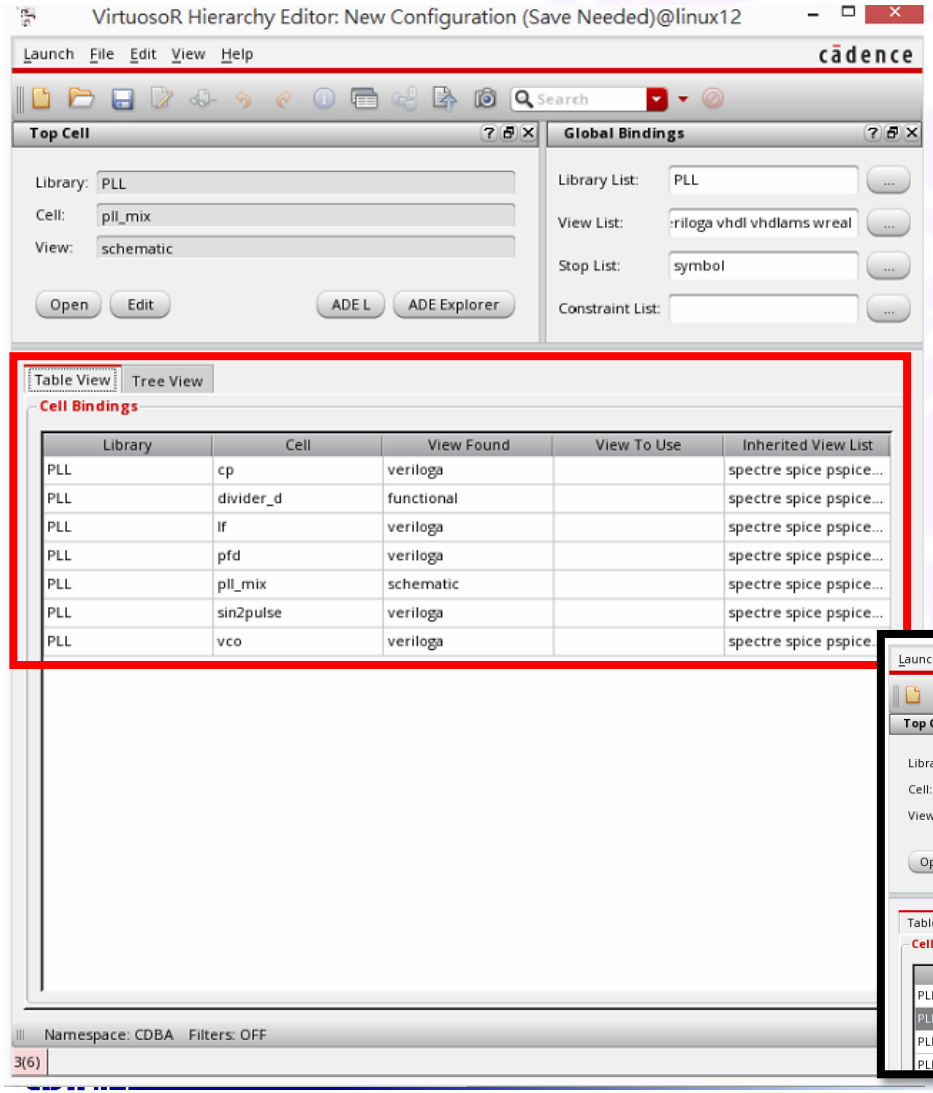
Cell name is top schematic cell for simulation

Choose **config** type

Set New Configuration

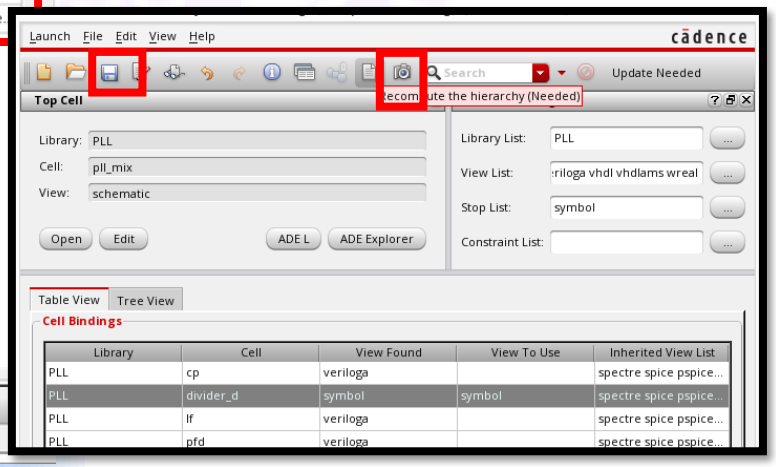


Configuration Setting



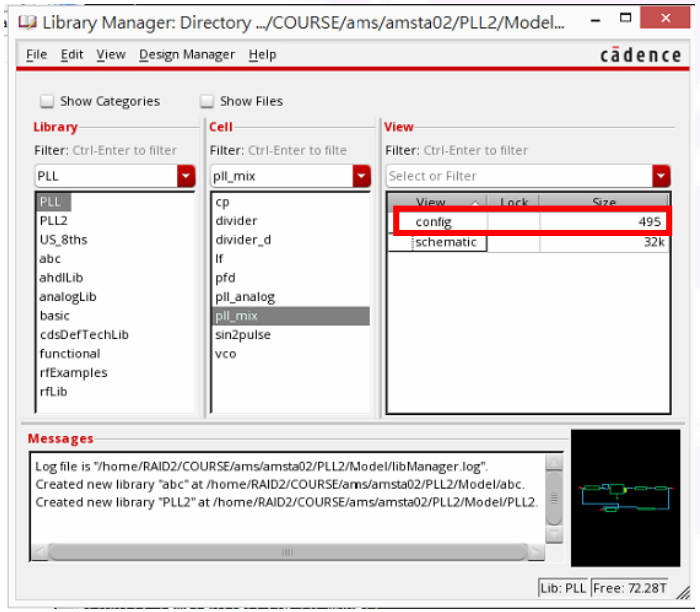
The hierarchy-editor will list all cells and views in the cell bindings

Must to save and recompute!

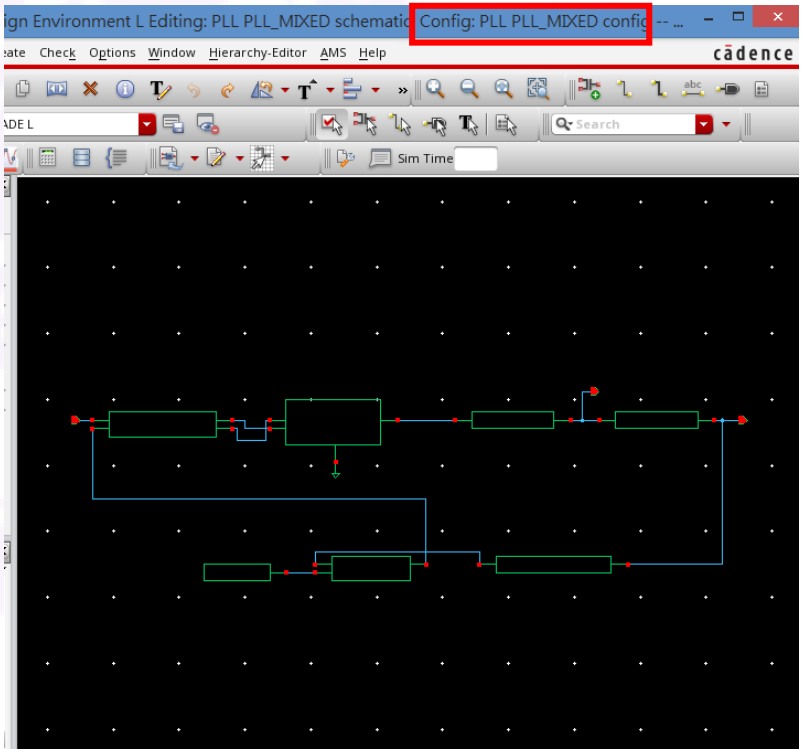


Open Simulation Tool

- Finish create config
  - Click config at library manager to open simulation tool
  - The simulation steps are the same as analog
    - Except give input information



Confirm the title has “config”



Digital Stimulus

- Create a behavioral or functional view for the stimulus block
  - The stimulus (Verilog) could be created to symbol view as the same procedure with digital cell

```
//Verilog HDL for "PLL", "stimulus_D" "functional"

`timescale 1ns/10ps
module stimulus_D (rst);
output rst;
reg rst;
initial begin
    rst=1'b0;
    #1 rst=1'b1;
end
endmodule
```

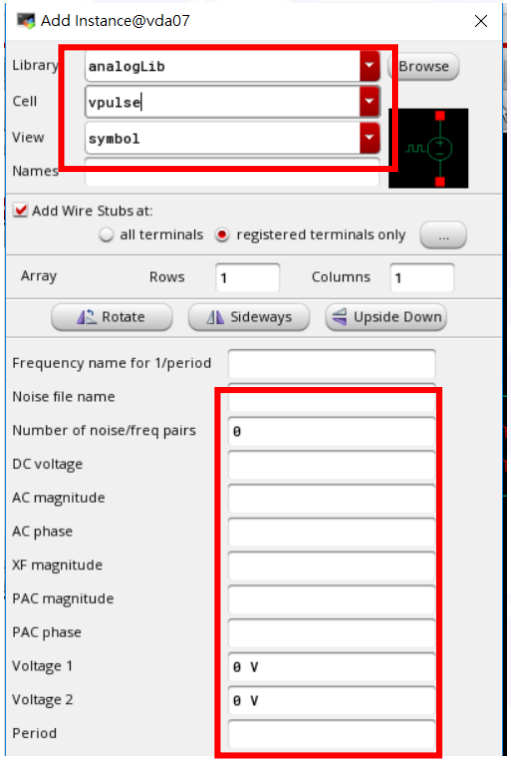
Analog Stimulus

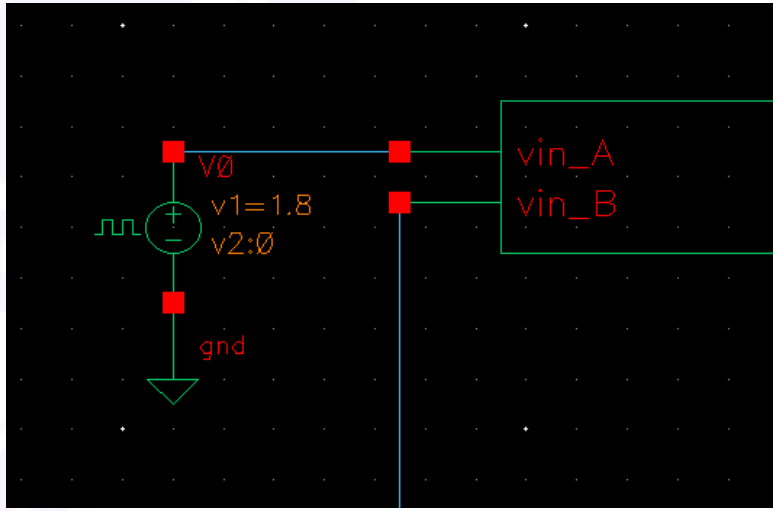
- The analog stimulus can be added as circuit instance

Add Instance

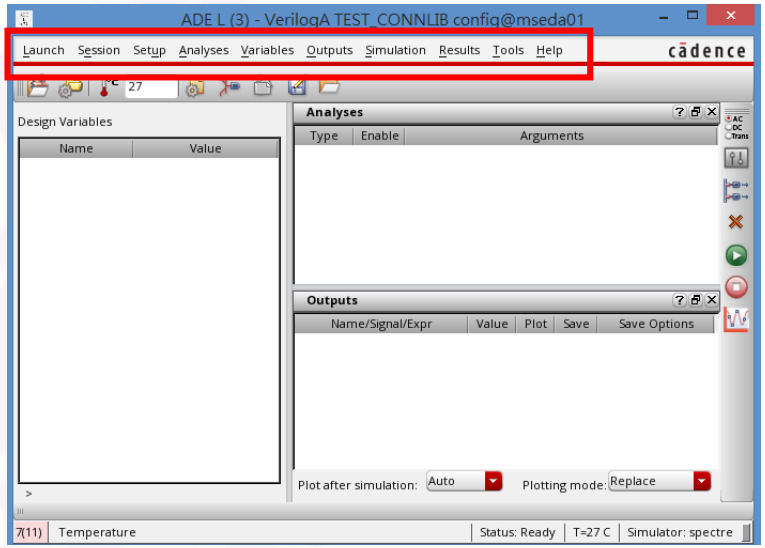
Choose analogLib & vpulse cell

Set voltage & frequency





1. Setup
   - ✓Simulator choose AMS
2. Analysis
   - ✓Tran analysis
   - ✓Set simulation time and enable
3. Outputs
   - ✓Save all or select on design
4. Run
5. Waveform viewer



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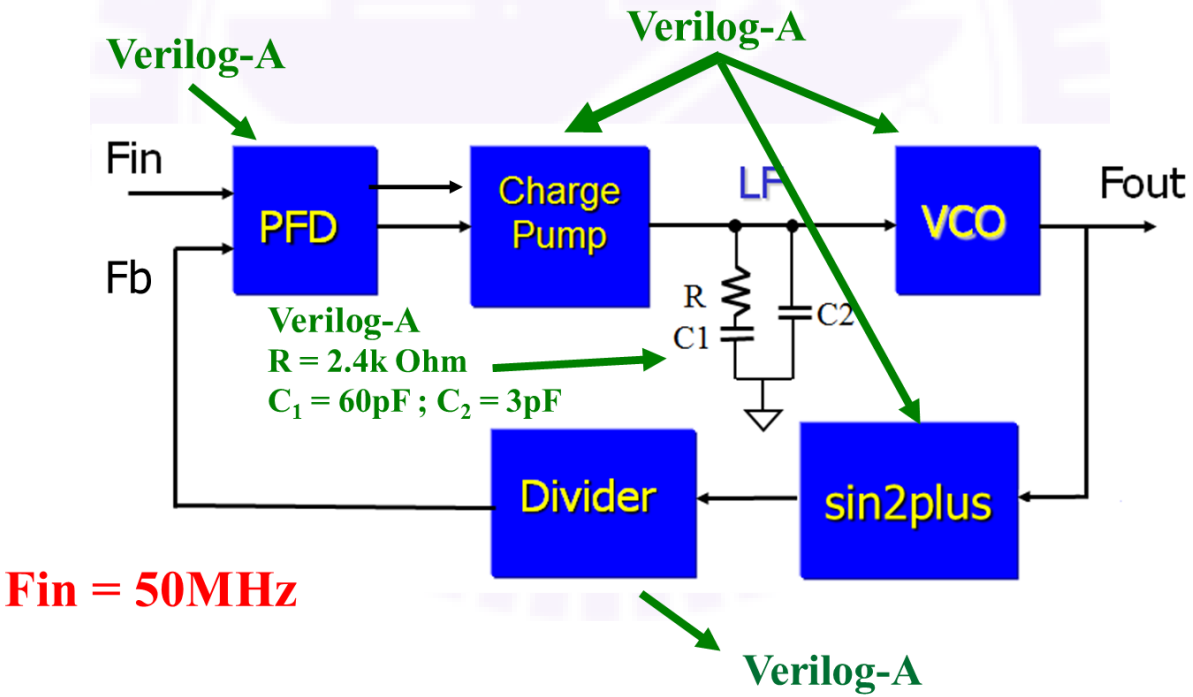
PLL Analog Model

- All Verilog-A models are given
  - PFD, CP, LF, VCO, sin2plus, divider
- Import the Verilog-A models and setup ADE



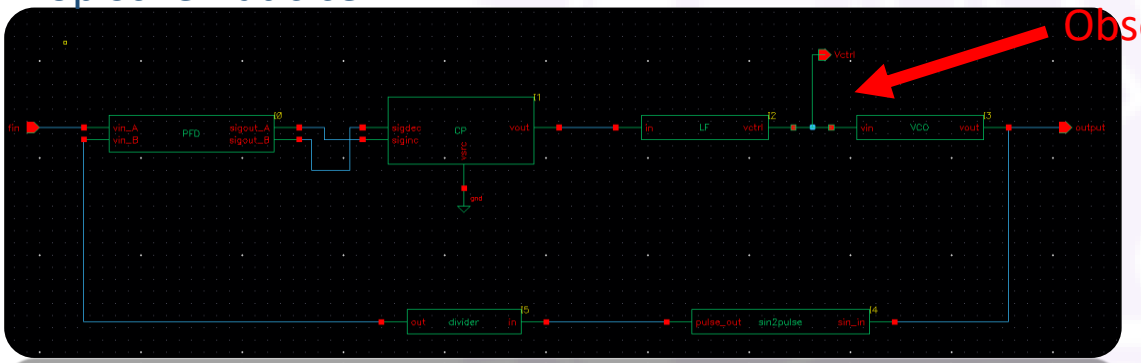
Additional Description

- Connection
  - **Connect *up* (*sigout_A*) signal of *PFD* to *siginc* signal of *CP***
  - **Connect *dn* (*sigout_B*) signal of *PFD* to *sigdec* signal of *CP***
  - **Connect *in* signal of *divider* to *sin2pulse***
  - **Charge pump(CP)**
    - Connect **vsrc** to **GND**
- VDD = 1.8V GND = 0V
- Simulator: **spectre**
- Input
  - **Fin=50M Hz : Set the ADE Stimuli**
- Simulation time $\geqq$ 6μs
  - Related to the lock time of PLL

Results

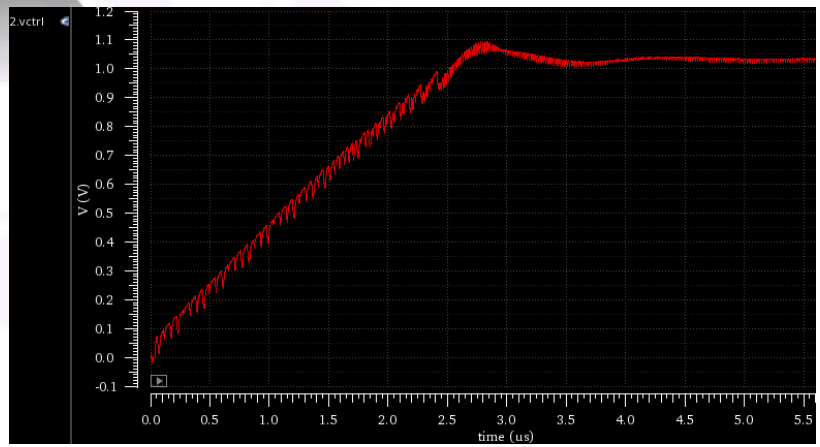
- Show the waveform of vctrl signal and schematic view

Top schematic cell



Observe the waveform of Vctrl

Open Results Brower



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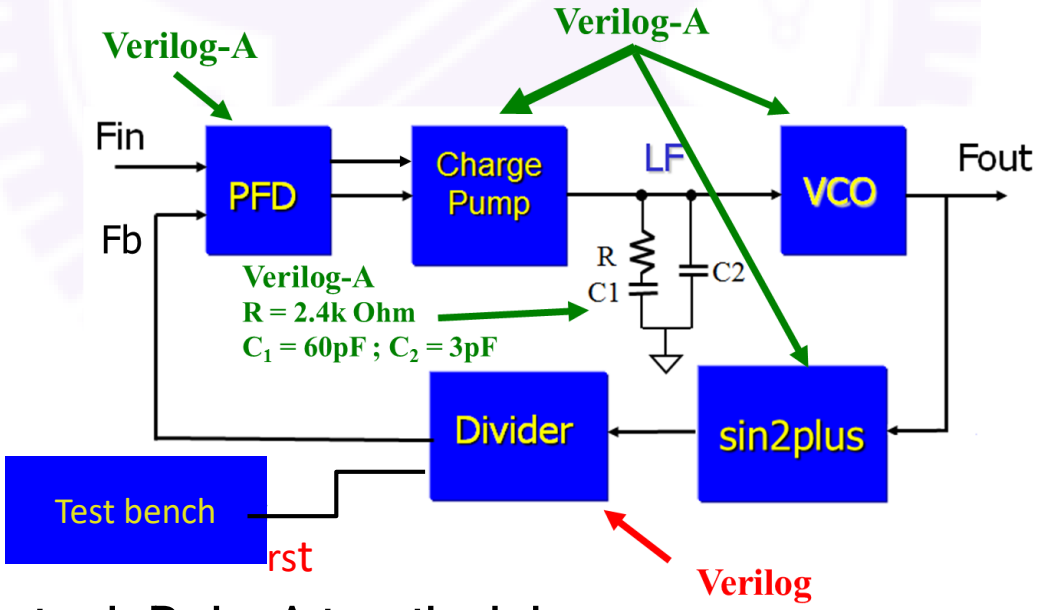
PLL Mixed-Signal Model

- All models are given
  - Analog model (Verilog-A): PFD, CP, LF, VCO, sin2plus
  - Digital model (Verilog): divider
- Import all models and create a testbench
  - Testbench : generate rst signal for divider



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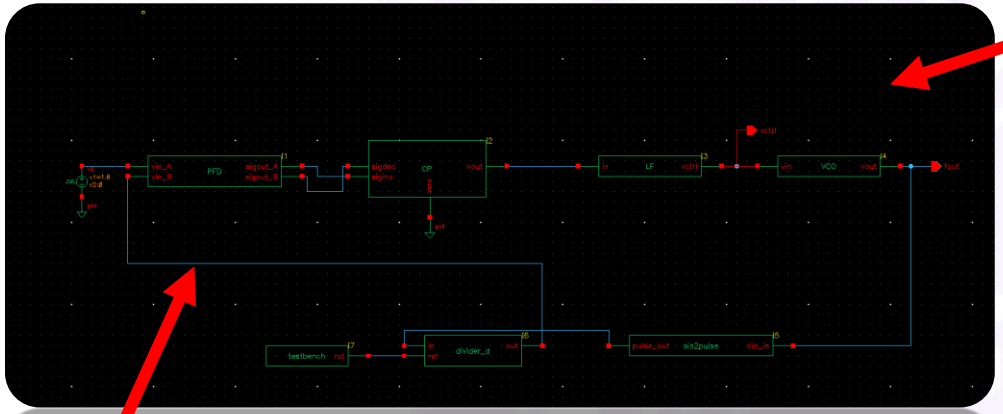
  - **Connect *up* (*sigout_A*) signal of *PFD* to *siginc* signal of *CP***
  - **Connect *dn* (*sigout_B*) signal of *PFD* to *sigdec* signal of *CP***
  - **Connect *in* signal of *divider* to *sin2pulse***
  - **Charge pump(CP)**
    - Connect **vsrc** to **GND**
- VDD = 1.8V GND = 0V
- Simulator: **AMS**
- Input
  - **Fin=50M Hz, Adding voltage source instance**
- Simulation time $\geqq$ 6μs
  - Related to the lock time of PLL

Results

- Show the waveform of vctrl, output of the divider and schematic view

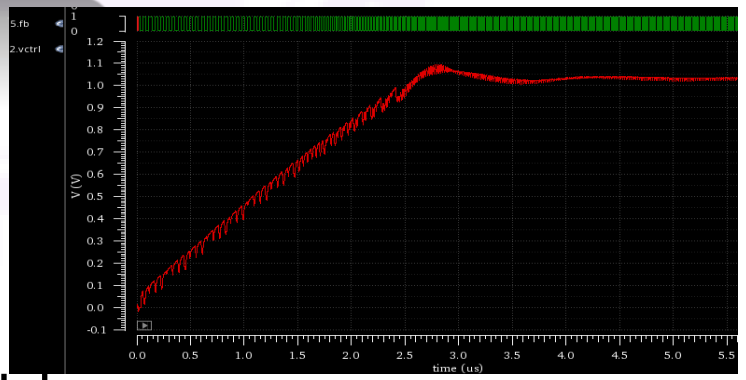
Top schematic cellview



Observe the waveform of Vctrl

Observe the output of divider.v

Open Results Brower

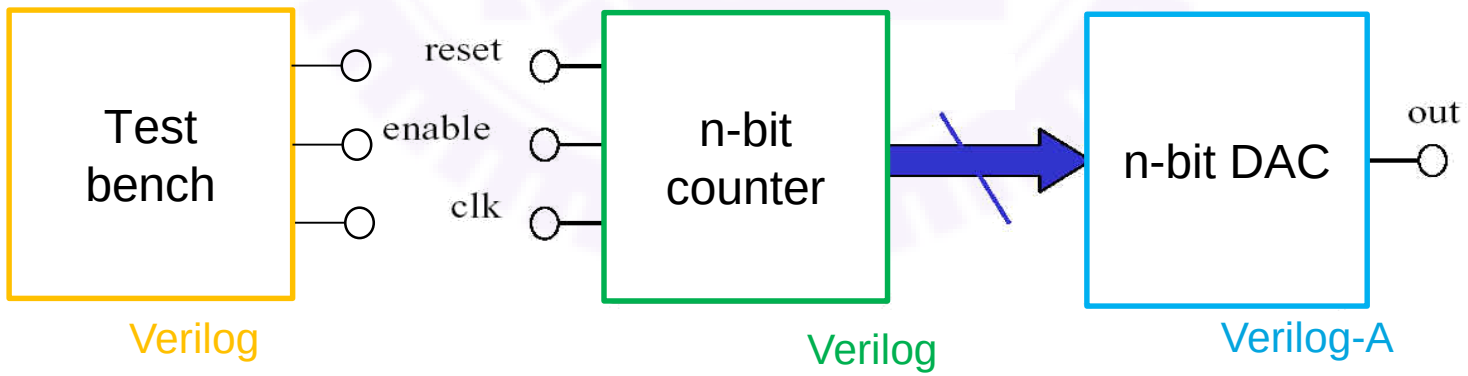


Outline

- Introduction to AMS
- AMS Simulation Setup
  - Analog Simulation with Verilog-A Model
  - Mixed-Signal Behavioral Model Simulation
    - Lab1: Analog Model Simulation with AMS
    - Lab2: Mixed-Signal Model Simulation with AMS
    - Lab3: Modeling Ideal Circuit with Verilog-A

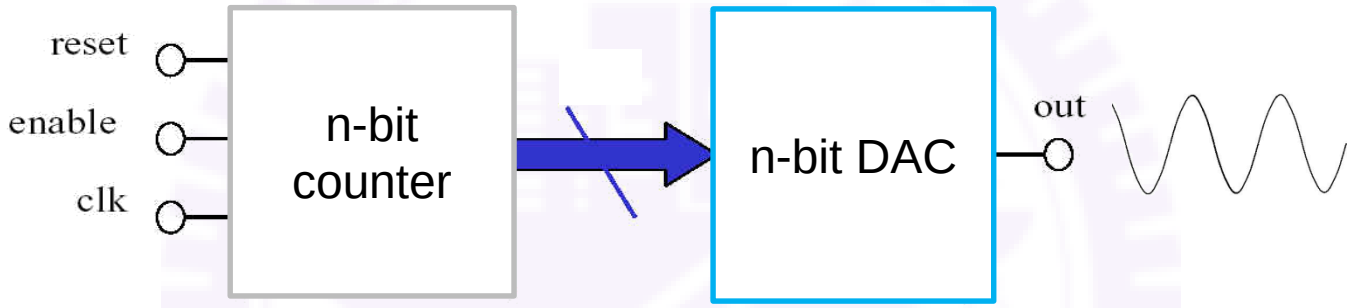
Description

- Create a system includes:
  - A DAC Verilog-A model
  - A clock counter
    - Generate a 3-bits bus for DAC model
  - Digital input -> the testbench includes three signals:
    - Reset
    - Enable
    - clk

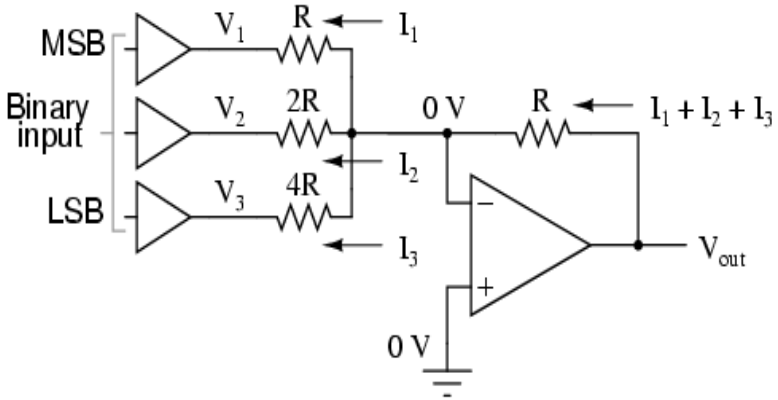


DAC Verilog-A Behavioral Model

- A 3-bit counter-controlled D/A Converter



- Type: binary weighted D/A Converter



$$\sum I = V_{REF}\left(\frac{B_3}{R}+\frac{B_2}{2R}+\frac{B_1}{4R}+\frac{B_0}{8R}\right)$$

$$V_{OUT} = I \cdot R_f = V_{REF}\left(B_3+\frac{B_2}{2}+\frac{B_1}{4}+\frac{B_0}{8}\right)$$

$$V_{OUT} = V_{REF}\sum\frac{B_i}{2^{n-i-1}}$$

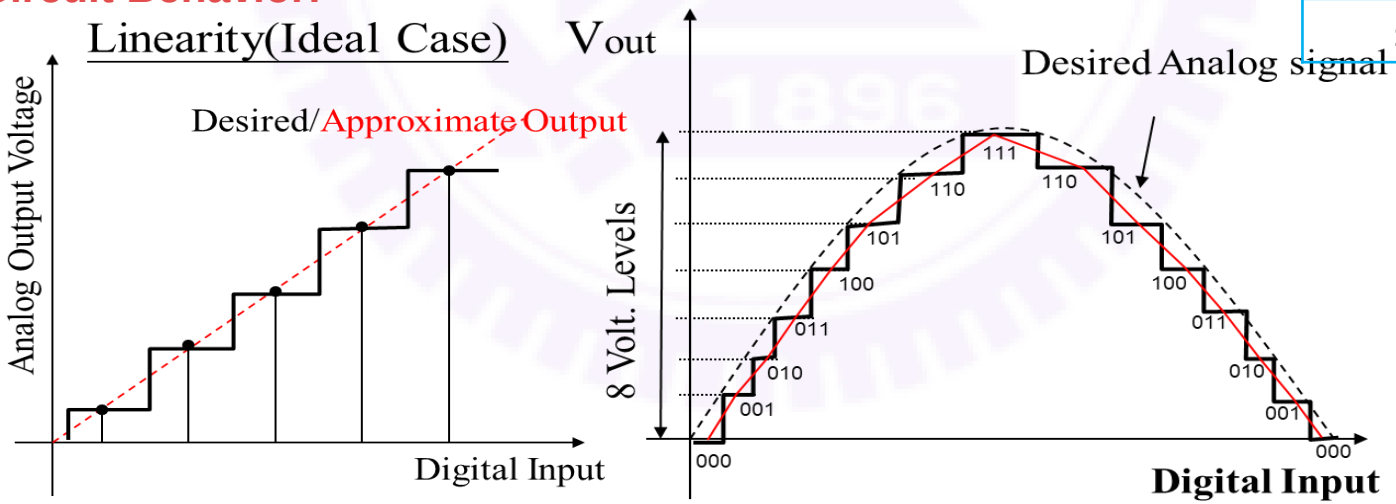
$$= V_{REF} \cdot \text{Digital Value} \cdot \text{Resolution}$$

Parameters of Ideal DAC Model

- Non-multiplier Reference Voltages: 0.8 V
- Resolution : 3bit → 0.2 V (V_{LSB})
- R=1k, Rref=R
- Linearity

B2,B1,B0 (bit)	Out (V)
000	0
001	-0.2
010	-0.4
011	-0.6
100	-0.8
101	-1.0
110	-1.2
111	-1.4

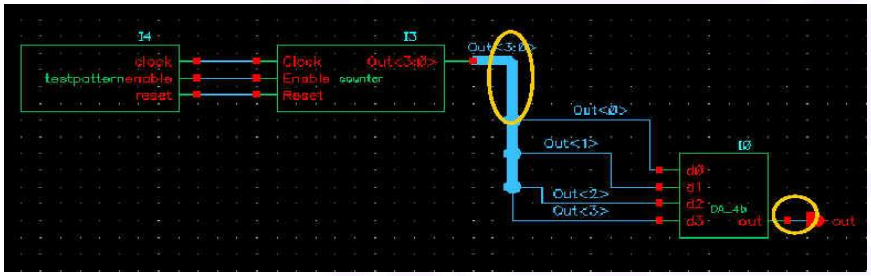
Circuit Behavior:

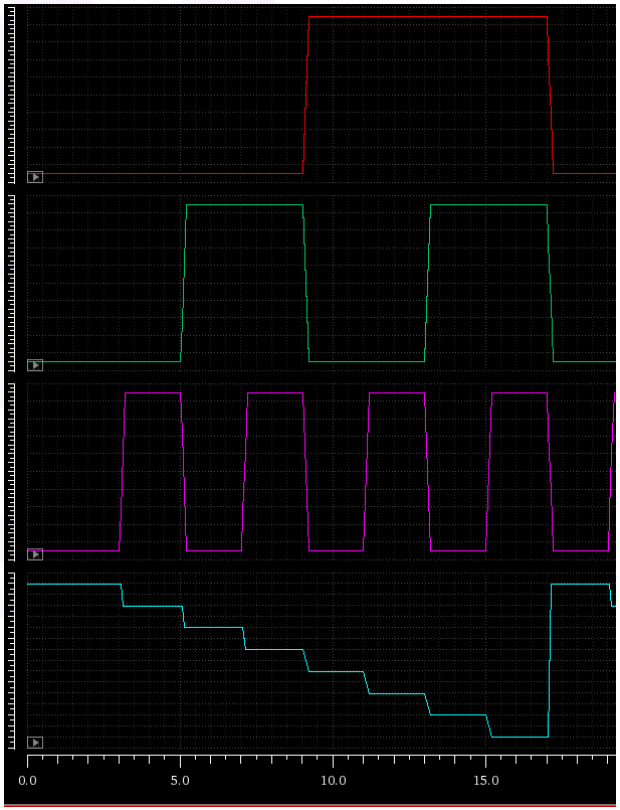


BM Results

- Hand in:
  - The waveform of outputs of counter and DAC model respectively
  - Schematic cellveiw

Choose two nets:





Hand in

- Please upload a compressed file includes:
  - **Programming files** (Verilog and Verilog-A files)
    - Lab2: Stimuli (testbech.v)
    - Lab3: DAC.va, counter.v, testbench.v
  - **Mini report**
    - Three simulation waveforms
      - Lab1: Analog simulation (Vctrl)
      - Lab2: Mixed-signal simulation (Vctrl & output of the divider)
      - Lab3: Outputs of counter and DAC (outputs of counter and DAC model)
    - Three schematic cellviews
    - What you have learned from this homework
    - Questions and solutions
- **Deadline: 23:55, January 3(Mon), 2022**