EE6094
CAD for VLSI Design

Tool Exercise

Spring 2022
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Introduction

- This exercise provides an opportunity for you to use two commercial EDA tools from Synopsys for front-end and back-end design procedure
  - Design Compiler
  - IC Compiler
- You are given an RTL design and the goal is to generate a GDSII Layout
- You need to submit a report to answer all questions during the tool exercise
- Report Submission deadline: 6/17(Fri) 23:59:59
  - Within 24hrs delay: 20% off
  - Within 48hrs delay: 40% off
  - More than 48hrs: 0 point
- Grading
  - Report 100%

Requirement

- You are asked to submit a report for your tool exercise assignment
- The report should at least include:
  - The Answer of each questions
  - The difficulties you encountered and how you solve the problems
  - What you learn from this assignment
  - Suggestions of this assignment
- Name your file as StudID_Name_tool_report.pdf (ex: 9862534_陳聿廣_tool_report.pdf).
  - Note that the only acceptable report file format is .pdf, no .doc/.docx or other files are acceptable.
  - Please upload your report to ee-class before deadline

Download File

1. Download file “PA5.tar.gz” from ee-class.
2. Upload “PA5.tar.gz” to server.
3. Unzip file “PA5.tar.gz”, $ tar zxvf PA5.tar.gz
4. $ cd PA5

Design Compiler
(Front End Design Procedure)

Design Compiler(DC)

1. $ cd dc_lab/
2. Source license
   $ source /usr/cad/synopsys/CIC/synthesis.cshrc
3. Active Design Compiler
   $ dv&

Design Compiler(DC)

DC command line

```
                        Design Compiler Graphical
                              DC Ultra (TM)
                               DFTMAX (TM)
                           Power Compiler (TM)
                              DesignWare (R)
                              DC Expert (TM)
                            Design Vision (TM)
                            HDL Compiler (TM)
                            VHDL Compiler (TM)
                               DFT Compiler
                            Design Compiler(R)

                    Version M-2016.12 for linux64 - Nov 21, 2016

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 Inc. This software may only be used in accordance with the terms and conditions
 of a written license agreement with Synopsys, Inc. All other use, reproduction,
            or distribution of this software is strictly prohibited.
Initializing...
design_vision> 4.1
design_vision>
```
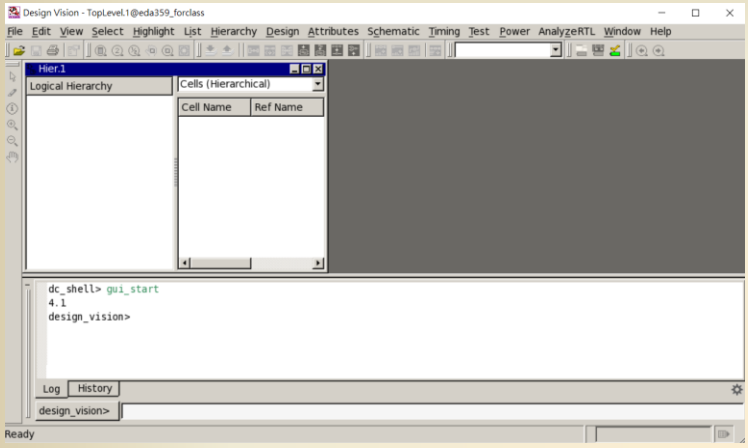


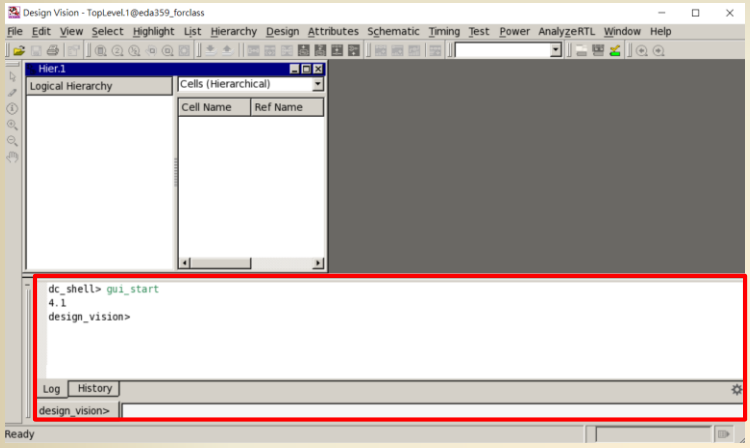
Design Compiler(DC)

DC GUI



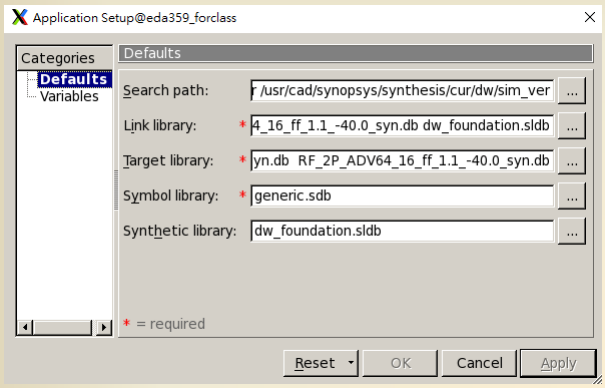
Design Compiler(DC)

Terminal: design vision



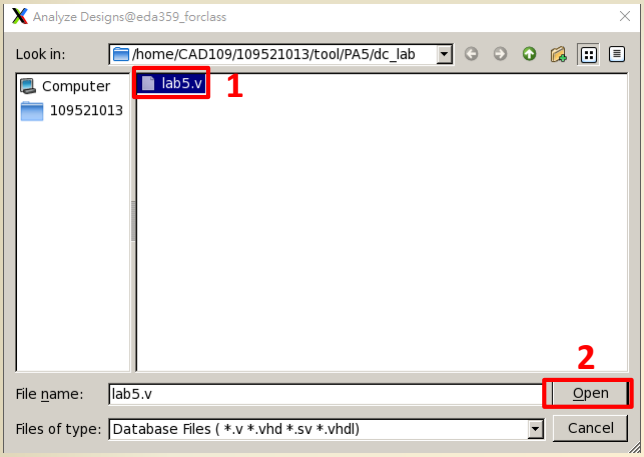
Design Compiler(DC)

Step1. Check setup (File > Setup…)



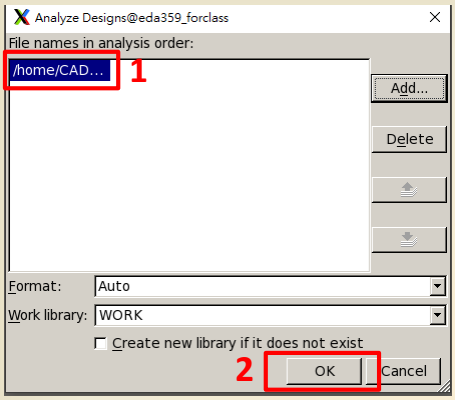
Design Compiler

Step2. Load design files “lab5.v” (File > Analyze …)



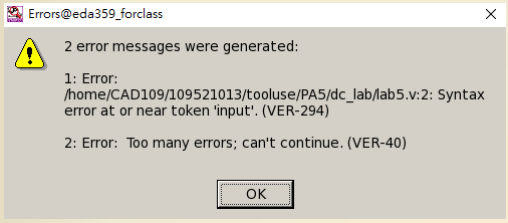
Design Compiler

Step3. Load design files “lab5.v”



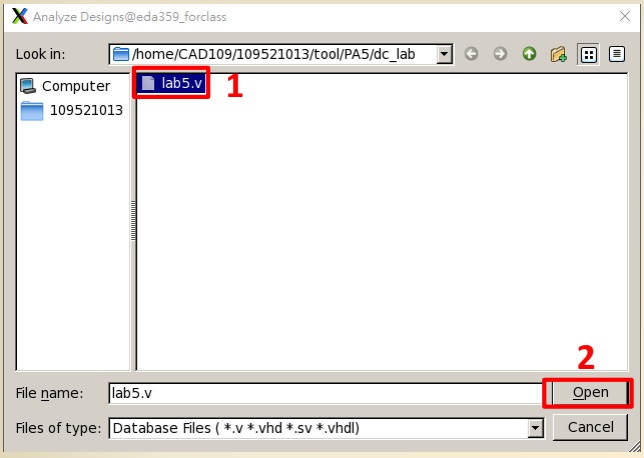
Design Compiler

Step4. Find the error code in “lab5.v”, and go back to step 2, reload the file “lab5.v” until the error window doesn’t pop up.



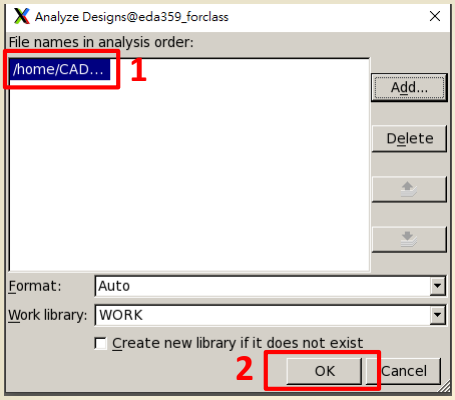
Design Compiler

Step5. Reload design files “lab5.v” (File > Analyze …)



Design Compiler

Step6. Reload design files “lab5.v”



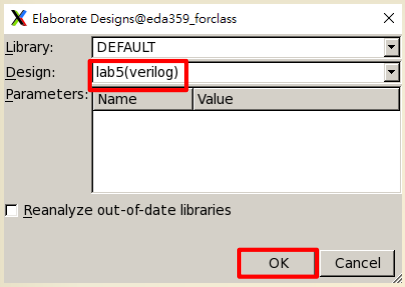
Design Compiler

Step7. Reload design files “lab5.v” successfully

```
design_vision> analyze -format verilog {/home/CAD109/109521013/tooluse/PA5/dc_lab/lab5.v}
Running PRESTO HDLC
Compiling source file /home/CAD109/109521013/tooluse/PA5/dc_lab/lab5.v
Presto compilation completed successfully.
```

Design Compiler

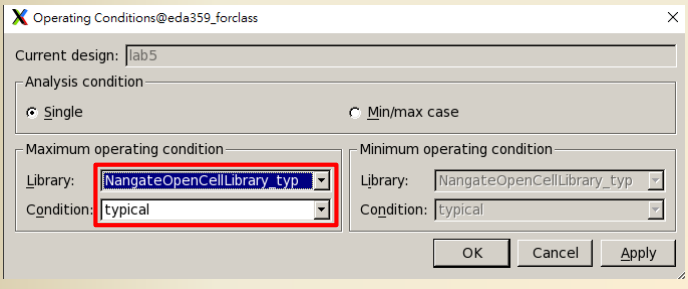
Step8. Select toplevel module “lab5.v” (File > Elaborate…)



Design Compiler

Step9. Setting operating conditions

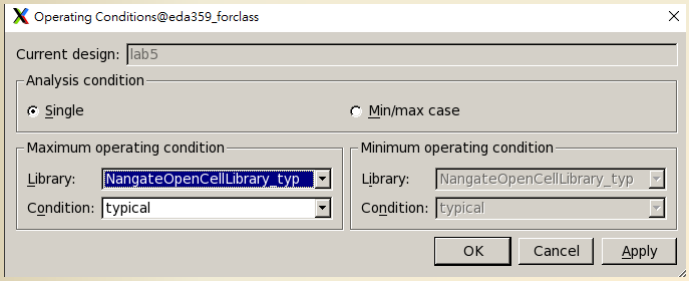
(Attributes > Operating Environment > Operating Conditions…)



Design Compiler

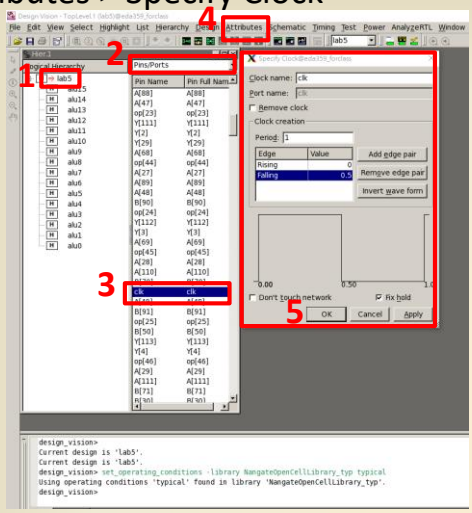
Setting operating conditions (optional)

1. Maximum operating condition (for setup time analysis):
   Library: slow, Condition: slow
2. Minimum operating condition (for hold time analysis):
   Library: fast, Condition: fast



Design Compiler

Step10. Attributes > Specify Clock



Design Compiler

Step11. (In command line)

design_vision> set ClockName clk

design_vision>

set_ideal_network -no_propagate [get_ports $ClockName]

Design Compiler

Step12. (In command line)

design_vision>

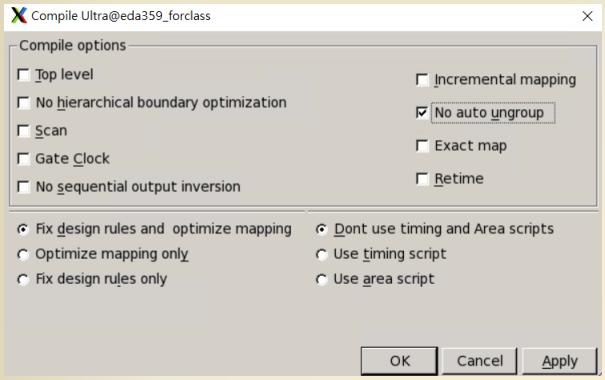
set_input_delay 0 -clock [get_clocks $ClockName] \
[remove_from_collection [all_inputs] [get_ports $ClockName]]

design_vision>

set_output_delay 0 -clock [get_clocks $ClockName] [all_outputs]

Design Compiler

Step13. Design > Compile Ultra



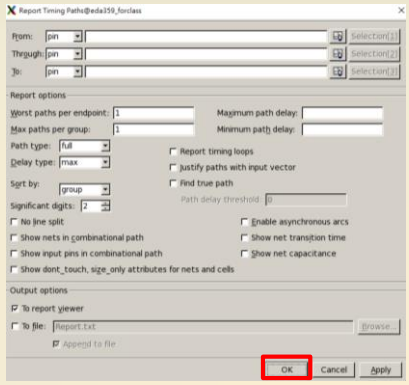
Design Compiler

Step14. Use “Timing > Report timing path…” to see the timing

Q1. data required time =____

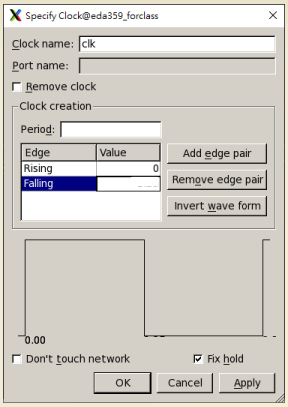
data arrival time =____

slack (VIOLATED) =____



Design Compiler

Step15. Adjust the Specify Clock and let timing slack ≥ 0



Design Compiler

Step16. (In command line)

design_vision> set ClockName clk

design_vision>

set_ideal_network -no_propagate [get_ports $ClockName]

Design Compiler

Step17. (In command line)

design_vision>

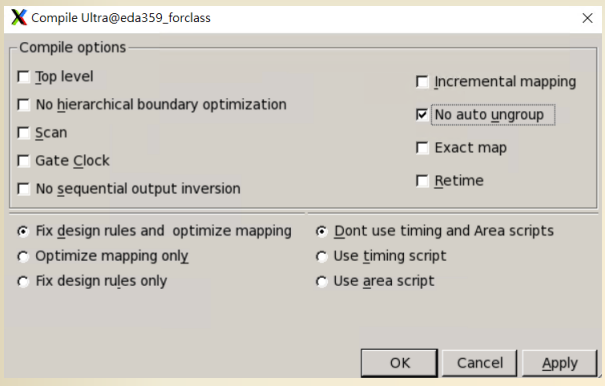
```
set_input_delay 0 -clock [get_clocks $ClockName] \
[remove_from_collection [all_inputs] [get_ports $ClockName]]
```

design_vision>

```
set_output_delay 0 -clock [get_clocks $ClockName] [all_outputs]
```


Design Compiler

Step18. Design > Compile Ultra



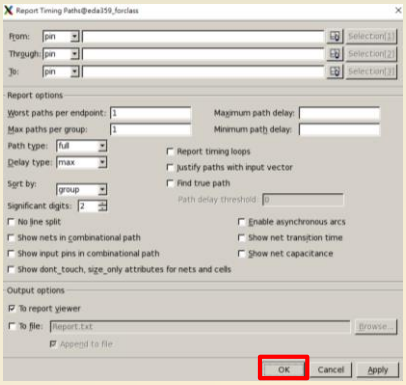
Design Compiler

Step19. Use “Timing > Report timing path…” to see the timing

Q2. data required time =____

data arrival time =____

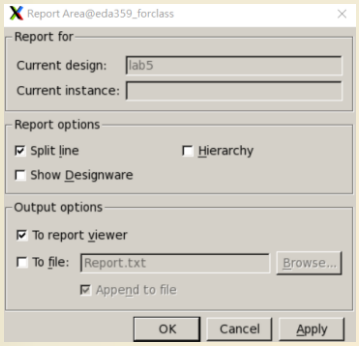
slack (VIOLATED) =____



Design Compiler

Step20. Use “Design/Report Area…” to see the area

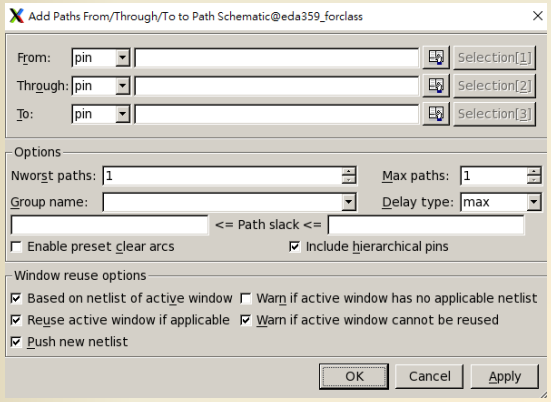
Q3. Total cell area = ____



Design Compiler

Q4. Please print screen of Critical Path. _____

(Schematic > Add Paths From/Through/To…)



Design Compiler

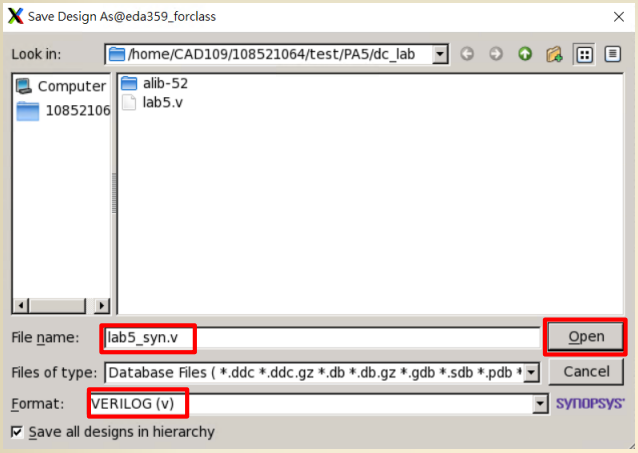
Step22. Generate Legal Verilog Netlist

(In command line)

design_vision> change_names -hierarchy -rules verilog

Design Compiler

Step23. Save Gate-Level Netlist (File > Save as)



Design Compiler

Step24. Write SDF file
(In command line)
design_vision> write_sdf -version 1.0 lab5.sdf

Step25. Write SDC file
(In command line)
design_vision> write_sdc lab5.sdc

Step26. Close Design Vision GUI
(In command line)
design_vision> quit

IC Compiler
(Back-end Design Procedure)

IC Compiler(ICC)

1. Change directory to ~/icc_lib/run
   $ cd ../icc_lab/run/
2. Copy design data from DC directory to ICC directory
   $ cp ../../dc_lab/lab5.sdc ../design_data/
   $ cp ../../dc_lab/lab5.sdf ../design_data/
   $ cp ../../dc_lab/lab5_syn.v ../design_data/

```
[108521064@eda359_forclass dc_lab]$ cd ../icc_lab/run/
[108521064@eda359_forclass run]$ cp ../../dc_lab/lab5.sdc ../design_data/
[108521064@eda359_forclass run]$ cp ../../dc_lab/lab5.sdf ../design_data/
[108521064@eda359_forclass run]$ cp ../../dc_lab/lab5_syn.v ../design_data/
```

IC Compiler(ICC)

1. Source
   $ source /usr/cad/synopsys/CIC/icc.cshrc
2. Active Design Compiler
   $ icc_shell -gui

```
[108521064@eda359_forclass run]$ source /usr/cad/synopsys/CIC/icc.cshrc
Platform = amd64
[108521064@eda359_forclass run]$ icc_shell -gui
```


IC Compiler(ICC)

ICC command line

```
                              IC Compiler (TM)
                            IC Compiler-PC (TM)
                            IC Compiler-XP (TM)
                            IC Compiler-DP (TM)
                            IC Compiler-AG (TM)

                Version N-2017.09-SP2 for linux64 - Nov 27, 2017

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            or distribution of this software is strictly prohibited.
Initializing...
icc_shell> Information: Visibility is turned ON for cells and cell contents because
I-026)
icc_shell>
```
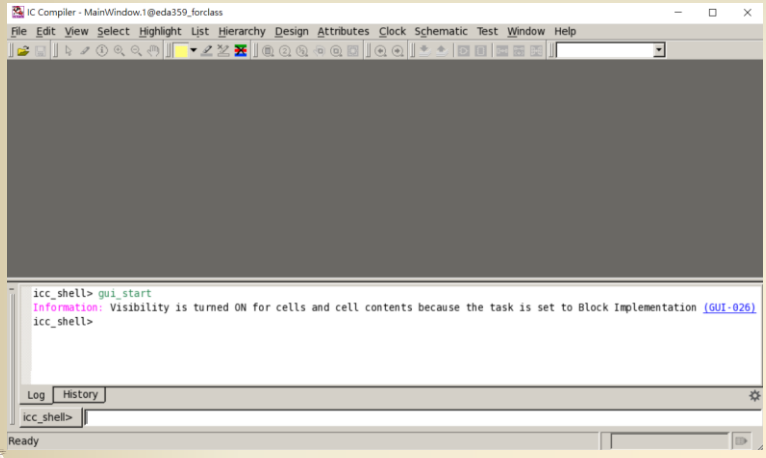

IC Compiler(ICC)

ICC GUI



1. Design Setup

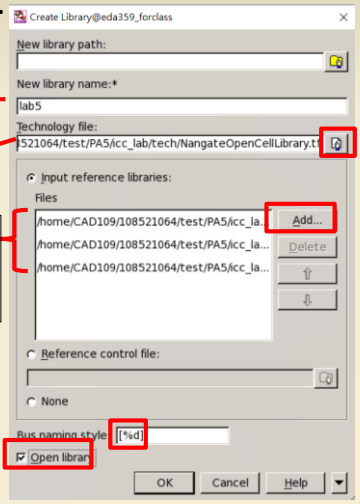
Design Setup

Step1. “File > Create Library…”

lab5

../tech/NangateOpenCellLibrary.tf

../physical_lib/NangateOpenCellLibrary
../physical_lib/RF_2P_ADV64_16
../physical_lib/tpz

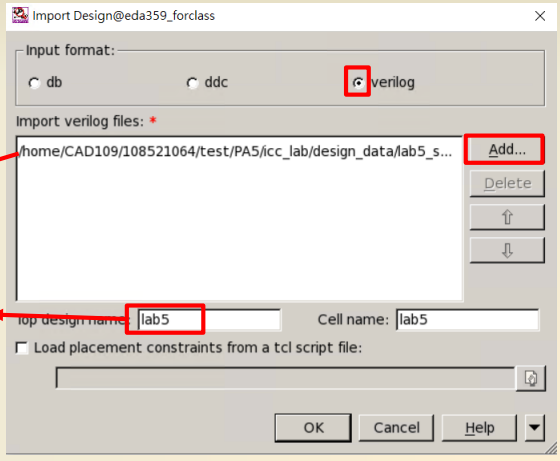


Design Setup

Step2. “File > Import Designs…”

../design_data/lab5_syn.v

lab5

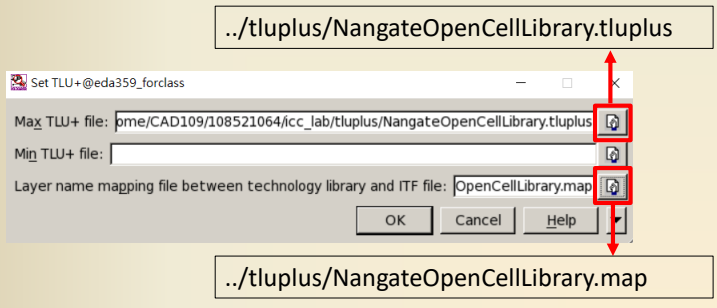


Design Setup

Q5. Please print screen of what you see in IC Compiler LatoutWindow. _____

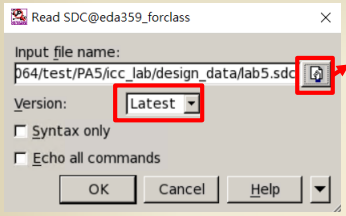
Design Setup

Step3. “File > Set TLU+…”



Design Setup

Step4. “File > Import > Read SDC…”



"../design_data/lab5.sdc

Design Setup

Step5: Save File

(In command line)

icc_shell> save_mw_cel -design "lab5"

icc_shell> save_mw_cel -design "lab5" -as "design_setup"

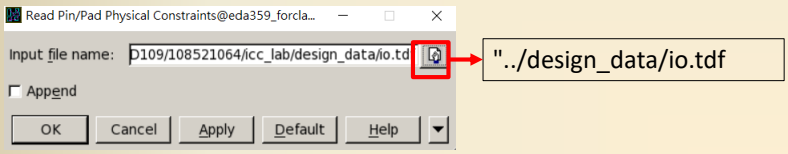
2. Design Planning

Design Planning

Step1. Add IO, P/G pad, POC pad, and Corner pad

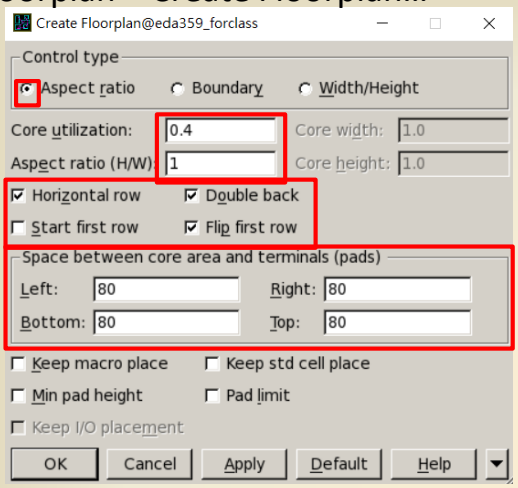
icc_shell> source ../scripts/create_phy_cell.tcl

Step2. “Floorplan > Read Pin/Pad Physical Constraints…”
(In LayoutWindows)



Design Planning

Step3. “Floorplan > Create Floorplan…”



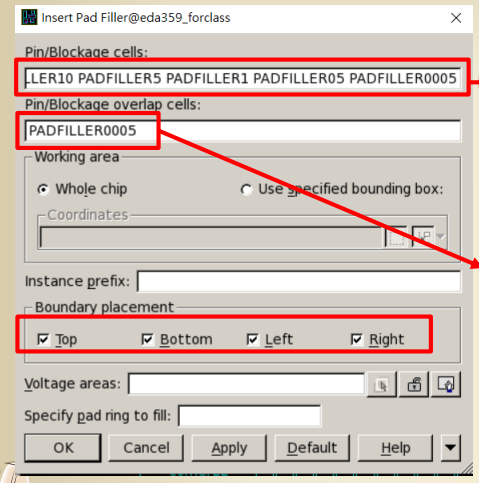
Design Planning

Q6. Please print screen of what you see in IC Compiler LatoutWindow. _____

What is the difference between Q5 and Q6? ____

Design Planning

Step4. “Finishing > Insert Pad Filler…”



PADFILLER20
PADFILLER10 PADFILLER5
PADFILLER1 PADFILLER05
PADFILLER0005
(Sort from big to small)

PADFILLER0005

Design Planning

Step5. save design

```
icc_shell> save_mw_cel  -design "lab5"
icc_shell> save_mw_cel  -design "lab5" -as "die_init"
```

Step6. place standard cells

```
icc_shell> create_fp_placement
```

Design Planning

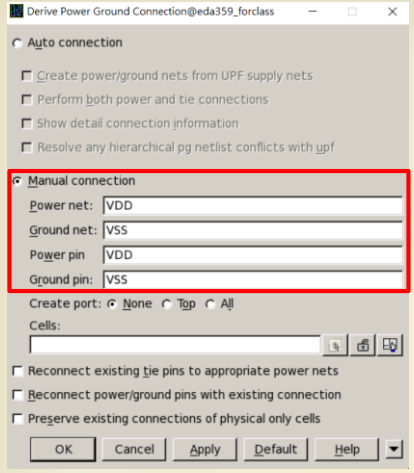
Step7. save design

icc_shell> save_mw_cel -design "lab5"

icc_shell> save_mw_cel -design "lab5" -as "before_PNS"

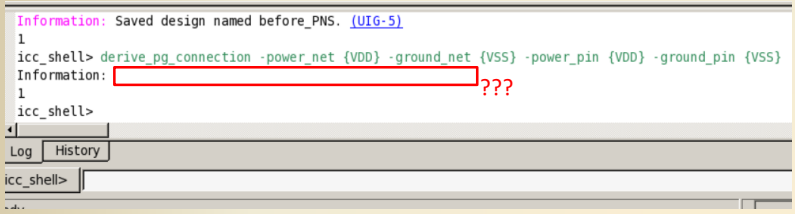
Design Planning

Step8. “Preroute > Derive PG Connection…”



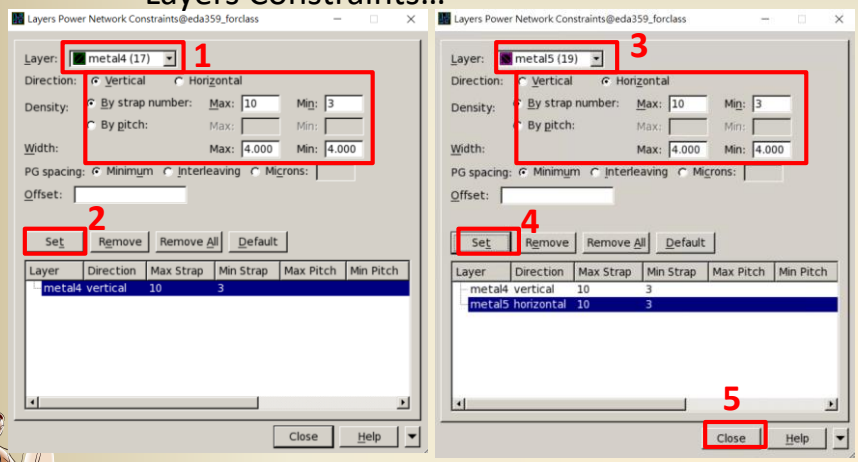
Design Planning

Q7. How many connected power ports and ground ports in this project? ____ , _____



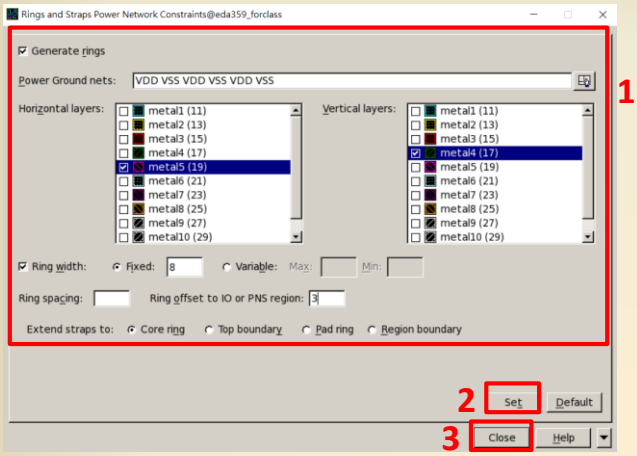
Design Planning

Step9. “Preroute > Power Network Constraints > Strap Layers Constraints…”



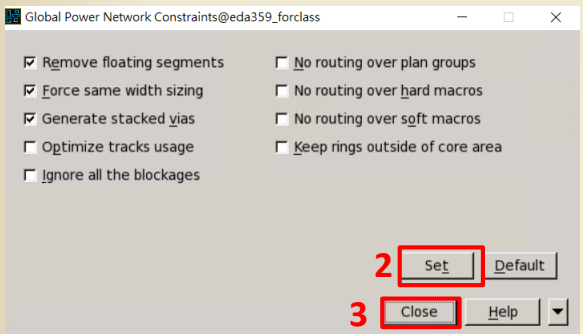
Design Planning

Step10. “Preroute > Power Network Constraints > Ring Constraints…”



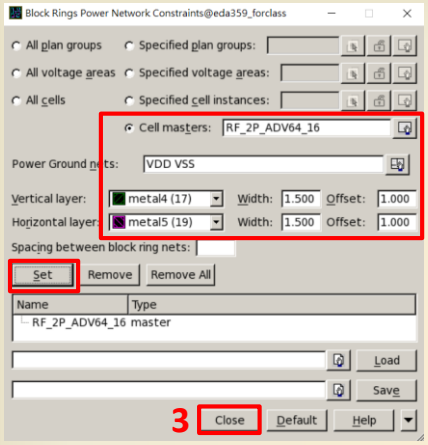
Design Planning

Step11. “Preroute > Power Network Constraints > Global Constraints…”



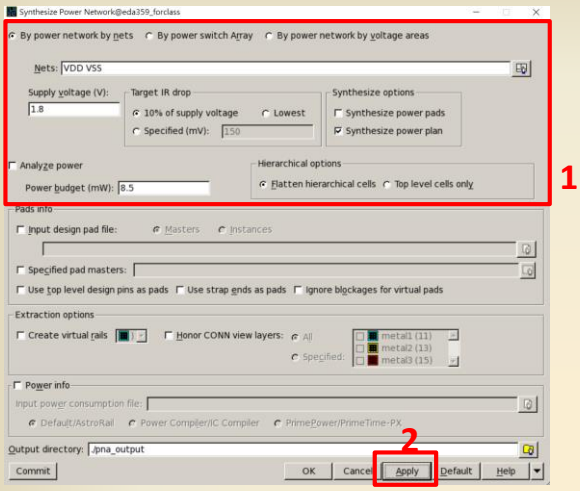
Design Planning

Step12. “Preroute > Power Network Constraints > Block Ring Constrains…”



Design Planning

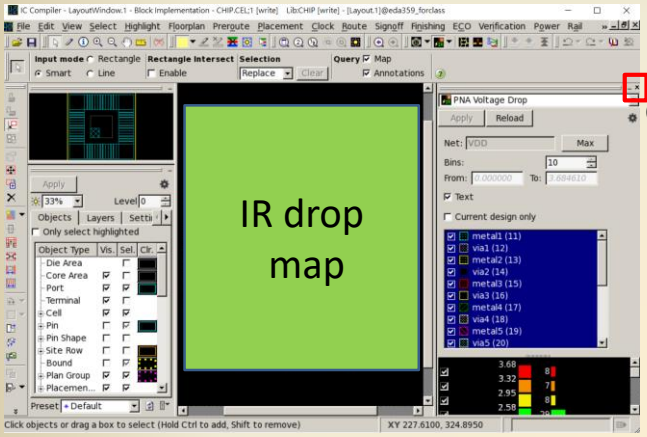
Step13. “Preroute > Synthesize Power Network…”



Design Planning

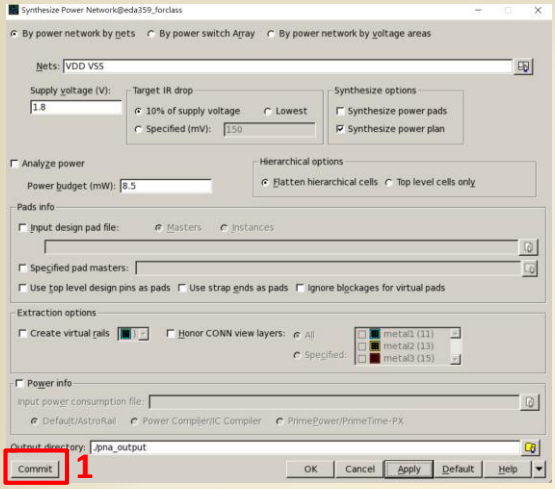
Q8. (a) Please print screen IR drop map. _____

(b) Explain IR drop. _____



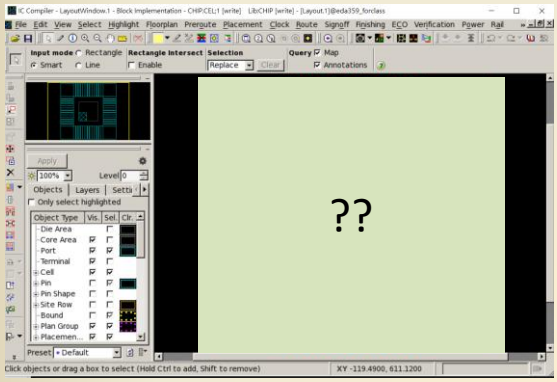
Design Planning

Step13. “Preroute > Synthesize Power Network…”



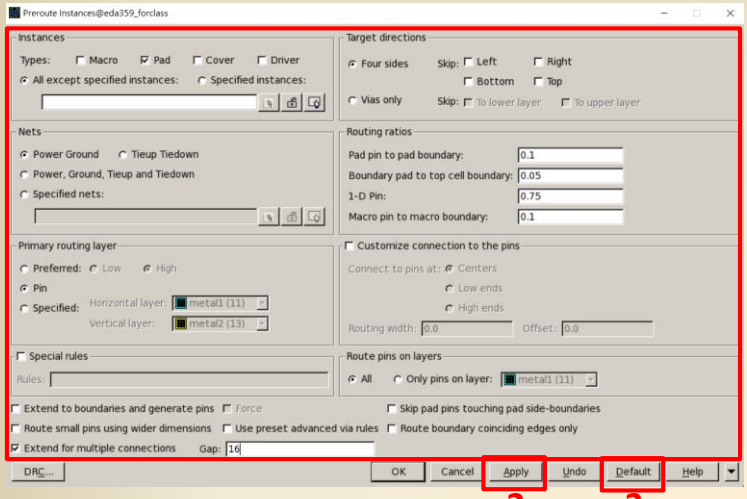
Design Planning

Q9. Please print screen of what you see in IC Compiler LatoutWindow. _____



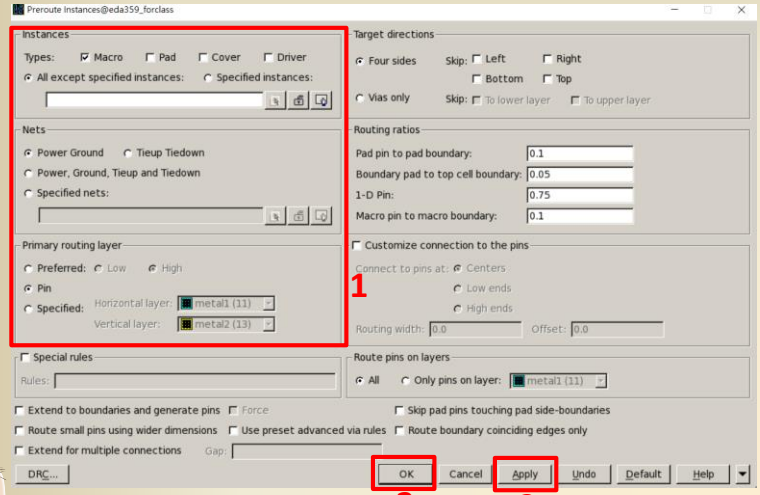
Design Planning

Step14. “Preroute > Preroute Instances…”



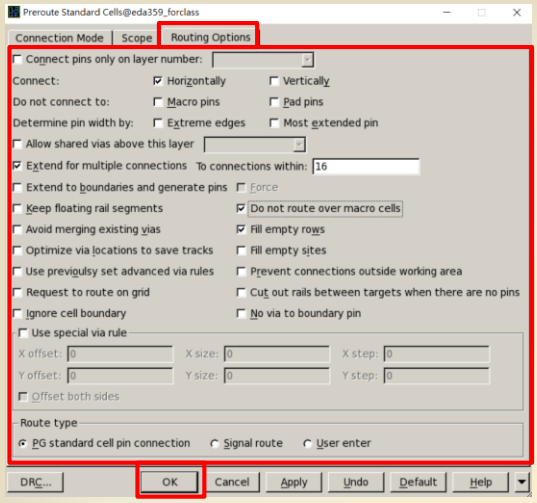
Design Planning

Step15. “Preroute > Preroute Instances”



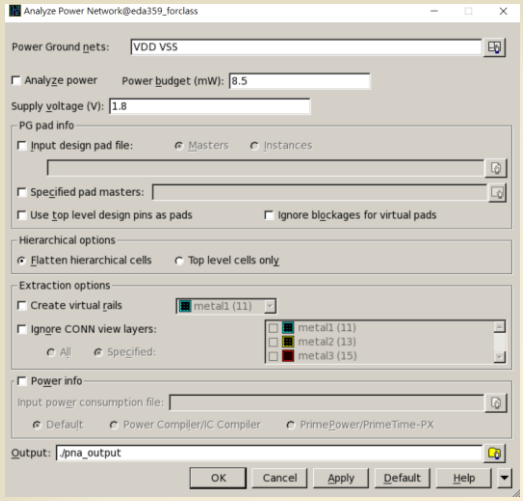
Design Planning

Step16. “Preroute > Preroute Strandard Cells…”



Design Planning

Step17. “Preroute > Analyze Power Network…”



Design Planning

Step18.

icc_shell> set_pnet_options -partial "metal4 metal5"

icc_shell> create_fp_placement -incremental all

Step19. save design

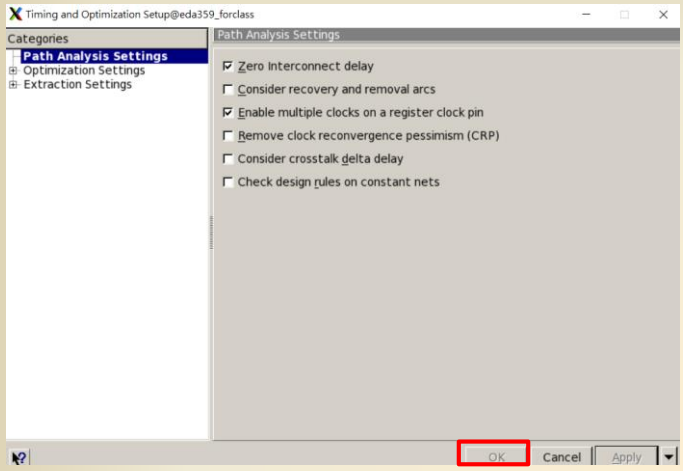
icc_shell> save_mw_cel -design "lab5"

icc_shell> save_mw_cel -design "lab5" -as "design_planning"

3. Placement

Placement

Step1. “Timing > Timing and Optimization Setup…”



Placement

Q10. data required time = _____

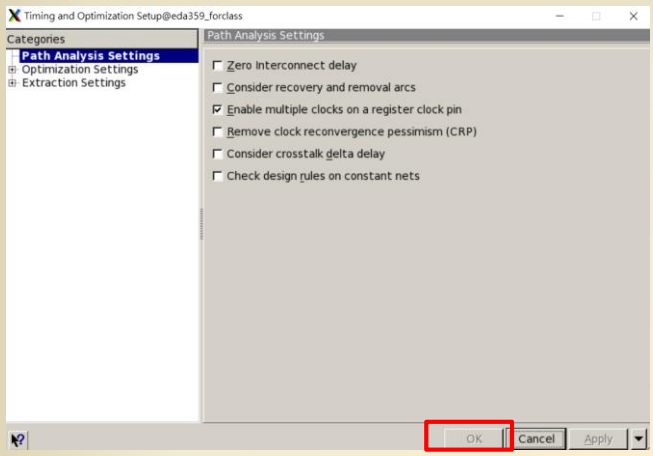
data arrival time = _____

slack (MET) = _____

(icc_shell> report_timing)

Placement

Step2. “Timing > Timing and Optimization Setup…”



Placement

Q11. data required time = _____

data arrival time = _____

slack (MET) = _____

(icc_shell> report_timing)

Placement

Q12. Internal power = _____

Switching power = _____

Leakage power = _____

(icc_shell> report_power)

Placement

Step3. The following commands should be executed before performing place_opt.

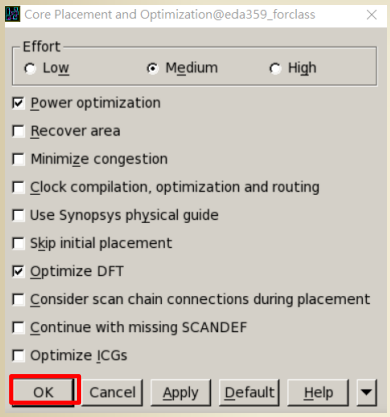
icc_shell> check_physical_design -stage pre_place_opt

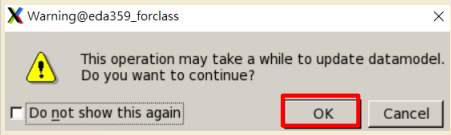
Step4. Setup the tie cell option

icc_shell> source ../scripts/add_tie.tcl

Placement

Step5. “Placement > Core Placement and Optimization…”





Placement

Q13. data required time = _____

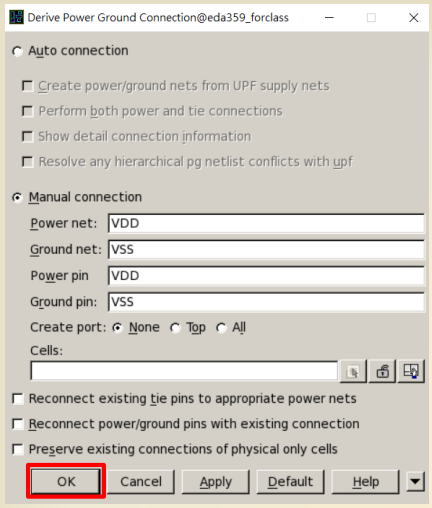
data arrival time = _____

slack (VIOLATED) = _____

(icc_shell> report_timing)

Placement

Step6. “Preroute > Derive PG Connection”



Placement

Q14. Internal power = _____

Switching power = _____

Leakage power = _____

Are the answers of Q12 and Q14 different?_____

(icc_shell> report_power)

Placement

Step7. save design

```
icc_shell> save_mw_cel  -design "lab5"
icc_shell> save_mw_cel  -design "lab5" -as "design_planning"
```


4. CTS


CTS

Step1. Check

icc_shell> check_physical_design -stage pre_clock_opt

Q15. Have any error? _____

Step2.

icc_shell> set_fix_hold [all_clocks]

CTS

Step3. Perform CTS optmization

icc_shell> clock_opt -fix_hold_all_clocks -no_clock_route

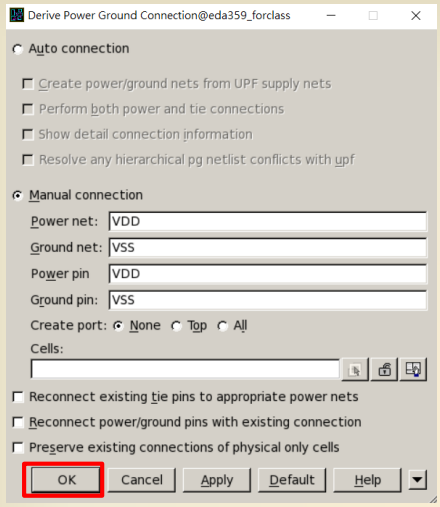
CTS

Step4. Review the global skew after CTS

icc_shell> report_clock_tree -summary

CTS

Step6. “Preroute > Derive PG Connection”



CTS

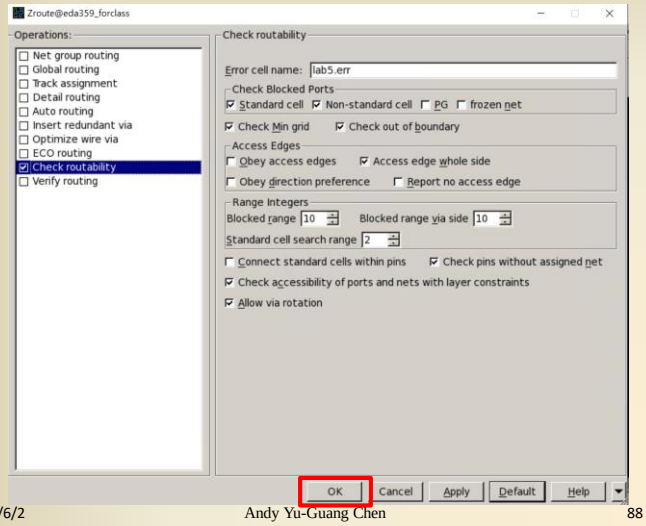
Step7. Save design

```
icc_shell> save_mw_cel -design "lab5"
icc_shell> save_mw_cel -design "lab5" -as "cts"
```

5. Route

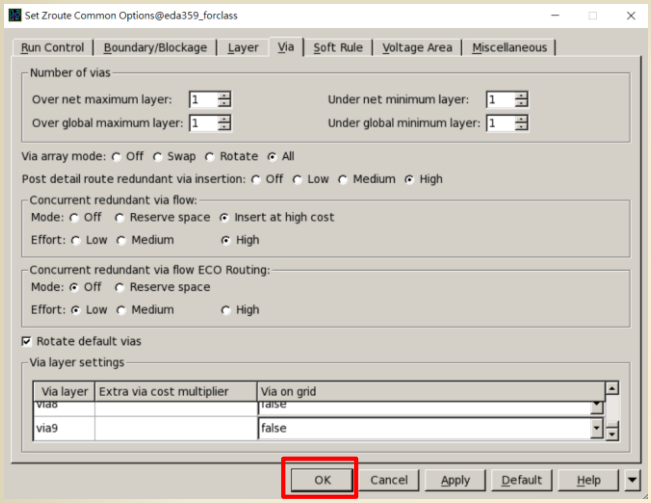
Route

Step1. “Route > Check Routability…”



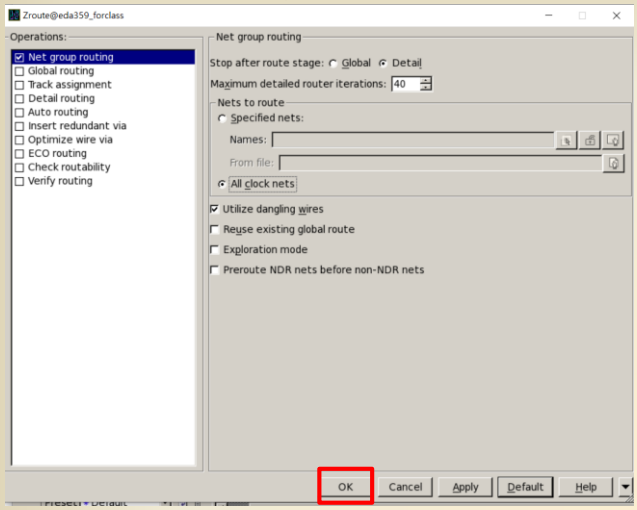
Route

Step2. “Route > Routing Setup > Set Common Route Option…”



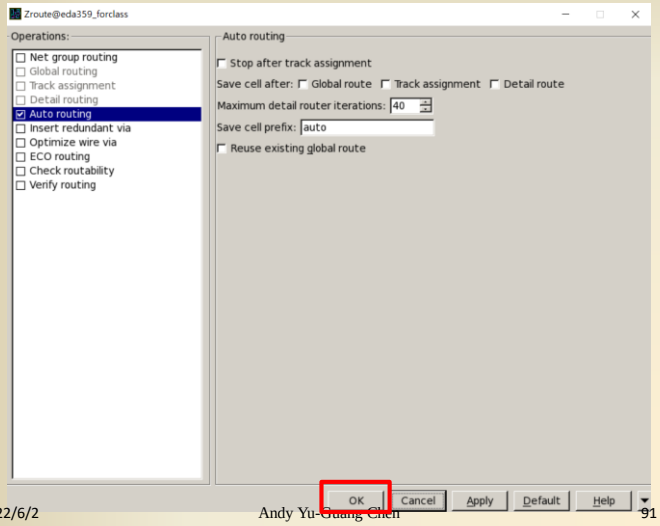
Route

Step3. “Route > Net Group Route…”



Route

Step4. “Route > Auto Route…”

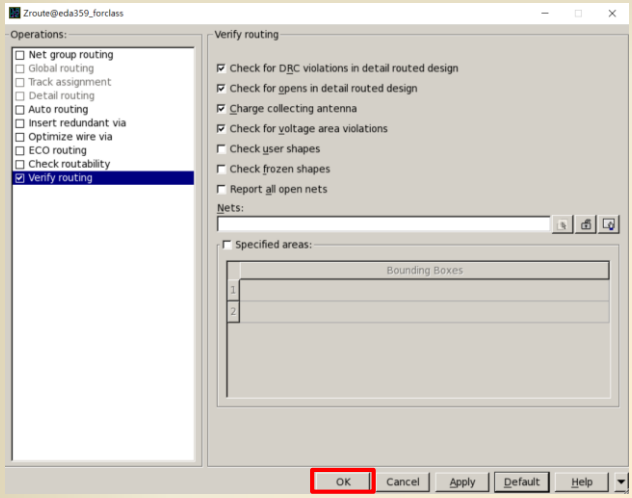


Route

Q16. Print Screen “Auto Route…”. _____

Route

Step5. “Route > Verify Route…”

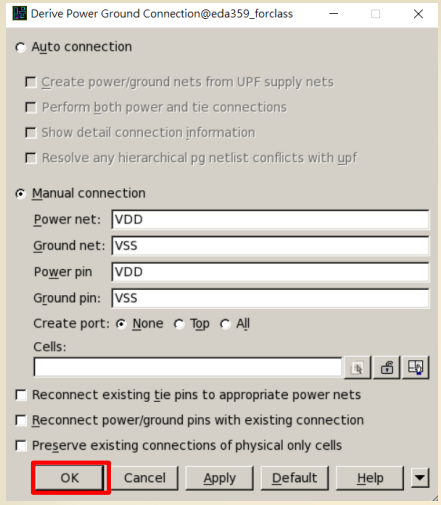


Route

Q17. Print Screen “Verify Summary”. (Step6) _____

Route

Step6. “Preroute > Derive PG connection…”



Route

Step7. Save design

```
icc_shell>  save_mw_cel  -design "lab5"
icc_shell>  save_mw_cel -design "lab5" -as " route "
icc_shell>  quit
```