



EE6094 CAD for VLSI Design



Tool Exercise

Spring 2022

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1



Introduction



- ◆ This exercise provides an opportunity for you to use two commercial EDA tools from Synopsys for front-end and back-end design procedure
 - Design Compiler
 - IC Compiler
- ◆ You are given an RTL design and the goal is to generate a GDSII Layout
- ◆ You need to submit a report to answer all questions during the tool exercise
- ◆ **Report Submission deadline: 6/17(Fri) 23:59:59**
 - Within 24hrs delay: 20% off
 - Within 48hrs delay: 40% off
 - More than 48hrs: 0 point
- ◆ Grading
 - Report 100%



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2



Requirement

- ◆ You are asked to submit a report for your tool exercise assignment
- ◆ The report should at least include:
 - The Answer of each questions
 - The difficulties you encountered and how you solve the problems
 - What you learn from this assignment
 - Suggestions of this assignment
- ◆ Name your file as StudID_Name_tool_report.pdf (ex: 9862534_陳聿廣_tool_report.pdf).
 - Note that the only acceptable report file format is .pdf, no .doc/.docx or other files are acceptable.
 - Please upload your report to ee-class before deadline



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3



Download File

1. Download file "PA5.tar.gz" from ee-class.
2. Upload "PA5.tar.gz" to server.
3. Unzip file "PA5.tar.gz", `$ tar zxvf PA5.tar.gz`
4. `$ cd PA5`



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4



Design Compiler

(Front End Design Procedure)



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5



Design Compiler(DC)



1. `$ cd dc_lab/`
2. Source license
`$ source /usr/cad/synopsys/CIC/synthesis.cshrc`
3. Active Design Compiler
`$ dv&`



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6

Design Compiler(DC)

DC command line

```

Design Compiler Graphical
  DC Ultra (TM)
  DFTMAX (TM)
Power Compiler (TM)
  DesignWare (R)
  DC Expert (TM)
  Design Vision (TM)
  HDL Compiler (TM)
  VHDL Compiler (TM)
  DFT Compiler
  Design Compiler(R)

Version M-2016.12 for linux64 - Nov 21, 2016

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Inc. This software may only be used in accordance with the terms and conditions
of a written license agreement with Synopsys, Inc. All other use, reproduction,
or distribution of this software is strictly prohibited.

Initializing...
design_vision> 4.1
design_vision>

```



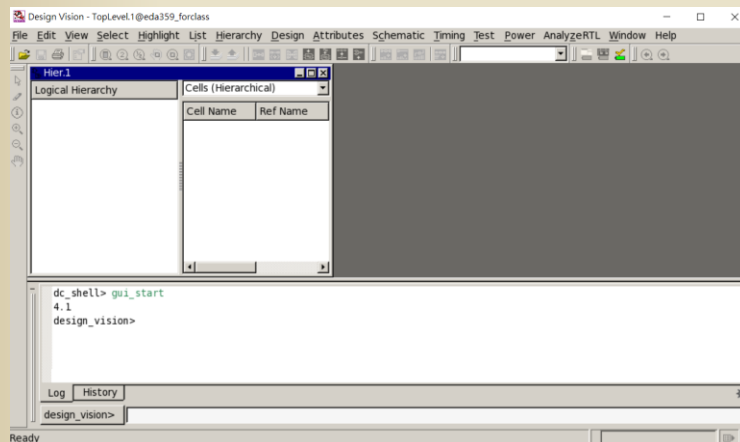
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7

Design Compiler(DC)

DC GUI



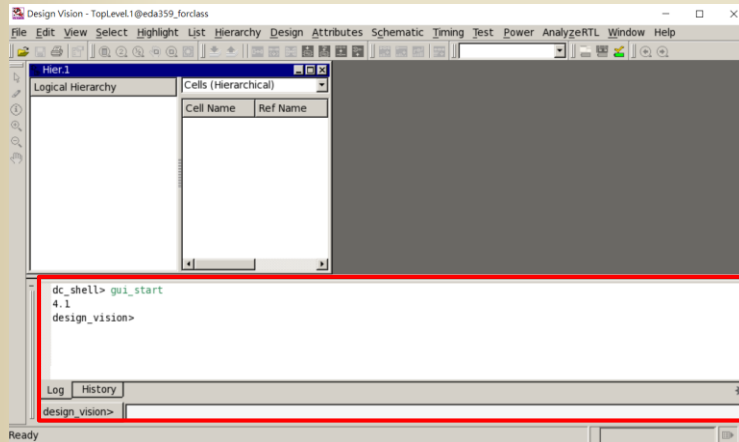
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8

Design Compiler(DC)

Terminal: design vision



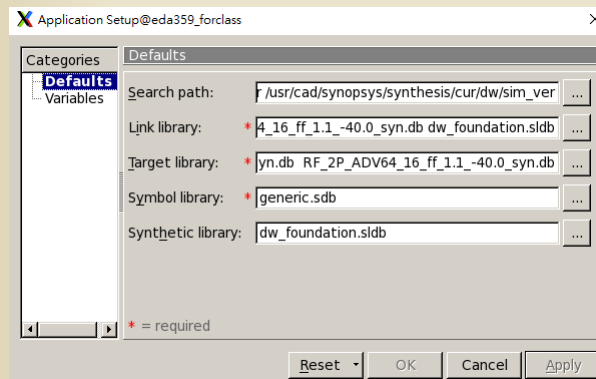
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9

Design Compiler(DC)

Step1. Check setup (File > Setup...)



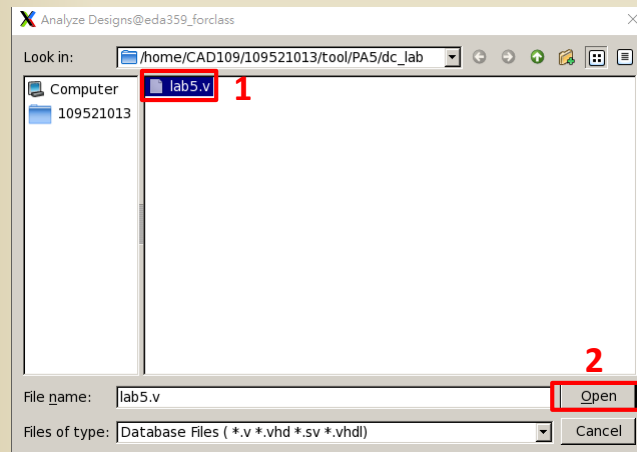
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10

Design Compiler

Step2. Load design files "lab5.v" (File > Analyze ...)



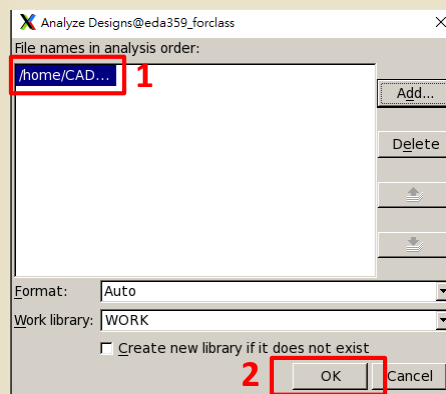
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11

Design Compiler

Step3. Load design files "lab5.v"



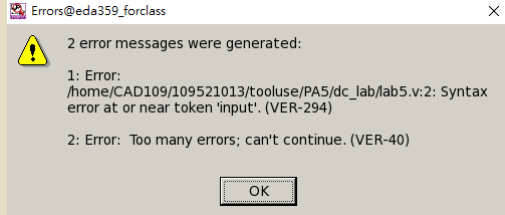
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12

Design Compiler

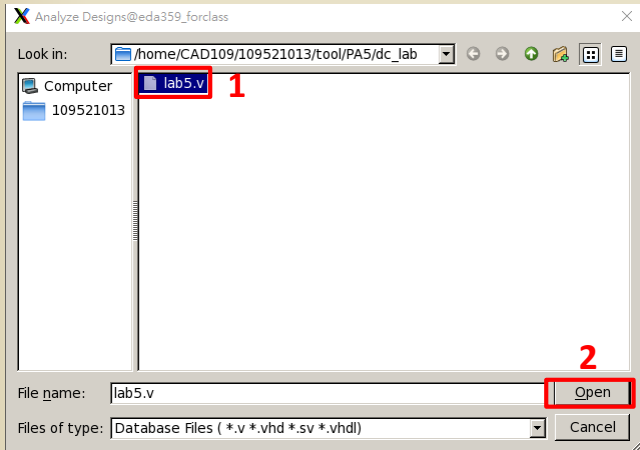
Step4. Find the error code in “lab5.v”, and go back to step 2, reload the file “lab5.v” until the error window doesn’t pop up.



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Design Compiler

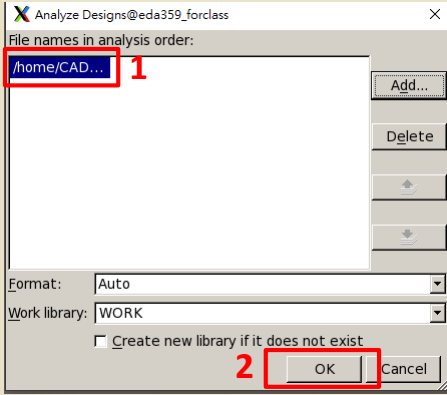
Step5. Reload design files “lab5.v” (File > Analyze ...)



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Design Compiler

Step6. Reload design files “lab5.v”



Analyze Designs@eda359_forclass

File names in analysis order:

/home/CAD... 1

Add...

Delete

Format: Auto

Work library: WORK

☐ Create new library if it does not exist

OK 2 Cancel

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15

Design Compiler

Step7. Reload design files “lab5.v” successfully

```
design_vision> analyze -format verilog {/home/CAD109/109521013/tooluse/PA5/dc_lab/lab5.v}
Running PRESTO HDLC
Compiling source file /home/CAD109/109521013/tooluse/PA5/dc_lab/lab5.v
Presto compilation completed successfully.
```

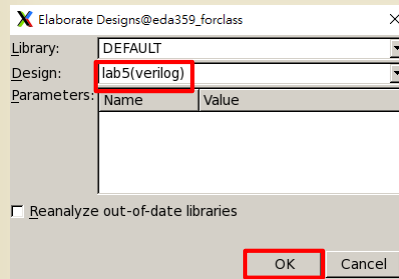
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16

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Step8. Select toplevel module "lab5.v" (File > Elaborate...)



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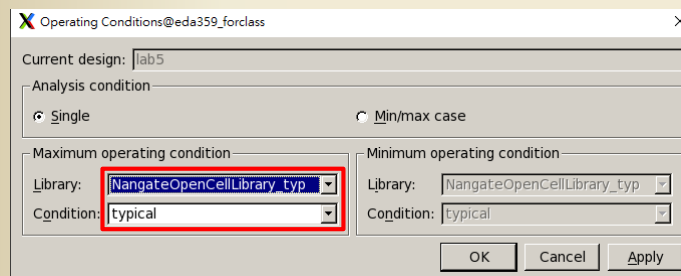
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17

Design Compiler

Step9. Setting operating conditions

(Attributes > Operating Environment > Operating Conditions...)



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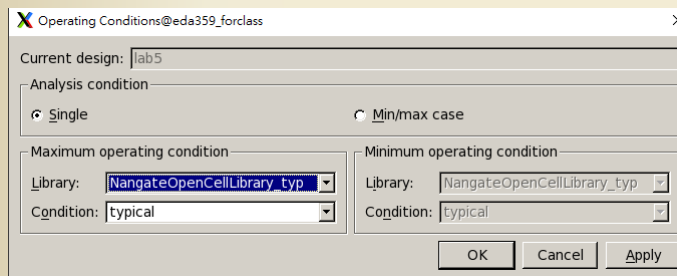
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18

Design Compiler

Setting operating conditions (optional)

1. Maximum operating condition (for setup time analysis):
Library: slow, Condition: slow
2. Minimum operating condition (for hold time analysis):
Library: fast, Condition: fast



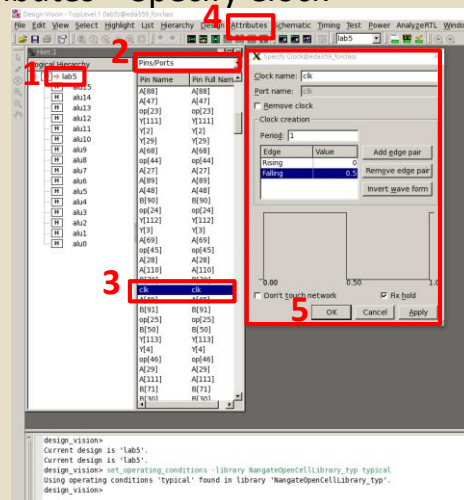
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19

Design Compiler

Step10. Attributes > Specify Clock



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20



Design Compiler



Step11. (In command line)

```
design_vision> set ClockName clk
```

```
design_vision>
```

```
set_ideal_network -no_propagate [get_ports $ClockName]
```



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21



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Step12. (In command line)

```
design_vision>
```

```
set_input_delay 0 -clock [get_clocks $ClockName] \  
[remove_from_collection [all_inputs] [get_ports $ClockName]]
```

```
design_vision>
```

```
set_output_delay 0 -clock [get_clocks $ClockName] [all_outputs]
```



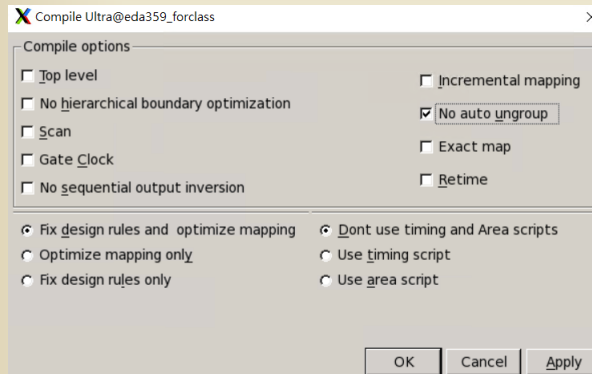
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22

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Step13. Design > Compile Ultra



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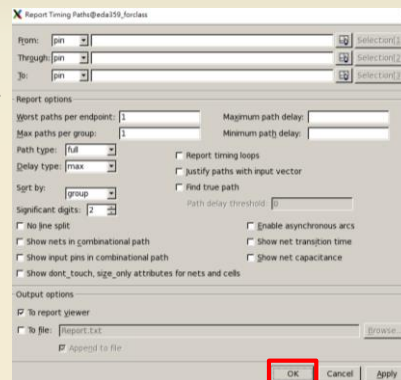
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23

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Step14. Use "Timing > Report timing path..." to see the timing

Q1. data required time = _____
 data arrival time = _____
 slack (VIOLATED) = _____



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24



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Step15. Adjust the Specify Clock and let timing slack ≥ 0



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25



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Step16. (In command line)

```
design_vision> set ClockName clk
```

```
design_vision>
```

```
set_ideal_network -no_propagate [get_ports $ClockName]
```



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26



Design Compiler



Step17. (In command line)

```
design_vision>
```

```
set_input_delay 0 -clock [get_clocks $ClockName] \  
[remove_from_collection [all_inputs] [get_ports $ClockName]]
```

```
design_vision>
```

```
set_output_delay 0 -clock [get_clocks $ClockName] [all_outputs]
```



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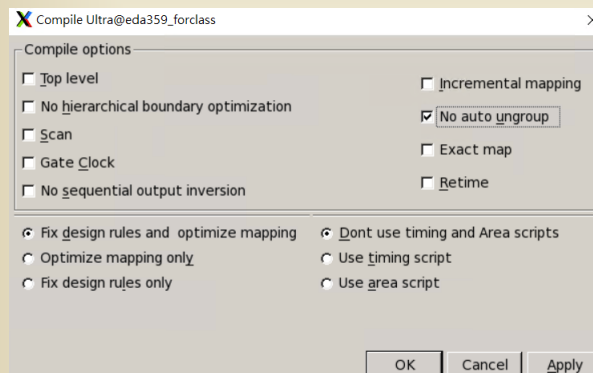
27



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Step18. Design > Compile Ultra



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28

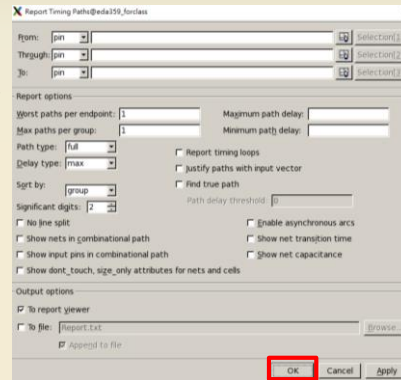


Design Compiler



Step19. Use “Timing > Report timing path...” to see the timing

Q2. data required time = _____
 data arrival time = _____
 slack (VIOLATED) = _____



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29

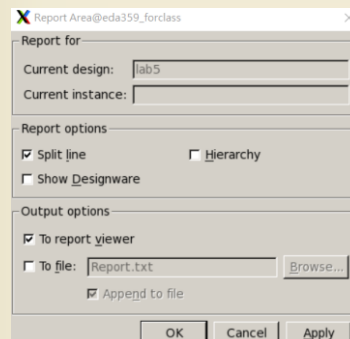


Design Compiler



Step20. Use “Design/Report Area...” to see the area

Q3. Total cell area = _____



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30



Design Compiler



Q4. Please print screen of Critical Path. _____
(Schematic > Add Paths From/Through/To...)



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31



Design Compiler



Step22. Generate Legal Verilog Netlist
(In command line)
design_vision> change_names -hierarchy -rules verilog



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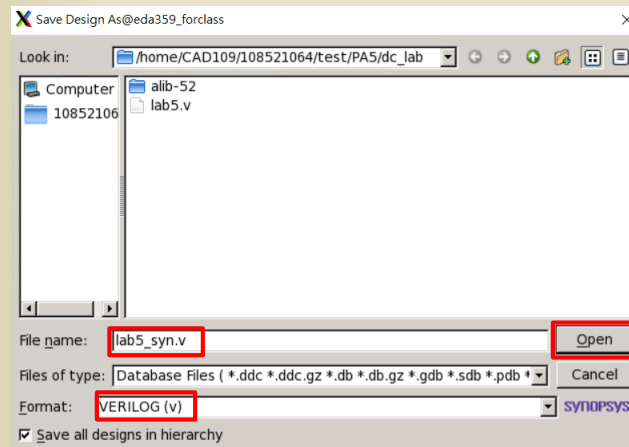
32



Design Compiler



Step23. Save Gate-Level Netlist (File > Save as)



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33



Design Compiler



Step24. Write SDF file

(In command line)

```
design_vision> write_sdf -version 1.0 lab5.sdf
```

Step25. Write SDC file

(In command line)

```
design_vision> write_sdc lab5.sdc
```

Step26. Close Design Vision GUI

(In command line)

```
design_vision> quit
```



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34



IC Compiler

(Back-end Design Procedure)



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35



IC Compiler(ICC)

1. Change directory to ~/icc_lib/run
\$ cd ../icc_lib/run/
2. Copy design data from DC directory to ICC directory
\$ cp ../../dc_lab/lab5.sdc ../design_data/
\$ cp ../../dc_lab/lab5.sdf ../design_data/
\$ cp ../../dc_lab/lab5_syn.v ../design_data/

```
[108521064@eda359_forclass dc_lab]$ cd ../icc_lib/run/
[108521064@eda359_forclass run]$ cp ../../dc_lab/lab5.sdc ../design_data/
[108521064@eda359_forclass run]$ cp ../../dc_lab/lab5.sdf ../design_data/
[108521064@eda359_forclass run]$ cp ../../dc_lab/lab5_syn.v ../design_data/
```



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36



IC Compiler(ICC)



1. Source
\$ source /usr/cad/synopsys/CIC/icc.cshrc
2. Active Design Compiler
\$ icc_shell -gui

```
[108521064@eda359_forclass run]$ source /usr/cad/synopsys/CIC/icc.cshrc
Platform = amd64
[108521064@eda359_forclass run]$ icc_shell -gui
```



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37



IC Compiler(ICC)



ICC command line

```
IC Compiler (TM)
IC Compiler-PC (TM)
IC Compiler-XP (TM)
IC Compiler-DP (TM)
IC Compiler-AG (TM)

Version N-2017.09-SP2 for linux64 - Nov 27, 2017

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Initializing...
icc_shell> Information: Visibility is turned ON for cells and cell contents because
I-026)
icc_shell> █
```



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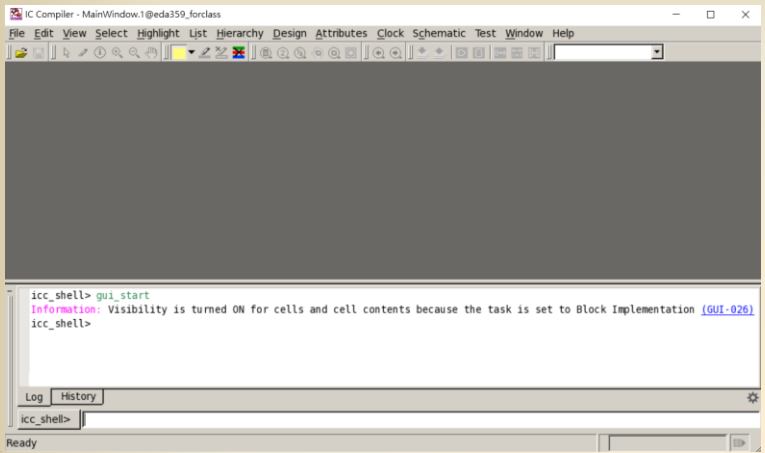

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38

IC Compiler(ICC)



ICC GUI


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39

1. Design Setup



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40

Design Setup

Step1. "File > Create Library..."

lab5

../tech/NangateOpenCellLibrary.tf

../physical_lib/NangateOpenCellLibrary
../physical_lib/RF_2P_ADV64_16
../physical_lib/tpz

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41

Design Setup

Step2. "File > Import Designs..."

../design_data/lab5_syn.v

lab5

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42



Design Setup



Q5. Please print screen of what you see in IC Compiler LatoutWindow. _____



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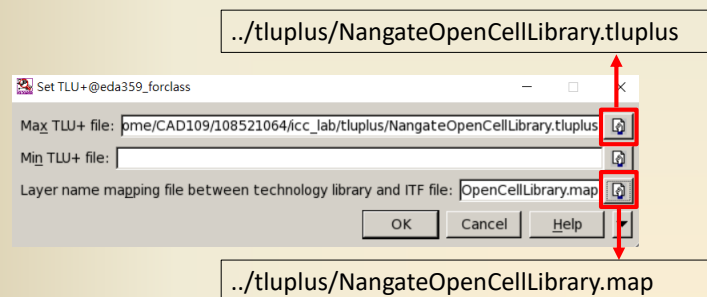
43



Design Setup



Step3. "File > Set TLU+..."



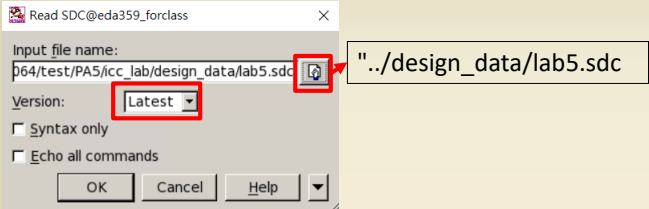
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44

Design Setup

Step4. "File > Import > Read SDC..."



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45

Design Setup


Step5: Save File
(In command line)

```
icc_shell> save_mw_cel -design "lab5"
icc_shell> save_mw_cel -design "lab5" -as "design_setup"
```

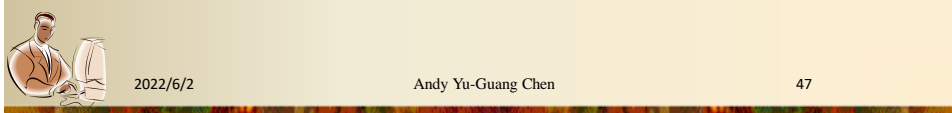
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46



2. Design Planning



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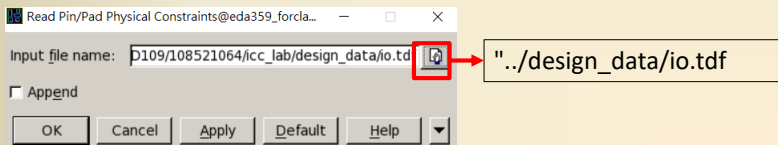


Design Planning

Step1. Add IO, P/G pad, POC pad, and Corner pad

```
icc_shell> source ../scripts/create_phy_cell.tcl
```

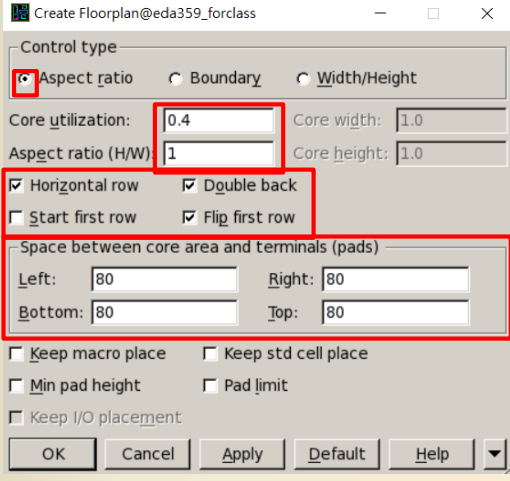
Step2. "Floorplan > Read Pin/Pad Physical Constraints..."
(In LayoutWindows)



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Design Planning

Step3. "Floorplan > Create Floorplan..."



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49

Design Planning

Q6. Please print screen of what you see in IC Compiler LatoutWindow. _____

What is the difference between Q5 and Q6? _____

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50



Design Planning

Step4. "Finishing > Insert Pad Filler..."

PADFILLER20
PADFILLER10 PADFILLER5
PADFILLER1 PADFILLER05
PADFILLER0005
(Sort from big to small)

PADFILLER0005



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51



Design Planning

Step5. save design

```
icc_shell> save_mw_cel -design "lab5"
```

```
icc_shell> save_mw_cel -design "lab5" -as "die_init"
```

Step6. place standard cells

```
icc_shell> create_fp_placement
```



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52



Design Planning

Step7. save design

```
icc_shell> save_mw_cel -design "lab5"
```

```
icc_shell> save_mw_cel -design "lab5" -as "before_PNS"
```



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53



Design Planning

Step8. "Preroute > Derive PG Connection..."

Derive Power Ground Connection@eda359_forclass

☒ Auto connection

- ☐ Create power/ground nets from UPF supply nets
- ☐ Perform both power and tie connections
- ☐ Show detail connection information
- ☐ Resolve any hierarchical pg netlist conflicts with upf

☒ Manual connection

Power net: VDD

Ground net: VSS

Power pin: VDD

Ground pin: VSS

Create port: ☒ None ☐ Top ☐ All

Cells:

☐ Reconnect existing tie pins to appropriate power nets

☐ Reconnect power/ground pins with existing connection

☐ Preserve existing connections of physical only cells

OK Cancel Apply Default Help



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54

Design Planning

Q7. How many connected power ports and ground ports in this project? _____ , _____

```
Information: Saved design named before_PNS. (UIG-5)
1
icc_shell> derive_pg_connection -power_net {VDD} -ground_net {VSS} -power_pin {VDD} -ground_pin {VSS}
Information: [redacted] ???
1
icc_shell>
Log History
icc_shell>
```



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55

Design Planning

Step9. "Preroute > Power Network Constraints > Strap
Layers Constraints..."

Layer: metal4 (17) **1**

☒ Vertical ☐ Horizontal

Density: ☐ By strap number: Max: 10 Min: 3
☐ By pitch: Max: Min:

Width: Max: 4.000 Min: 4.000

PG spacing: ☒ Minimum ☐ Interleaving ☐ Microns:

Offset:

2 Set Remove Remove All Default

Layer	Direction	Max Strap	Min Strap	Max Pitch	Min Pitch
metal4 vertical	vertical	10	3		

Close Help

Layer: metal5 (19) **3**

☒ Vertical ☐ Horizontal

Density: ☐ By strap number: Max: 10 Min: 3
☐ By pitch: Max: Min:

Width: Max: 4.000 Min: 4.000

PG spacing: ☒ Minimum ☐ Interleaving ☐ Microns:

Offset:

4 Set Remove Remove All Default

Layer	Direction	Max Strap	Min Strap	Max Pitch	Min Pitch
metal4 vertical	vertical	10	3		
metal5 horizontal	horizontal	10	3		

5 Close Help



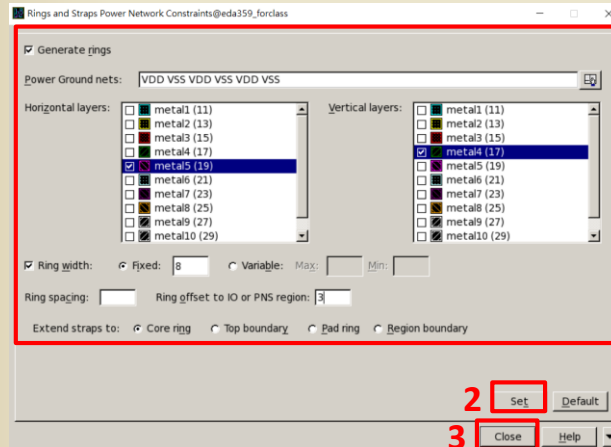
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56

Design Planning

Step10. "Preroute > Power Network Constraints > Ring Constraints..."



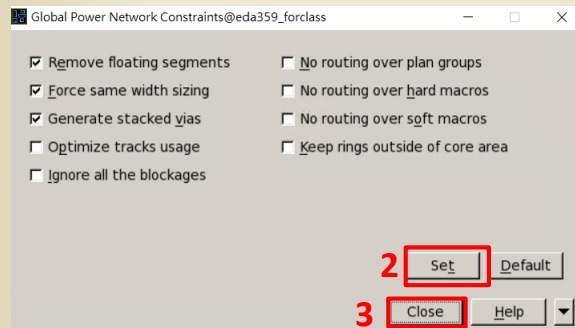
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57

Design Planning

Step11. "Preroute > Power Network Constraints > Global Constraints..."



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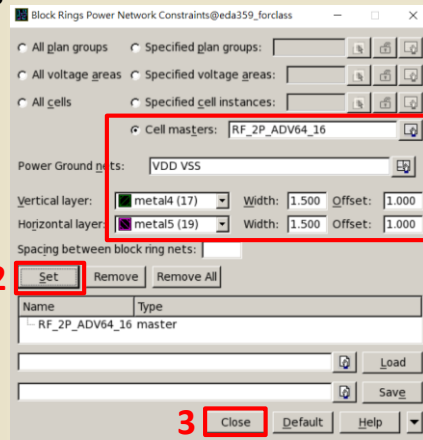
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58



Design Planning

Step12. "Preroute > Power Network Constraints > Block Ring Constrains..."



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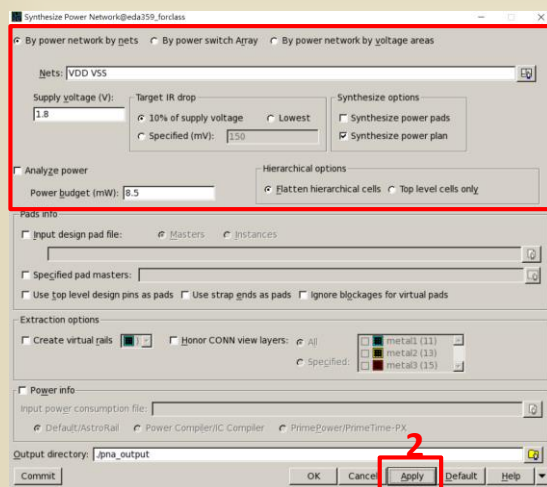
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59



Design Planning

Step13. "Preroute > Synthesize Power Network..."



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60



Design Planning

- Q8. (a) Please print screen IR drop map. _____
 (b) Explain IR drop. _____

Close

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Design Planning

Step13. "Preroute > Synthesize Power Network..."

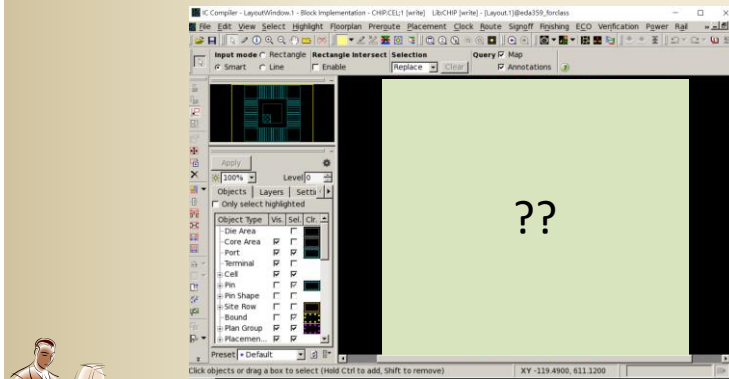
Commit 1

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Design Planning

Q9. Please print screen of what you see in IC Compiler LayoutWindow. _____



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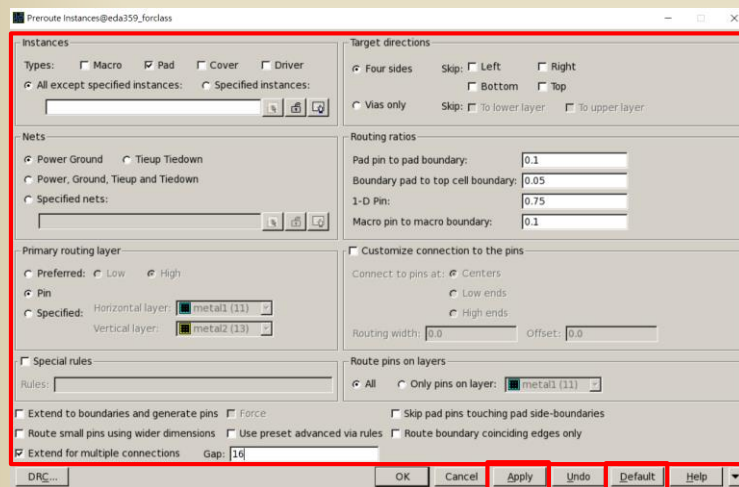
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63



Design Planning

Step14. "Preroute > Preroute Instances..."



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64

Design Planning

Step15. “Preroute > Preroute Instances”

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Design Planning

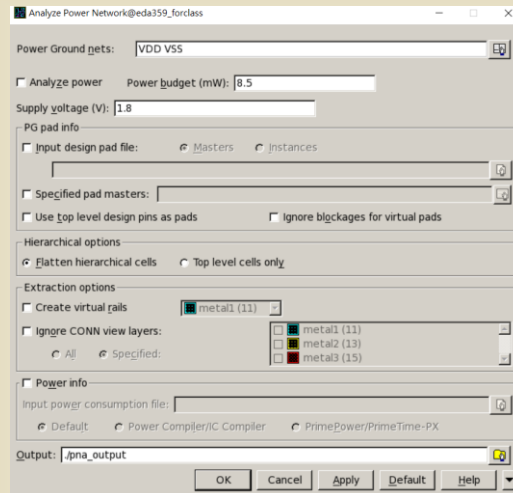
Step16. “Preroute > Preroute Standard Cells...”

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Design Planning

Step17. "Preroute > Analyze Power Network..."



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67



Design Planning

Step18.

```
icc_shell> set_pnet_options -partial "metal4 metal5"
```

```
icc_shell> create_fp_placement -incremental all
```

Step19. save design

```
icc_shell> save_mw_cel -design "lab5"
```

```
icc_shell> save_mw_cel -design "lab5" -as "design_planning"
```



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68

3. Placement

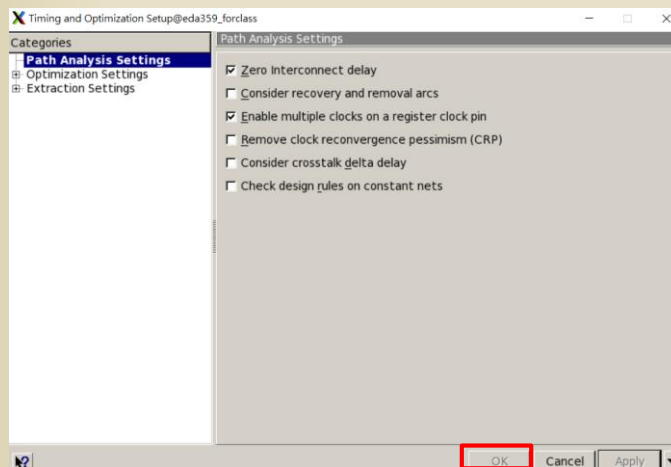
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69

Placement

Step1. "Timing > Timing and Optimization Setup..."



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70



Placement

Q10. data required time = _____

data arrival time = _____

slack (MET) = _____

(icc_shell> report_timing)



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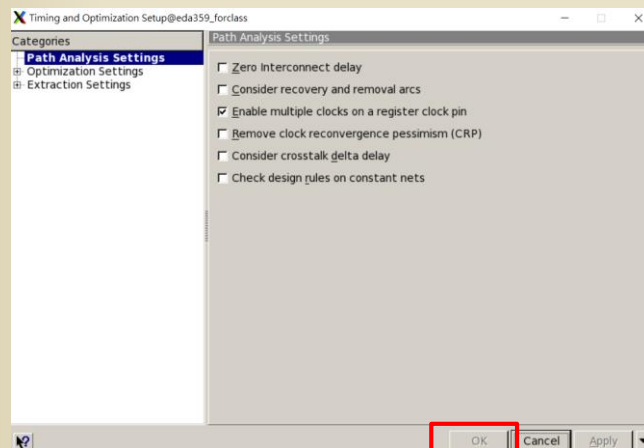
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71



Placement

Step2. "Timing > Timing and Optimization Setup..."



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72



Placement

Q11. data required time = _____

data arrival time = _____

slack (MET) = _____

(icc_shell> report_timing)



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73



Placement

Q12. Internal power = _____

Switching power = _____

Leakage power = _____

(icc_shell> report_power)



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74



Placement

Step3. The following commands should be executed before performing place_opt.

```
icc_shell> check_physical_design -stage pre_place_opt
```

Step4. Setup the tie cell option

```
icc_shell> source ../scripts/add_tie.tcl
```



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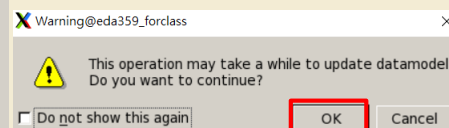
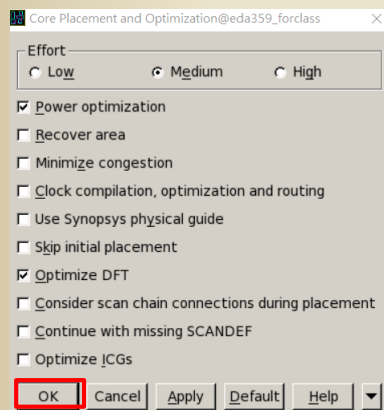
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75



Placement

Step5. "Placement > Core Placement and Optimization..."



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76



Placement

Q13. data required time = _____

data arrival time = _____

slack (VIOLATED) = _____

(icc_shell> report_timing)



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77



Placement

Step6. "Preroute > Derive PG Connection"

Derive Power Ground Connection@eda359_forclass

☐ Auto connection

- ☐ Create power/ground nets from UPF supply nets
- ☐ Perform both power and tie connections
- ☐ Show detail connection information
- ☐ Resolve any hierarchical pg netlist conflicts with upf

☒ Manual connection

Power net:

Ground net:

Power pin:

Ground pin:

Create port: ☒ None ☐ Top ☐ All

Cells:

- ☐ Reconnect existing tie pins to appropriate power nets
- ☐ Reconnect power/ground pins with existing connection
- ☐ Preserve existing connections of physical only cells



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78



Placement

Q14. Internal power = _____

Switching power = _____

Leakage power = _____

Are the answers of Q12 and Q14 different? _____

(icc_shell> report_power)



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79



Placement

Step7. save design

```
icc_shell> save_mw_cel -design "lab5"
```

```
icc_shell> save_mw_cel -design "lab5" -as "design_planning"
```



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80



4. CTS



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81



CTS

Step1. Check

```
icc_shell> check_physical_design -stage pre_clock_opt
```

Q15. Have any error? _____

Step2.

```
icc_shell> set_fix_hold [all_clocks]
```



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82



CTS



Step3. Perform CTS optimization

```
icc_shell> clock_opt -fix_hold_all_clocks -no_clock_route
```



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83



CTS



Step4. Review the global skew after CTS

```
icc_shell> report_clock_tree -summary
```



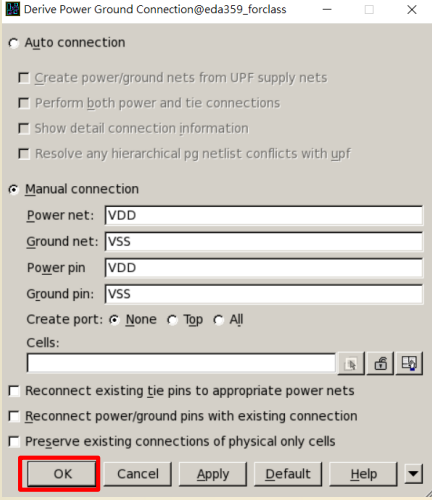
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84

CTS

Step6. "Preroute > Derive PG Connection"



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85

CTS

Step7. Save design

```
icc_shell> save_mw_cel -design "lab5"
icc_shell> save_mw_cel -design "lab5" -as "cts"
```

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86

5. Route

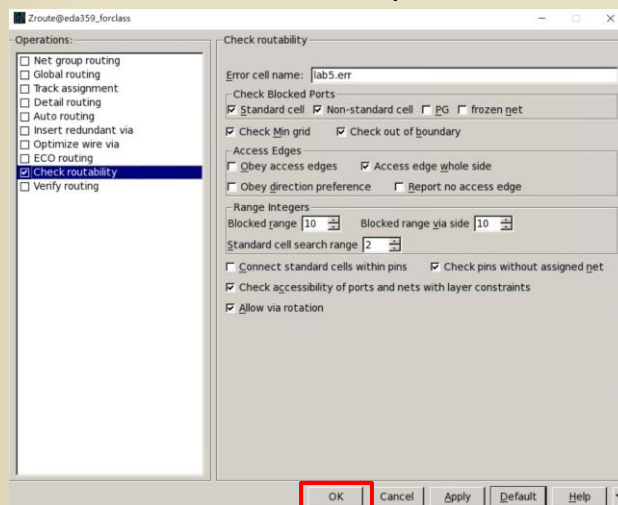
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87

Route

Step1. "Route > Check Routability..."



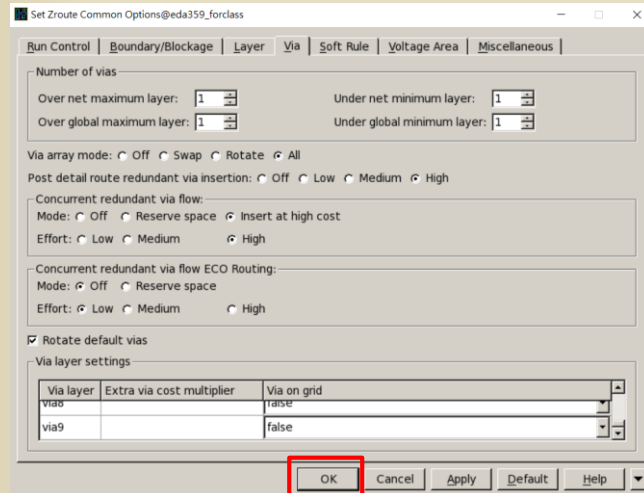
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88

Route

Step2. "Route > Routing Setup > Set Common Route Option..."



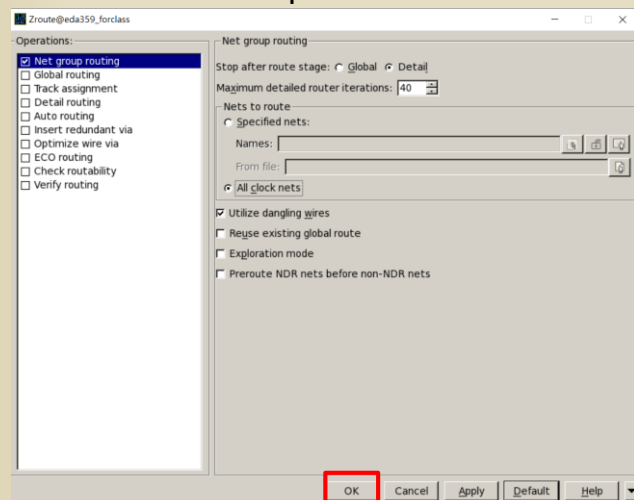
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89

Route

Step3. "Route > Net Group Route..."



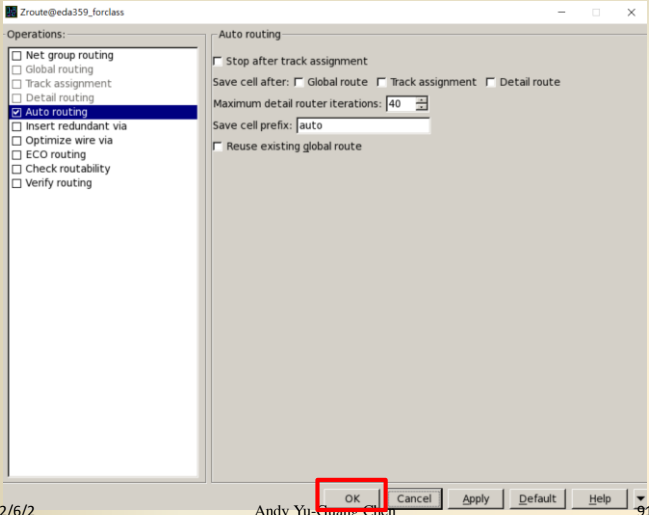
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90

Route

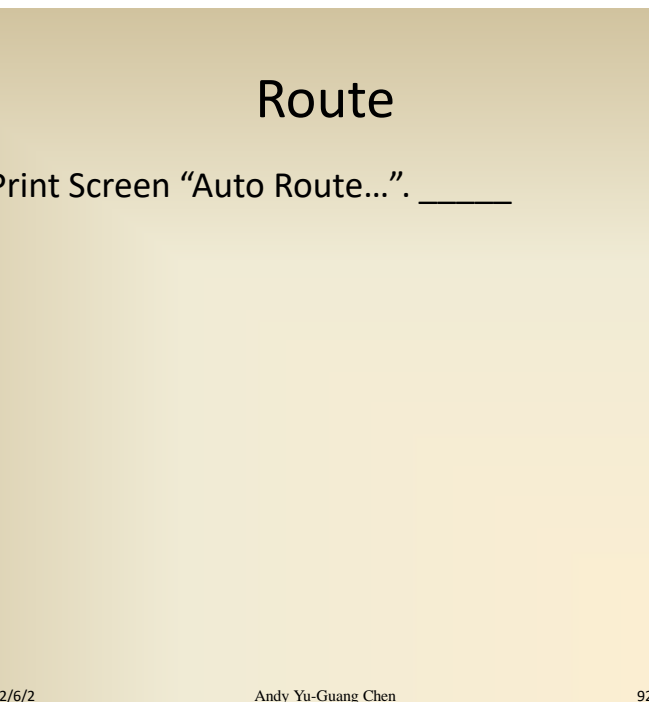
Step4. "Route > Auto Route..."




2022/6/2 Andy Yu-Guang Chen 91

Route

Q16. Print Screen "Auto Route...". _____

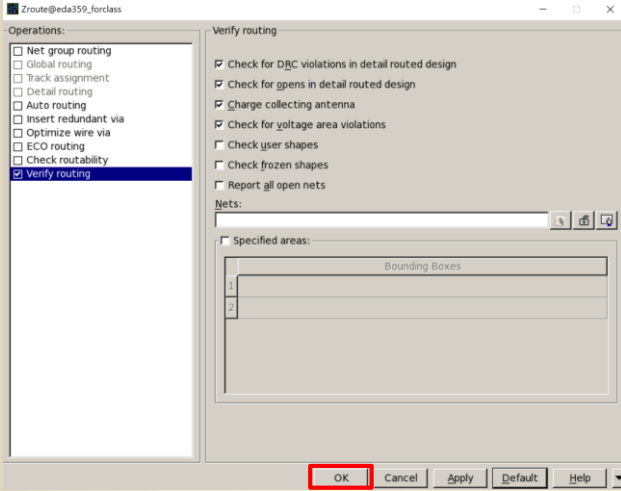


2022/6/2 Andy Yu-Guang Chen 92



Route


Step5. "Route > Verify Route..."



2022/6/2



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93



Route

Q17. Print Screen "Verify Summary". (Step6) _____

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94



Route



Step6. "Preroute > Derive PG connection..."

Derive Power Ground Connection@eda359_forclass

☒ Auto connection

☐ Create power/ground nets from UPF supply nets

☐ Perform both power and tie connections

☐ Show detail connection information

☐ Resolve any hierarchical pg netlist conflicts with upf

☒ Manual connection

Power net: VDD

Ground net: VSS

Power pin: VDD

Ground pin: VSS

Create port: ☒ None ☐ Top ☐ All

Cells:

☐ Reconnect existing tie pins to appropriate power nets

☐ Reconnect power/ground pins with existing connection

☐ Preserve existing connections of physical only cells

OK Cancel Apply Default Help



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95



Route



Step7. Save design

```
icc_shell> save_mw_cel -design "lab5"
icc_shell> save_mw_cel -design "lab5" -as "route "
icc_shell> quit
```



2022/6/2

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96