EE6094

CAD for VLSI Design

Hardware Trojan Detection With VCS & Verdi

Andy, Yu-Guang Chen
Assistant Professor, Department of EE
National Central University
andyygchen@ee.ncu.edu.tw

Slides Credit: TA李宗穎

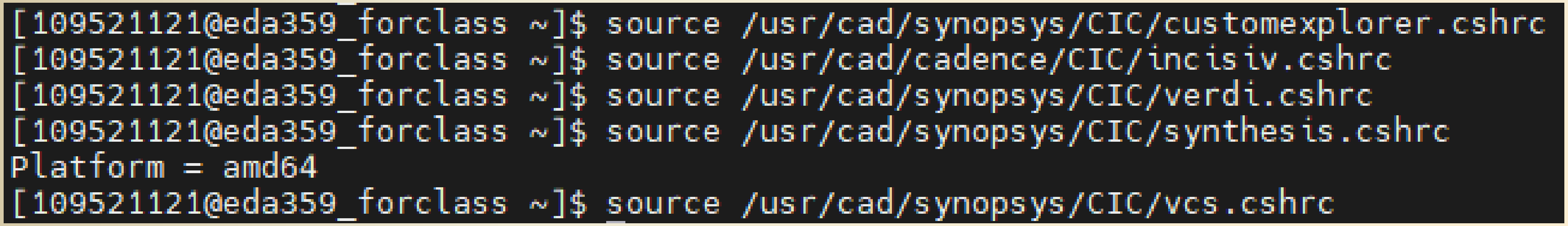
Outline

- ◆Verilog with VCS & Verdi
- ◆Examples

Verilog with VCS & Verdi

◆Source

- ➢ Step1: Key in the following source commands.
  source /usr/cad/synopsys/CIC/customexplorer.cshrc
  source /usr/cad/cadence/CIC/incisiv.cshrc
  source /usr/cad/synopsys/CIC/verdi.cshrc
  source /usr/cad/synopsys/CIC/synthesis.cshrc
  source /usr/cad/synopsys/CIC/vcs.cshrc

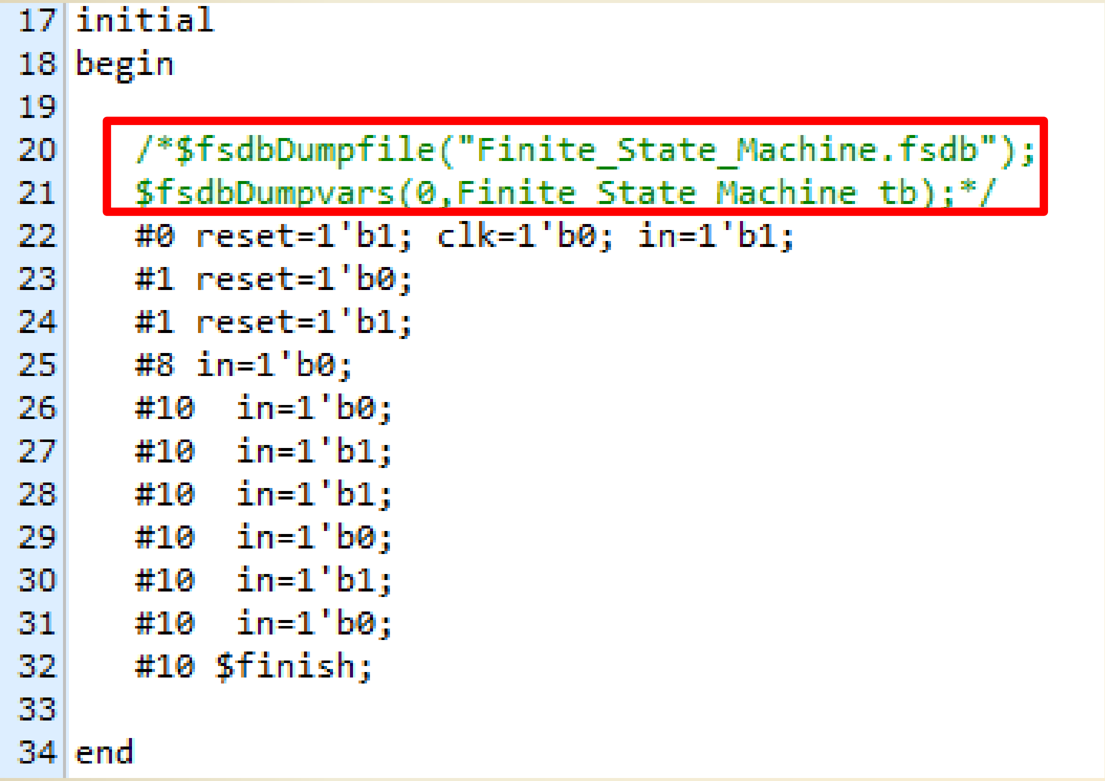


```
[109521121@eda359_forclass ~]$ source /usr/cad/synopsys/CIC/customexplorer.cshrc
[109521121@eda359_forclass ~]$ source /usr/cad/cadence/CIC/incisiv.cshrc
[109521121@eda359_forclass ~]$ source /usr/cad/synopsys/CIC/verdi.cshrc
[109521121@eda359_forclass ~]$ source /usr/cad/synopsys/CIC/synthesis.cshrc
Platform = amd64
[109521121@eda359_forclass ~]$ source /usr/cad/synopsys/CIC/vcs.cshrc
```

Verilog with VCS & Verdi

◆VCS & Verdi

- ➢ Step2: Annotate FSDB-related syntax



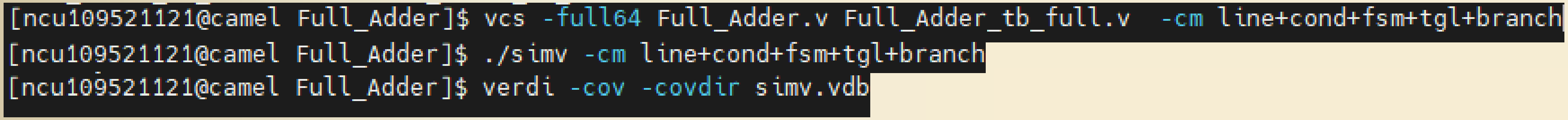
```
initial
begin

    /*$fsdbDumpfile("Finite_State_Machine.fsdb");
    $fsdbDumpvars(0,Finite_State_Machine_tb);*/
    #0 reset=1'b1; clk=1'b0; in=1'b1;
    #1 reset=1'b0;
    #1 reset=1'b1;
    #8 in=1'b0;
    #10  in=1'b0;
    #10  in=1'b1;
    #10  in=1'b1;
    #10  in=1'b0;
    #10  in=1'b1;
    #10  in=1'b0;
    #10 $finish;

end
```

Verilog with VCS & Verdi

◆VCS & Verdi

- Step3: Key in the following commands.

vcs -full64 ***.v ***_tb.v -cm line+fsm+tgl+branch
./simv -cm line+fsm+tgl+branch
verdi -cov -covdir simv.vdb



```
[ncu109521121@camel Full_Adder]$ vcs -full64 Full_Adder.v Full_Adder_tb_full.v  -cm line+cond+fsm+tgl+branch
[ncu109521121@camel Full_Adder]$ ./simv -cm line+cond+fsm+tgl+branch
[ncu109521121@camel Full_Adder]$ verdi -cov -covdir simv.vdb
```

Verilog with VCS & Verdi

◆The types of code coverage

- ➢ Line Coverage
  - This gives an indication of how many lines are covered in the simulation
  - This is important in all kinds of design and has to be 100% for verification closure.
- ➢ FSM Coverage
  - FSM coverage reports, whether the simulation run could reach all of the states and cover all possible transitions or arcs in a given state machine.

Verilog with VCS & Verdi

◆The types of code coverage

- ➢ Toggle Coverage
  - Toggle coverage gives a report that how many times signals and ports are toggled during a simulation run.
  - Signal: 1->0 、0->1
- ➢ Branch Coverage
  - In Branch coverage or Decision coverage reports, conditions like if-else, case and the ternary operator (?:) statements are evaluated in both true and false cases.

Verilog with VCS & Verdi

◆The types of code coverage

- ➢ Toggle Coverage
    - Toggle coverage gives a report that how many times signals and ports are toggled during a simulation run.
    - Signal: 1->0 、0->1
- ➢ Branch Coverage
    - In Branch coverage or Decision coverage reports, conditions like if-else, case and the ternary operator (?:) statements are evaluated in both true and false cases.

Verilog with VCS & Verdi

- **Reference**
  - Code Coverage Fundamentals
  - https://vlsi.pro/code-coverage-fundamentals/

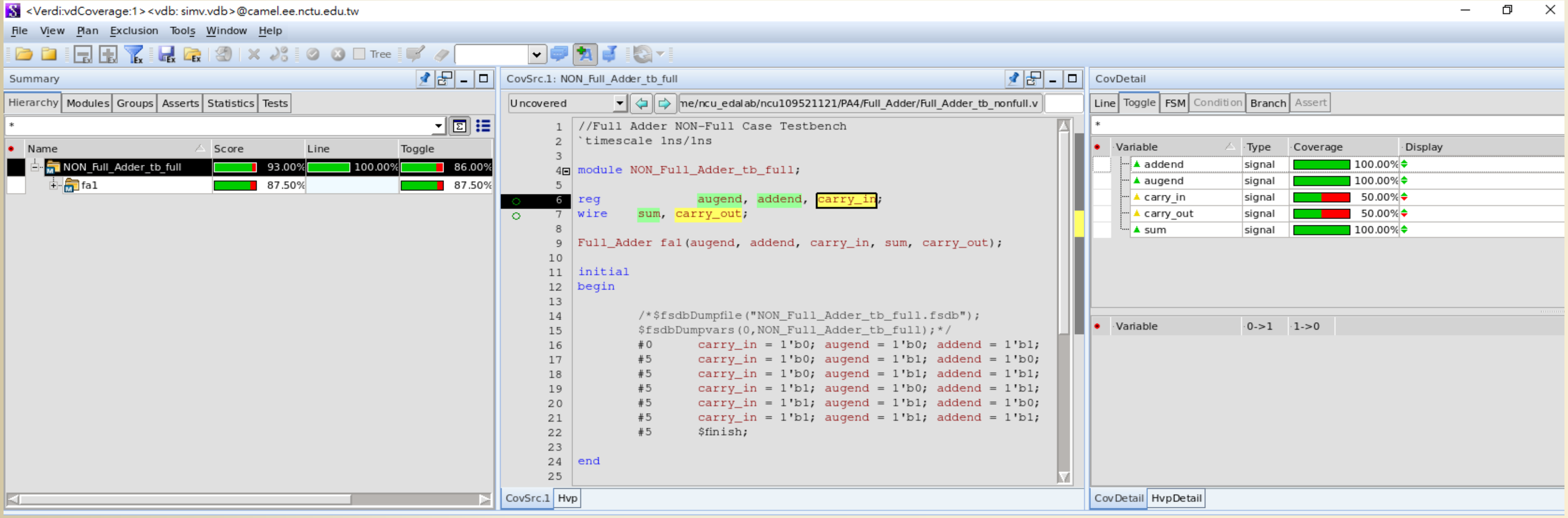
Outline

- Verilog with VCS & Verdi
- Examples

Examples

◆Full Adder

➢ Non Full Condition



<Verdi:vdCoverage:1><vdb: simv.vdb>@camel.ee.nctu.edu.tw
File View Plan Exclusion Tools Window Help
Tree
Summary
Hierarchy Modules Groups Asserts Statistics Tests
*
CovSrc.1: NON_Full_Adder_tb_full
Uncovered
me/ncu_edalab/ncu109521121/PA4/Full_Adder/Full_Adder_tb_nonfull.v
CovSrc.1 Hvp
CovDetail
Line Toggle FSM Condition Branch Assert
*
CovDetail HvpDetail

Name	Score	Line	Toggle
NON_Full_Adder_tb_full	93.00%	100.00%	86.00%
fa1	87.50%		87.50%

```
//Full Adder NON-Full Case Testbench
`timescale 1ns/1ns

module NON_Full_Adder_tb_full;

reg             augend, addend, carry_in;
wire    sum, carry_out;

Full_Adder fa1(augend, addend, carry_in, sum, carry_out);

initial
begin

        /*$fsdbDumpfile("NON_Full_Adder_tb_full.fsdb");
        $fsdbDumpvars(0,NON_Full_Adder_tb_full);*/
        #0      carry_in = 1'b0; augend = 1'b0; addend = 1'b1;
        #5      carry_in = 1'b0; augend = 1'b1; addend = 1'b0;
        #5      carry_in = 1'b0; augend = 1'b1; addend = 1'b1;
        #5      carry_in = 1'b1; augend = 1'b0; addend = 1'b1;
        #5      carry_in = 1'b1; augend = 1'b1; addend = 1'b0;
        #5      carry_in = 1'b1; augend = 1'b1; addend = 1'b1;
        #5      $finish;

end
```

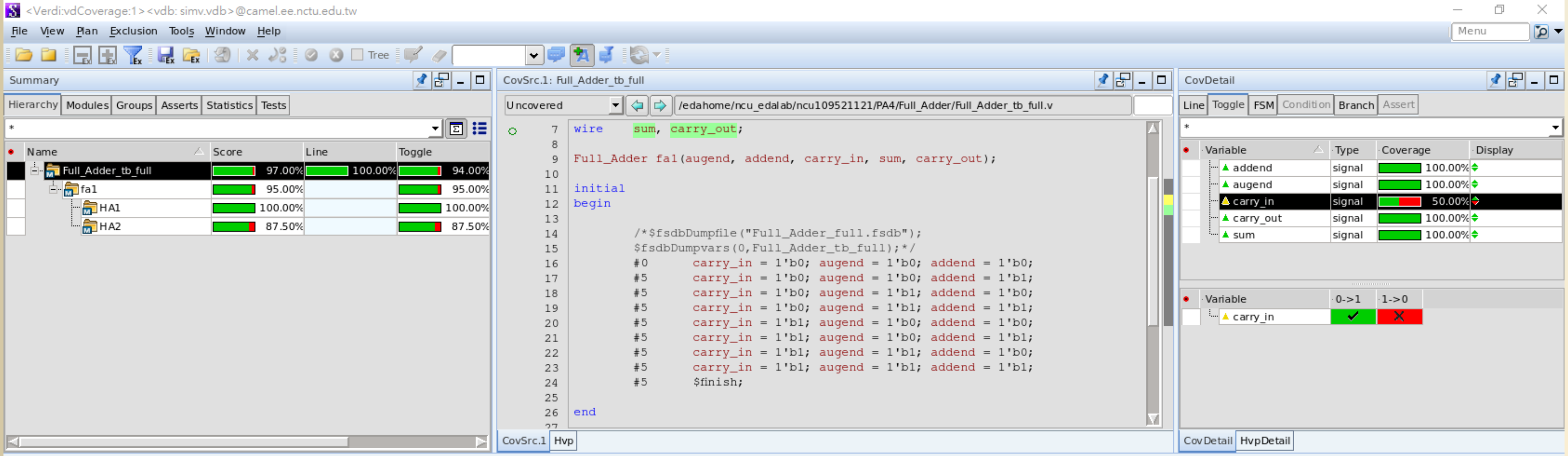
Variable	Type	Coverage	Display
addend	signal	100.00%	
augend	signal	100.00%	
carry_in	signal	50.00%	
carry_out	signal	50.00%	
sum	signal	100.00%	

Variable	0->1	1->0

Examples

◆Full Adder

➢ Full Condition



<Verdi:vdCoverage:1><vdb: simv.vdb>@camel.ee.nctu.edu.tw
File View Plan Exclusion Tools Window Help
Tree
Menu
Summary
Hierarchy Modules Groups Asserts Statistics Tests
*
CovSrc.1: Full_Adder_tb_full
Uncovered
/edahome/ncu_edalab/ncu109521121/PA4/Full_Adder/Full_Adder_tb_full.v
CovSrc.1 Hvp
CovDetail
Line Toggle FSM Condition Branch Assert
*
CovDetail HvpDetail

Name	Score	Line	Toggle
Full_Adder_tb_full	97.00%	100.00%	94.00%
fa1	95.00%		95.00%
HA1	100.00%		100.00%
HA2	87.50%		87.50%

```
wire     sum, carry_out;

Full_Adder fa1(augend, addend, carry_in, sum, carry_out);

initial
begin

        /*$fsdbDumpfile("Full_Adder_full.fsdb");
        $fsdbDumpvars(0,Full_Adder_tb_full);*/
        #0      carry_in = 1'b0; augend = 1'b0; addend = 1'b0;
        #5      carry_in = 1'b0; augend = 1'b0; addend = 1'b1;
        #5      carry_in = 1'b0; augend = 1'b1; addend = 1'b0;
        #5      carry_in = 1'b0; augend = 1'b1; addend = 1'b1;
        #5      carry_in = 1'b1; augend = 1'b0; addend = 1'b0;
        #5      carry_in = 1'b1; augend = 1'b0; addend = 1'b1;
        #5      carry_in = 1'b1; augend = 1'b1; addend = 1'b0;
        #5      carry_in = 1'b1; augend = 1'b1; addend = 1'b1;
        #5      $finish;

end
```

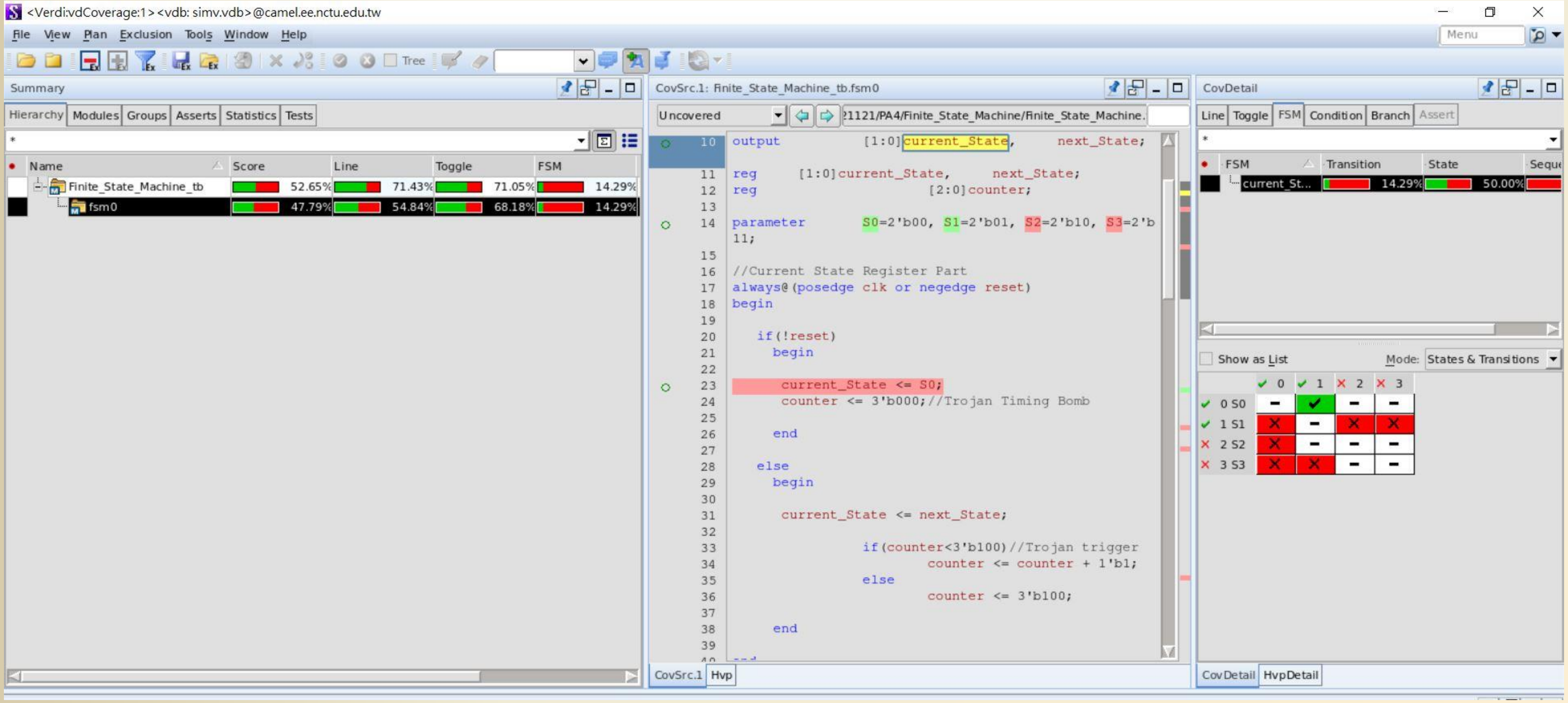
Variable	Type	Coverage	Display
addend	signal	100.00%	
augend	signal	100.00%	
carry_in	signal	50.00%	
carry_out	signal	100.00%	
sum	signal	100.00%	

Variable	0->1	1->0
carry_in	✓	✗

Examples

◆Finite State Machine

➢ Non Full Condition



<Verdi:vdCoverage:1><vdb: simv.vdb>@camel.ee.nctu.edu.tw
File View Plan Exclusion Tools Window Help
Tree
Menu
Summary
Hierarchy Modules Groups Asserts Statistics Tests
CovSrc.1: Finite_State_Machine_tb.fsm0
Uncovered
21121/PA4/Finite_State_Machine/Finite_State_Machine.
CovDetail
Line Toggle FSM Condition Branch Assert
CovSrc.1 Hvp
CovDetail HvpDetail

●	Name	Score	Line	Toggle	FSM
	Finite_State_Machine_tb	52.65%	71.43%	71.05%	14.29%
	fsm0	47.79%	54.84%	68.18%	14.29%

```
output          [1:0]current_State,     next_State;

reg     [1:0]current_State,     next_State;
reg                     [2:0]counter;

parameter       S0=2'b00, S1=2'b01, S2=2'b10, S3=2'b
11;

//Current State Register Part
always@(posedge clk or negedge reset)
begin

   if(!reset)
     begin

      current_State <= S0;
      counter <= 3'b000;//Trojan Timing Bomb

     end

   else
     begin

      current_State <= next_State;

                if(counter<3'b100)//Trojan trigger
                        counter <= counter + 1'b1;
                else
                        counter <= 3'b100;

     end

end
```

●	FSM	Transition	State	Seque
	current_St...	14.29%	50.00%	

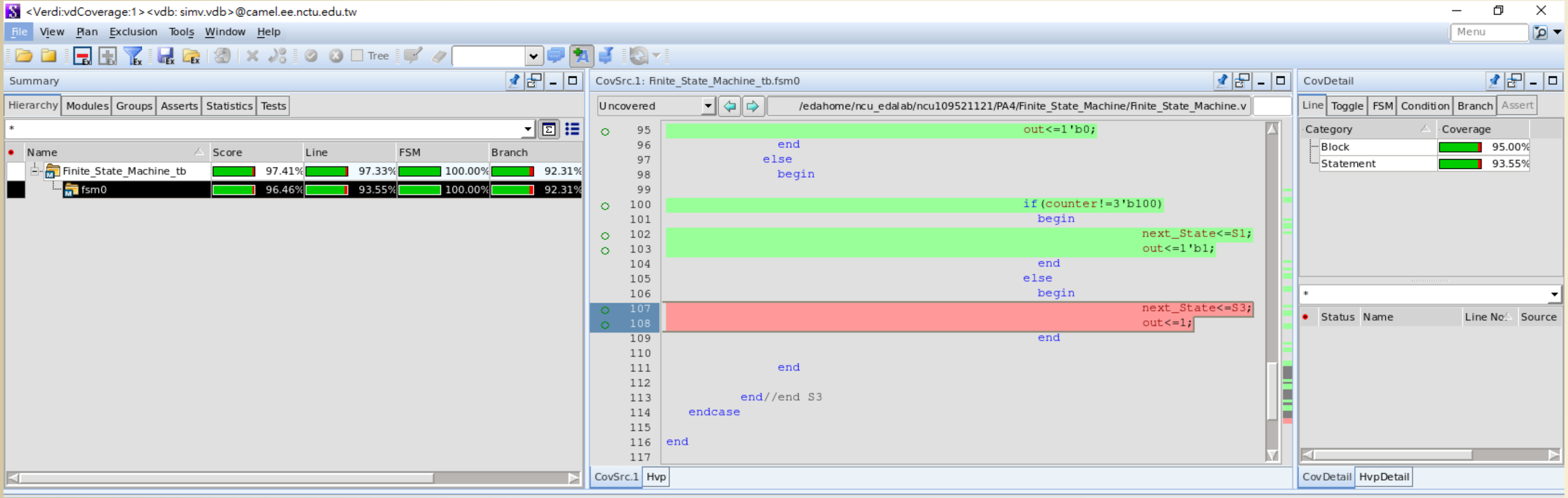
☐ Show as List   Mode: States & Transitions

	✓ 0	✓ 1	✗ 2	✗ 3
✓ 0 S0	–	✓	–	–
✓ 1 S1	✗	–	✗	✗
✗ 2 S2	✗	–	–	–
✗ 3 S3	✗	✗	–	–

Examples

◆Finite State Machine

➢ Full Condition



<Verdi:vdCoverage:1><vdb: simv.vdb>@camel.ee.nctu.edu.tw

Name	Score	Line	FSM	Branch
Finite_State_Machine_tb	97.41%	97.33%	100.00%	92.31%
fsm0	96.46%	93.55%	100.00%	92.31%

CovSrc.1: Finite_State_Machine_tb.fsm0

/edahome/ncu_edalab/ncu109521121/PA4/Finite_State_Machine/Finite_State_Machine.v

```
                        out<=1'b0;
       end
      else
       begin

                        if(counter!=3'b100)
                         begin
                                next_State<=S1;
                                out<=1'b1;
                         end
                        else
                         begin
                                next_State<=S3;
                                out<=1;
                         end

       end

     end//end S3
  endcase

end

```

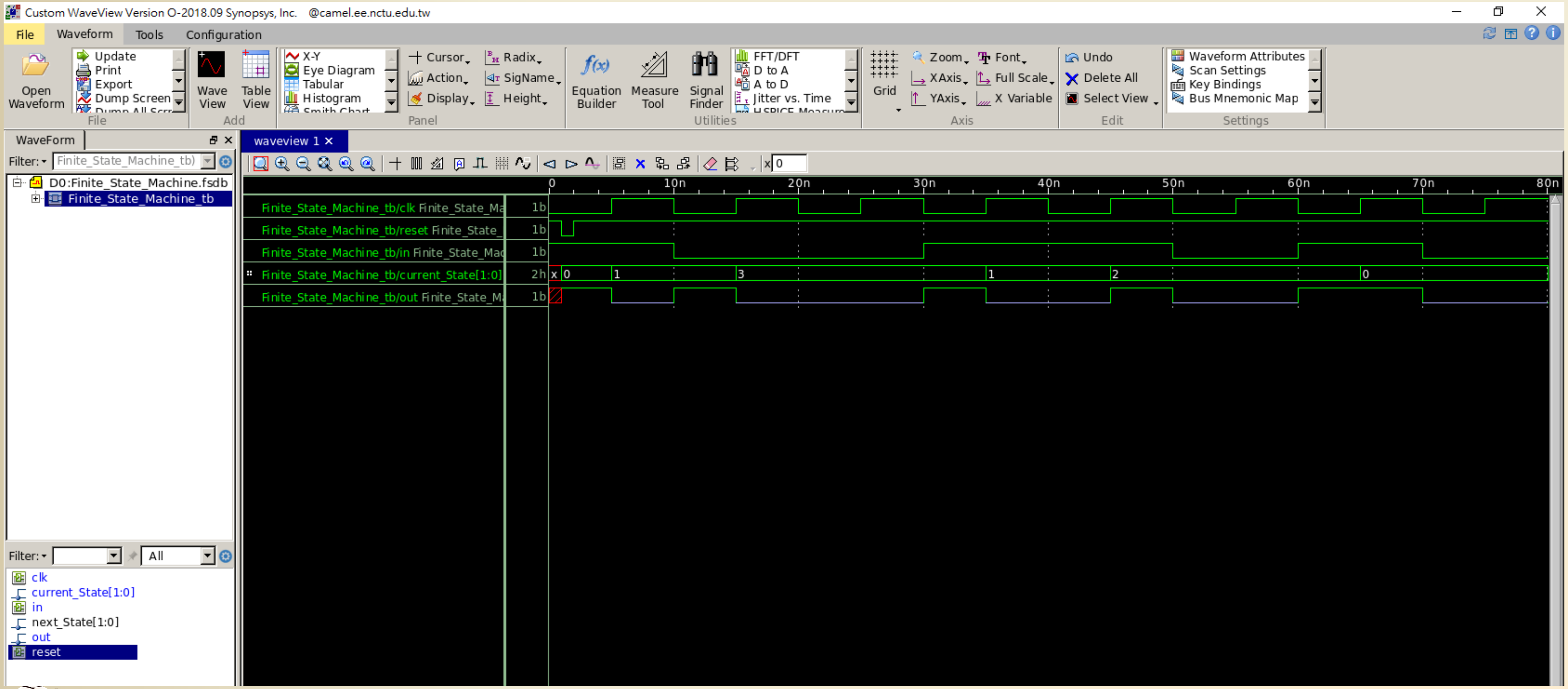
Category	Coverage
Block	95.00%
Statement	93.55%

●	Status	Name	Line No	Source

Examples

◆Finite State Machine

➢ Full Condition



Thank You.