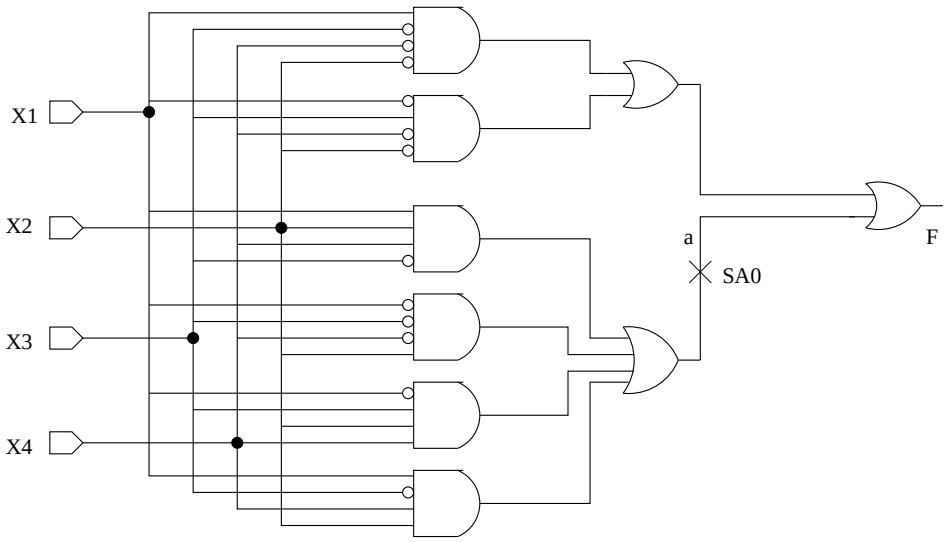
EE6083 VLSI Testing—Homework 3

1. **Signature Analysis**
   Suppose that a modular LFSR with a characteristic polynomial $1+X+X^4$ is used as a signature analyzer for the circuit under test shown below. Please complete the following questions.

   (a) Use Verilog code to realize the LFSR and simulate the signature of the good circuit. (4 points)

   (b) Let line a have an SA0. Simulate the signature if the test sequence is 1,2,3,...,15. (2 points)

No.	X1	X2	X3	X4	F
1	0	0	0	1	1
2	1	1	0	0	1
3	0	1	1	0	0
4	0	0	1	1	0
5	1	1	0	1	0
6	1	0	1	0	0
7	0	1	0	1	0
8	1	1	1	0	1
9	0	1	1	1	1
10	1	1	1	1	0
11	1	0	1	1	1
12	1	0	0	1	0
13	1	0	0	0	1
14	0	1	0	0	1
15	0	0	1	0	0



2. **Syndrome Compaction**
   For the circuit shown below, use the stuck-at test given and find the signature of the good circuit if the time compaction used (a) Parity testing; and (2) one's count. For each scheme, list the undetected faults and explain why they were not detected. (4 points)