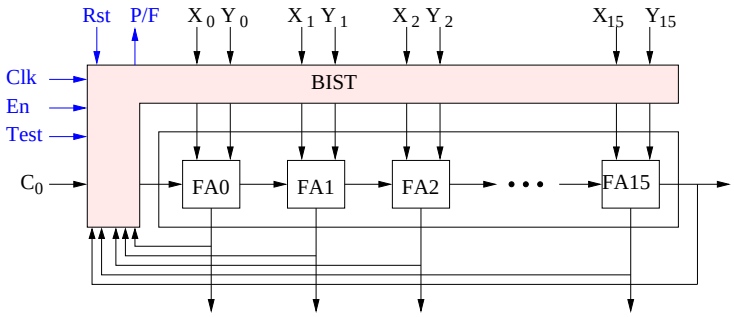
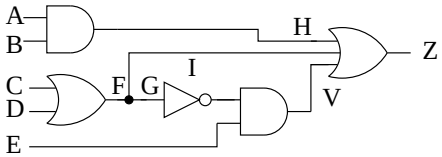
EE6083 VLSI Testing—Homework 1

1. Design BIST circuit for an 16-bit ripple carray adder using Verilog if the single cell fault is targeted. As the figure shown below, the additional test pins are in blue. Test is used to switch the circuit between normal mode and test mode. En is used to assert the embedded pattern generator and P/F is used to indicate the ripple carry adder is fault-free or faulty. (6 points)



2. List the fault list of the circuit shown below if the equivalence and dominance collapsing techniques are used to reduce the fault list. (2 points)



3. The five test vectors will detect all port faults of the circuit shown below. Find a stuck-at fault inside the circuit that is not detected by the five test vectors. (2 points)