EE6083 VLSI Testing—Homework 2

1. **Fault Detection and Diagnosis**
   Consider a two-input multiplexer with with the output f and the inputs g_1 and g_2 and the control signal x_i. Assume that $f = g_1$ when $x_i = 1$ and $f = g_2$ when $x_i = 0$. Then, the Boolean function of the multiplexer can be expressed as $f = x_i g_1 + \overline{x_i} g_2$.

   (a) Derive a complete test set for detecting the stuck-at faults of the two-input multiplexer as shown in Fig. 1(a). (1 points)

   (b) Derive diagnostic test patterns to identify the faults g_0 and g_1 in the four-input multiplexer as shown in Fig. 1(b). (3 points)

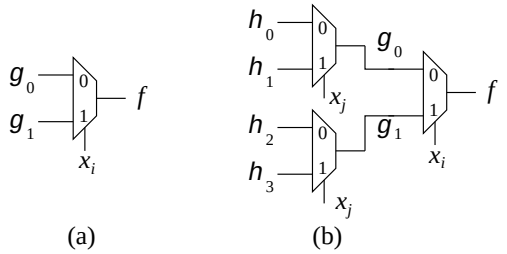

Figure 1: (a) A 2-1 multiplexer (b) A 4-1 multiplexer.

2. **Deductive Fault Simulation**
   Use deductive fault simulation methodology to find the detected faults by the test pattern {ABCDE}={01011} which are applied to the circuit shown in Fig. 2. (2 points)

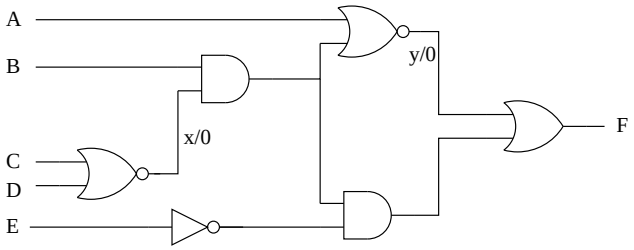

Figure 2: A combinational circuit.

3. **Fault Simulation**
   Implement a serial fault simulator using Verilog for the circuit shown in Fig. 2. Then, use the fault simulator to evaluate the fault coverage of single stuck-at faults of the test patterns {10101, 10010, 00010, 10100}. (4 points)