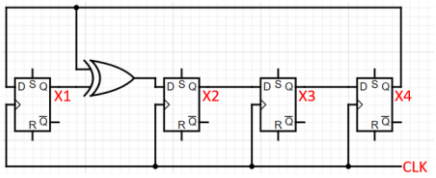
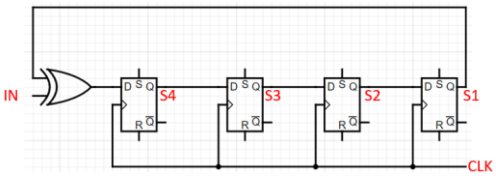
VLSI Testing HW3 110521167 曹寓恆

1.

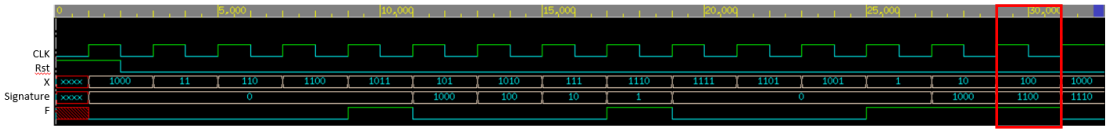


Test pattern generator



Output response analyzer

(a) BIST

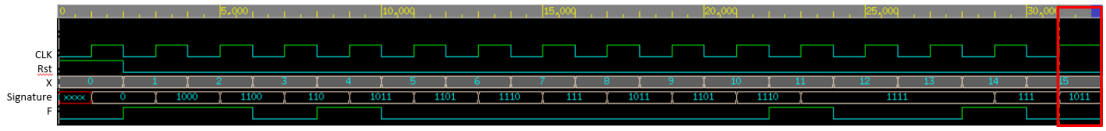


Fault-free sequence(LFSR) = 000_0100_0100_0111

Characteristic polynomial = $1+X+X^4$

Signature = 000_0100_0100_0111 / 1_0011

= 100_1000…1100



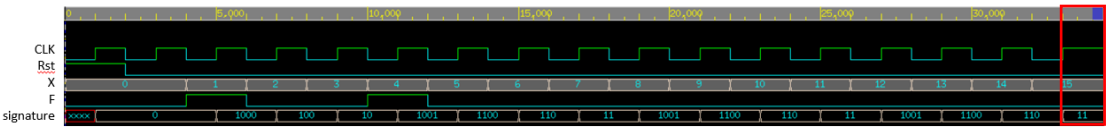
Fault-free sequence(counter) = 011_0100_0001_0010

Characteristic polynomial = $1+X+X^4$

Signature = 0110_1000_0001_0010 / 1_0011

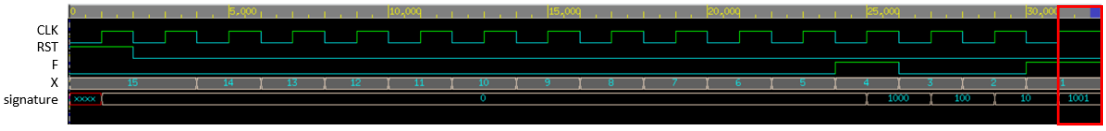
= 110_0010_0111…1011

(b) X = 1,2,3,...,15



a/0 results in a faulty signature = 0011

(c) X = 15, 14, 13,...,1



a/0 results in a faulty signature = 1001

2.

	Output response	Parity check	One count
a/0	10101010	even	4
a/1	00100010	even	2
b/0	10101010	even	4
b/1	00001010	even	2
c/0	00000000	even	0
c/1	00101110	even	4
d/0	00000000	even	0
d/1	00101010	odd	3
e/0	10101010	even	4
e/1	00000000	even	0
f/0	00111111	even	6
f/1	00000000	even	0
z/0	00000000	even	0
z/1	11111111	even	8
Fault-free	00101010	odd	3

Parity check 和 One count 都無法檢查出 d/0，因為針對{c, d} test pattern 不完整缺少{c=1, d=0}，無法 sensitize fault 導致 faulty output response 與 fault-free output response 一致。