Low-Noise 1-, 2-Channel Analog Front-End for ECG and Biopotential Measurements

Features

♦ Single/Dual-channel low-noise analog front-end;

♦ Supply current: ~130 μA (1-channel);

~200 μA (2-channel);

♦ Shut down mode: <0.1 μA;

♦ Low input-referred noise: ~3 μVrms;

♦ Common-mode rejection ratio: ~85 dB (DC-100 Hz);

♦ Single supply operation: 1.8 V to 3.6 V;

♦ Digital IO level: 1.8 V to 3.6 V;

♦ Programmable gain: 50 to 720;

♦ Built-in filter bandwidth: 0.05 to 220 Hz;

♦ Built-in right leg drive amplifier with lead off;

♦ Built-in high precision 1.8 V LDO;

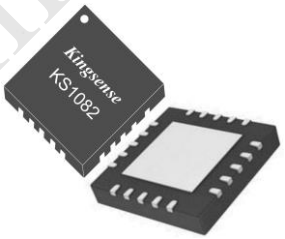
♦ Built-in SPI-compatible serial interface;

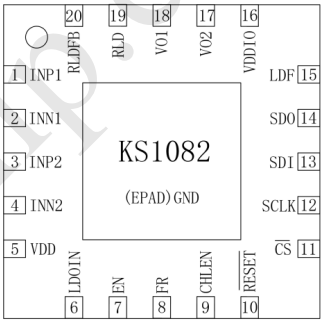
♦ Supports baseline fast restoring;

♦ Supports DC-coupled input;

♦ Supports dry-electrode input;

♦ ±4 kV HBM ESD rating;





Revision History

Rev. 1.0, Initial Version: May. 2018

Rev. 1.1.1, Revised Version: Aug. 2020 (updated application circuits)

Table of Contents

General Description

The KS1081/KS1082 is an integrated single/dual-channel signal conditioning integrated circuit for ECG and other biopotential measurements. It incorporates programmable gain amplifiers (PGAs), filters, internal references, oscillators, digital serial peripheral interface (SPI), right leg drive (RLD) circuitry, and a high precision low dropout regulator (LDO). The KS1081/KS1082 is designed to extract, amplify, and filter small biopotential signals in the presence of noisy conditions, such as those created by motion or remote electrode placement.

The KS1081/KS1082 adopts novel design of input impedance boosting. This feature allows dry electrodes such as metal-plate electrodes and flexible fabric electrodes to be used for weak biopotential recording. It dramatically enhances the user experience for wearable/portable health monitoring.

The KS1081/KS1082 has a flexible and wide-range gain (50 to 720) configuration per channel through the onboard SPI to suit different types of applications.

The KS1081/KS1082 implements a high-pass filter for eliminating motion artifacts and the electrode half-cell potential. Additional low-pass filter is also incorporated to remove additional noise.

The KS1081/KS1082 includes a fast restore function that reduces the duration of the otherwise long settling tails of the high-pass filtering when an abrupt signal changes. This feature allows the KS1081/KS1082 to take valid measurements soon after connecting the electrodes to the subject.

The KS1081/KS1082 also with a built-in RLD amplifier for driven lead applications, which helps improve the common-mode rejection of the line frequencies in the system and other undesired interferences.

The KS1081/KS1082 is packaged in a 3 mm×3 mm, 20-pin quad flat no-lead pack (QFN). Performance is specified from 0°C to 70°C and is operational from −40°C to +85°C.

Benefit for high level integration and exceptional low noise performance, the KS1081/KS1082 allows an analog-to-digital converter (ADC) with medium-resolution or an embedded microcontroller to easily acquire the target signal. It enables the development of scalable wearable/portable health monitoring (ECG/Heart rate) devices and medical instrumentation systems (ECG/EMG, etc.) at significantly reduced size, power and overall cost.

Applications

• Wearable/Portable Health Devices

- Wearable ECG/Heart rate devices (ECG watch/wristband, etc.);
- Finger ECG/Heart rate recording;
- Fitness, sports, and training;
- Gaming peripherals;

• Medical Equipment

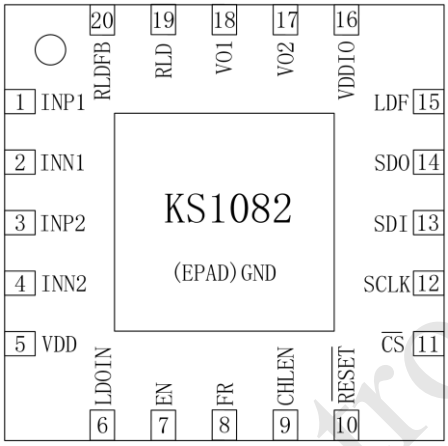
- Clinic ECG monitors;
- HRV monitors;
- Mobile/Remote ECG monitors, such as holter, etc.

• High-Precision Signal Acqusitions

- Biosignal such as EMG/Sleep/Blood Pressure, etc.
- Other signals such as Pressure, Tempreature, Light, etc.

Pin Configuration and Description

Pin Configuration



Pin Description

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	INP1(1)	Analog input	Differential analog positive input 1.
2	INN1(1)	Analog input	Differential analog negative input 1.
3	INP2(1)(2)	Analog input	Differential analog positive input 2. (2)
4	INN2(1)(2)	Analog input	Differential analog negative input 2. (2)
5	VDD	Supply	Internal LDO output, 1.8V.
6	LDOIN	Supply	Internal LDO input. Chip power supply 1.8-3.6V.
7	EN	Digital input	Chip enable input. Active High. Connected to LDOIN or external logic high. Drive EN low to enter the low power shutdown mode.
8	FR	Digital input	Fast restore control input. Drive FR high to enable fast recovery mode; other wise, drive it low.
9	CHLEN(3)	Digital input	Signal channel enable input. Details see *SPI Registers* setting.
10	$\overline{\text{RESET}}$	Digital input	System reset. Active low. Connect to VDD, if not used.
11	$\overline{\text{CS}}$	Digital input	SPI Chip select. Active low.
12	SCLK	Digital input	SPI master clock input.
13	SDI	Digital input	SPI data in.
14	SDO	Digital output	SPI data out.
15	LDF(4)	Digital output	Leads off detection output. Logic high for leads off and logic low for leads on.
16	VDDIO	Supply	Digital interface (SPI) IO level control input (typical 1.8/3.3 V).
17	VO2(2)	Analog output	Signal channel 2 output. Connected to the input of an ADC.
18	VO1	Analog output	Signal channel 1 output. Connected to the input of an ADC.
19	RLD	Analog output	Right leg drive output. Connect to the driven electrode.
20	RLDFB	Analog input	Right leg drive feedback input. Feedback terminal for the right leg drive circuit.
EPAD	GND	Supply	Exposed pad. Chip supply ground. Connects to the global ground.

*(1) connect to GND if not used.

*(2) available for dual-channel chip KS1082.

*(3) available for KS1082. To enable channel 1 and 2 simultaneously, configure both CHLEN and SPI ***CHLnSET*** register are required.

*(4) only supports RLD lead off detection in strong power line interference condition.

Electrical Characteristics

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. LDOIN = 1.8 V to 3.3 V ± 10%, VDD = 1.8 V, VCM = VDD/2. All specifications are at VDD = 1.8 V, GND = 0 V, Gain=360, unless otherwise noted.

Symbol	Parameter	Test Conditions/Note	Min.	Typ.	Max.	Unit
Analog Input						
	Differential Input Mode		DC-coupling			
V_{in}	Differential Input Range		(VDD-0.15)/Gain			V
V_{dc_diff}	DC Differential Input Range		-180		180	mV
$R_{in,amp}$	DC Input Impedance	No pull-up or pull-down current source		~5		GΩ
		Pull-up or pull-down current source		15		MΩ
Channel Performance						
A_v	Gain Setting	The first stage	5, 9			
		The second stage	10, 20, 30, 40, 60, 80			
BW	Bandwidth		0.05		220	Hz
CMRR	Common-Mode Rejection Ratio	Vcm=0.9 V, Vc=0 V, f=DC to 100 Hz		85		dB
PSRR	Power Supply Rejection Ratio	LDOIN=1.8 V to 3.3 V	75	95		dB
V_n	Input-Referred Noise	f = 0.1 Hz to 220 Hz		3		μVrms
Right Leg Drive Circuitry						
	Out Voltage Swing		0.1		VDD -0.1	V
R_{RLD}	Load Resistor		10		100	kΩ
GDP	Gain Bandwidth Product			10		kHz
Logic Interface						
V_{IH}	Input Voltage High		1.3			V
V_{IL}	Input Voltage Low				0.4	V
V_{OH}	Output Voltage High		0.9× VDDIO			V
V_{OL}	Output Voltage Low				0.3	V
System Specification						

LDOIN	Supply Range		1.8	1.8/ 3.3	3.6	V
V_{LDO}	LDO Output Voltage	LDOIN=1.8V		1.79		V
		LDOIN=3.3V		1.8		V
V_{drop}	LDO drop-out Voltage	LDO output (PIN 5: VDD)		10	30	mV
I_{supply}	Supply Current	Single-channel, LDOIN=1.8 to 3.3V		130		µA
		Dual-channel, LDOIN=1.8 to 3.3V		200		µA
I_L	Load Current	LDO output (PIN 5: VDD)		10	30	mA
T_{st}	Startup Time	Supply voltage=1.8 to 3.6V	60		100	µS
I_{leak}	Shutdown Current	EN=Low		0.5		µA
I_L	Load Current	LDO output (PIN 5: VDD)		10	30	mA
C	Load Capacitor	LDO output (PIN 5: VDD)	0.5		4.7	µF
T_a	Operation Temperature	Normal mode	0		+70	℃
ESD	ESD Ratings	Human body model (HBM)		±4		kV
		Charged device model (CDM)		±500		V

Absolute Maximum Ratings*

Symbol	Parameter	Test Conditions	Value	Unit
LDOIN	Supply Voltage	LDOIN to GND	1.65 to 3.7	V
VDDIO	Digital Interface Logic Level	VDDIO to GND	1.65 to 3.7	V
Ta	Operational Temperature		-40 to +85	℃
ESD	ESD Ratings	Human body model (HBM)	8	kV
		Charged device model (CDM)	1	kV

*Stresses at or above those listed under Absolute Maximum Ratings may, or will, cause permanent damage to the product. This is a stress rating only, and functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may degrade device performance and affect product reliability.

ESD Caution

ESD (Electrostatic Discharge) sensitive device.
Although this product features priority protection circuitry, damage may occur on devices subjected to high energy ESD or improper handling and installation procedure. ESD damage can range from subtle performance degradation to complete device failure. Therefore, appropriate ESD precautions should be taken to avoid performance degradation or loss of functionality, particularly for precision integrated circuits.

Theory of Operation

Architecture Overview

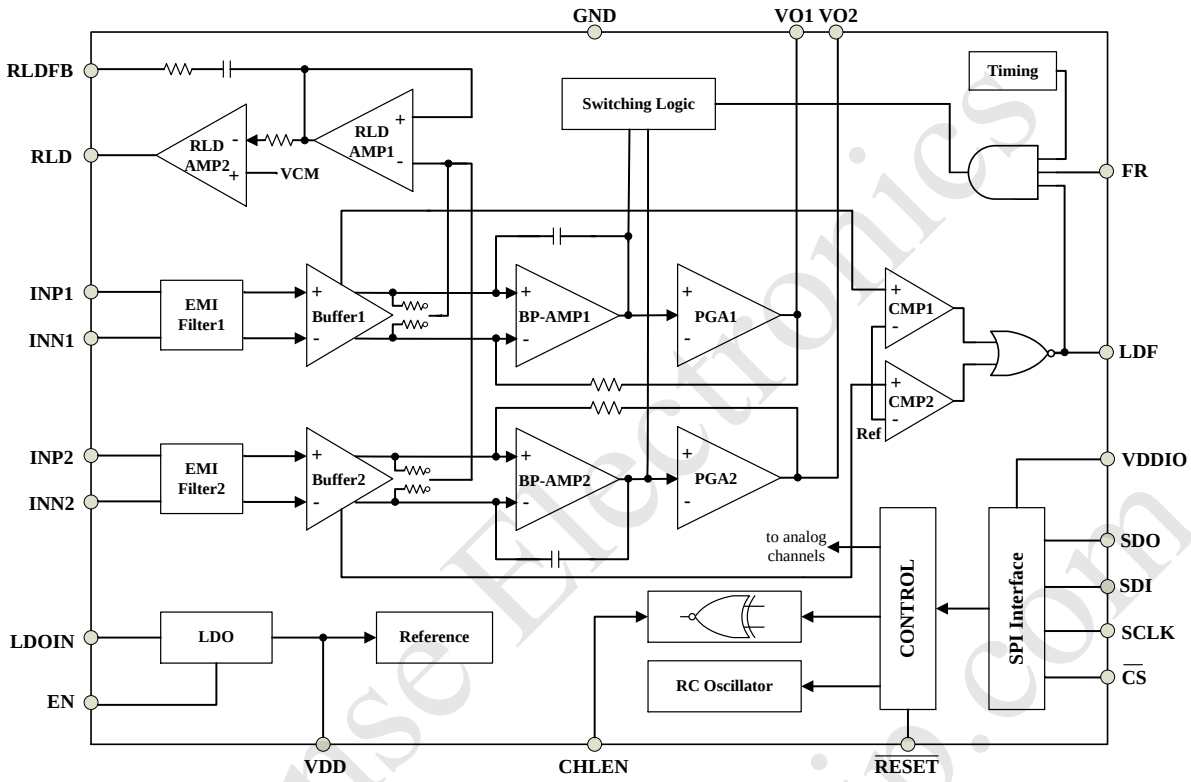


Figure 1. Function Block Diagram

The KS1081/KS1082 is an integrated single/dual-channel front end for signal conditioning of small biopotentials monitoring. Each channel consists of a buffer with high input impedance, a band-pass amplifier (BP-AMP) and a low noise and programmable gain amplifier (PGA). The KS1081/ KS1082 contains a specialized band-pass amplifier with suitable bandwidth for low frequency biopotential and an optimized low noise amplifier with wide-range gain setting that can be configured by the serial peripheral interface (SPI). In addition, the KS1081/KS1082 includes leads off detection circuitry and an automatic fast restore circuitry that restores the signal shortly after leads are reconnected. To suppress undesired noise and interference, a right leg drive amplifier (RLD-AMP), high precision references and a low noise low dropout regulator (LDO) are also incorporated in this integrated circuit.

Signal Conditioning

The signal channel in the KS1081/KS1082 has two-stage gain setting to achieve large dynamic range for weak biosignals. Each stage gain can be programmed by the SPI register, independently. The

KS1081/KS1082 has high DC input impedance that allows DC-coupling input for biopotential acquisitions by means of extinctive impedance isolation design skills. What's more, this feature supports signal input from dry-contact electrodes in practical application. The built-in BP-AMP amplifies the ECG signal while rejecting the DC offsets and electrode half-cell potential on the same stage. Consequently, DC offsets as large as 360 mV across the inputs will not saturate the signal channel. Meanwhile, the amplification of the bipotential and the rejection of the DC signal are possible with an indirect current feedback architecture, which reduces size and power compared with traditional implementations. After that, signal with large voltage dynamic range can be obtained by the PGA through reasonable gain setting, which can be easily captured by an analog-to-digital converter (ADC) or an embedded ADC in microcontroller.

Analog Input

The KS1081/KS1082 analog input is fully differential. The differential input (INP-INN) can span between $\frac{VDD-0.15}{2}$ V. Generally, there are two different methods of driving the KS1081/KS1082 analog input: Single-Ended or Differential, as shown in Figure 2. Note that INP and INN are 180°C out-of-phase in the differential input method.

When the input is Single-Ended, the INN input is held at the common-mode voltage, preferably at mid-supply. When the input is differential, the common-mode is given by $\frac{INP+INN}{2}$ V. For optimal performance, it is recommended that the KS1081/KS1082 be used in a **differential configuration**.

Sing-End Input Differential Input

Figure 2. Methods of Driving the KS1081/KS1082: Single-Ended or Differential.

Channel Gain Setting

The KS1081/KS1082 offers flexible gain with two-stage independent gain setting through SPI interface for differential biopotential measurements. The channel gain can be chosen from one of twelve settings (50, 90, 100, 150, 180, 200, 270, 300, 360, 400, 540, and 720), that can be set by writing to the CH1SET/CH2SET register. The details of CH1SET and CH2SET registers are shown in the SPI

Interface (SPI Register Definition) section.

The default gain setting of the KS1081/KS1082 is 360. In practical application, keeping the gain in a reasonable low range helps with any motion artifacts picked up in band. To optimize the dynamic range of the system, the gain level is adjustable through the SPI registers, depending on the input signal amplitude (which may vary with electrode placement) and ADC input range.

Right Leg Drive (RLD) Circuitry

The right leg drive (RLD) circuitry is used as a means to counter the common-mode interference in a biopotential measurement system as a result of power lines and other sources, including fluorescent lights. The basic principle is that the RLD amplifier (RLD-AMP) senses the common-mode signal that present at the device inputs, and forms a negative feedback loop by driving the subject with an inverted common-mode signal. The negative feedback loop restricts the common-mode variations to a narrow range.

As shown in Figure 3, the common-mode signal that is present across the inputs of the signal channel is derived from the RLD-AMP1. It is then connected to the inverting input of RLD-AMP2 through a resistor. An integrator can be built by connecting a capacitor between the RLDFB and RLD terminals. A 1-nF capacitor is available in practical applications. This configuration results in a good common-mode line rejection at a frequency range from 50 Hz to 60 Hz. Higher capacitor values may reduce the loop gain that is available for rejection and, consequently, increasing the line noise. Lower capacitor values move the crossover frequency to higher frequencies, allowing increased gain. The tradeoff is that with higher gain, the system can become unstable and saturate the output of the RLD-AMP2.

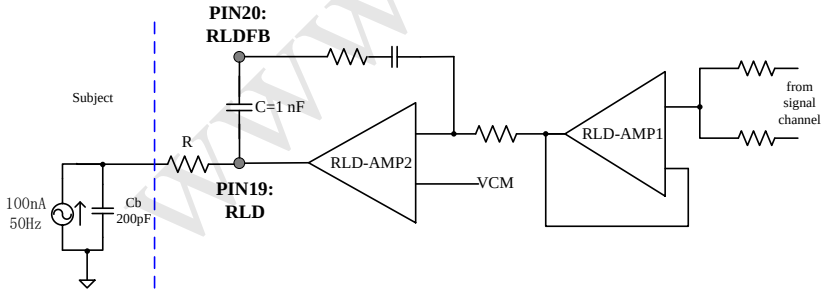


Figure 3. Typical Configuration of RLD Circuitry.

For absolute safety consideration, when using this RLD circuitry to drive an electrode, a resistor R in series with the output (PIN19: RLD) to limit the current to be less than around 20 μA is

recommended. For example, if the supply used is 1.8 V, ensure that the resistor is greater than 100 kΩ to account for component and supply variations. It is important to point out that large resistor R between RLD output and subject may degrade the interference rejection performance. Thus, the value of the resistor R can be used from 10 kΩ to 100 kΩ in battery-powered system for general purpose.

Fast Restore Circuitry

The KS1081/KS1082 adopts band-pass amplifier (BP-AMP). Due to ultra-low cutoff frequency of the high-pass filtering characteristic, signals may require several seconds to settle. This settling time can result in a frustrating delay for the user after a step response: for example, when the electrodes are first connected. This fast restore control block, as shown in Figure 4, is implemented to reduce the large delay. The output of the signal channel is connected to a window comparator. Once a saturation condition at the output of the signal path is detected by the window comparator, which triggers a timing circuit. Thus, a low resistance loop path between input and output of the BP-AMP will be created to deliver a quicker settling time. If, by the end of the timing, the saturation condition persists, the cycle repeats. Otherwise, the KS1081/KS1082 returns to its normal operation.

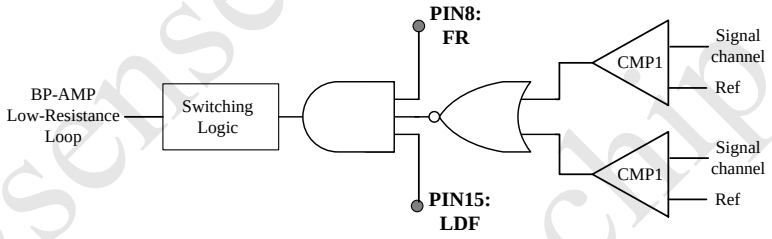


Figure 4. Fast Restor Circuitry.

The KS1081/KS1082 allows user select the input to trigger the timing switches of this fast restore function block: internal leadoff detection output (PIN15: LDF) and external control signal (PIN8: FR). External signal can be created by specified circuits and embedded program in Microcontrollers (MCUs).

To disable fast restore, drive the FR pin low or tie it permanently to GND.

Power Supply Regulation

With a high-precision low dropout regulator (LDO), the KS1081/KS1082 is designed to be powered directly from a single supply voltage ranges from 1.8 V to 3.6V. The output voltage of this LDO is 1.8 V (PIN5: VDD), which provides a precision supply voltage for internal circuits of the KS1081/KS1082.

The KS1081/KS1082 can be driven by a single 3 V battery, such as CR2025 or CR2032 type. It

can also operate from rechargeable Li-Ion batteries, but the designer must take into account that the voltage during a charge cycle may exceed the absolute maximum ratings of the KS1081/KS1082. To avoid damage to the device, use a power switch or a DC-DC buck device.

Benefit from the built-in low noise LDO, additional off-the-shelf high-precision LDO chip for analog circuits in system solution is not required when this product is used for small biopotential measurements. It can help reduce the system size and power, as well as cost.

Shutdown Mode

The KS1081/KS1082 includes a enable pin (PIN7: EN) that further enhances the flexibility and ease of use in portable applications where power consumption is critical. A logic level signal can be applied to this pin to switch to shutdown mode, even when the supply is still on.

Driving the EN pin low places the KS1081/KS1082 in shutdown mode and draws less than 0.1 μA of supply current, offering considerable power savings. To enter normal operation, drive EN high. If not using this feature, permanently tie EN to chip supply (PIN6: LDOIN).

Notice that all circuits in the KS1081/KS1082 will enter sleep mode during shutdown operation.

I/O Protection

All terminals of the KS1081/KS1082 are protected against ESD with specialized circuitry. The measured ESD rating for each pin of the KS1081/KS1082 is about ±4 kV for HBM mode, and ±500 V for CDM mode. In addition, the input structure allows DC overload conditions that are a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, it is necessary to ensure each of the inputs with limited voltage that does not exceed the supplies.

SPI Interface

I/O Description

The serial peripheral interface (SPI)-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, SDI, and SDO. The interface reads and writes registers, and controls KS1081/KS1082 operation.

• Chip Select ($\overline{CS}$)

CS selects the KS1081/KS1082 for SPI communication. CS must remain low for the entire duration of the serial communication. After the serial communication is finished, always wait four or more t_{CLK} cycles before taking CS high. When CS is taken high, the serial interface is reset, SCLK and SDI are ignored, and SDO enters a high-impedance state.

• Serial Clock (SCLK)

SCLK is the SPI serial clock. SCLK is used to shift commands in and shift data out from the device. The serial clock features a Schmitt-triggered input and clocks data on the SDI and SDO pins into and out of the KS1081/KS1082. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so could result in the device serial interface being placed into an unknown state, requiring CS to be taken high to recover.

• Data Input (SDI)

The data input pin (SDI) is used along with SCLK to communicate with the KS1081/KS1082 (opcode commands and register data). The device latches data on SDI on the SCLK falling edge.

• Data Output (SDO)

The data output pin (SDO) is used with SCLK to read register data from the KS1081/KS1082. Data on SDO are shifted out on the SCLK rising edge. SDO goes to a high-impedance state when CS is high. In read data continuous mode (see the SPI Command Definitions section for more details), the SDO output line also indicates when new data are available. This feature can be used to minimize the number of connections between the device and the system controller.

Timing Characteristics

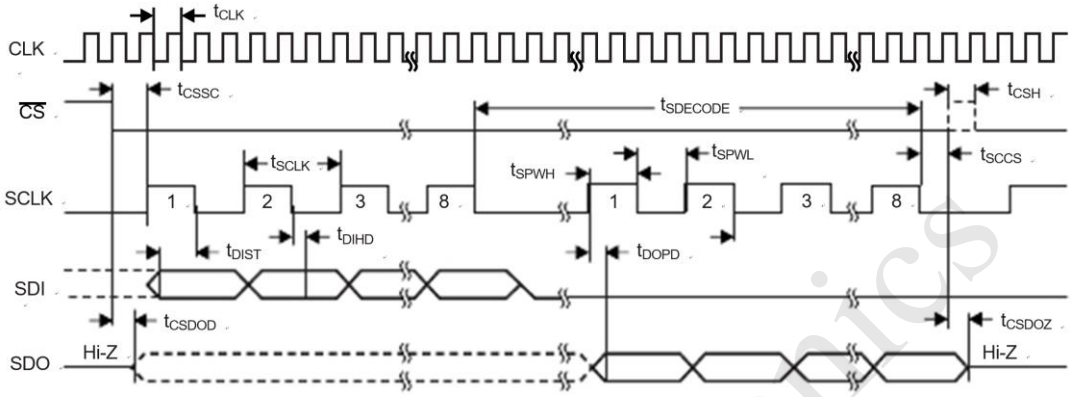


Figure 5. SPI Timing Diagram

Parameter	Description
t_{CLK}	Master clock period
t_{CSSC}	CS low to first SCLK, setup time
t_{SCLK}	SCLK period
$t_{SPWH, L}$	SCLK pulse width, high and low
t_{DIST}	SDI valid to SCLK falling edge: setup time
t_{DIHD}	Valid SDI after SCLK falling edge: hold time
t_{DOPD}	SCLK rising edge to SDO valid
t_{CSH}	CS high pulse
t_{CSDOD}	CS low to SDO driven
t_{SCCS}	Eighth SCLK falling edge to CS high
$t_{SDECODE}$	Command decode time
t_{CSDOZ}	CS high to SDO Hi-Z

SPI Command Definitions

The KS1081/KS1082 provides flexible configuration control. The opcode commands summarized in following table control and configure the KS1081/KS1082 operation. The opcode commands are stand-alone, except for the register read and register write operations that require a second command byte plus data. CS can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the KS1081/KS1082 on the seventh SCLK falling edge. The register read and write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling CS high after issuing a command.

Command	Description	Opcodes	Operand
RESET	Reset the device	1111_1110(0xFE)	--
RDATA	Read data by command; supports multiple read back.	0000_0001(0x01)	--
RREG	Read nnnn registers starting at address rrrr	0001_rrrr(0x1x)	xxxx_nnnn
WREG	Write nnnn registers starting at address rrrr	0010_rrrr(0x2x)	xxxx_nnnn

(1) nnnn = number of registers to be read or written. For example, to read or write three registers, set nnnn = 0010.
(2) rrrr =starting register address for read and write opcodes.

• RESET: Reset Registers to Default Values

This command resets and returns all register settings to the default values. There are no restrictions on the SCLK rate for this command and it can be issued any time. Avoid sending any commands during this time.

• RDATA: Read Data

There is no restriction on the SCLK rate for this command, and there is no wait time needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after RDATA command is issued. The following figure shows the recommended way to use the RDATA command.

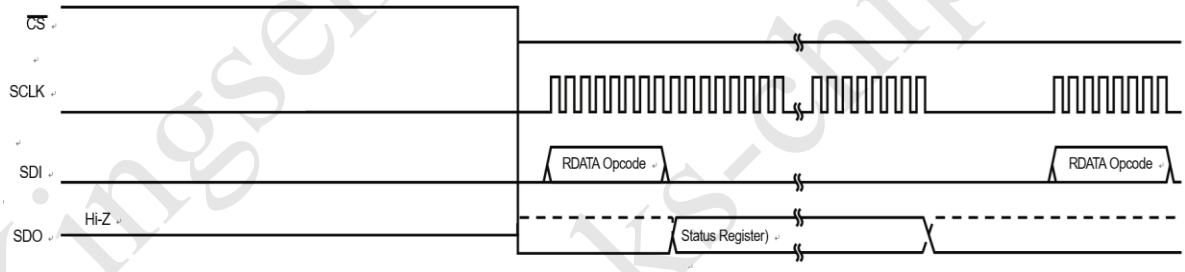


Figure 6. RDATA Usage

• RREG: Read from Register

This opcode reads register data. The Register Read command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read.

First opcode byte: 0001 rrrr, where rrrr is the starting register address.

Second opcode byte: 0000 nnnn, where nnnn is the number of registers to read.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in the following figure. The RREG command can be issued at any time. However, because this command

is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the Serial Clock (SCLK) subsection of the SPI Interface section for more details. Note that CS must be low for the entire command.

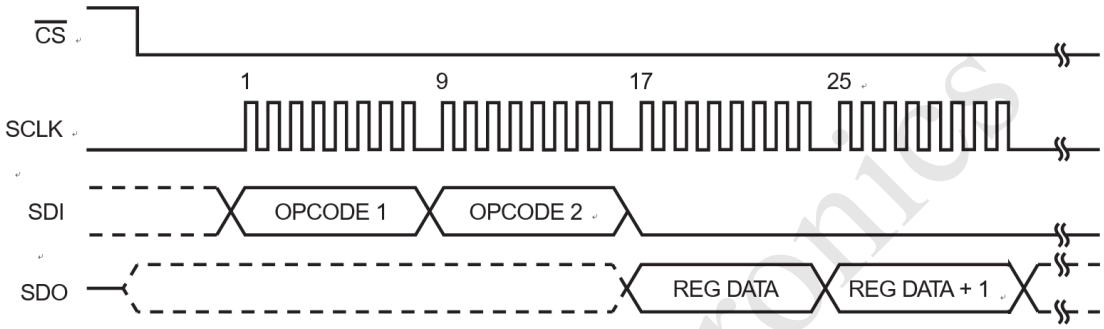


Figure 7. RREG Command Example: Read Two Registers Starting from Register 00h (CH1SET Register in KS1081/KS1082). (OPCODE 1 = 0001 0000, OPCODE 2 = 0000 0001)

• WREG: Write to Register

This opcode writes register data. The Register Write command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to write.

First opcode byte: 0010 rrrr, where rrrr is the starting register address.

Second opcode byte: 0000 nnnn, where nnnn is the number of registers to write.

After the opcode bytes, the register data follows (in MSB-first format), as shown in the following figure. The WREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the Serial Clock (SCLK) subsection of the SPI Interface section for more details. Note that CS must be low for the entire command.

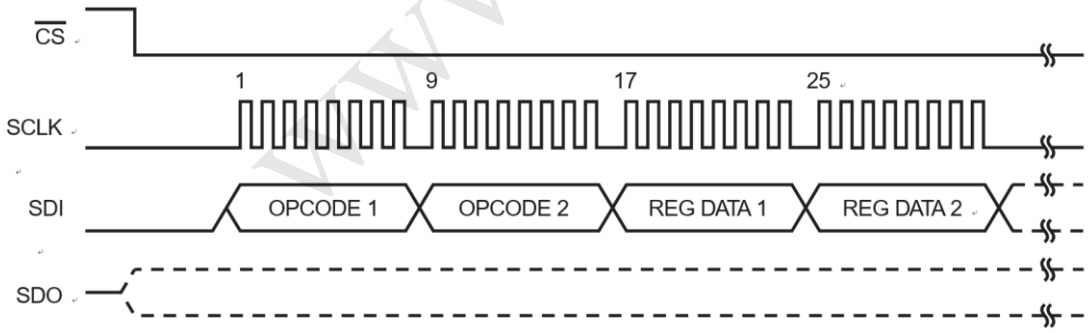


Figure 8. WREG Command Example: Write Two Registers Starting from 00h (CH1SET Register in KS1081/KS1082). (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

SPI Register Definition

• Register Assignment

Address	Register	Default Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	CH1SET	0010_0000	Reserved	Reserved	CHLPD	Gain2_2	Gain2_1	Gain2_0	Gain1_1	Gain1_0
01h	CH2SET	0010_0000	Reserved	Reserved	CHLPD	Gain2_2	Gain2_1	Gain2_0	Gain1_1	Gain1_0

• User Register Description

(1) ***CH1SET: Channel 1 Settings*** (Address=0000, Default Value=0010_0000)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	CHL1PD	Gain2_2	Gain2_1	Gain2_0	Gain1_1	Gain1_0
Bit[7:6]	**Reserved** 00 (default).						
Bit[5] (1)	**CHL1PD[1] together with PIN 9 (CHLEN):Channel Power Down and Power Up.** 1(default); 0. **NOTE(2):** CHL1PD **XOR** CHLEN=1, Enable Channel 1; CHL1PD **XOR** CHLEN=0, Shut Down Channel 1.						
Bit[4:2]	**Gain2[2:0]: the second-stage gain setting of Channel 1** 000=40 (default); 001=10; 010=20; 011=30; 100=60; 101=80.						
Bit[1:0]	**Gain1[1:0]: the first-stage gain setting of Channel 1** 00=9 (default); 01=5.						

(2) ***CH2SET: Channel 2 Settings*** (Address=0001, Default Value=0010_0000)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	CHL2PD	Gain2_2	Gain2_1	Gain2_0	Gain1_1	Gain1_0
Bit[7:6]	**Reserved** 00 (default).						
Bit[5] (1)	**CHL2PD[1] together with PIN 9 (CHLEN):Channel Power Down and Power Up.** 1(default);						

	0. **NOTE(2):** CHL2PD **XNOR** CHLEN=1, Enable Channel 2; CHL2PD **XNOR** CHLEN=0, Shut Down Channel 2.
Bit[4:2]	**Gain2[2:0]: the second-stage gain setting of Channel 2** 000=40 (default); 001=10; 010=20; 011=30; 100=60; 101=80.
Bit[1:0]	**Gain1[1:0]: the first-stage gain setting of Channel 2** 00=9 (default); 01=5.

*(1) available for dual-channel chip KS1082.

*(2) details see the following truth table for channel selection.

• Channel Selection Description

#Channel 1

CHL1PD	CHLEN	CHANNEL 1	Logic Operation
1	**0**	ON	**XOR:** CHL2PD⊕CHLEN
1	**1**	OFF	
0	**0**	OFF	
0	**1**	ON	

#Channel 2

CHL2PD	CHLEN	CHANNEL 2	Logic Operation
1	**0**	OFF	**XNOR:** CHL2PD⊙CHLEN
1	**1**	ON	
0	**0**	ON	
0	**1**	OFF	

Application Information

As a case, the KS1081/KS1082 can be used to record complete shape of ECG waveform with minimal distortion. With high performance, the KS1081/KS1082 enables the acquisitions of ECG from subject's chest, hand, and fingers for different application scenarios. In addition, space is at a premium for wearable device configuration. As shown in Figure 9 and 10, by using as few external components as possible, the application circuit based on the KS1081/KS1082 is optimized for size.

Application Circuits

There are two different types of circuit configuration according to the chip category. The circuits in Figure 9 and Figure 10 are designed for monitoring single-lead and dual-channel ECG, respectively.

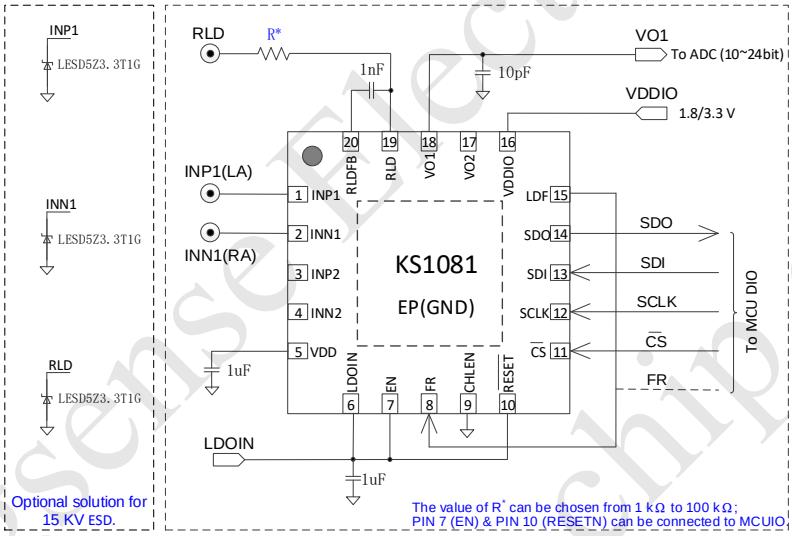


Figure 9. Signal-Channel Signal Conditioning with ***THREE*** Electrodes

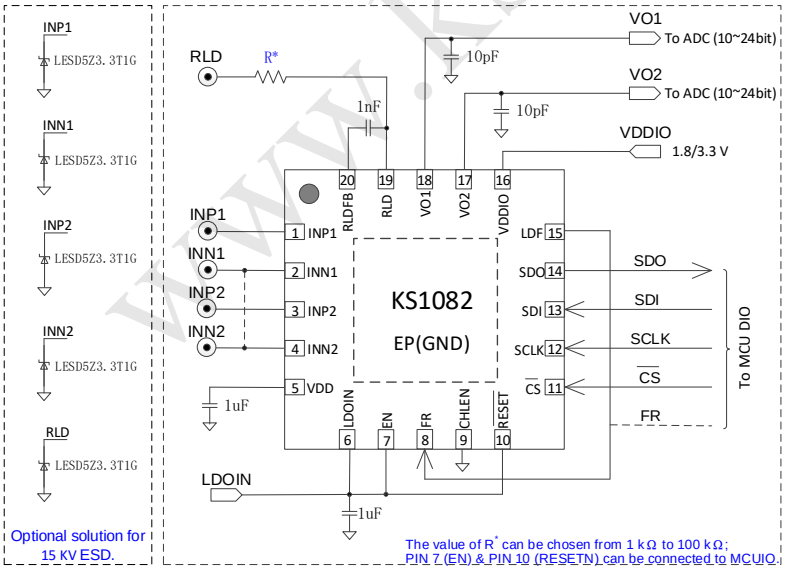


Figure 10. Dual-Channel Signal Conditioning with ***FOUR/FIVE*** Electrodes

RLD Electrode (Reference Electrode) Configuration

To improve the system CMRR performance, a driven lead (or reference electrode) is recommended to be implemented when the KS1081/KS1082 is adopted in practical applications. It is available through the RLD circuitry to minimize the effects of common-mode voltages induced by the power line and other interfering sources. As a safety measure, place a resistor between the RLD pin (PIN19: RLD) and the electrode connected to the subject to ensure that current flow in a limited range, details see the Theory of Operation Section (RLD Circuitry).

For chest-based ECG system, electrodes are typically placed on chest near the heart. The two sense electrodes are placed under the pectoral muscles. Because the distance from the heart to the KS1081/KS1082 is small, and the heart signal is strong and there is less muscle artifact interference. In this application, RLD electrode as an alternative configuration is recommended. Definitely, the use of RLD electrode can significantly improve the rejection of noise and motion artifacts.

For hand/finger-based EGG system, ECG signal is measured at the hands or fingers. Source signal is weaker than when measured closer to the heart. Additionally, the arm and upper body movement of the subject create large motion artifacts, and the long lead length makes the system susceptible to common-mode interference. RLD electrode is strongly recommended in this application to maintain high quality signals.

What's important, there is no strict requirement of the location of RLD electrode. It can be placed near one of the sense electrodes (either INP or INN), or far away from which. It's worth to note that RLD electrode must be isolated from each of input electrodes, avoiding short connection.

Driving ADCs

The ability of KS1081/KS1082 to drive capacitive loads makes it ideal for driving an ADC without an additional buffer. However, depending on the input architecture of the ADC, a simple, low-pass RC network may be required to decouple the transients from the switched capacitor input typical of modern ADCs. That can effectively reduce noise and aliasing. Therefore, output pin of each signal channel (VO1: PIN17, VO2: PIN18), is recommended to be bypassed with a 10-pF capacitor in practical applications.

Definitely, high-resolution ADC with high effective number bits (ENOB) is preferable when high quality ECG waveforms are expected in certain application.

ESD Protection

The measured ESD rating for each pin of the KS1081/KS1082 is about ±4 kV for HBM mode, and ±500 V for CDM mode. For further safety consideration, a complete solution includes further clamping to either supply using additional ESD devices, such as LESD5Z3.3T1G. In this case, the ESD rating of the system can achieve about 15 KV level.

Sensor Electrodes Material

The KS1081/KS1082 supports both wet-contact electrodes and dry-contact electrodes input for small biopotential recording. The sensor electrodes can be adopted are listed as follows,

- Wet electrodes: Silver-Silver Chloride (Ag-AgCl), etc.
- Dry electrodes: Metal (Cu, Ag, et al.), conductive fabric, graphene, etc.

PCB Layout Recommendations

Due to the weak biosignals, it is pretty important to follow good layout practices to optimize system performance.

• Power Supplies and Grounding

The KS1081/KS1082 has a built-in LDO. VDD as the output of the LDO, provides the supply for the entire integrated circuit, which should be as quiet as possible. For supply pins LDOIN and VDD, each pin should be bypassed with a 1-μF capacitor. Alternatively, decoupling circuit uses a 1-μF capacitor in parallels with a 0.1-μF capacitor is also recommended. Place a 0.1-μF capacitor close to the supply pin. A 1-μF capacitor can be used farther away from the device. The placement of the digital circuits (such as the DSP, microcontrollers, and FPGAs) in the system is done such that the return currents on those devices do not cross the KS1081/KS1082 analog return path. It is worth to note that excessive decoupling capacitance may increase power dissipation during power cycling.

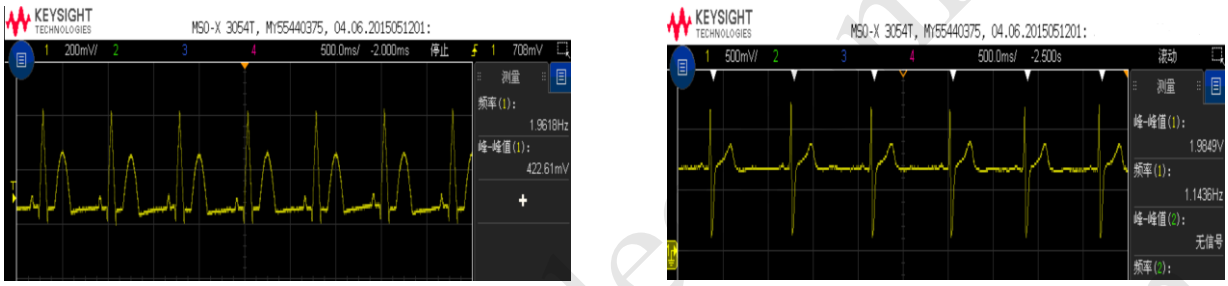
• Shielding Analog Signal Paths

As for precision circuit, it is essential to keep the input traces symmetrical and length matched and make wires short, direct interconnections and avoid stray wiring capacitance, particularly at the analog input pins. These pins are high-impedance and extremely sensitive to extraneous noise. Digital signals should be kept as far as possible from the analog input signals on the PCB. What's more, splitting the ground plane (Digital and Analog) on mixed-signal PCB to isolate the digital circuits from

analog circuit is recommended, which may significantly improve the noise rejection of the system.

ECG Measurements

The KS1081/KS1082 provides a promising and attractive solution for wearable ECG applications, particularly for hand-based ECG and finger-based ECG recording when dry-electrodes are preferred. The ECG waveforms recorded by the application circuit includes KS1081/KS1082 are shown in Figure 11 and Figure 12.



(a) Simulated ECG Recording (b) Human ECG Recording with Dry-Electrodes

Figure 11. Performance Test for ECG Recording by KS1082-EB(1).

(c) Chest-Based ECG Monitoring with Dry-Electrodes (d) Finger-Based ECG Monitoring with Dry-Electrodes

Figure 12. Real-Time ECG Monitoring by the KSECG-DB(1) with Dry-Electrodes on Subject's Chest (1), and Subject's Fingers (b).

*(1) details see Ordering Guide Section

Package Information

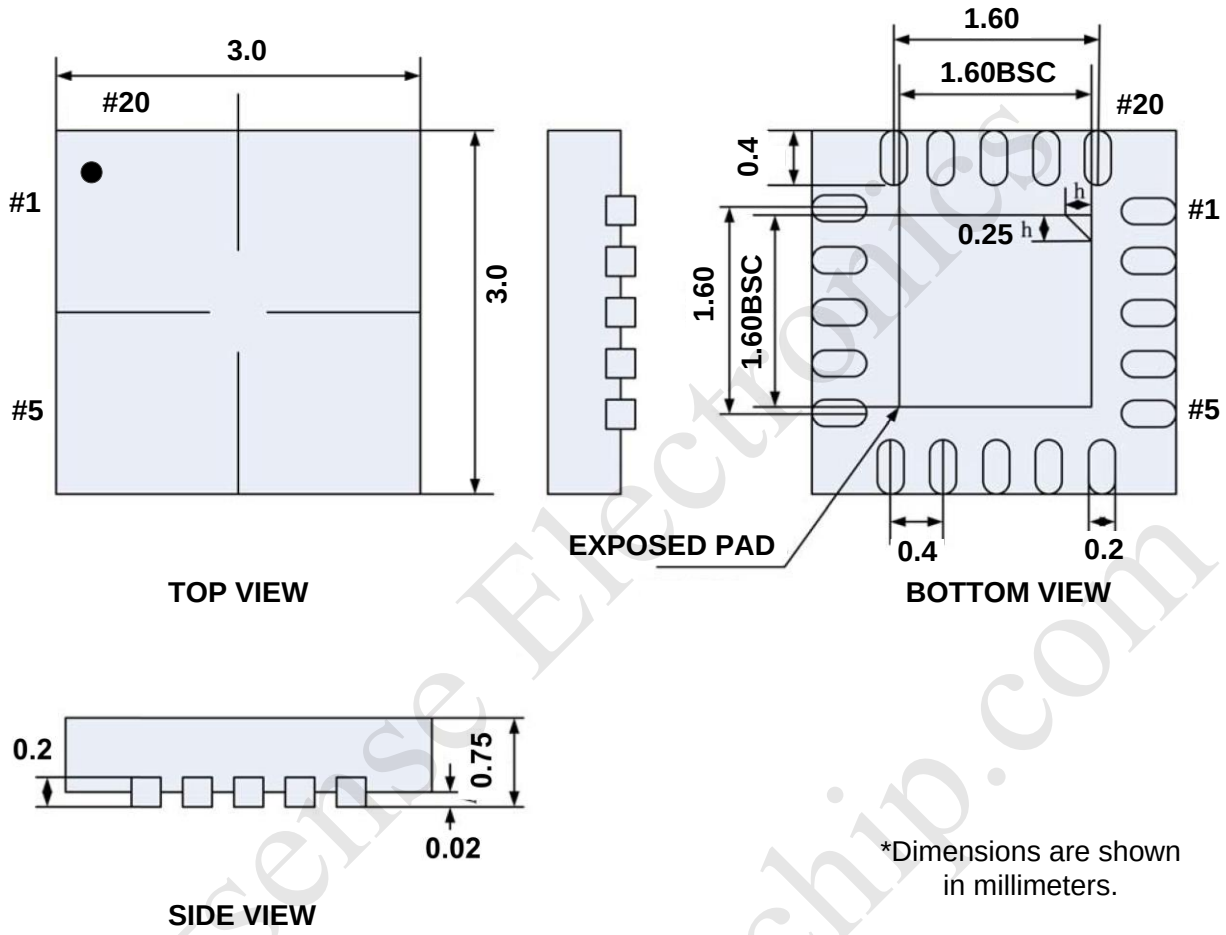
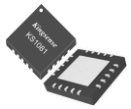
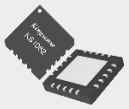
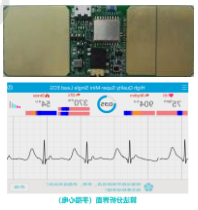


Figure 13. 20-Pin Quad Flat No-Lead Package.

NOTE for Exposed PAD:

This package incorporates an exposed pad that is designed for circuit ground and thermal heatsink. This pad **must** be soldered directly to the ground plane of the printed circuit board (PCB).

Ordering Guide

Model	Device Name	Description	Package Information	Picture
KS1081	AFE Chip	1-channel analog front-end chip.	QFN-20 3×3 mm	
KS1082	AFE Chip	2-channel analog front-end chip.	QFN-20 3×3 mm	
KS1082-EB	Analog performance evaluation board	PCB board with KS1082 and scalable in/out test pin for analog performance evaluation.	PCB 36×66 mm	
KSECG101	Bluetooth ECG module	Small PCB board with KS1081/1082, low BLE 5.0 chip for wireless ECG recording.	PCB 10×12 mm	
KSECG-DB	Bluetooth ECG demo board	PCB board with KSECG101, power/ battery management, on board print metal-pads as sensor electrodes, and android APP for real-time ECG/EMG recording demonstration.	PCB 30×80 mm	

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