

U1A

BANK 1

IO, (DQS2L/CQ3L)/(DQS2L/CQ3L)  
IO, DIFFIO\_L1p  
IO, DIFFIO\_L1n, (DATA1,ASDO)  
IO, VREFB1N0  
IO, DIFFIO\_L2p, (FLASH\_nCE,nCSO)  
IO, DIFFIO\_L2n  
IO, DIFFIO\_L3p  
IO, DIFFIO\_L3n  
IO, DIFFIO\_L4p, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)  
IO, DIFFIO\_L4n  
IO, (DATA0)

D4 EXT1\_01  
D5 EXT1\_09  
D5 EXT1\_13  
B1 VGA\_R0  
C2 VGA\_G5  
C1 FPGA\_ASDO  
F3 EXT1\_11  
D2 FPGA\_NCSO  
D1 VGA\_G4  
G5 EXT1\_14  
F2 VGA\_G3  
F1 VGA\_G2  
G2 VGA\_G1  
G1 VGA\_G0  
H2 FPGA\_DATA

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U1B

BANK 2

IO, DIFFIO\_L5p, (DQ1L)/(C)  
IO, DIFFIO\_L5n, (DQ1L)/(C)  
IO, DIFFIO\_L6p  
IO, DIFFIO\_L6n  
IO, DIFFIO\_L7p  
IO, DIFFIO\_L7n, (DQ1L)/(C)  
IO, DIFFIO\_L8p, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)  
IO, DIFFIO\_L8n, (DQ1L)/(C)  
IO, VREFB2N0  
IO, DIFFIO\_L9p, (DQ1L)/(C)  
IO, DIFFIO\_L9n, (DQ1L)/(C)  
IO, RUP1, (DQ1L)/(C)  
IO, RDN1, (DQ1L)/(C)  
IO, (DQS3L/CQ3L#)/(DQS3L/CQ3L#)  
IO, DIFFIO\_L10p, (DQ1L)/(C)  
IO, DIFFIO\_L10n, (DM1L/BWS#1L)/(C)

J2 VGA\_B3  
J1 VGA\_B4  
K6 EXT1\_16  
K6 EXT1\_17  
K6 EXT1\_15  
K2 VGA\_B1  
K1 VGA\_B2  
J2 EXT1\_02  
J1 VGA\_B0  
J3 SM\_SEL1  
N2 EXT1\_06  
N1 EXT1\_04  
K5 EXT1\_18  
J4 SM\_SEL2  
K1 EXT1\_12  
P2 EXT1\_10  
P1 EXT1\_08

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BANK 3

IO, DIFFIO\_B1p  
IO, DIFFIO\_B1n, (DM3B/BWS#3B)/(DM5B/BWS#5B)  
IO, DIFFIO\_B2p, (DQ3B)/(DQ5B)  
IO, DIFFIO\_B2n  
IO, (DQS1B/CQ1B#,DPCLK2)/(DQS1B/CQ1B#,DPCLK2)  
IO, PLL1\_CLKOUTp  
IO, PLL1\_CLKOUTn  
IO, DIFFIO\_B4p, (DQ3B)/(DQ5B)  
IO, DIFFIO\_B4n, (DQ3B)/(DQ5B)  
IO, (DQ3B)/(DQ5B)  
IO, VREFB3N0  
IO, DIFFIO\_B5p, (DQS3B/CQ3B#)/(DQS3B/CQ3B#)  
IO, DIFFIO\_B5n  
IO, DIFFIO\_B6p, (DQ3B)/(DQ5B)  
IO, DIFFIO\_B6n  
IO, DIFFIO\_B7p, (DQ3B)/(DQ5B)  
IO, DIFFIO\_B7n  
IO, (DQ3B)/(DQ5B)  
IO, DIFFIO\_B8p, (DQ3B)/(DQ5B)  
IO, DIFFIO\_B8n, (DQS5B/CQ5B#)/(DQS5B/CQ5B#)  
IO, DIFFIO\_B9p, (DQ3B)/(DQ5B)  
IO, DIFFIO\_B9n, (DM5B/BWS#5B)/(DM5B/BWS#5B)  
IO, DIFFIO\_B10p, (DQ5B)/(DQ5B)  
IO, DIFFIO\_B10n, (DQ5B)/(DQ5B)  
IO, DIFFIO\_B11p  
IO, DIFFIO\_B11n

N3 SDRAM\_A5  
P3 SDRAM\_A6  
K3 SDRAM\_A2  
J3 SDRAM\_A1  
J2 SDRAM\_A3  
R4 SDRAM\_A0  
J4 SDRAM\_A10  
J5 SDRAM\_A8  
N6 SDRAM\_A9  
M6 SDRAM\_A7  
P6 SDRAM\_A11  
M7 SDRAM\_A12  
K8 SDRAM\_DQ9  
R5 SDRAM\_BA1  
F5 SDRAM\_BA0  
K6 SDRAM\_CS  
J6 SDRAM\_RAS  
J7 SDRAM\_A4  
R7 SDRAM\_CAS  
J7 SDRAM\_WE  
J8 SDRAM\_DQ8  
M8 SDRAM\_UDQM  
N8 SDRAM\_CKE  
P8 SDRAM\_CLK  
R8 SDRAM\_LDQM  
F8 SDRAM\_DQ7

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BANK 4

IO, DIFFIO\_B12p  
IO, DIFFIO\_B12n  
IO, DIFFIO\_B13p  
IO, DIFFIO\_B13n  
IO, DIFFIO\_B14p  
IO, DIFFIO\_B14n, (DQ5B)/(DQ5B)  
IO, DIFFIO\_B15p, (DQ5B)/(DQ5B)  
IO, DIFFIO\_B15n, (DQS4B/CQ5B)/(DQS4B/CQ5B)  
IO, DIFFIO\_B16p, (DQ5B)/(DQ5B)  
IO, DIFFIO\_B16n  
IO, DIFFIO\_B17p, (DQ5B)/(DQ5B)  
IO, DIFFIO\_B17n, (DQ5B)/(DQ5B)  
IO, DIFFIO\_B18p  
IO, DIFFIO\_B18n  
IO, (DQS2B/CQ3B)/(DQS2B/CQ3B)  
IO, VREFB4N0  
IO, DIFFIO\_B19p  
IO, DIFFIO\_B19n, (DQ5B)/(DQ5B)  
IO, RUP2  
IO, RDN2  
IO, DIFFIO\_B20p, (DQ5B)/(DQ5B)  
IO, DIFFIO\_B20n, (DQS0B/CQ1B,DPCLK3)/(DQS0B/CQ1B,DPCLK3)  
IO, DIFFIO\_B21p  
IO, DIFFIO\_B21n  
IO, DIFFIO\_B22p  
IO, DIFFIO\_B22n

R9 SDRAM\_DQ5  
F9 SDRAM\_DQ6  
K9 KEY2  
J9 KEY1  
M9 SDRAM\_DQ10  
N9 SDRAM\_DQ12  
R10 SDRAM\_DQ3  
T10 SDRAM\_DQ4  
R11 SDRAM\_DQ1  
T11 SDRAM\_DQ2  
R12 SDRAM\_DQ15  
T12 SDRAM\_DQ0  
K10 KEY0  
L10 SYS\_RSTN  
P9 SDRAM\_DQ11  
P11 SDRAM\_DQ14  
R13 UART\_TXD  
T13 UART\_RXD  
M10 SDRAM\_DQ13  
N11 ST\_RMII\_TXEN  
T14 FSMC\_D10  
T15 FSMC\_D8  
R14 FSMC\_D9  
P14 ST\_RMII\_TXD1  
L11 FSMC\_D2  
M11 FSMC\_D11  
N12 ST\_RMII\_TXD0

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U1E

BANK 5

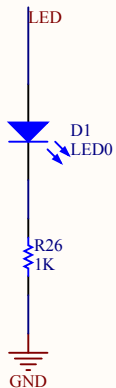
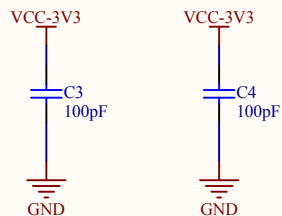
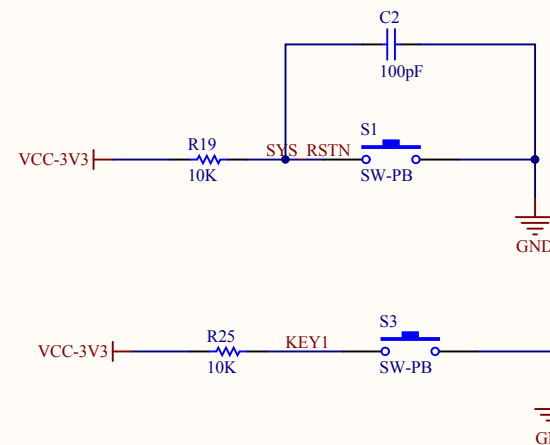
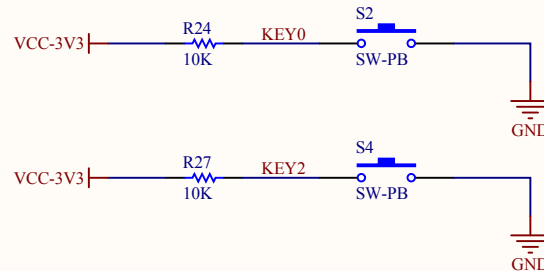
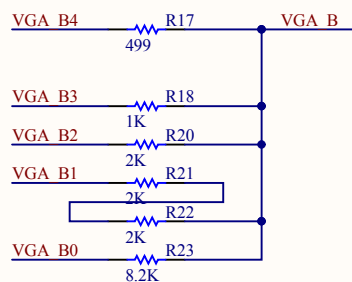
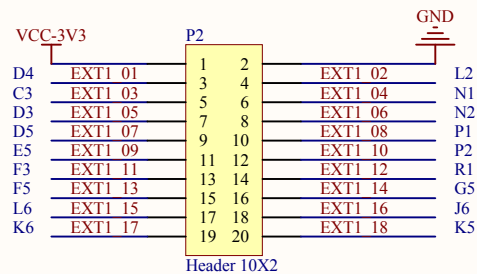
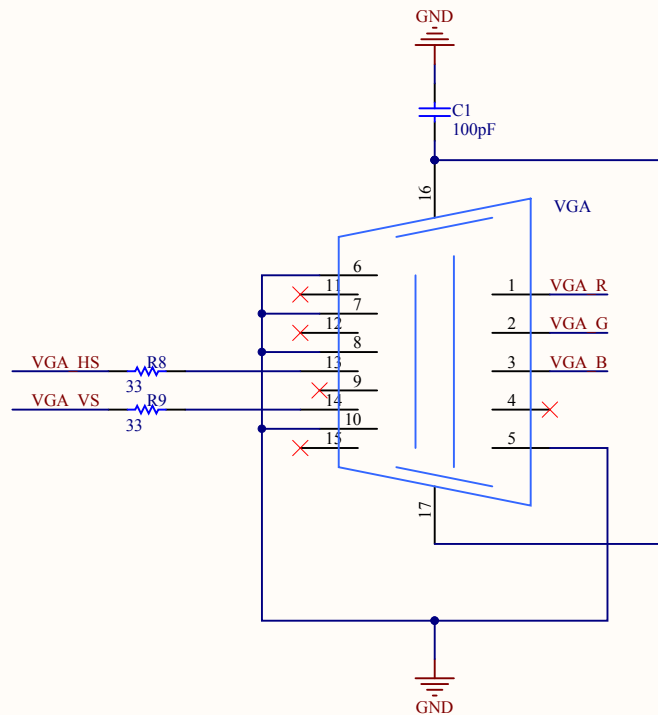
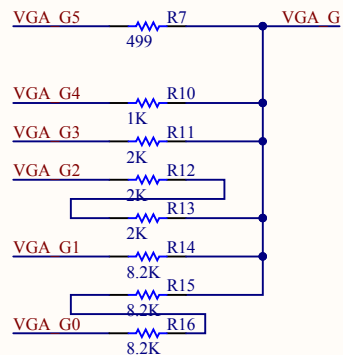
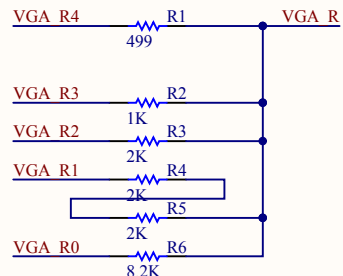
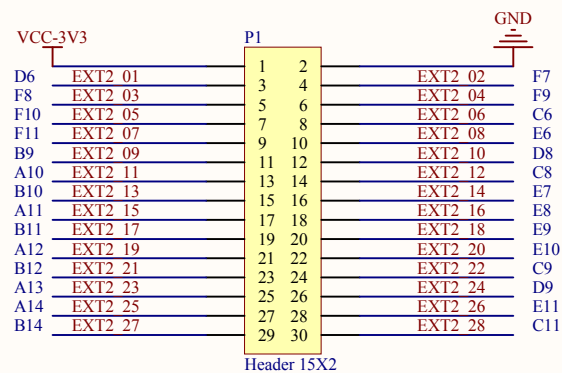
IO, RUP3, (DM1R/BWS#1R)/(C)  
IO, RDN3, (DQ1R)/(C)  
IO, DIFFIO\_R11n, (DQS3R/CQ3R#)/(DQS3R/CQ3R#)  
IO, DIFFIO\_R11p, (DQ1R)/(C)  
IO, DIFFIO\_R10n, (DQ1R)/(C)  
IO, DIFFIO\_R10p, (DQ1R)/(C)  
IO, VREFB5N0  
IO, (DQ1R)/(C)  
IO, DIFFIO\_R9n, (DQ1R)/(C)  
IO, DIFFIO\_R9p  
IO, DIFFIO\_R8n, (DQ1R)/(C)  
IO, DIFFIO\_R8p, (DQS1R/CQ1R#,DPCLK4)/(DQS1R/CQ1R#,DPCLK4)  
IO, DIFFIO\_R7n, (DEV\_OE)  
IO, DIFFIO\_R7p, (DEV\_CLRn)  
IO, DIFFIO\_R6n, (DQ1R)/(C)  
IO, DIFFIO\_R6p  
IO, (DQ1R)/(C)

N13 FSMC\_D13  
M12 FSMC\_D15  
L12 DCMI\_D1  
K12 FSMC\_A18  
N14 FSMC\_D14  
P15 FSMC\_D6  
P16 FSMC\_D5  
R16 FSMC\_D7  
K11 DCMI\_D3  
N16 ST\_RMII\_RXD1  
N15 FSMC\_D4  
L14 FSMC\_A17  
L13 FSMC\_A16  
L16 DCMI\_HSYNC  
L15 ST\_RMII\_RXD0  
J11 DCMI\_D2  
K16 ST\_RMII\_CRSDV  
K15 DCMI\_PIXCLK  
J16 FSMC\_A22  
J15 ST\_RMII\_REFCLK  
J14 FSMC\_D1  
J12 DCMI\_D0  
J13 FSMC\_D0

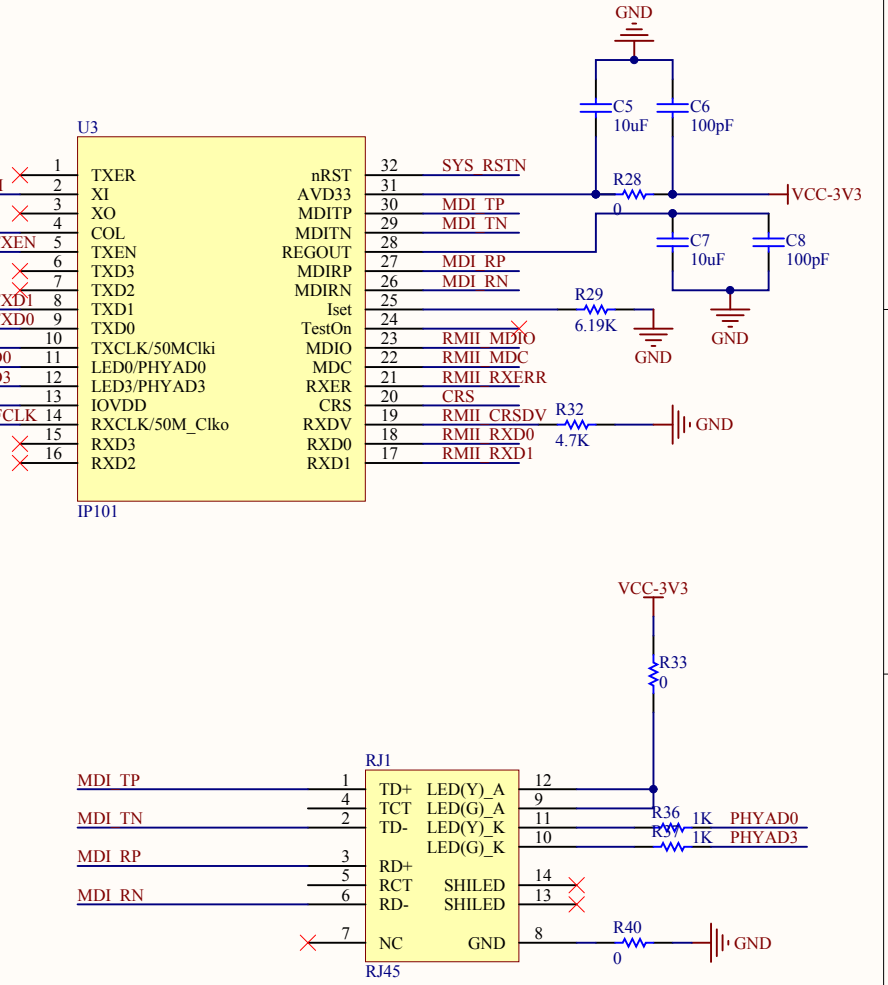
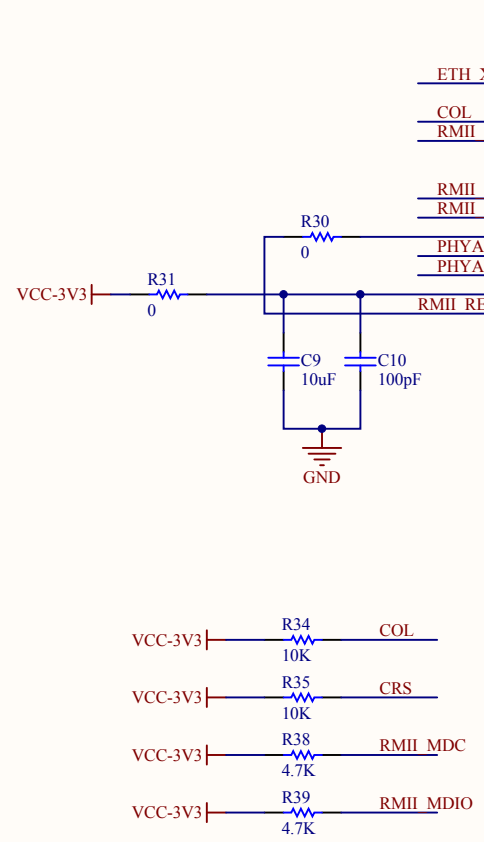
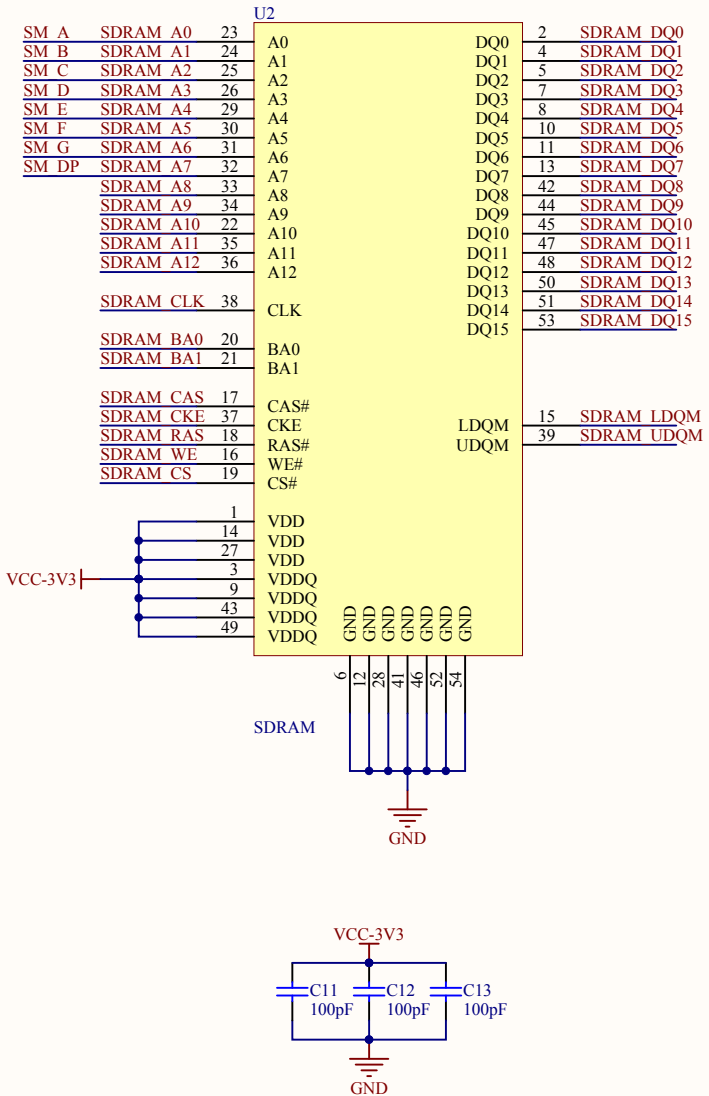
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Title		
Size	Number	Revision
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Date:	2020/5/29	Sheet of
File:	E:\MyProject\...\SDRAM.SchDoc	Drawn By: