Advanced Information
Preliminary Datasheet

OV2640 Color CMOS UXGA (2.0 MegaPixel) CAMERACHIP™ with OmniPixel2™ Technology

General Description

The OV2640 CAMERACHIP™ is a low voltage CMOS image sensor that provides the full functionality of a single-chip UXGA (1632x1232) camera and image processor in a small footprint package. The OV2640 provides full-frame, sub-sampled, scaled or windowed 8-bit/10-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 15 frames per second (fps) in UXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, white pixel canceling, noise canceling, and more, are also programmable through the SCCB interface. The OV2640 also includes a compression engine for increased processing power. In addition, OmniVision CAMERACHIPS use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable color image.

Note: The OV2640 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable apps
- Standard SCCB interface
- Output support for Raw RGB, RGB (RGB565/555), GRB422, YUV (422/420) and YCbCr (4:2:2) formats
- Supports image sizes: UXGA, SXGA, SVGA, and any size scaling down from SXGA to 40x30
- VarioPixel® method for sub-sampling
- Automatic image control functions including Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Band Filter (ABF), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, gamma, sharpness (edge enhancement), lens correction, white pixel canceling, noise canceling, and 50/60 Hz luminance detection
- Line optical black level output capability
- Video or snapshot operation
- Zooming, panning, and windowing functions
- Internal/external frame synchronization
- Variable frame rate control
- Supports LED and flash strobe mode
- Supports scaling
- Supports compression
- Embedded microcontroller

Ordering Information

Product	Package
OV02640-VL9A (Color, lead-free)	38-pin CSP2

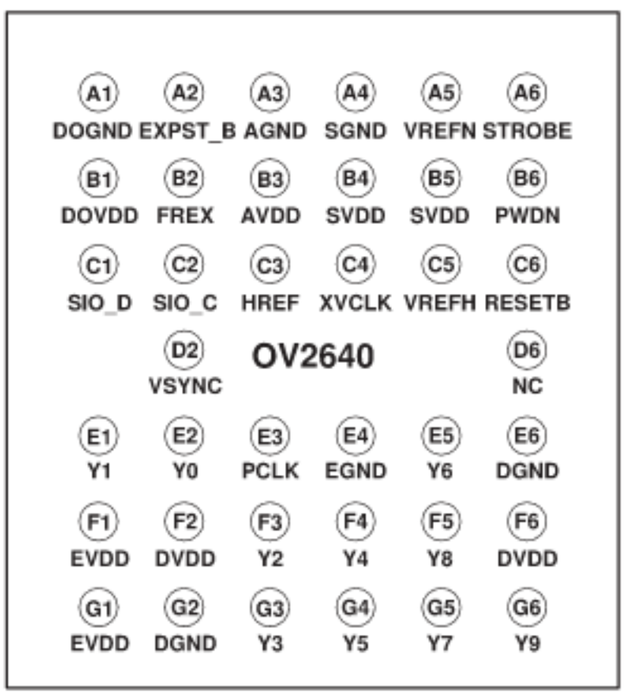
Applications

- Cellular and Camera Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

Array Size	**UXGA**	1600 x 1200
Power Supply	**Core**	1.3VDC ± 5%
	Analog	2.5 ~ 3.0VDC
	I/O	1.7V to 3.3V
Power Requirements	**Active**	125 mW (for 15 fps, UXGA YUV mode)
		140 mW (for 15 fps, UXGA compressed mode)
	Standby	600 µA
Temperature Range	**Stable Image**	0°C to 50°C
Output Formats (8-bit)		• YUV(422/420)/YCbCr422 • RGB565/555 • 8-bit compressed data • 8-/10-bit Raw RGB data
Lens Size		1/4"
Chief Ray Angle		25° non-linear
Maximum Image Transfer Rate	**UXGA/SXGA**	15 fps
	SVGA	30 fps
	CIF	60 fps
Sensitivity		0.6 V/Lux-sec
S/N Ratio		40 dB
Dynamic Range		50 dB
Scan Mode		Progressive
Maximum Exposure Interval		1247 x t_{ROW}
Gamma Correction		Programmable
Pixel Size		2.2 µm x 2.2 µm
Dark Current		15 mV/s at 60°C
Well Capacity		12 Ke
Fixed Pattern Noise		<1% of $V_{PEAK-TO-PEAK}$
Image Area		3590 µm x 2684 µm
Package Dimensions		5725 µm x 6285 µm

Figure 1 OV2640 Pin Diagram (Top View)



Functional Description

Figure 2 shows the functional block diagram of the OV2640 image sensor. The OV2640 includes:

- Image Sensor Array (1632 x 1232 total image array)
- Analog Signal Processor
- 10-Bit A/D Converters
- Digital Signal Processor (DSP)
- Output Formatter
- Compression Engine
- Microcontroller
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram

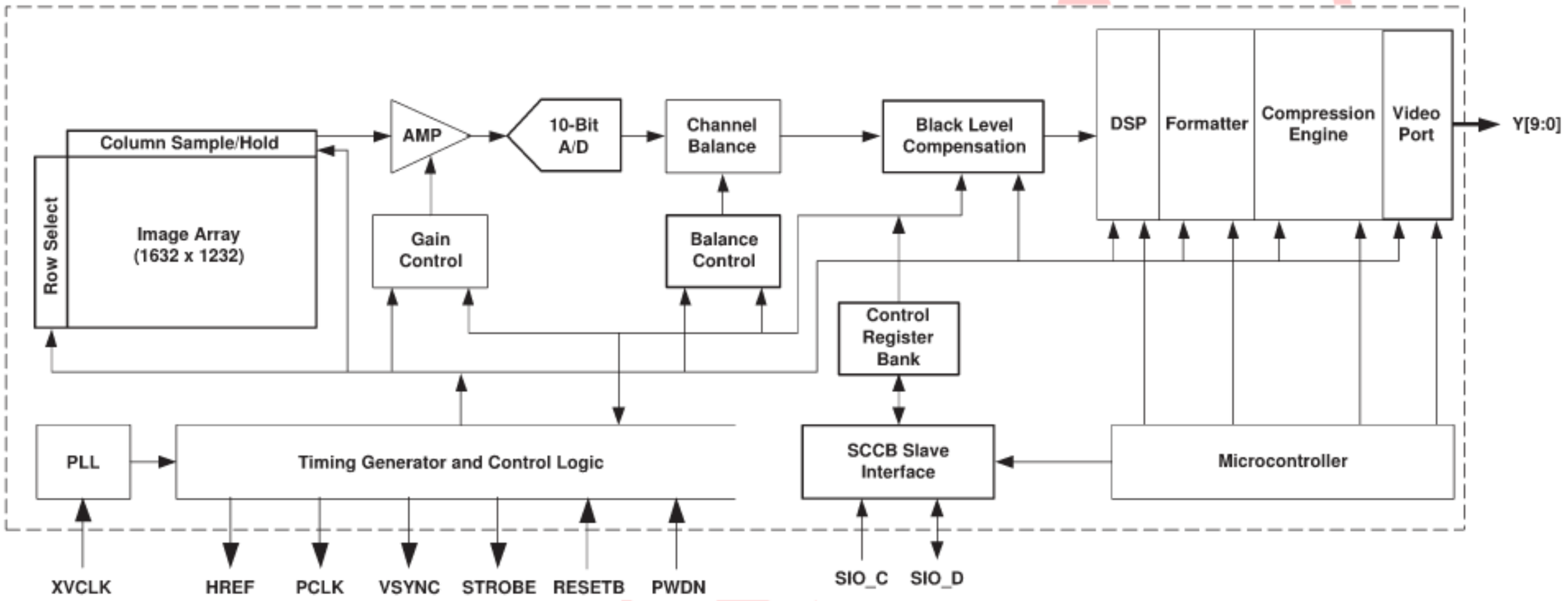
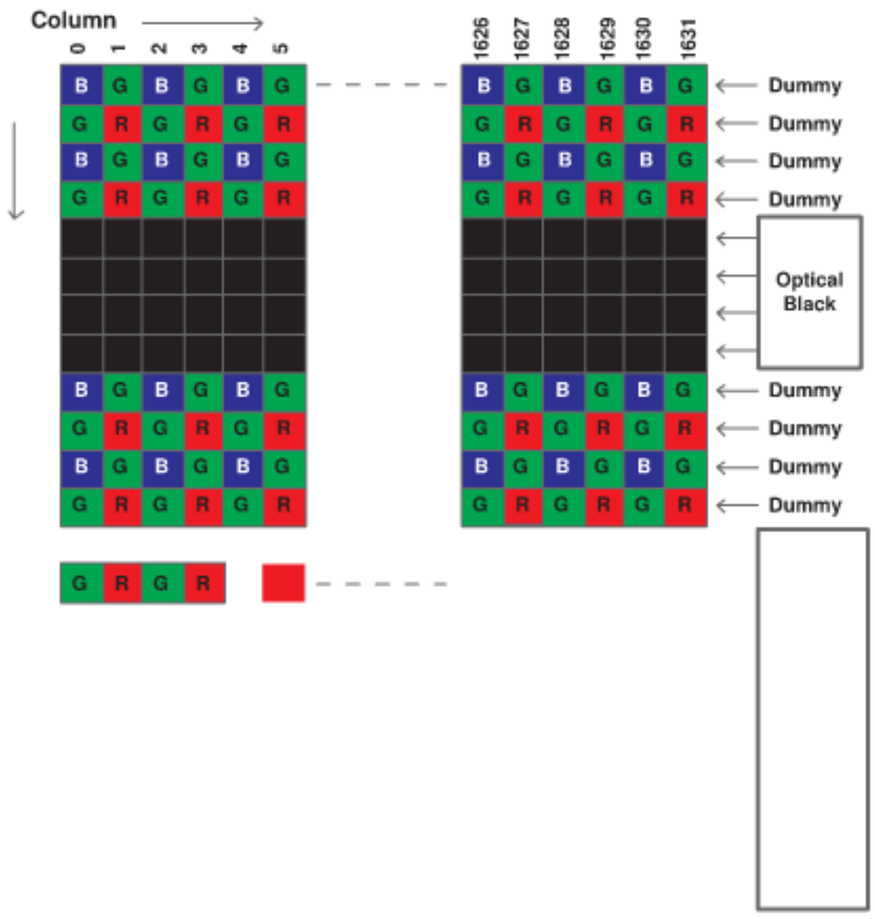


Image Sensor Array

The OV2640 sensor has an image array of 1632 columns by 1232 rows (2,010,624 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Sensor Array Region Color Filter Layout



The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 2,010,624 pixels, 1,991,040 (1632x1220) are active. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

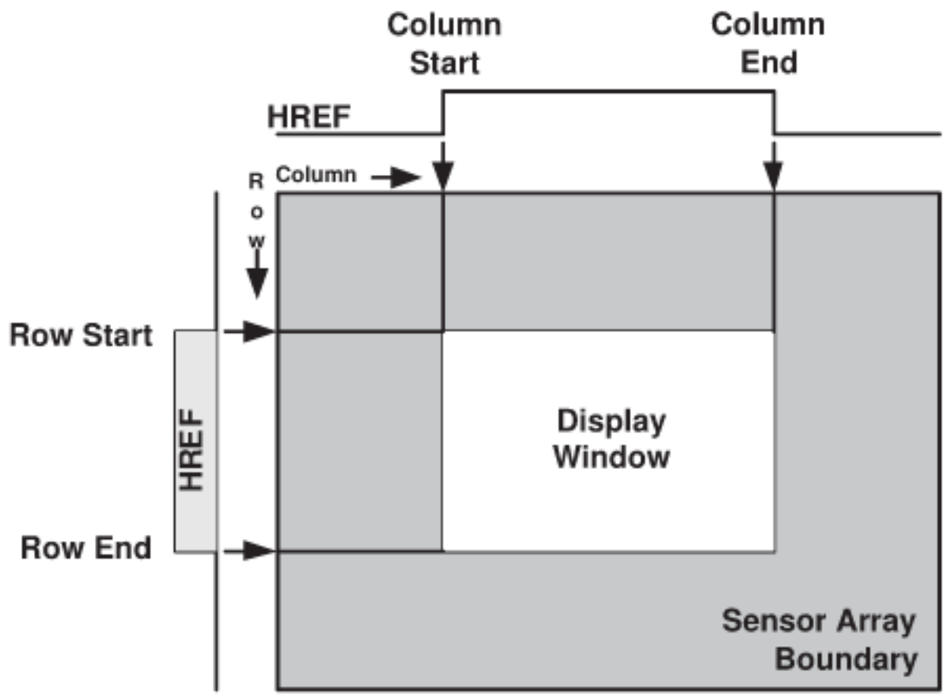
Analog Amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

Gain Control

The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC).

Figure 4 Windowing



Zooming and Panning Mode

The OV2640 provides zooming and panning modes. The user can select this mode under SVGA/CIF mode timing. The related zoom ratios will be 2:1 of UXGA for SVGA and 4:1 of UXGA for CIF. Registers ZOOMS[7:0] (0x49) and COM19[1:0] (0x48) define the vertical line start point. Register ARCOM2[2] (0x34) defines the horizontal start point.

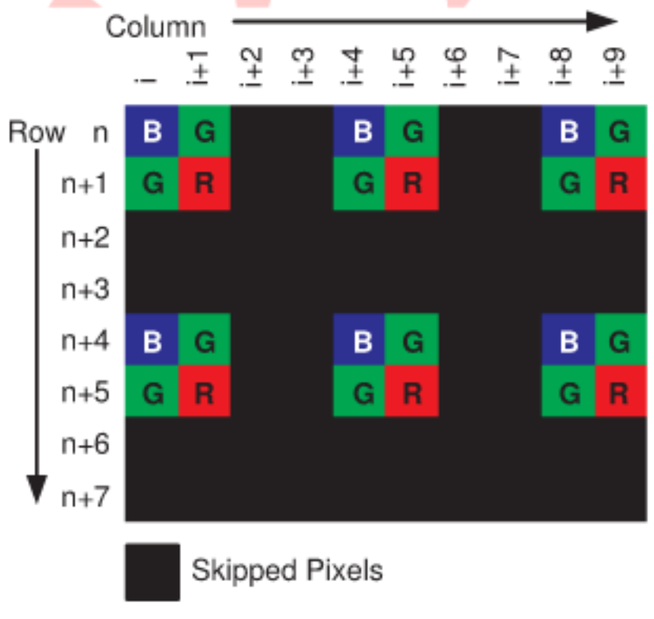
Sub-sampling Mode

The OV2640 supports two sub-sampling modes. Each sub-sampling mode has different resolution and maximum frame rate. These modes are described in the following sections.

SVGA mode

The OV2640 can be programmed to output 800 x 600 (SVGA) sized images for applications where higher resolution image capture is not required. In this mode, both horizontal and vertical pixels will be sub-sampled with an aspect ratio of 4:2 as shown in Figure 5.

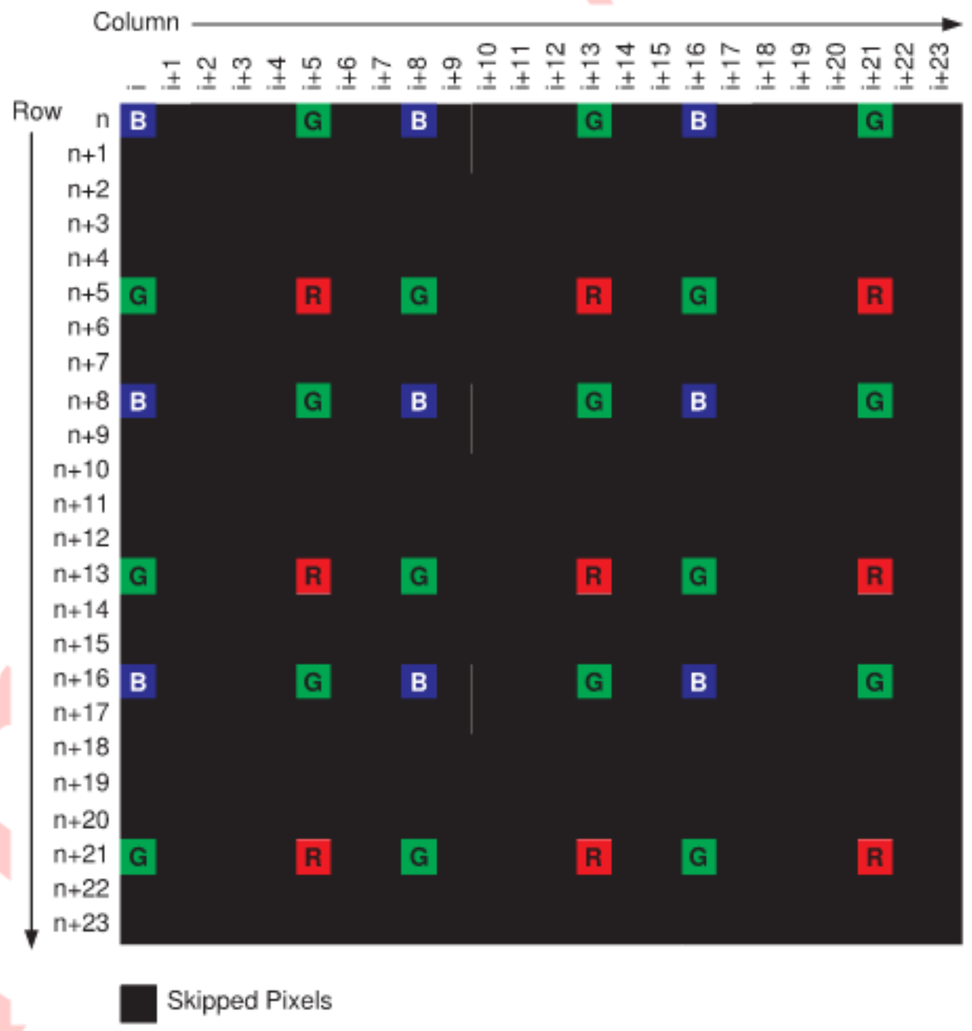
Figure 5 SVGA Sub-Sampling Mode



CIF Mode

The OV2640 can also operate at a higher frame rate to output 400 x 296 sized images. Figure 6 shows the sub-sampling diagram in both horizontal and vertical directions for CIF mode.

Figure 6 CIF Sub-Sampling Mode



Timing Generator and Control Logic

In general, the timing generator controls the following:

- Frame Exposure Mode Timing
- Frame Rate Adjust
- Frame Rate Timing

Frame Exposure Mode Timing

The OV2640 supports frame exposure mode. Typically, the frame exposure mode must work with the aid of an external shutter.

The frame exposure pin, FREX (pin B2), is the frame exposure mode enable pin and the EXPST_B pin (pin A2) serves as the sensor's exposure start trigger. When the external master device asserts the FREX pin high, the sensor array is quickly pre-charged and stays in reset mode until the EXPST_B pin goes low (sensor exposure time can be defined as the period between EXPST_B low and shutter close). After the FREX pin is pulled low, the video data stream is then clocked to the output port in a line-by-line manner. After completing one frame of data

output, the OV2640 will output continuous live video data unless in single frame transfer mode. Figure 18 and Figure 19 show the detailed timing and Table 11 shows the timing specifications for this mode.

Frame Rate Adjust

The OV2640 offers three methods for frame rate adjustment:

- Clock prescaler: (see "CLKRC" on page 23)
  By changing the system clock divide ratio and PLL, the frame rate and pixel rate will change together. This method can be used for dividing the frame/pixel rate by: 1/2, 1/3, 1/4 … 1/64 of the input clock rate.
- Line adjustment: (see "REG2A" on page 26 and "FRARL" on page 26)
  By adding a dummy pixel timing in each line (between HSYNC and pixel data out), the frame rate can be changed while leaving the pixel rate as is.
- Vertical sync adjustment:
  By adding dummy line periods to the vertical sync period (see "ADDVSL" on page 26 and "ADDVSH" on page 26 or see "FLL" on page 27 and "FLH" on page 27), the frame rate can be altered while the pixel rate remains the same.

Frame Rate Timing

Default frame timing is illustrated in Figure 15, Figure 16, and Figure 17. Refer to Table 1 for the actual pixel rate at different frame rates.

Table 1 Frame/Pixel Rates in UXGA Mode

Frame Rate (fps)	15	7.5	2.5	1.25
PCLK (MHz)	36	18	6	3

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit
- White pixel canceling
- De-noise

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Scaling Image Output

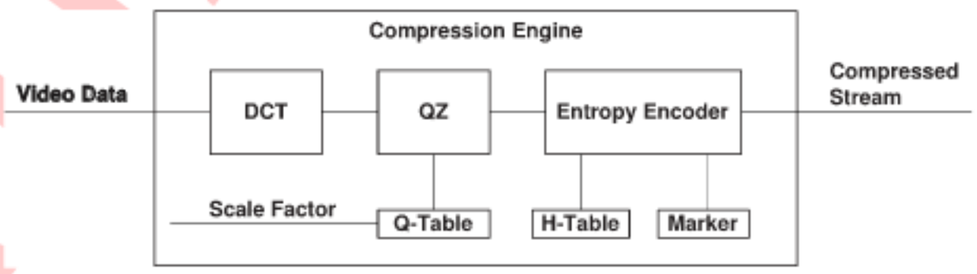
The OV2640 is capable of scaling down the image size from CIF to 40x30. By using SCCB registers, the user can output the desired image size. At certain image sizes, HREF is not consistent in a frame.

Compression Engine

As shown in Figure 7, the Compression Engine consists of three major blocks:

- DCT
- QZ
- Entropy Encoder

Figure 7 Compression Engine Block Diagram



Microcontroller

The OV2640 embeds an 8-bit microcontroller with 512-byte data memory and 4 KB program memory. It provides the flexibility of decoding protocol commands from the host for controlling the system, as well as the ability to fine tune image quality.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Slave Operation Mode

The OV2640 can be programmed to operate in slave mode (default is master mode).

When used as a slave device, COM7[3] (0x12), CLKRC[6] (0x11), and COM2[2] (0x09) register bits should be set to

"1" and the OV2640 will use PWDN and RESETB pins as vertical and horizontal synchronization triggers supplied by a master device. The master device must provide the following signals:

1. System clock MCLK to XVCLK pin
2. Horizontal sync MHSYNC to RESETB pin
3. Vertical frame sync MVSYNC to PWDN pin

See Figure 8 for slave mode connections and Figure 9 for detailed timing considerations.

Figure 8 Slave Mode Connection

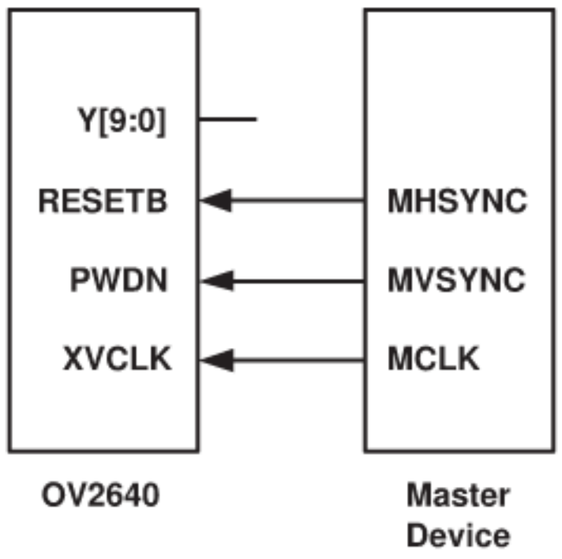
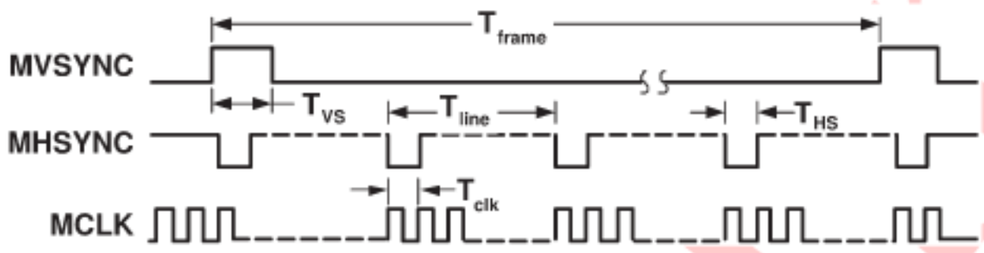


Figure 9 Slave Mode Timing



NOTE:

1) $T_{HS} > 6\ T_{clk}$, $Tvs > T_{line}$
2) $T_{line} = 1922 \times T_{clk}$ (UXGA); $T_{line} = 1190 \times T_{clk}$ (SVGA); $T_{line} = 595 \times T_{clk}$ (CIF)
3) $T_{frame} = 1248 \times T_{line}$ (UXGA); $T_{frame} = 672 \times T_{line}$ (SVGA); $T_{frame} = 336 \times T_{line}$ (CIF)

Strobe Mode

The OV2640 has a Strobe mode that allows it to work with an external flash and LED.

Reset

The OV2640 includes a RESETB pin (pin C6) that forces a complete hardware reset when it is pulled low (GND). The OV2640 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface.

Power Down Mode

Two methods are available to place the OV2640 into power-down mode: hardware power-down and SCCB software power-down.

To initiate hardware power-down, the PWDN pin (pin B6) must be tied to high. When this occurs, the OV2640 internal device clock is halted and all internal counters are reset. The current draw is less than 15 µA in this standby mode.

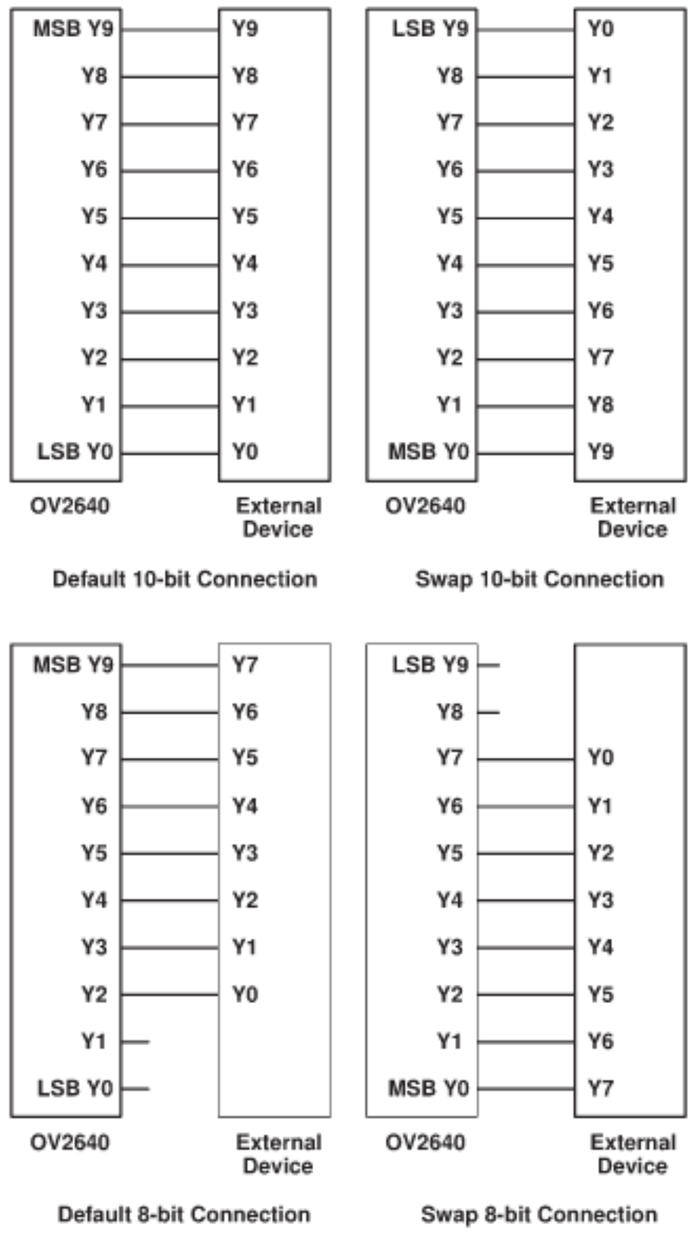
Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. The current requirements drop to less than 1 mA in this mode. All register content is maintained in standby mode.

Digital Video Port

MSB/LSB Swap

The OV2640 has a 10-bit digital video port. The MSB and LSB can be swapped with the control registers. Figure 10 shows some examples of connections with external devices.

Figure 10 Connection Examples



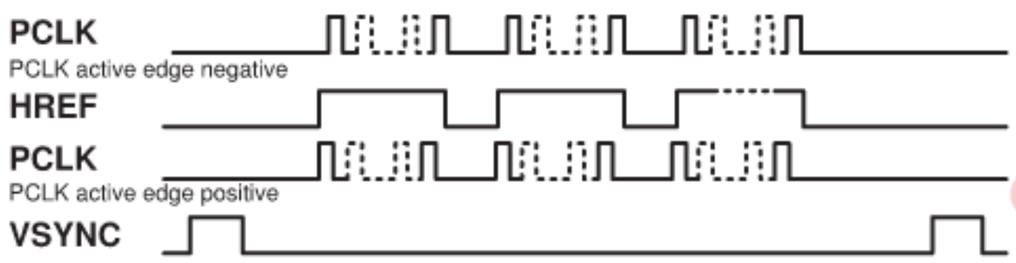
Line/Pixel Timing

The OV2640 digital video port can be programmed to work in either master or slave mode.

In both master and slave modes, pixel data output is synchronous with PCLK (or MCLK if port is a slave), HREF, and VSYNC. The default PCLK edge for valid data is the negative edge but may be programmed using register COM10[4] for the positive edge. Basic line/pixel output timing and pixel timing specifications are shown in Figure 14 and Table 10.

Also, using register COM10[5], PCLK output can be gated by the active video period defined by the HREF signal. See Figure 11 for details.

Figure 11 PCLK Output Only at Valid Pixels



The specifications shown in Table 10 apply for DVDD = +1.2 V, DOVDD = +2.8 V, T_A = 25°C, sensor working at 15 fps, external loading = 20 pF.

Pixel Output Pattern

Table 2 shows the output data order from the OV2640. The data output sequence following the first HREF and after VSYNC is: $B_{0,0}$ $G_{0,1}$ $B_{0,2}$ $G_{0,3}$... $B_{0,1598}$ $G_{0,1599}$. After the second HREF the output is $G_{1,0}$ $R_{1,1}$ $G_{1,2}$ $R_{1,3}$... $G_{1,1598}$ $R_{1,1599}$..., etc. If the OV2640 is programmed to output SVGA resolution data, horizontal and vertical sub-sampling will occur. The default output sequence for the first line of output will be: $B_{0,0}$ $G_{0,1}$ $B_{0,4}$ $G_{0,5}$... $B_{0,1596}$ $G_{0,1597}$. The second line of output will be: $G_{1,0}$ $R_{1,1}$ $G_{1,4}$ $R_{1,5}$... $G_{1,1596}$ $R_{1,1597}$.

Table 2 Data Pattern

R/C	0	1	2	3	. . .	1598	1599
0	$B_{0,0}$	$G_{0,1}$	$B_{0,2}$	$G_{0,3}$	. . .	$B_{0,1598}$	$G_{0,1599}$
1	$G_{1,0}$	$R_{1,1}$	$G_{1,2}$	$R_{1,3}$	. . .	$G_{1,1598}$	$R_{1,1599}$
2	$B_{2,0}$	$G_{2,1}$	$B_{2,2}$	$G_{2,3}$	. . .	$B_{2,1598}$	$G_{2,1599}$
3	$G_{3,0}$	$R_{3,1}$	$G_{3,2}$	$R_{3,3}$	. . .	$G_{3,1598}$	$R_{3,1599}$
. .					. .		
1198	$B_{1198,0}$	$G_{1198,1}$	$B_{1198,2}$	$G_{1198,3}$	. . .	$B_{1198,1598}$	$G_{1198,1599}$
1199	$G_{1199,0}$	$R_{1199,1}$	$G_{1199,2}$	$R_{1199,3}$	. . .	$G_{1199,1598}$	$R_{1199,1599}$

Pin Description

Table 3 Pin Description

Pin Location	Name	Pin Type	Function/Description
A1	DOGND	Ground	Ground for digital video port
A2	EXPST_B	Input	Snapshot Exposure Start Trigger 0: Sensor starts exposure (only effective in snapshot mode) 1: Sensor stays in reset mode Note: There is no internal pull-up/pull-down resistor.
A3	AGND	Ground	Ground for analog circuit
A4	SGND	Ground	Ground for sensor array
A5	VREFN	Reference	Internal analog reference - connect to ground using a 0.1 µF capacitor
A6	STROBE	I/O	Flash control output Default: Input Note: There is no internal pull-up/pull-down resistor.
B1	DOVDD	Power	Power for digital video port
B2	FREX	Input	Snapshot trigger - use to activate a snapshot sequence Note: There is no internal pull-up/pull-down resistor.
B3	AVDD	Power	Power for analog circuit
B4	SVDD	Power	Power for sensor array
B5	SVDD	Power	Power for sensor array
B6	PWDN	Input	Power-down mode enable, active high Note: There is an internal pull-down resistor.
C1	SIO_D	I/O	SCCB serial interface data I/O
C2	SIO_C	Input	SCCB serial interface clock input Note: There is no internal pull-up/pull-down resistor.
C3	HREF	I/O	Horizontal reference output Default: Input Note: There is no internal pull-up/pull-down resistor.
C4	XVCLK	Input	System clock input Note: There is no internal pull-up/pull-down resistor.
C5	VREFH	Reference	Internal analog reference - connect to ground using a 0.1 µF capacitor
C6	RESETB	Input	Reset mode, active low Note: There is an internal pull-up resistor.
D2	VSYNC	I/O	Vertical synchronization output Default: Input Note: There is no internal pull-up/pull-down resistor.
D6	NC	–	No connection
E1	Y1	I/O	Video port output bit[1] Default: Input Note: There is no internal pull-up/pull-down resistor.

Table 3 Pin Description

Pin Location	Name	Pin Type	Function/Description
E2	Y0	I/O	Video port output bit[0] Default: Input Note: There is no internal pull-up/pull-down resistor.
E3	PCLK	I/O	Pixel clock output Default: Input Note: There is no internal pull-up/pull-down resistor.
E4	EGND	Ground	Ground for internal regulator
E5	Y6	I/O	Video port output bit[6] Default: Input Note: There is no internal pull-up/pull-down resistor.
E6	DGND	Ground	Ground for digital core
F1	EVDD	Power	Power for internal regulator
F2	DVDD	Power	Sensor digital power (Core)
F3	Y2	I/O	Video port output bit[2] Default: Input Note: There is no internal pull-up/pull-down resistor.
F4	Y4	I/O	Video port output bit[4] Default: Input Note: There is no internal pull-up/pull-down resistor.
F5	Y8	I/O	Video port output bit[8] Default: Input Note: There is no internal pull-up/pull-down resistor.
F6	DVDD	Power	Sensor digital power (Core)
G1	EVDD	Power	Power for internal regulator
G2	DGND	Ground	Ground for digital core
G3	Y3	I/O	Video port output bit[3] Default: Input Note: There is no internal pull-up/pull-down resistor.
G4	Y5	I/O	Video port output bit[5] Default: Input Note: There is no internal pull-up/pull-down resistor.
G5	Y7	I/O	Video port output bit[7] Default: Input Note: There is no internal pull-up/pull-down resistor.
G6	Y9	I/O	Video port output bit[9] Default: Input Note: There is no internal pull-up/pull-down resistor.

Figure 12 Pinout Diagram

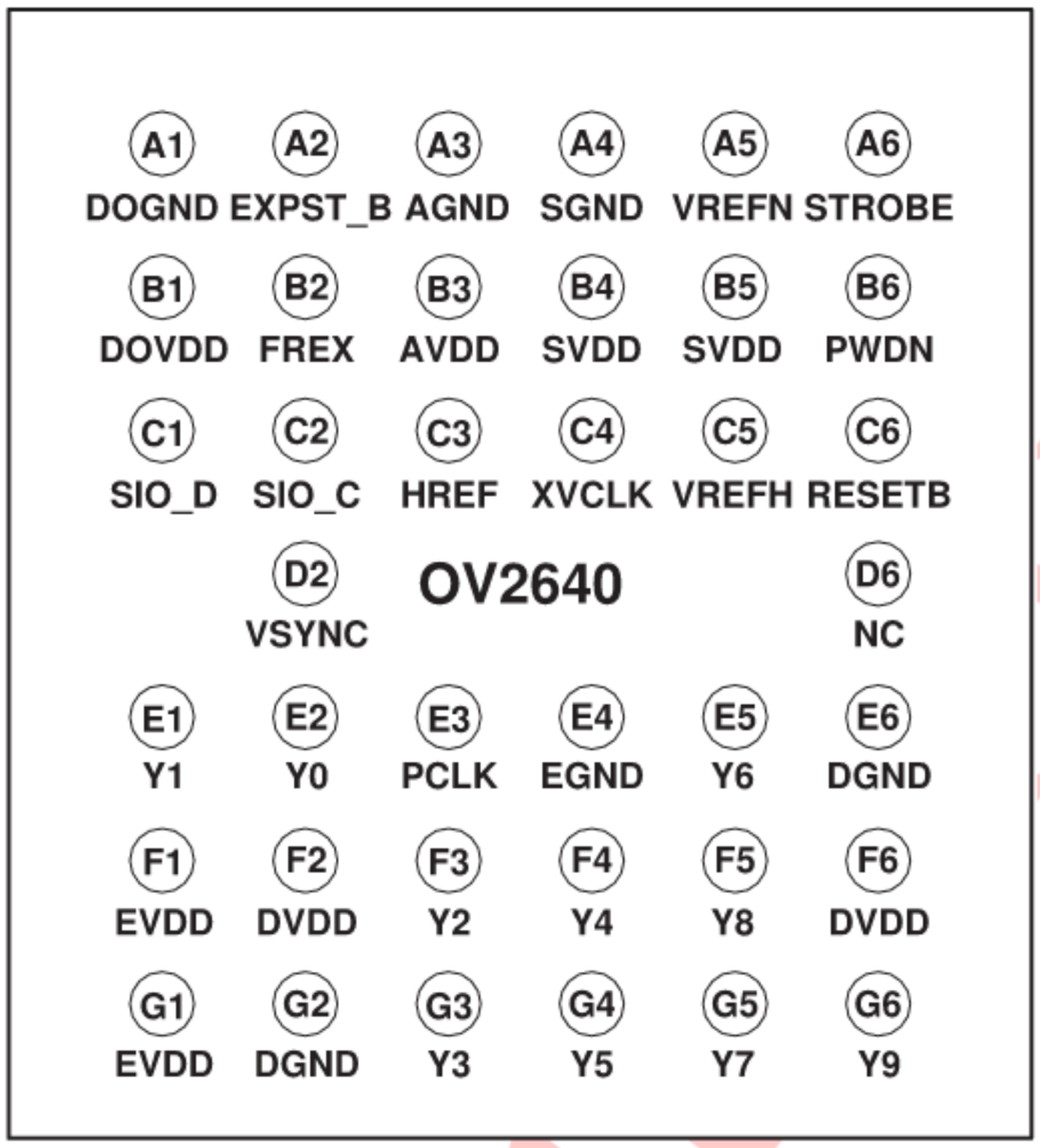


Table 4 Ball Matrix

	1	2	3	4	5	6
A	DOGND	EXPST_B	AGND	SGND	VREFN	STROBE
B	DOVDD	FREX	AVDD	SVDD	SVDD	PWDN
C	SIO_D	SIO_C	HREF	XVCLK	VREFN	RESETB
D		VSYNC				NC
E	Y1	Y0	PCLK	EGND	Y6	DGND
F	EVDD	DVDD	Y2	Y4	Y8	DVDD
G	EVDD	DGND	Y3	75	Y7	Y9

Electrical Characteristics

Table 5 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+1V
Lead-free Temperature, Surface-mount process		245ºC

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 6 DC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD-A}	Supply voltage	2.5[a]	2.8	3.0	V
V_{DD-D}	Supply voltage	1.24	1.3	1.36	V
V_{DD-IO}	Supply voltage[b]	1.71	2.8	3.3	V
I_{DDA-A}	Active (Operating) Current[c]		30	40	mA
I_{DDA-D}	Active (Operating) Current[c]		30 (YUV) 45 (Compressed)	40 (YUV) 60 (Compressed)	mA
I_{DDA-IO}	Active (Operating) Current[c]		6	15	mA
$I_{DDS-SCCB}$	Standby Current[d]		1	2	mA
$I_{DDS-PWDN}$			600	1200	µA
Digital Inputs					
V_{IL}	Input voltage LOW			0.54	V
V_{IH}	Input voltage HIGH	1.26			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF)					
V_{OH}	Output voltage HIGH	1.62			V
V_{OL}	Output voltage LOW			0.18	V
Serial Interface Inputs					
V_{IL}	SIO_C and SIO_D	-0.5	0	0.54	V
V_{IH}	SIO_C and SIO_D	1.26	1.8	2.3	V

a. If using internal regulator for DVDD, V_{DD-A} requires greater than or equal to 2.65V

b. 1.8V I/O is supported. Contact your local OmniVision FAE for further details.

c. V_{DD-A} = 2.8V, V_{DD-D} = 1.3V, and V_{DD-IO} = 1.8V for 15 fps in UXGA mode

d. $I_{DDS-SCCB}$ refers to SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to PWDN pad-initiated Standby

Table 7 AC Characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

Symbol	Parameter	Min	Typ	Max	Unit
ADC Parameters					
B	Analog bandwidth		20		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for UXGA/SVGA mode change			<1	ms
	Settling time for register setting			<300	ms

Table 8 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XVCLK)	6	24		MHz
t_r, t_f	Clock input rise/fall time			5	ns
	Clock input duty cycle	45	50	55	%

Timing Specifications

Figure 13 SCCB Interface Timing Diagram

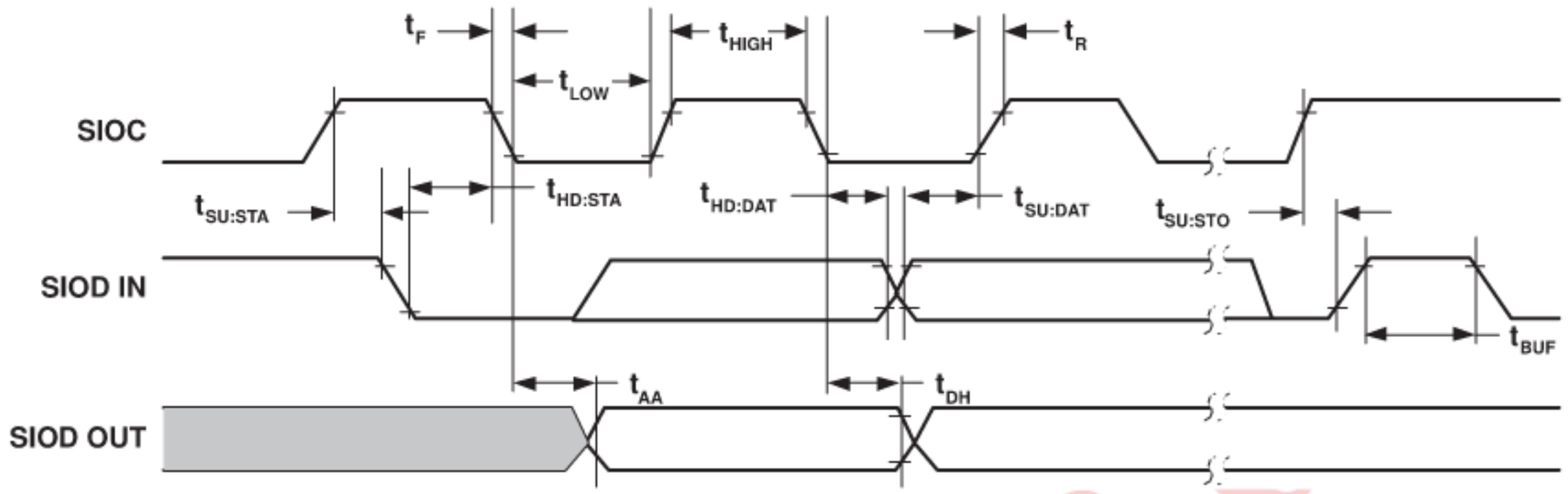


Table 9 SCCB InterfaceTiming Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIOC low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Figure 14 UXGA, SVGA, and CIF Line/Pixel Output Timing

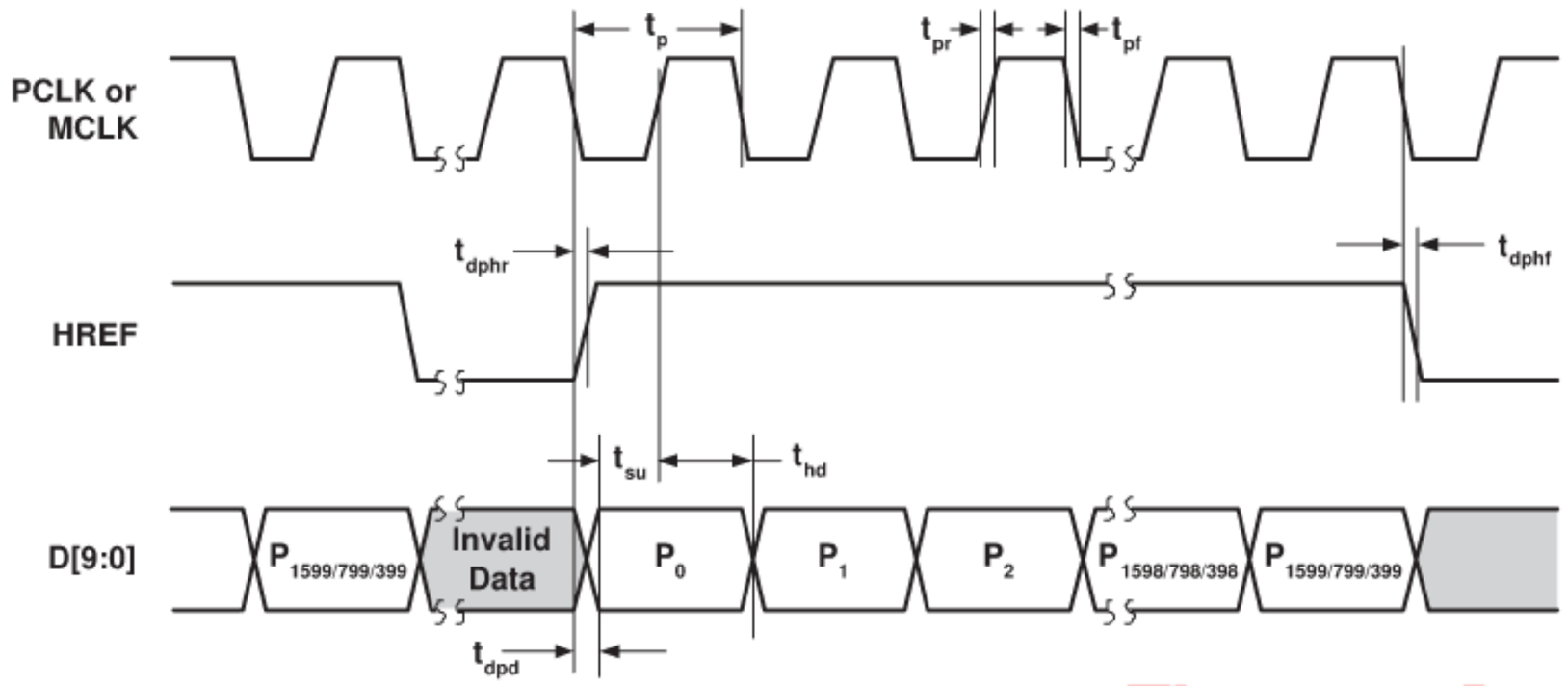


Table 10 Pixel Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period		27.78		ns
t_{pr}	PCLK rising time		3.5		ns
t_{pf}	PCLK falling time		2.2		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 15 UXGA Frame Timing

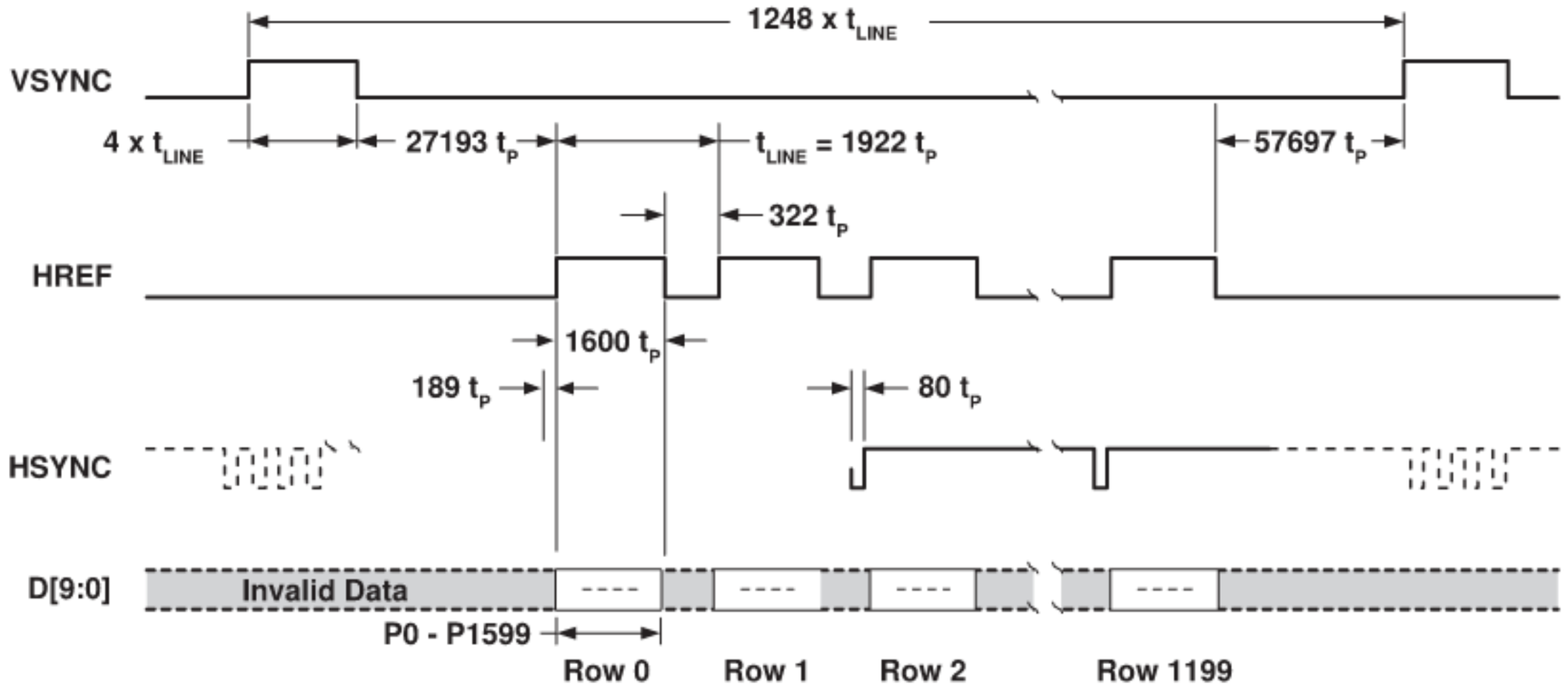


Figure 16 SVGA Frame Timing

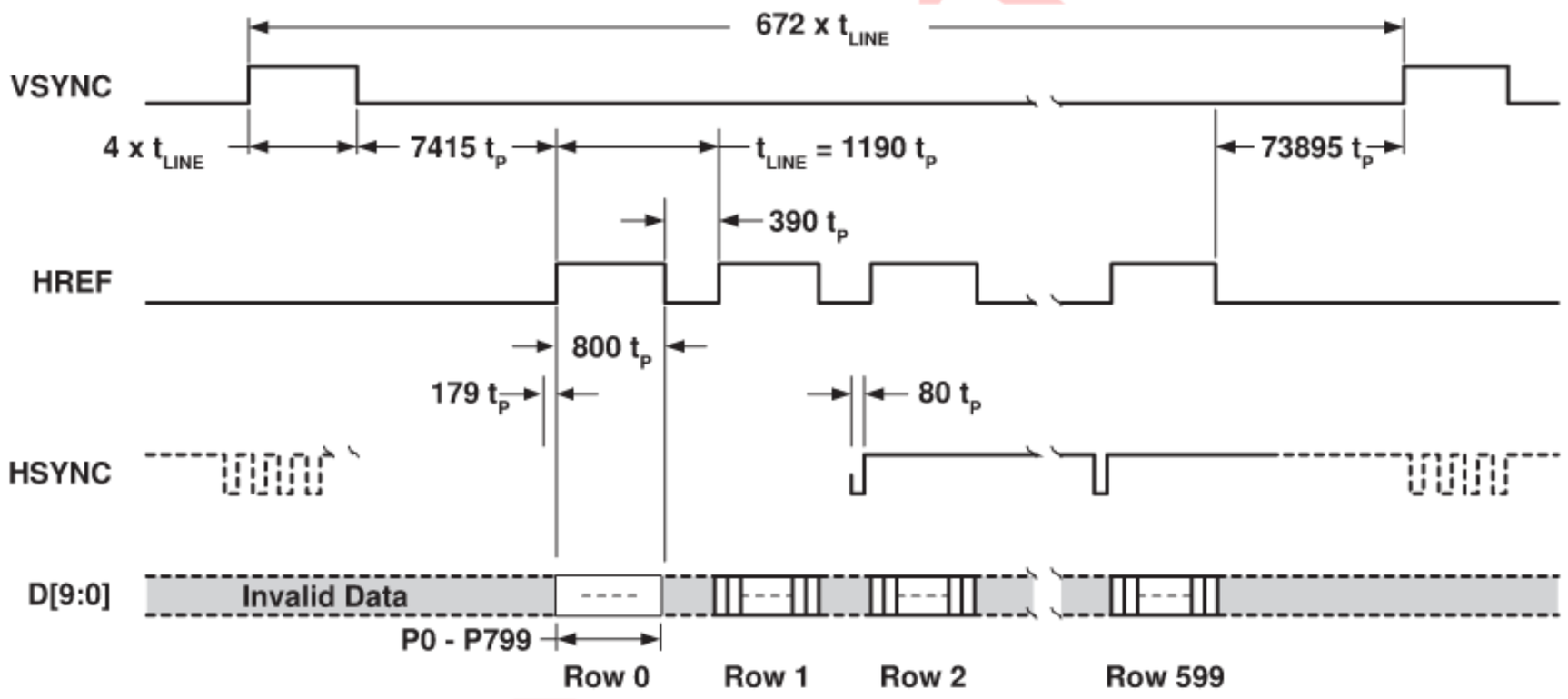


Figure 17 CIF Mode Frame Timing

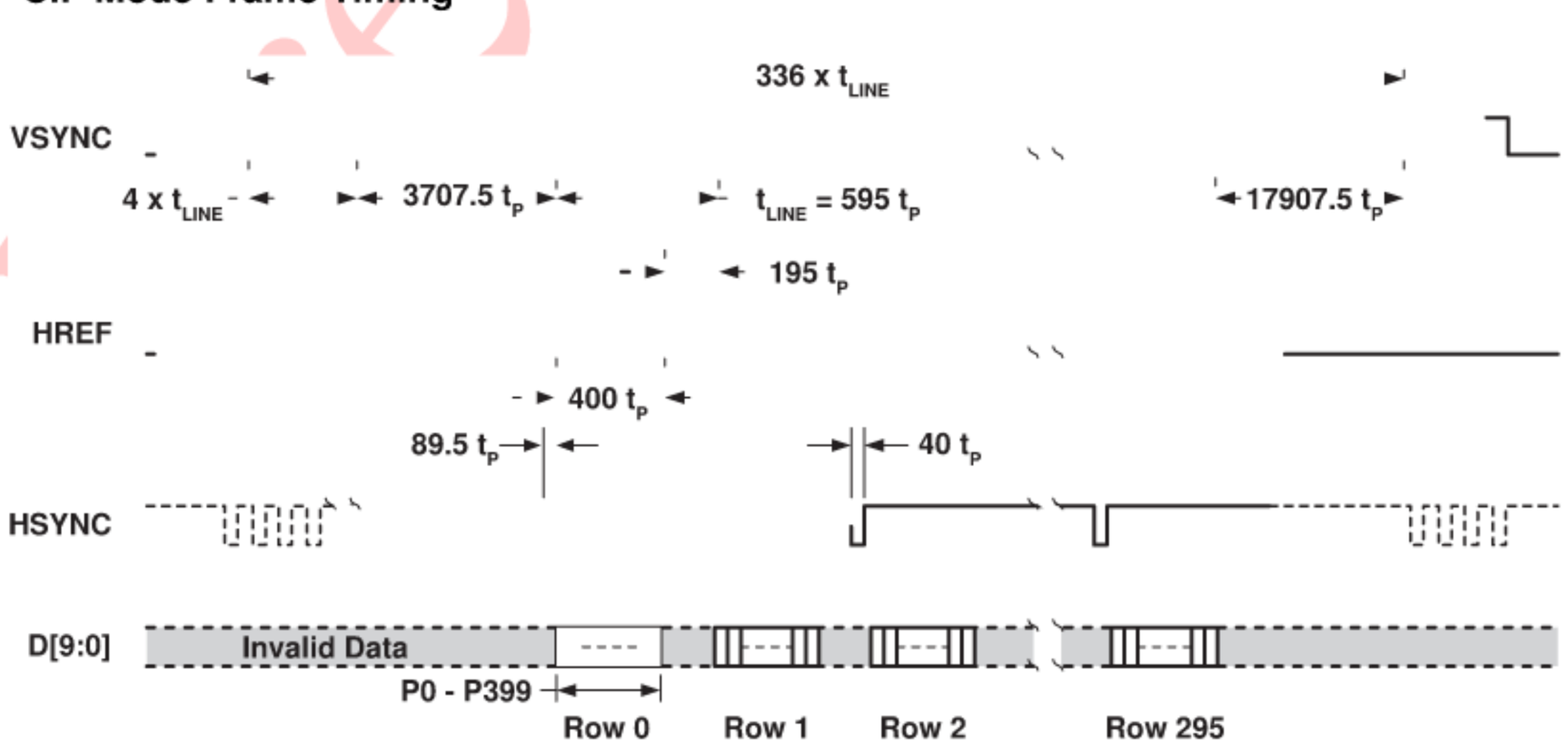


Figure 18 Frame Exposure Mode Timing with EXPST_B Staying Low

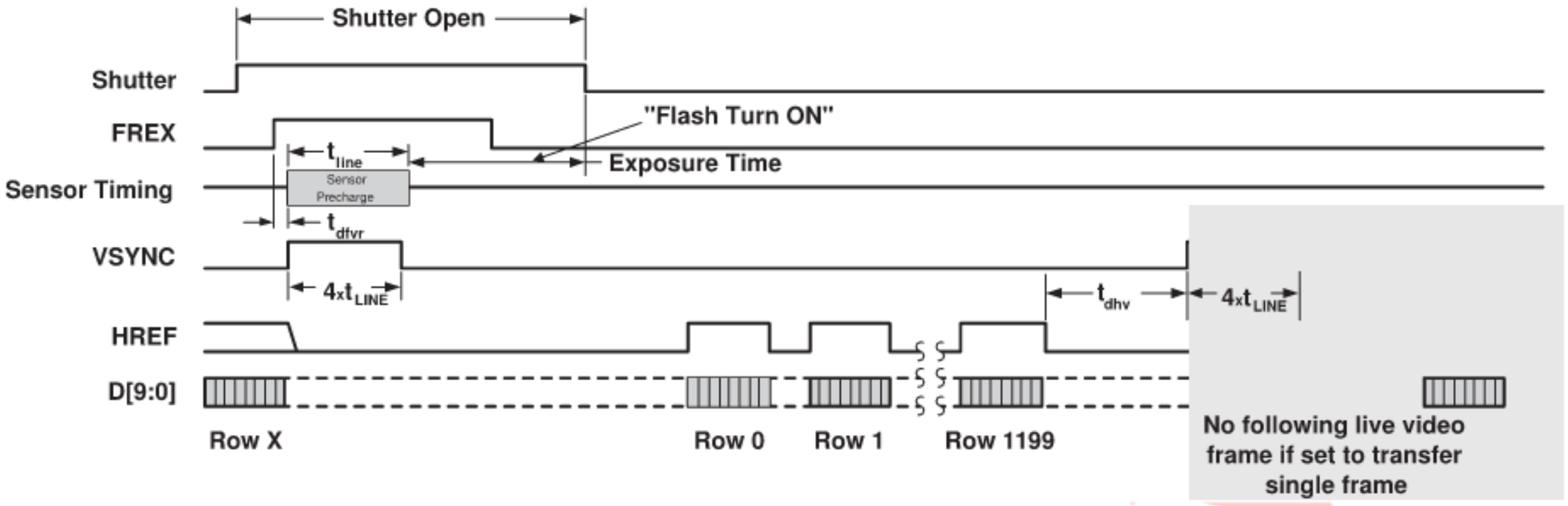


Figure 19 Frame Exposure Mode Timing with EXPST_B Asserted

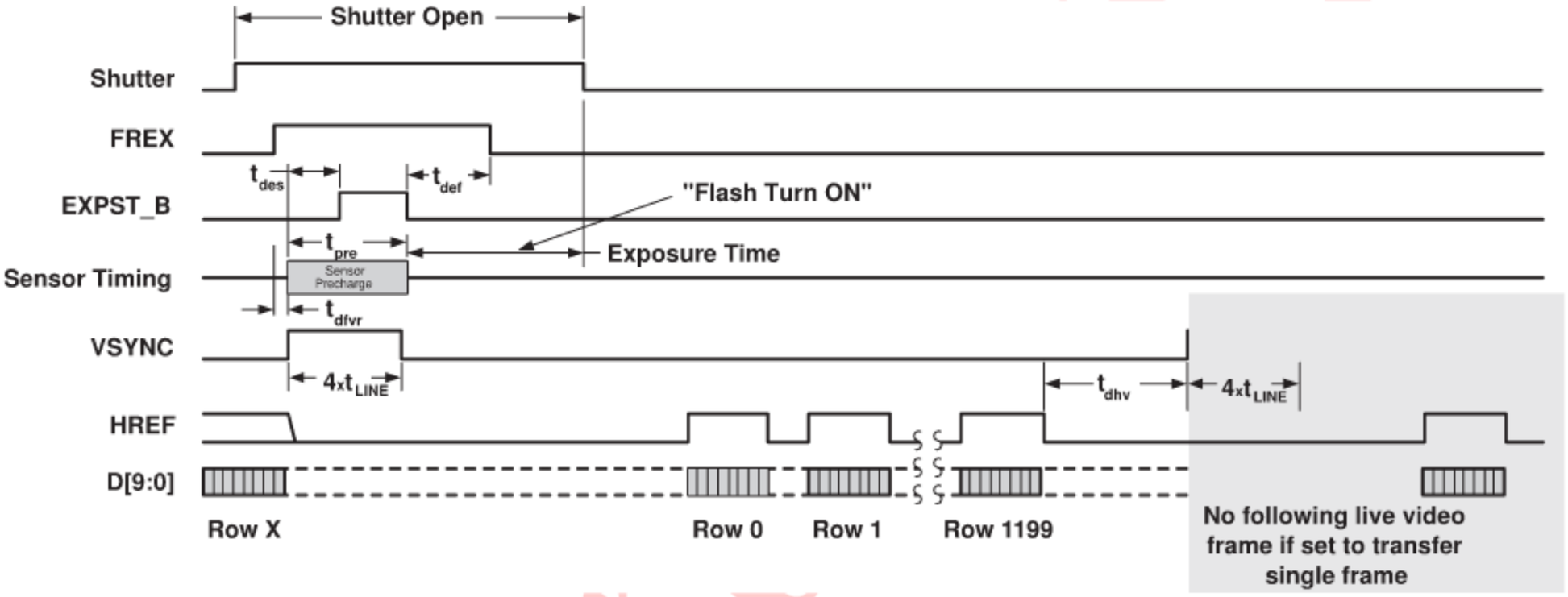


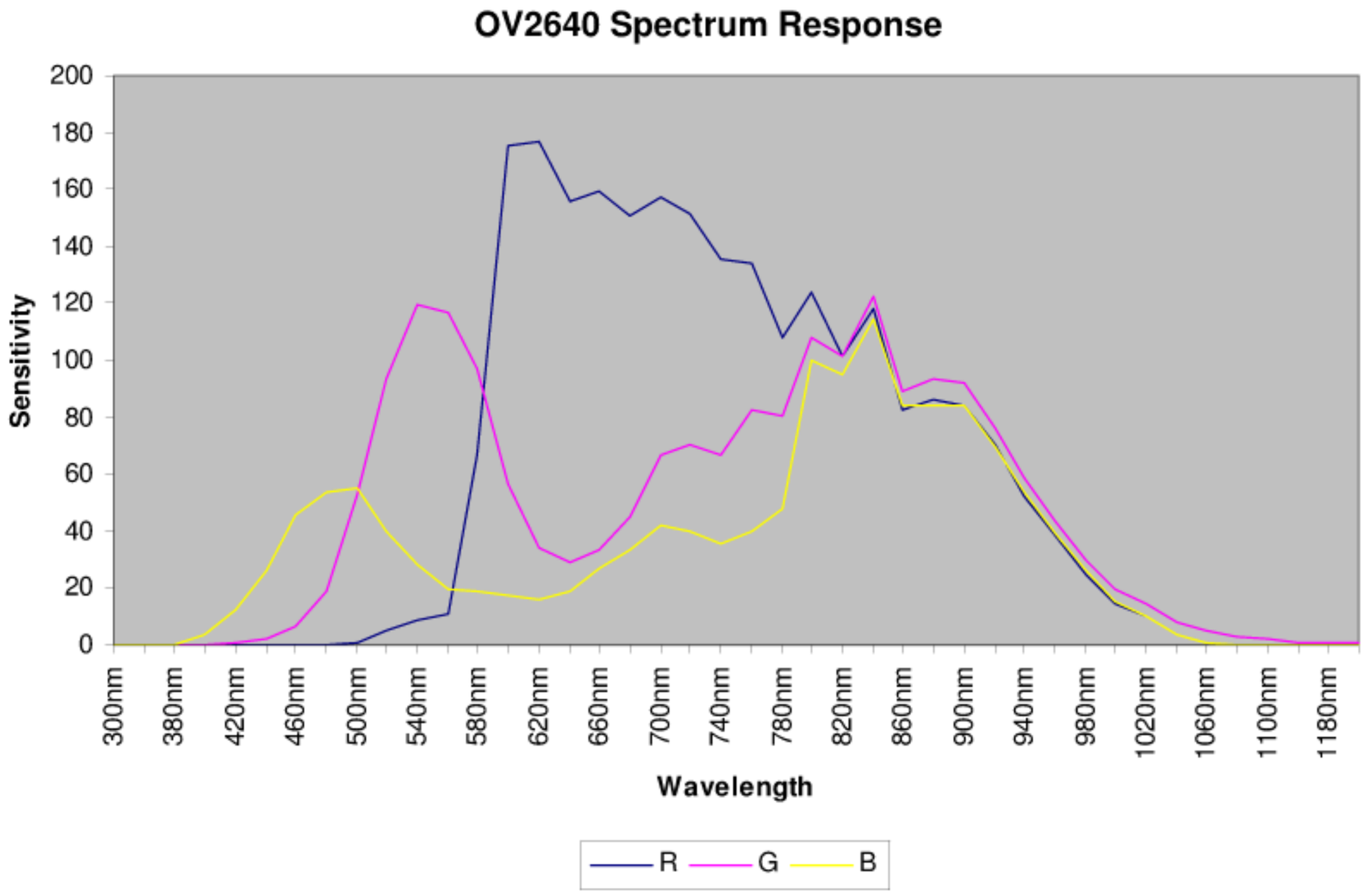
Table 11 Frame Exposure Timing Specifications

Symbol	Min	Typ	Max	Unit
tline		1922 (UXGA)		tp
tvs		4		tline
tdfvr	8		9	tp
tdhv		38964 (UXGA)		tp
tdhso	0			ns
tdef	20			tp
tdes	8		1900 (UXGA)	tp

NOTE 1) FREX must stay high long enough to ensure the entire sensor has been reset.
2) Shutter must be closed no later then 3896 tp after VSYNC falling edge.

OV2640 Light Response

Figure 20 OV2640 Light Response



Register Set

Table 12 and Table 13 provides a list and description of the Device Control registers contained in the OV2640. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 60 for write and 61 for read.

There are two different sets of register banks. Register 0xFF controls which set is accessible. When register 0xFF=00, Table 12 is effective. When register 0xFF=01, Table 13 is effective.

Table 12 Device Control Register List (when 0xFF = 00) (Sheet 1 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00-04	RSVD	XX	–	Reserved
05	R_BYPASS	0x1	RW	Bypass DSP Bit[7:1]: Reserved Bit[0]: Bypass DSP select 0: DSP 1: Bypass DSP, sensor out directly
06-43	RSVD	XX	–	Reserved
44	Qs	0C	RW	Quantization Scale Factor
45-4F	RSVD	XX	–	Reserved
50	CTRLI[7:0]	00	RW	Bit[7]: LP_DP Bit[6]: Round Bit[5:3]: V_DIVIDER Bit[2:0]: H_DIVIDER
51	HSIZE[7:0]	40	RW	H_SIZE[7:0] (real/4)
52	VSIZE[7:0]	F0	RW	V_SIZE[7:0] (real/4)
53	XOFFL[7:0]	00	RW	OFFSET_X[7:0]
54	YOFFL[7:0]	00	RW	OFFSET_Y[7:0]
55	VHYX[7:0]	08	RW	Bit[7]: V_SIZE[8] Bit[6:4]: OFFSET_Y[10:8] Bit[3]: H_SIZE[8] Bit[2:0]: OFFSET_X[10:8]
56	DPRP[7:0]	00	RW	Bit[7:4]: DP_SELY Bit[3:0]: DP_SELX
57	TEST[3:0]	00	RW	Bit[7]: H_SIZE[9] Bit[6:0]: Reserved
5A	ZMOW[7:0]	58	RW	OUTW[7:0] (real/4)
5B	ZMOH[7:0]	48	RW	OUTH[7:0] (real/4)
5C	ZMHH[1:0]	00	RW	Bit[7:4]: ZMSPD (zoom speed) Bit[2]: OUTH[8] Bit[1:0]: OUTW[9:8]
5D-7B	RSVD	XX	–	Reserved
7C	BPADDR[3:0]	00	RW	SDE Indirect Register Access: Address

Table 12 Device Control Register List (when 0xFF = 00) (Sheet 2 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
7D	BPDATA[7:0]	00	RW	SDE Indirect Register Access: Data
7E-85	RSVD	XX	–	Reserved
86	CTRL2	0D	RW	Module Enable Bit[7:6]: Reserved Bit[5]: DCW Bit[4]: SDE Bit[3]: UV_ADJ Bit[2]: UV_AVG Bit[1]: Reserved Bit[0]: CMX
87	CTRL3	50	RW	Module Enable Bit[7]: BPC Bit[6]: WPC Bit[5:0]: Reserved
88-8B	RSVD	XX	–	Reserved
8C	SIZEL[5:0]	00	RW	{HSIZE[11], HSIZE[2:0], VSIZE[2:0]}
8D-BF	RSVD	XX	–	Reserved
C0	HSIZE8[7:0]	80	RW	Image Horizontal Size HSIZE[10:3]
C1	VSIZE8[7:0]	60	RW	Image Vertical Size VSIZE[10:3]
C2	CTRL0	0C	RW	Module Enable Bit[7]: AEC_EN Bit[6]: AEC_SEL Bit[5]: STAT_SEL Bit[4]: VFIRST Bit[3]: YUV422 Bit[2]: YUV_EN Bit[1]: RGB_EN Bit[0]: RAW_EN
C3	CTRL1	FF	RW	Module Enable Bit[7]: CIP Bit[6]: DMY Bit[5]: RAW_GMA Bit[4]: DG Bit[3]: AWB Bit[2]: AWB_GAIN Bit[1]: LENC Bit[0]: PRE
C4-D2	RSVD	XX	–	Reserved

Table 12 Device Control Register List (when 0xFF = 00) (Sheet 3 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
D3	R_DVP_SP	82	RW	Bit[7]: Auto mode Bit[6:0]: DVP output speed control DVP PCLK = sysclk (48)/[6:0] (YUV0); = sysclk (48)/(2*[6:0]) (RAW)
D4-D9	RSVD	XX	–	Reserved
DA	IMAGE_MODE	00		Image Output Format Select Bit[7]: Reserved Bit[6]: Y8 enable for DVP Bit[5]: Reserved Bit[4]: JPEG output enable 0: Non-compressed 1: JPEG output Bit[3:2]: DVP output format 00: YUV422 01: RAW10 (DVP) 10: RGB565 11: Reserved Bit[1]: HREF timing select in DVP JPEG output mode 0: HREF is same as sensor 1: HREF = VSYNC Bit[0]: Byte swap enable for DVP 0: High byte first YUYV (C2[4]=0) YVYU (C2[4] = 1) 1: Low byte first UYVY (C2[4] =0) VYUY (C2[4] =1)
DB-DF	RSVD	XX	–	Reserved
E0	RESET	04	RW	Reset Bit[7]: Reserved Bit[6]: Microcontroller Bit[5]: SCCB Bit[4]: JPEG Bit[3]: Reserved Bit[2]: DVP Bit[1]: IPU Bit[0]: CIF
E1-EF	RSVD	XX	–	Reserved
F0	MS_SP	04	RW	SCCB Master Speed
F1-F6	RSVD	XX	–	Reserved
F7	SS_ID		RW	SCCB Slave ID

Table 12 Device Control Register List (when 0xFF = 00) (Sheet 4 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
F8	SS_CTRL	01	RW	SCCB Slave Control Bit[7:6]: Reserved Bit[5]: Address auto-increase enable Bit[4]: Reserved Bit[3]: SCCB enable Bit[2]: Delay SCCB master clock Bit[1]: Enable SCCB master access Bit[0]: Enable sensor pass through access
F9	MC_BIST		RW	Bit[7]: Microcontroller Reset Bit[6]: Boot ROM select Bit[5]: R/W 1 error for 12K-byte memory Bit[4]: R/W 0 error for 12K-byte memory Bit[3]: R/W 1 error for 512-byte memory Bit[2]: R/W 0 error for 512-byte memory Bit[1]: BIST busy bit for read; One-shot reset of microcontroller for write Bit[0]: Launch BIST
FA	MC_AL		RW	Program Memory Pointer Address Low Byte
FB	MC_AH		RW	Program Memory Pointer Address High Byte
FC	MC_D	80	RW	Program Memory Pointer Access Address Boundary of register address to separate DSP and sensor register
FD	P_CMD	00	RW	SCCB Protocol Command Register
FE	P_STATUS	00	RW	SCCB Protocol Status Register
FF	RA_DLMT	7F	RW	Register Bank Select Bit[7:1]: Reserved Bit[0]: Register bank select 0: DSP address 1: Sensor address
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 1 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control LSBs Bit[7:0]: Gain setting • Range: 1x to 32x Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16) ***Note:*** *Set COM8[2] = 0 to disable AGC.*
01-02	RSVD	XX	–	Reserved
03	COM1	0F (UXGA) 0A (SVGA), 06 (CIF)	RW	Common Control 1 Bit[7:6]: Dummy frame control 00: Reserved 01: Allow 1 dummy frame 10: Allow 3 dummy frames 11: Allow 7 dummy frames Bit[5:4]: Reserved Bit[3:2]: Vertical window end line control 2 LSBs (8 MSBs in VEND[7:0] (0x1A)) Bit[1:0]: Vertical window start line control 2 LSBs (8 MSBs in VSTRT[7:0] (0x19))
04	REG04	20	RW	Register 04 Bit[7]: Horizontal mirror Bit[6]: Vertical flip Bit[4]: VREF bit[0] Bit[3]: HREF bit[0] Bit[2]: Reserved Bit[1:0]: AEC[1:0] (AEC[15:10] is in register REG45[5:0] (0x45), AEC[9:2] is in register AEC[7:0] (0x10))
05-07	RSVD	XX	–	Reserved
08	REG08	40	RW	Frame Exposure One-pin Control Pre-charge Row Number
09	COM2	00	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Standby mode enable 0: Normal mode 1: Standby mode Bit[3]: Reserved Bit[2]: Pin PWDN/RESETB used as SLVS/SLHS Bit[1:0]: Output drive select 00: 1x capability 01: 3x capability 10: 2x capability 11: 4x capability
0A	PIDH	26	R	Product ID Number MSB (Read only)
0B	PIDL	41	R	Product ID Number LSB (Read only)

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 2 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0C	COM3	38	RW	Common Control 3 Bit[7:3]: Reserved Bit[2]: Set banding manually 0: 60 Hz 1: 50 Hz Bit[1]: Auto set banding Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D	COM4	07	RW	Common Control 4 Bit[7:3]: Reserved Bit[2]: Clock output power-down pin status 0: Tri-state data output pin upon power-down 1: Data output pin hold at last state before power-down Bit[1:0]: Reserved
0E-0F	RSVD	XX	–	Reserved
10	AEC	33	RW	Automatic Exposure Control 8 bits for AEC[9:2] (AEC[15:10] is in register REG45[5:0] (0x45), AEC[1:0] is in register REG04[1:0] (0x04)) AEC[15:0]: Exposure time $T_{EX} = t_{LINE}$ x AEC[15:0] ***Note:*** *The maximum exposure time is 1 frame period even if TEX is longer than 1 frame period.*
11	CLKRC	00	RW	Clock Rate Control Bit[7]: Internal frequency doublers ON/OFF selection 0: OFF 1: ON Bit[6]: Reserved Bit[5:0]: Clock divider CLK = XVCLK/(decimal value of CLKRC[5:0] + 1)

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 3 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	COM7	00	RW	Common Control 7 Bit[7]: SRST 1: Initiates system reset. All registers are set to factory default values after which the chip resumes normal operation Bit[6:4]: Resolution selection 000: UXGA (full size) mode 001: CIF mode 100: SVGA mode Bit[3]: Reserved Bit[2]: Zoom mode Bit[1]: Color bar test pattern 0: OFF 1: ON Bit[0]: Reserved
13	COM8	C7	RW	Common Control 8 Bit[7:6]: Reserved Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure time to 1/120s Bit[4:3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: Reserved Bit[0]: Exposure control 0: Manual 1: Auto
14	COM9	50	RW	Common Control 9 Bit[7:5]: AGC gain ceiling, GH[2:0] 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 11x: 128x Bit[4:0]: Reserved

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 4 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COM10	00	RW	Common Control 10 (if Bypass DSP is selected) Bit[7]: CHSYNC pin output swap 0: CHSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: CHSYNC Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF Bit[4]: PCLK edge selection 0: Data is updated at the falling edge of PCLK (user can latch data at the next rising edge of PCLK) 1: Data is updated at the rising edge of PCLK (user can latch data at the next falling edge of PCLK) Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
16	RSVD	XX	–	Reserved
17	HREFST	11	RW	Horizontal Window Start MSB 8 bits (3 LSBs in REG32[2:0] (0x32)) Bit[10:0]: Selects the start of the horizontal window, each LSB represents two pixels
18	HREFEND	75 (UXGA), 43 (SVGA, CIF)	RW	Horizontal Window End MSB 8 bits (3 LSBs in REG32[5:3] (0x32)) Bit[10:0]: Selects the end of the horizontal window, each LSB represents two pixels
19	VSTRT	01 (UXGA), 00 (SVGA, CIF)	RW	Vertical Window Line Start MSB 8 bits (2 LSBs in COM1[1:0] (0x03)) Bit[9:0]: Selects the start of the vertical window, each LSB represents two scan lines.
1A	VEND	97	RW	Vertical Window Line End MSB 8 bits (2 LSBs in COM1[3:2] (0x03)) Bit[9:0]: Selects the end of the vertical window, each LSB represents two scan lines.
1B	RSVD	XX	–	Reserved
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-23	RSVD	XX	–	Reserved

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 5 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC Operation AEC/AGC values will decrease in auto mode when average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC Operation AEC/AGC values will increase in auto mode when average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Threshold - effective only in AEC/AGC fast mode (COM8[7] = 1) Bit[7:4]: High threshold Bit[3:0]:Low threshold ***Note:*** *AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0].*
27-29	RSVD	XX	–	Reserved
2A	REG2A	00	RW	Register 2A Bit[7:4]: Line interval adjust value 4 MSBs (LSBs in FRARL[7:0] (0x2B)) Bit[3:2]: HSYNC timing end point adjustment MSB 2 bits (LSBs in register HEDY[7:0] (0x31)) Bit[1:0]: HSYNC timing start point adjustment MSB 2 bits (LSBs in register HSDY[7:0] (0x30))
2B	FRARL	00	RW	Line Interval Adjustment Value LSB 8 bits (MSBs in REG2A[7:4] (0x2A)) The frame rate will be adjusted by changing the line interval. Each LSB will add 1/1922 T_{frame} in UXGA and 1/1190 T_{frame} in SVGA mode to te frame period.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width LSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse Width MSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each MSB count will add 256 x t_{line} to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average (this register will auto update) Average Luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + (2 x GbAVG[7:0]) + RAVG[7:0]) x 0.25
30	HSDY	08	RW	HSYNC Position and Width, Start Point LSB 8 bits This register and REG2A[1:0] (0x2A) define HSYNC start position, each LSB will shift HSYNC start by 2 pixel period

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 6 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
31	HEDY	30	RW	HSYNC Position and Width, End Point LSB 8 bits This register and REG2A[3:2] (0x2A) define HSYNC end position, each LSB will shift HSYNC end by 2 pixel period
32	REG32	36 (UXGA), 09 (SVGA, CIF)	RW	Common Control 32 Bit[7:6]: Pixel clock divide option 00: No effect on PCLK 01: No effect on PCLK 10: PCLK frequency divide by 2 11: PCLK frequency divide by 4 Bit[5:3]: Horizontal window end position 3 LSBs (8 MSBs in register HREFEND[7:0] (0x18)) Bit[2:0]: Horizontal window start position 3 LSBs (8 MSBs in register HREFST[7:0] (0x17))
33	RSVD	XX	–	Reserved
34	ARCOM2	20	RW	Bit[7:3]: Reserved Bit[2]: Zoom window horizontal start point Bit[1:0]: Reserved
35-44	RSVD	XX	–	Reserved
45	REG45	00	RW	Register 45 Bit[7:6]: AGC[9:8], AGC highest gain control Bit[5:0]: AEC[15:10], AEC MSBs
46	FLL	00	RW	Frame Length Adjustment LSBs Each bit will add 1 horizontal line timing in frame
47	FLH	00	RW	Frame Length Adjustment MSBs Each bit will add 256 horizontal lines timing in frame
48	COM19	00	RW	Common Control 19 Bit[7:2]: Reserved Bit[1:0]: Zoom mode vertical window start point 2 LSBs
49	ZOOMS	00	RW	Zoom Mode Vertical Window Start Point 8 MSBs
4A	RSVD	XX	–	Reserved
4B	COM22	20	RW	Common Control 22 Bit[7:0]: Flash light control
4C-4D	RSVD	XX	–	Reserved
4E	COM25	00	RW	Common Control 25 - reserved for banding Bit[7:6]: 50Hz Banding AEC 2 MSBs Bit[5:4]: 60HZ Banding AEC 2 MSBs Bit[3:0]: Reserved
4F	BD50	CA	RW	50Hz Banding AEC 8 LSBs
50	BD60	A8	RW	60Hz Banding AEC 8 LSBs
51-5C	RSVD	XX	–	Reserved

Table 13 Device Control Register List (when 0xFF = 01) (Sheet 7 of 7)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
5D	REG5D	00	RW	Register 5D Bit[7:0]: AVGsel[7:0], 16-zone average weight option
5E	REG5E	00	RW	Register 5E Bit[7:0]: AVGsel[15:8], 16-zone average weight option
5F	REG5F	00	RW	Register 5F Bit[7:0]: AVGsel[23:16], 16-zone average weight option
60	REG60	00	RW	Register 60 Bit[7:0]: AVGsel[31:24], 16-zone average weight option
61	HISTO_LOW	80	RW	Histogram Algorithm Low Level
62	HISTO_HIGH	90	RW	Histogram Algorithm High Level
63-7E	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV2640 uses a 38-ball Chip Scale Package 2 (CSP2). Refer to Figure 11 for package information, Table 9 for package dimensions and Figure 12 for the array center on the chip.

Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 21 OV2640 Package Specifications

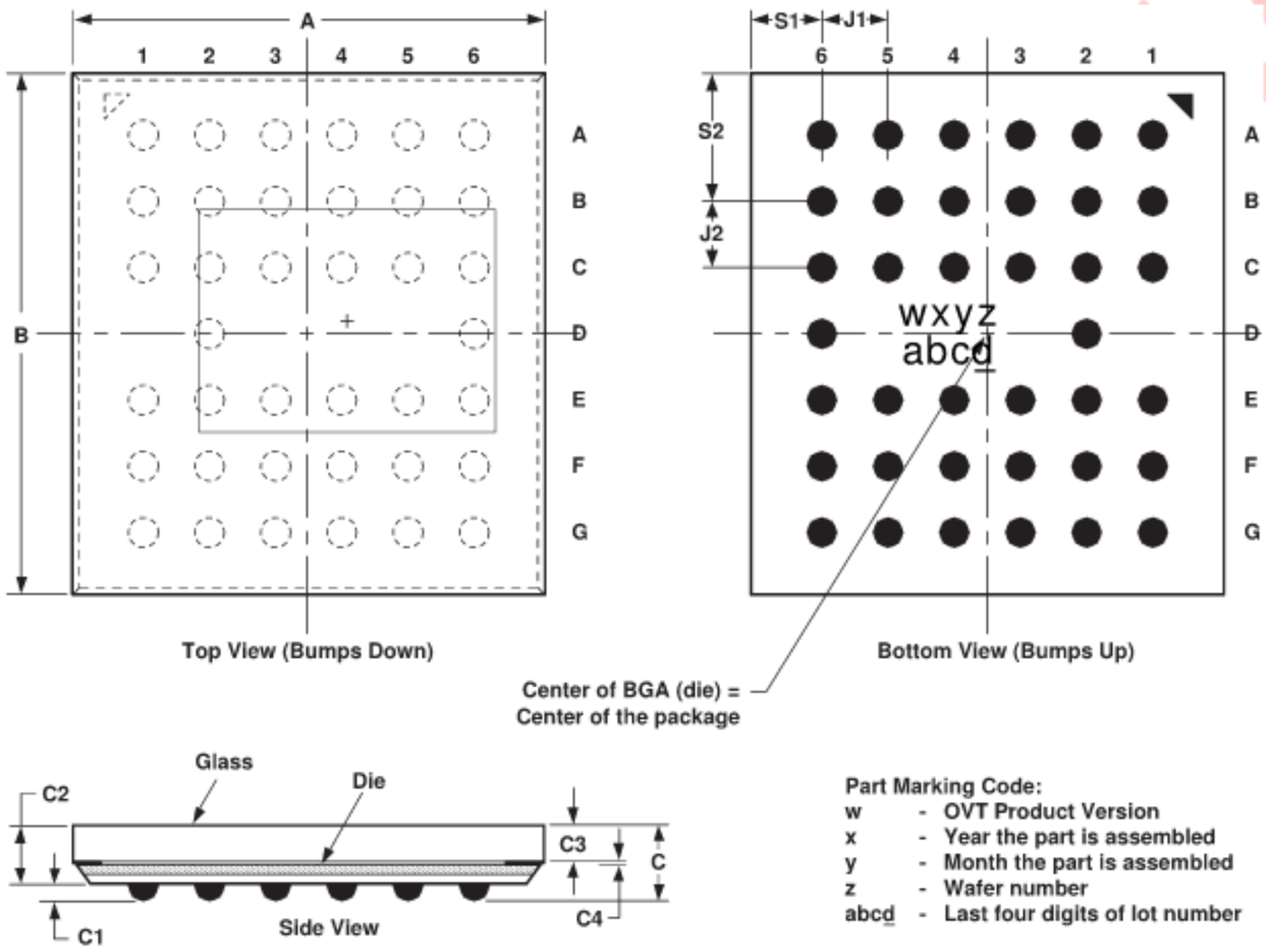
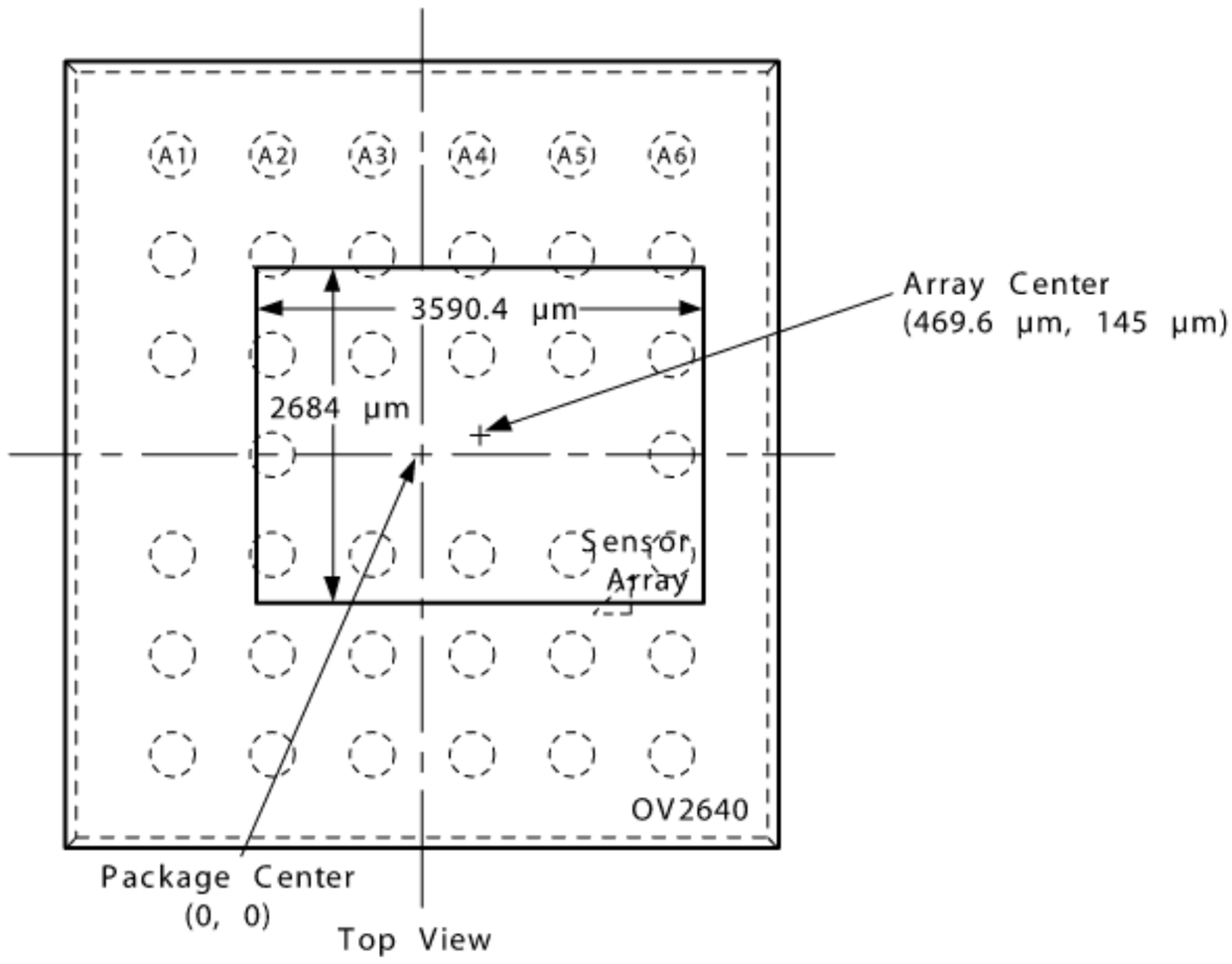


Table 14 OV2640 Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package Body Dimension X	A	5700	5725	5750	µm
Package Body Dimension Y	B	6260	6285	6310	µm
Package Height	C	845	905	965	µm
Ball Height	C1	150	180	210	µm
Package Body Thickness	C2	680	725	770	µm
Cover Glass Thickness	C3	375	400	425	µm
Airgap Between Cover Glass and Sensor	C4	30	45	60	µm
Ball Diameter	D	320	350	380	µm
Total Pin Count	N		38 (1 NC)		
Pin Count X-axis	N1		6		
Pin Count Y-axis	N2		7		
Pins Pitch X-axis	J1		800		µm
Pins Pitch Y-axis	J2		800		µm
Edge-to-Pin Center Distance Analog X	S1	833	863	893	µm
Edge-to-Pin Center Distance Analog Y	S2	713	743	773	µm

Sensor Array Center

Figure 22 OV2640 Sensor Array Center



NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

IR Reflow Ramp Rate Requirements

OV2640 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 23 IR Reflow Ramp Rate Requirements

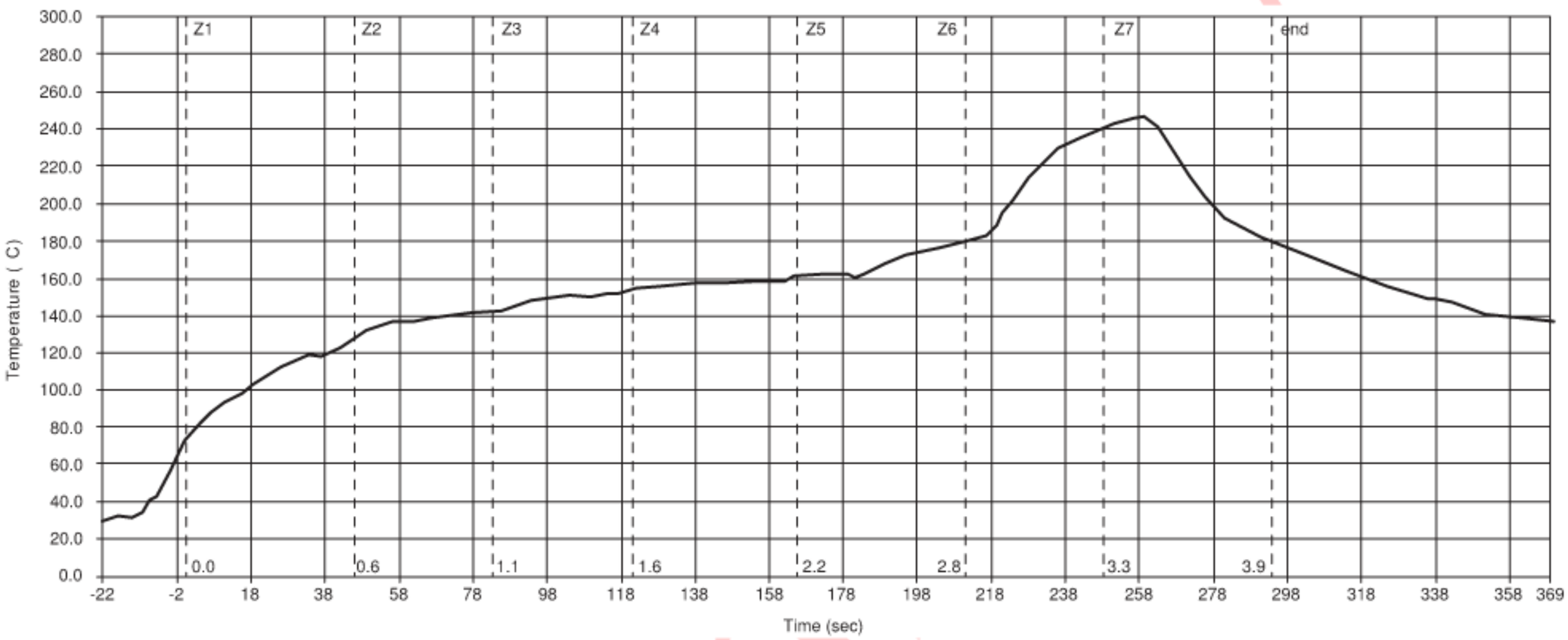


Table 15 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

Initial Release

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.01

DESCRIPTION OF CHANGES

The following changes were made to version 1.0:

- Under Key Specifications on page 1, changed specification for Core Power Supply from "1.2VDC ± 10%" to "1.2VDC ± 5%"
- Under Key Specifications on page 1, changed specification for Analog Power Supply from "2.8VDC ± 10%" to "2.5 ~ 3.0VDC"
- Under Key Specifications on page 1, changed specification for I/O Power Supply from "1.8V to 3.3V" to "1.7V to 3.3V"
- On pages 17 to 20, changed title of Table 12 from "Device Control Register (for 0x00 ~ 0xFF at 0xF8 = 00 and 0xFF = 00)" to "Device Control Register (when 0xFF = 00)"
- On pages 21 to 27, changed title of Table 13 from "Device Control Register (for 0x00 ~ 0x7E at 0xF8 = 01 and 0xFF = 7F)" to "Device Control Register (when 0xFF = 01)"
- In Table 12 on pages 18, changed description of register CTRL3 (0x87) from:

  Module Enable

  Bit[7:6]: Reserved
  Bit[5]: DCW
  Bit[4]: SDE
  Bit[3]: UV_ADJ
  Bit[2]: UV_AVG
  Bit[1]: Reserved
  Bit[0]: CMX

  to

  Module Enable

  Bit[7]: BPC
  Bit[6]: WPC
  Bit[5:0]: Reserved

- In Table 15 on page 30, changed specification for Peak Temperature from "Greater than 245°C" to "245°C"

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.01:

- Under Features on page 1, changed bulleted item from “Supports image sizes: UXGA, SVGA, and any size scaling down from SVGA to 40x30” to “Supports image sizes: UXGA, SXGA, SVGA, and any size scaling down from SXGA to 40x30”
- Under Key Specifications on page 1, deleted specifications for SVGA and CIF Array Size
- Under Key Specifications on page 1, changed Standby Power Requirements specification to “TBD”
- Under Key Specifications on page 1, changed specification for Chief Ray Angle from “TBD” to “25° non-linear”
- Under Key Specifications on page 1, changed specification for Well Capacity from “TBD” to “12 Ke”
- Under Electrical Characteristics on page 10, changed title of Table 6 from “DC Characteristics (-20°C < T_A < 70°C)” to “DC Characteristics (-30°C < T_A < 70°C)”
- In Table 6 on page 10, changed specification for Typ Standby Current from “10” to “TBD”
- In Table 6 on page 10, changed specification for Max Input voltage LOW (V_{IL}) from “0.8” to “0.54”
- In Table 6 on page 10, changed specification for Min Input voltage HIGH (V_{IH}) from “2” to “1.26”
- In Table 6 on page 10, changed subtitle “Digital Outputs (standard loading 25 pF, 1.2 KΩ to 2.8V)” to “Digital Outputs (standard loading 25 pF)”
- In Table 6 on page 10, changed specification for Min Output voltage HIGH (V_{OH}) from “2.2” to “1.62”
- In Table 6 on page 10, changed specification for Max Output voltage LOW (V_{OL}) from “0.6” to “0.18”
- In Table 6 on page 10, changed specification for Serial Interface Inputs Max SIO_C and SIO_D (V_{IL}) from “1” to “0.54”
- In Table 6 on page 10, changed specification for Serial Interface Inputs Min, Typ, and Max SIO_C and SIO_D (V_{IH}) from “2.5, 2.8, and VDD-IO + 0.5” to “1.26, 1.8, and 2.3”, respectively
- In Table 6 on page 10, changed table footnote b from “...V_{DD-IO} = 2.8V” to “...V_{DD-IO} = 1.8V”

DESCRIPTION OF CHANGES (CONTINUED)

- In Figure 21 on page 28, changed callout C3 to measure from thickness of glass and added callout C4 to measure airgap from glass to die.
- In Table 14 on page 28, changed C3 parameter name from “Thickness of Glass Surface to Wafer” to “Cover Glass Thickness”
- In Table 14 on page 28, changed C3 Minimum, Nominal, and Maximum specifications from “425, 445, and 465” to “375, 400, and 425”
- In Table 14 on page 28, added C4 parameter, Airgap Between Cover Glass and Sensor, and Minimum, Nominal, and Maximum specifications “30, 45, and 60”, respectively

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.2

DESCRIPTION OF CHANGES

The following changes were made to version 1.1:

- Under Key Specifications on page 1, changed Active Power Requirements specification to "TBD" to "125 mW (for 15 fps, UXGA YUV mode)" and "140 mW (for 15 fps, UXGA compressed mode)"
- Under Key Specifications on page 1, changed Standby Power Requirements specification to "TBD" to "600 µA"
- Under Key Specifications on page 1, deleted Preview (CIF) Power Requirements specification
- In Table 6 on page 10, changed specification for Typ Active (Operating) Current (I_{DDA-A}) from "TBD" to "30"
- In Table 6 on page 10, changed specification for Typ Active (Operating) Current (I_{DDA-D}) from "TBD" to "25 (YUV)" and "35 (Compressed)"
- In Table 6 on page 10, changed specification for Typ Active (Operating) Current (I_{DDA-IO}) from "TBD" to "6"
- IIn Table 6 on page 10, changed specification for Typ Standby Current from "10" to "600"
- In Table 6 on page 10, changed table footnote b from "...V_{DD-IO} = 1.8V" to "...V_{DD-IO} = 1.8V for 15 fps in UXGA mode"

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.21

DESCRIPTION OF CHANGES

The following changes were made to version 1.2:

- In Figure 1 on page 21, corrected the bottom view of the package by correcting the column numbers corresponding to the ball locations from (left to right) “1”, “2”, “3”, “4”, “5”, and “6” to (left to right) “6”, “5”, “4”, “3”, “2”, and “1”, respectively

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.3

DESCRIPTION OF CHANGES

The following changes were made to version 1.21:

- In Table 1 on page 8, made the following changes/corrections:
  - Corrected pin type of pin A1 from Power to Ground
  - Corrected pin type of pin A2 from I/O to Input and added “Note: There is no internal pull-up/pull-down resistor”
  - Corrected pin type of pin A3 from Power to Ground
  - Corrected pin type of pin A4 from Power to Ground
  - Corrected pin type of pin A5 from I/O to Reference
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin A6
  - Corrected pin type of pin B2 from Power to Input and added “Note: There is no internal pull-up/pull-down resistor”
  - Corrected pin type of pin B3 from Input to Power
  - Corrected pin type of pin B4 from I/O to Power
  - Corrected pin type of pin B5 from Input to Power
  - Corrected pin type of pin B6 from I/O to Input and “Note: There is an internal pull-down resistor”
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin C3
  - Added “Note: There is no internal pull-up/pull-down resistor” to description of pin C4
  - Added “Note: There is an internal pull-up resistor” to description of pin C6
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin D2
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin E1
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin E2
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin E3
  - Corrected pin type of pin E4 from Power to Ground
  - Added “Default: Input” and “Note: There is no internal pull-up/pull-down resistor” to description of pin E5
  - Corrected pin type of pin E6 from Power to Ground

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 1 on page 8, made the following changes/corrections:
  - Corrected pin type of pin F2 from Analog to Power and changed description to "Sensor digital power (Core)"
  - Added "Default: Input" and "Note: There is no internal pull-up/pull-down resistor" to description of pins F3, F4, and F5
  - Corrected pin type of pin F6 from Analog to Power and changed description to be the same as pin F2
  - Corrected pin type of pin G2 from Power to Ground
  - Added "Default: Input" and "Note: There is no internal pull-up/pull-down resistor" to description of pins G3, G4, G5, and G6

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.4

DESCRIPTION OF CHANGES

The following changes were made to version 1.3:

- In Table 6 on page 11, made the following changes:
  - Added “40 mA” for Maximum specification of I_{DDA-A}
  - Added “35 mA (YUV)” and “50 mA (Compressed)” for Maximum specification of I_{DDA-D}
  - Added “10 mA” for Maximum specification of I_{DDA-IO}
  - Added “2 mA” for Maximum specification of $I_{DDS-SCCB}$
  - Added “1200 µA” for Maximum specification of $I_{DDS-PWDN}$

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.5

DESCRIPTION OF CHANGES

The following changes were made to version 1.4:

- Under Register Set section on page 18, changed the second paragraph from
  "There are two different sets for register address from 0x00 to 0x7E. Both register 0xF8 and register 0xFF control which set is accessible. When 0xF8=00 and 0xFF=00, Table 12 is effective. When 0xF8=01, 0xFF=7F, Table 13 is effective."
  to
  "There are two different sets of register banks. Register 0xFF controls which set is accessible. When register 0xFF=00, Table 12 is effective. When register 0xFF=01, Table 13 is effective."

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.6

DESCRIPTION OF CHANGES

The following changes were made to version 1.5:

- In Table 12 on page 18, changed name, default, R/W, and description of register 0x44 from “RSVD”, “XX”, “–”, and “Reserved” to “Qs”, “0C”, “RW”, and “Quantization Scale Factor”
- In Table 12 on page 21, changed description of register RA_DLMT (0xFF) from:

  Sensor/Device Register Address Delimiter
  <(value of register 0xFF): Sensor address
  (value of register 0xFF): DSP address

  to:

  Register Bank Select
  Bit[7:1]: Reserved
  Bit[0]: Register bank select
  0: DSP address
  1: Sensor address
- In Table 13 on page 22, changed default value for register REG08 (0x08) from “00” to “40”
- In Table 13 on page 22, changed description of register bits COM2[1:0] (0x09) from:

  00: Weakest
  01: Double capability
  10: Double capability
  11: Triple drive capability

  to:

  00: 1x capability
  01: 3x capability
  10: 2x capability
  11: 4x capability
- In Table 13 on page 22, changed default value for register PIDL (0x0B) from “40” to “41”
- In Table 13 on page 23, changed description of register bit CLKRC[6] (0x11) to “Reserved”
- In Table 13 on page 25, added “(if Bypass DSP is selected)” to description of register COM10 (0x15)

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.7

DESCRIPTION OF CHANGES

The following changes were made to version 1.6:

- In Table 5 on page 11, deleted row for ESD Rating, Human Body model specification
- In Figure 18 on page 16, deleted callouts for t_{dfvf}, t_{dvsc}, and t_{dvh}
- In Figure 18 on page 16, shortened first VSYNC cycle to match the second VSYNC cycle and added callout "$4xt_{LINE}$" to both cycles
- In Figure 19 on page 16, deleted callouts for t_{dfvf}, t_{dvsc}, and t_{dvh}
- In Figure 19 on page 16, shortened first VSYNC cycle to match the second VSYNC cycle and added callout "$4xt_{LINE}$" to both cycles
- In Table 11 on page 15, deleted rows for tdfvf, tdvsc, and tdvh

REVISION CHANGE LIST

Document Title: OV2640 Datasheet **Version:** 1.8

DESCRIPTION OF CHANGES

The following changes were made to version 1.7:

- Under Key Specifications on page 1, changed Power Supply (Core) specification from "1.2VDC ± 5%" to "1.3VDC ± 5%"
- Under Key Specifications on page 1, deleted Operation Temperature Range specification
- In Table 6 on page 11, changed Min, Typ, and Max for Supply Voltage (V_{DD-D}) from "1.14", "1.2", and "1.26" to "1.24", "1.3", and "1.36", respectively
- In Table 6 on page 11, changed Typ for Active (Operating) Current (t_{DDA-D}) from "25 (YUV) 35 (Compressed)" to "30 (YUV) 45 (Compressed)"
- In Table 6 on page 11, changed Max for Active (Operating) Current (t_{DDA-D}) from "35 (YUV) 50 (Compressed)" to "40 (YUV) 60 (Compressed)"
- In Table 6 on page 11, changed Max for Active (Operating) Current (t_{DDA-IO}) from "10" to "15"
- In Table 6 on page 11, added footnote a (and changed previous footnote a and b to b and c, respectively) "If using internal regulator for DVDD, V_{DD-A}requires greater than or equal to 2.65V" to Minimum value of Supply voltage (V_{DD-A}) specification
- In Table 6 on page 11, changed footnote c (previously footnote b) from "V_{DD-A}=2.8V, V_{DD-D}=1.2V, and V_{DD-IO}=1.8V for 15 fps in UXGA mode" to "V_{DD-A}=2.8V, V_{DD-D}=1.3V, and V_{DD-IO}=1.8V for 15 fps in UXGA mode"