TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 DSC

Silicon Errata

Literature Number: SPRZ272G
September 2007–Revised January 2012

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TMS320F2833x and TMS320F2823x DSC Silicon Errata

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320F2833x and TMS320F2823x digital signal controllers (DSCs).

The updates are applicable to:

- 179-ball MicroStar BGA™, ZHH Suffix
- 176-ball Plastic BGA, ZJZ Suffix
- 176-pin Low-profile Thin Quad Flatpack, PGF Suffix

2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all [TMS320] DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**320F28335). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZJZ) and temperature range (for example, A).

3 Device Markings

Figure 1 provides an example of the F2833x and F2823x device markings and defines each of the markings. The device revision can be determined by the symbols marked on the top of the package as shown in Figure 1. Some prototype devices may have markings different from those illustrated. Figure 2 shows the device nomenclature.

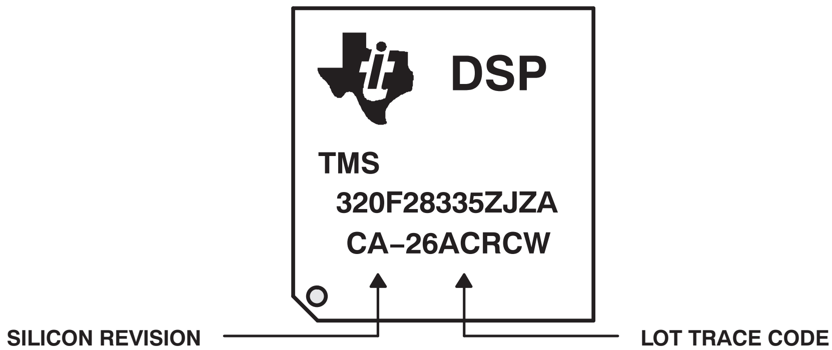


Figure 1. Example of Device Markings

Table 1. Determining Silicon Revision From Lot Trace Code (F2833x and F2823x)

SECOND LETTER IN PREFIX OF LOT TRACE CODE	SILICON REVISION	REVISION ID (0x0883)	COMMENTS
Blank (no second letter in prefix)	Indicates Revision 0	0x0000	This silicon revision is available as TMX only.
A	Indicates Revision A	0x0001	This silicon revision is TMS.

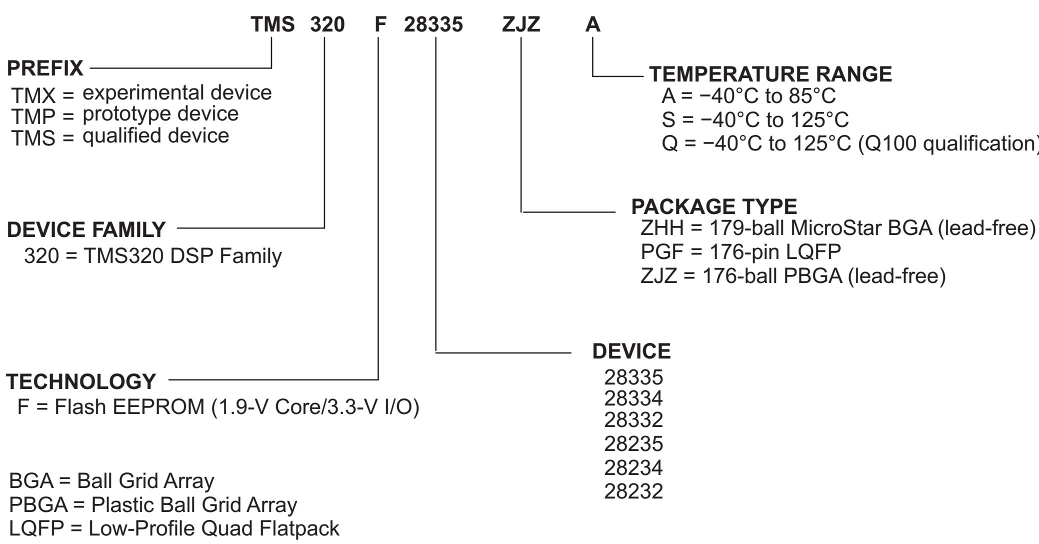


Figure 2. Device Nomenclature

4 Silicon Change Overview

Table 2 lists the change(s) made to each silicon revision.

Table 2. TMS320F2833x and TMS320F2823x Silicon Change Overview

REVISION	CHANGES MADE
0	First silicon release
A	**Changes** The following changes are implemented with Revision A: • Flash API version 2.00 is needed for Rev A silicon. This version is backward-compatible with Rev 0 silicon. • McBSP boot loader McBSP loader will now echo back the data received. This was not the case on Rev 0. • DMA connection to ePWM The ePWM/HRPWM modules can be re-mapped to peripheral frame 3 where they can be accessed by the DMA module. In addition, the SOCA and SOCB of each EPWM module is connected to the DMA at the following peripheral interrupt select positions in each channel MODE register (MODE[PERINTSEL(4:0)] bits): EPWM1-SOCA → PERINTSEL(18) EPWM1-SOCB → PERINTSEL(19) EPWM2-SOCA → PERINTSEL(20) EPWM2-SOCB → PERINTSEL(21) EPWM3-SOCA → PERINTSEL(22) EPWM3-SOCB → PERINTSEL(23) EPWM4-SOCA → PERINTSEL(24) EPWM4-SOCB → PERINTSEL(25) EPWM5-SOCA → PERINTSEL(26) EPWM5-SOCB → PERINTSEL(27) EPWM6-SOCA → PERINTSEL(28) EPWM6-SOCB → PERINTSEL(29) • The PARTID register moved to address 0x380090. PARTID values changed. See the *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers (DSCs) Data Manual* (SPRS439) for details. • The address 0x882 (formerly the PARTID register) is now called the CLASSID register. See the *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers (DSCs) Data Manual* (SPRS439) for details. **Advisories Fixed** The following advisories are fixed in rev A : • Boot to XINTF x16, x32 and Parallel Boot Setup Issue • M1 memory access conflict • XINTF rogue write for back-to-back accesses to x16/x32 zones. Behavior changed such that external delay logic is no longer required to avoid this issue on Rev A. The behavior of the XA0/$\overline{\text{XWE1}}$ signal has been modified such that it goes high during inactive cycles. Use the XBANK feature to force inactive cycles between back-to-back zone accesses. See the *TMS320x2833x, 2823x External Interface (XINTF) Reference Guide* (SPRU949) for more information.

5 Known Design Marginality/Exceptions to Functional Specifications

The table of contents for advisories is shown in Table 3.

Table 3. Advisory List

Title **Page**

Advisory — *Memory: Prefetching Beyond Valid Memory*

Revision(s) Affected 0, A

Details The C28x CPU prefetches instructions beyond those currently active in its pipeline. If the prefetch occurs past the end of valid memory, then the CPU may receive an invalid opcode.

Workaround The prefetch queue is 8 x16 words in depth. Therefore, code should not come within 8 words of the end of valid memory. This restriction applies to all memory regions and all memory types (flash, OTP, SARAM, XINTF) on the device. Prefetching across the boundary between two valid memory blocks is all right.

Example 1: M1 ends at address 0x7FF and is not followed by another memory block. Code in M1 should be stored no farther than address 0x7F7. Addresses 0x7F8–0x7FF should not be used for code.

Example 2: M0 ends at address 0x3FF and valid memory (M1) follows it. Code in M0 can be stored up to and including address 0x3FF. Code can also cross into M1 up to and including address 0x7F7.

Advisory — *Memory: M1 Memory Access Conflict*

Revision(s) Affected 0

Details If an opcode fetch is issued to M1 while a write is pending, then an arbitration condition can cause the write to be lost.

Workaround(s) This has been fixed in Rev A silicon.

Advisory — *Memory: Possible Incorrect Operation of XINTF Module After Power Up*

Revision(s) Affected 0, A

Details The XINTF module may not get reset properly upon power up. When this happens, accesses to XINTF addresses may cause the CPU to hang. This issue occurs only upon power up. It does not happen for other resets such as a reset initiated by the watchdog or an external (warm) reset using the $\overline{\text{XRS}}$ pin.

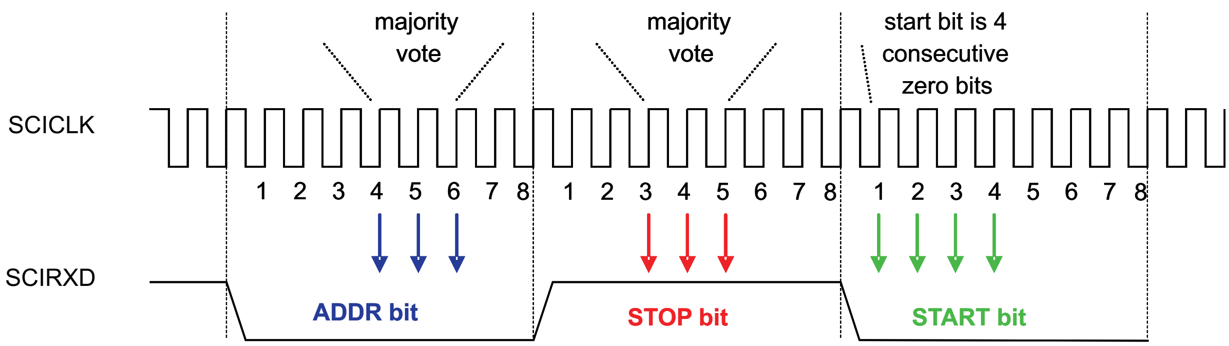
Workaround(s) After coming out of reset, software should force a watchdog (WD) reset if WDFLAG = 0 in the WDCR register. WDFLAG = 0 implies that an external reset occurred, for example, a power-on reset. After exiting the WD reset, WDFLAG will be 1. In this case, software should clear the WDFLAG bit before continuing normal code execution. This issue affects only the XINTF module.

Advisory *SCI: Incorrect Operation of SCI in Address Bit Mode*

Revision(s) Affected 0, A

Details SCI does not look for STOP bit after the ADDR bit. Instead, SCI starts looking for the start bit beginning on sub-sample 6 of the ADDR bit. Slow rise-time from ADDR to STOP bit can cause the false START bit to occur since the 4th sub-sample for the start bit may be sensed low.

Expected Operation:



Erroneous Operation:

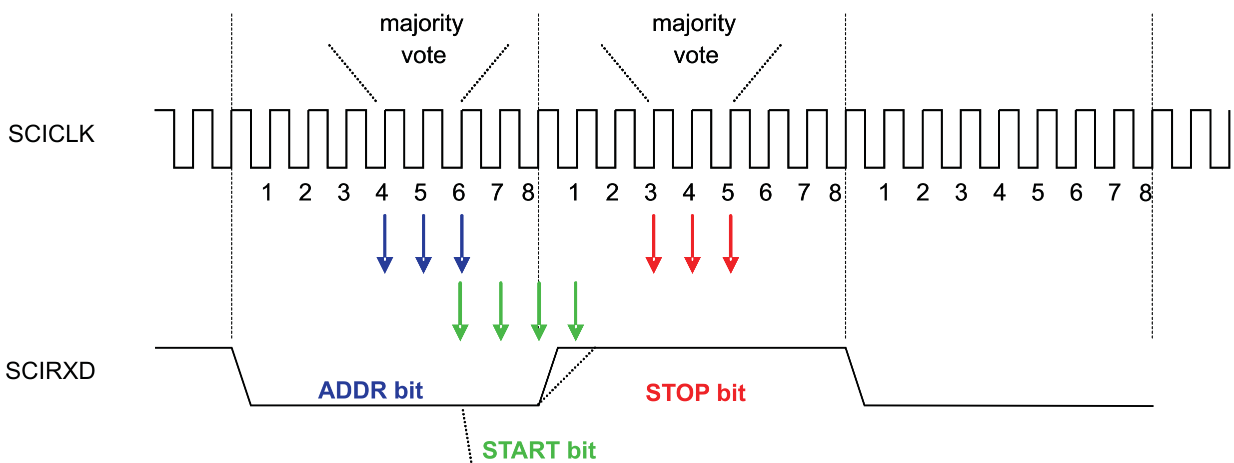


Figure 3. Difference Between Expected and Erroneous Operation of START Bit

Workaround(s) Program the baud rate of the SCI to be slightly slower than the actual. This will cause the 4th sub-sample of the false START bit to be delayed in time, and therefore occur more towards the middle of the STOP bit (away from the signal transition region). The amount of baud slowing needed depends on the rise-time of the signal in the system. Alternatively, IDLE mode of the SCI module may be used, if applicable.

Advisory — *ADC: Simultaneous Sampling Latency*

Revision(s) Affected 0, A

Details When the ADC conversions are initiated in simultaneous mode, the first sample pair will not give correct conversion results.

Workaround(s) 1. If the ADC is used with a sampling window ≤ 160 nS, then the first sample pair must be discarded and a second sample of the same pair must be taken. For instance, if the sequencer is set to sample channel A0:B0/A1:B1/A2:B2 in that order, then load the sequencer with A0:B0/A0:B0/A1:B1/A2:B2 and only use the last three conversions.

2. If the ADC is used with a sampling window greater than 160 ns, there is no issue.

Advisory — *eCAN: Abort Acknowledge Bit Not Set*

Revision(s) Affected 0, A

Details After setting a Transmission Request Reset (TRR) register bit to abort a message, there are some rare instances where the TRRn and TRSn bits will clear without setting the Abort Acknowledge (AAn) bit. The transmission itself is correctly aborted, but no interrupt is asserted and there is no indication of a pending operation.

In order for this rare condition to occur, all of the following conditions must happen:

1. The previous message was not successful, either because of lost arbitration or because no node on the bus was able to acknowledge it or because an error frame resulted from the transmission. The previous message need not be from the same mailbox in which a transmit abort is currently being attempted.
2. The TRRn bit of the mailbox should be set in a CPU cycle immediately following the cycle in which the TRSn bit was set. The TRSn bit remaining set due to incompletion of transmission satisfies this condition as well. i.e. the TRSn bit could have been set in the past, but the transmission remains incomplete.
3. The TRRn bit must be set in the exact SYSCLKOUT cycle where the CAN module is in idle state for one cycle. The CAN module is said to be in idle state when it is not in the process of receiving/transmitting data.

If these conditions occur, then the TRRn and TRSn bits for the mailbox will clear t_{clr} SYSCLKOUT cycles after the TRR bit is set where:

t_{clr} = [(mailbox_number) * 2] + 3 SYSCLKOUT cycles

The TAn and AAn bits will not be set if this condition occurs. Normally, either the TA or AA bit sets after the TRR bit goes to zero.

Workaround(s) When this problem occurs, the TRRn and TRSn bits will clear within t_{clr} SYSCLKOUT cycles. To check for this condition, first disable the interrupts. Check the TRRn bit t_{clr} SYSCLKOUT cycles after setting the TRRn bit to make sure it is still set. A set TRRn bit indicates that the problem did not occur.

If the TRRn bit is cleared, it could be because of the normal end of a message and the corresponding TAn or AAn bit is set. Check both the TAn and AAn bits. If either one of the bits is set, then the problem did not occur. If they are both zero, then the problem did occur. Handle the condition like the interrupt service routine would except that the AAn bit does not need clearing now.

If the TAn or AAn bit is set, then the normal interrupt routine will happen when the interrupt is re-enabled.

Advisory — *GPIO: GPIO Qualification*

Revision(s) Affected 0, A

Details If a GPIO pin is configured for "n" SYSCLKOUT cycle qualification period (where $1 \le n \le 510$) with "m" qualification samples (m = 3 or 6), it is possible that an input pulse of [n * m – (n – 1)] width may get qualified (instead of n * m). This depends upon the alignment of the asynchronous GPIO input signal with respect to the phase of the internal prescaled clock, and hence, is not deterministic. The probability of this kind of wrong qualification occurring is "1/n".

Worst-case example:

If n = 510, m = 6, a GPIO input width of (n * m) = 3060 SYSCLKOUT cycles is required to pass qualification. However, because of the issue described in this advisory, the minimum GPIO input width which may get qualified is [n * m – (n – 1)] = 3060 – 509 = 2551 SYSCLKOUT cycles.

Workaround(s) None. Ensure a sufficient margin is in the design for input qualification.

Advisory — *Boot to XINTF x16, x32 and Parallel Boot Setup Issue*

Revision(s) Affected 0

Details The following signals are not configured for XINTF functionality in the GPIO MUX registers: $\overline{\text{XZCS6}}$, XA19, $\overline{\text{XWE0}}$, XA16.

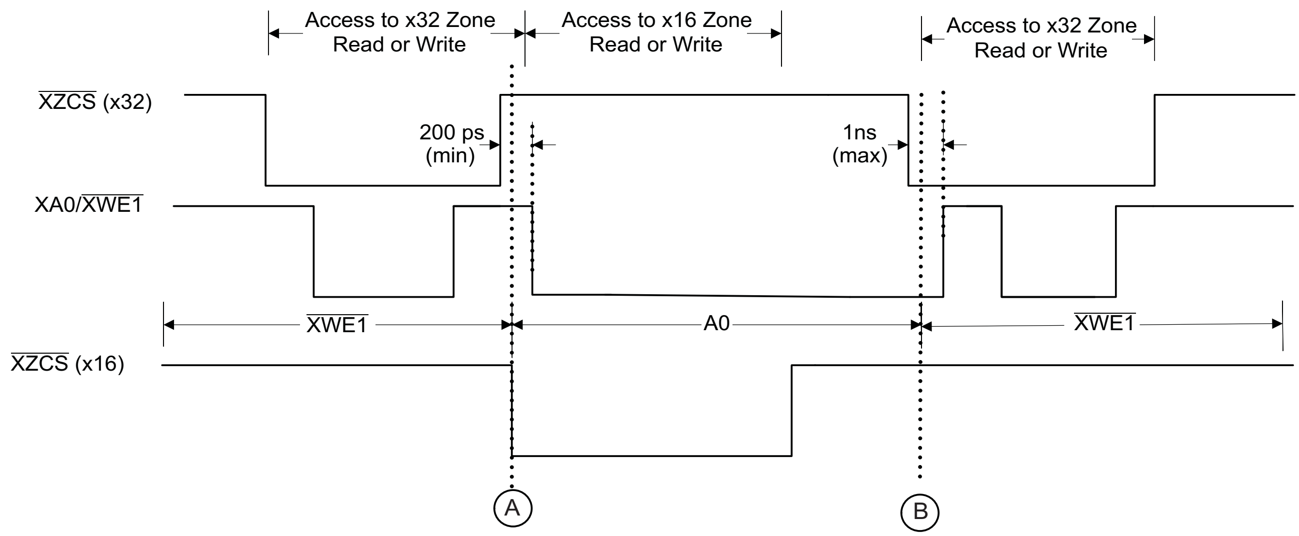
Workaround This has been fixed in Rev A silicon.

Advisory *XINTF Rogue Write for Back-to-Back Accesses to x16/x32 Zones*

Revision(s) Affected 0

Details Figure 4 shows the behavior of zone chip select signals and XA0/$\overline{\text{XWE1}}$ for back-to-back accesses between zones configured for different data bus widths.

For the x32-bit zone (XTIMINGx[XSIZE] = 1) the A0/$\overline{\text{XWE1}}$ signal is the write enable $\overline{\text{XWE1}}$. For the x16-bit zone (XTIMINGx[XSIZE] = 3) the A0/$\overline{\text{XWE1}}$ signal is address line A0.



A Design simulation data indicates the delta between $\overline{\text{XZCS}}$ (x32) high and XA0/$\overline{\text{XWE1}}$ low can be as small as 200 ps.

B Design simulation data indicates XA0/$\overline{\text{XWE1}}$ can stay low for as long as 1 ns after $\overline{\text{XZCS}}$ (x32) goes low.

Figure 4. Behavior of Zone Chip Select Signals and XA0/$\overline{\text{XWE1}}$

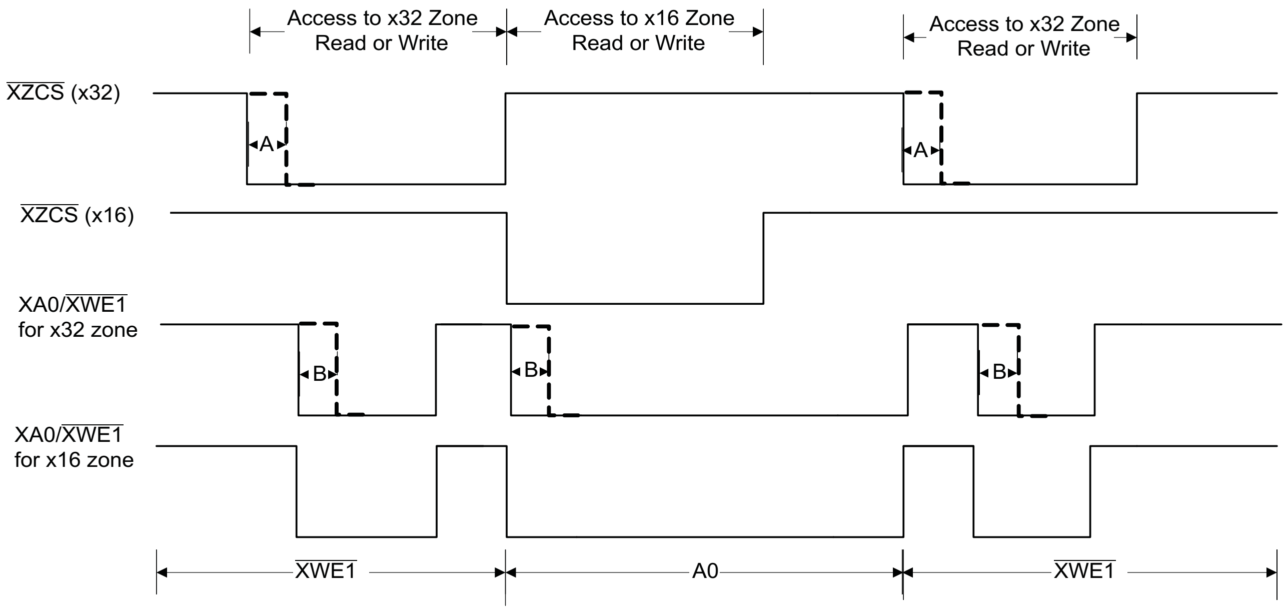
When A0/$\overline{\text{XWE1}}$ changes functionality, the x32 zone chip select signal ($\overline{\text{XZCS}}$ x32) changes state. Depending on the board design and peripherals attached to the XINTF, it is possible that an external memory or peripheral on the x32 zone may respond to A0/$\overline{\text{XWE1}}$ switching as a write access. If this happens, a rogue write to the x32 zone can occur.

Workaround(s)

1. If all zones are configured for x16 operation, then no action is required.
2. If all zones are configured for x32 operation, then XA0/$\overline{\text{XWE1}}$ will switch from XA0 to $\overline{\text{XWE1}}$ on the first access. After the first access, the XA0/$\overline{\text{XWE1}}$ pin will remain as $\overline{\text{XWE1}}$. To keep external devices from responding to the XA0/$\overline{\text{XWE1}}$ change, follow these steps when configuring the XINTF module:
   (a) Enable the clock to the XINTF module.
   (b) Configure the data-width and timing of the XINTF zones.
   (c) Configure the zone chip select pins as GPIO inputs for the next step. This is the default behavior after reset.
   (d) Perform a dummy read from a x32 XINTF zone. This read will force XA0/$\overline{\text{XWE1}}$ to behave as $\overline{\text{XWE1}}$. Since the zone chip selects are configured as GPIO inputs, the external devices will not respond to XA0/$\overline{\text{XWE1}}$ switching to $\overline{\text{XWE1}}$. After the first read, XA0/$\overline{\text{XWE1}}$ will continue to behave as $\overline{\text{XWE1}}$.
   (e) Configure the GPIO MUX registers for XINTF operation.
3. Use external logic to delay the falling edge of the x32 zone chip select signal and the falling edge of the $\overline{\text{XWE1}}$ signal as shown in Figure 5. With the delay the x32 zone

chip select sees the XWE1 signal high at the critical points.

The timing configuration of the x32 zone must account for the additional delay. The zone chip select delay may require additional lead time. The XWE1 delay enable may require additional active write time. In addition, specify at least 1 trail cycle for writes to the x32 zone.



A Delayed falling edge of zone chip select for x32 zone.

B Delayed falling edge of XWE1. The x16 zone will not see this delay.

Figure 5. Behavior After Application of Delay

The delay can be created by using 74LVC32 quad OR gates or similar logic to create a delay line as shown in Figure 6.

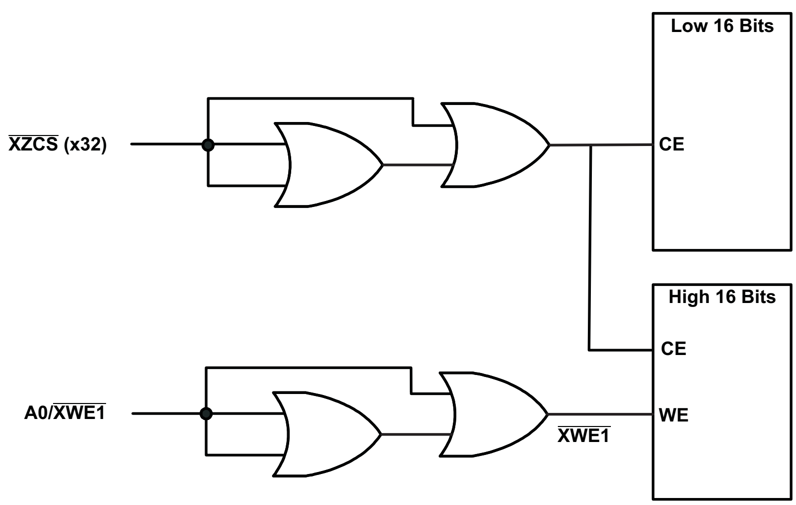


Figure 6. Example Delay Line Circuit

This has been fixed in Rev A silicon. The external delay logic is no longer required to avoid this issue in Rev A. The behavior of the XA0/XWE1 signal has been modified such that it goes high during inactive cycles. Use the XBANK feature to force inactive cycles between back-to-back zone accesses. See the *TMS320x2833x, 2823x DSC External Interface (XINTF) Reference Guide* (SPRU949) for more information.

Advisory — *eQEP: Missed First Index Event*

Revision(s) Affected

A

Details

If the first index event edge at the QEPI input occurs at any time from one system clock cycle before the corresponding QEPA/QEPB edge to two system clock cycles after the corresponding QEPA/QEP edge, then the eQEP module may miss this index event. This can result in the following behavior:

- QPOSCNT will not be reset on the first index event if QEPCTL[PCRM] = 00b or 10b (position counter reset on an index event or position counter reset on the first index event).
- The first index event marker flag (QEPSTS[FIMF]) will not be set.

Workaround(s)

Reliable operation is achieved by delaying the index signal such that the QEPI event edge occurs at least two system clock cycles after the corresponding QEPA/QEPB signal edge. For cases where the encoder may impart a negative delay (t_d) to the QEPI signal with respect to the corresponding QEPA/QEPB signal (i.e., QEPI edge occurs before the corresponding QEPA/QEPB edge), the QEPI signal should be delayed by an amount greater than "t_d + 2*SYSCLKOUT".

Advisory — *eQEP: eQEP Inputs in GPIO Asynchronous Mode*

Revision(s) Affected

0, A

Details

If any of the eQEP input pins are configured for GPIO asynchronous input mode via the GPxQSELn registers, the eQEP module may not operate properly. For example, QPOSCNT may not reset or latch properly, and pulses on the input pins may be missed. This is because the eQEP peripheral assumes the presence of external synchronization to SYSCLKOUT on inputs to the module.

For proper operation of the eQEP module, input GPIO pins should be configured via the GPxQSELn registers for synchronous input mode (with or without qualification). This is the default state of the GPxQSEL registers at reset. All existing eQEP peripheral examples supplied by TI also configure the GPIO inputs for synchronous input mode.

The asynchronous mode should not be used for eQEP module input pins.

Workaround(s)

Configure GPIO inputs configured as eQEP pins for non-asynchronous mode (any GPxQSELn register option except “11b = Asynchronous”).

6 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: http://www.ti.com.

For further information regarding the 2833x, 2823x devices, see the *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers (DSCs) Data Manual* (literature number SPRS439).

7 Revision History

This revision history highlights the technical changes made to the SPRZ272F errata document to make it an SPRZ272G revision.

Scope: See table below.

LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Table 1	Determining Silicon Revision From Lot Trace Code (F2833x and F2823x): • Added data for Revision 0 silicon
Section 5	Known Design Marginality/Exceptions to Functional Specifications: • Added "eQEP: eQEP Inputs in GPIO Asynchronous Mode" advisory

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