Application Report
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Power Line Communication for Lighting Applications Using Binary Phase Shift Keying (BPSK) with a Single DSP Controller

C2000 - Systems Application

ABSTRACT

DSP controllers provide the on-chip peripherals and computational power needed to implement various power electronics applications. A single-chip DSP controller allows designers to implement multiple functions such as power line communication, power-factor correction, and inverter control, all needed for an overall dimmable lighting ballast application. This application report presents a complete implementation of a power line modem following CEA-709 protocol using a single DSP. This paper is a shorter version of the detailed documentation of this implementation titled *TMS320C2000 Digital Signal Controller Power Line Communication User's Guide* (SPRU714) which can be downloaded from http:www.ti.com.

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1 Introduction

Power line communication [1] is a cost-effective solution for communicating with and controlling a group of stand alone units for many applications such as dimmable ballasts, e-metering, or motor control. There are various methods of implementing power line communication, and in many cases a dedicated communication chip is utilized to implement the modem portion of the system. The application portion (ballast, e-metering, etc.) typically utilize a second controller. This two-chip implementation is a good solution for many systems, however, cost-sensitive applications like dimmable lighting ballasts can further benefit from additional system integration. An advanced DSP controller can offer this system integration by combining the power line modem functionality as well as system operations using the on chip peripherals of the device. The DSP controllers can implement the complete modem function in software and can utilize the on-chip power electronics peripherals to receive and transmit over the power line with an analog front end interface. The DSP controller can also implement other system functions like power-factor correction and inverter control for ballast operations by utilizing the extra MIPS and the on-chip peripheral set, thus offering integration for lower system cost.

This application note presents a complete software and hardware implementation of a power line modem conforming to the CEA-709[2] protocol using a single fixed-point DSP controller. The paper presents the detailed analog front end design necessary for a robust receive and transmit operation. Finally, the hardware implementation of a complete system is presented as a design reference. More detailed documentation of this implementation can be found at http://www.ti.com titled *TMS320C2000 Digital Signal Controller Power Line Communication User's Guide*, SPRU714.

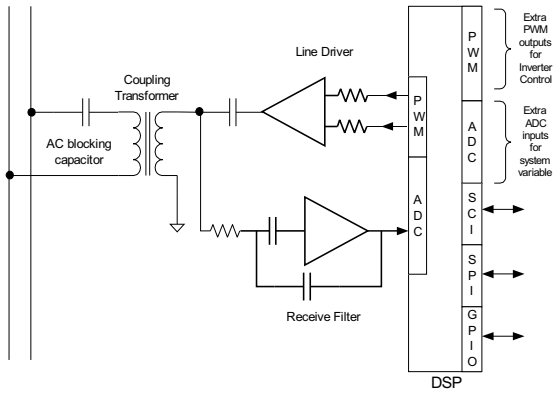

Figure 1. System Block Diagram

A system block diagram is shown in Figure 1. A single fixed-point DSP (TMS320F2812[3]) is utilized to implement the complete modem function. This particular DSP provides 150 MIPS of computational capability. Signal sensing is provided using an on-chip analog-to-digital converter with 12 MSPS conversion speed with 12 bits of resolution. The DSP offers multiple PWM channels to accommodate power line modem as well as other applications like inverter control or lighting ballast control.

Two on-chip PWM outputs are utilized with a line driver for the transmit function of the modem. One analog-to-digital (ADC) input is utilized to sample the band-pass input signal to implement the receive function of the modem. The band-pass filter is implemented using a discrete filter. An AC-blocking capacitor and a coupling transformer complete the analog front end design of this interface. The remaining PWM channels and ADC inputs are utilized to control an inverter to show the potential of system integration with power line modem functionality.

The DSP code combines the MAC, Link, Network, Transport and Application layers in the command handler portion of the software. Figure 2 shows a block diagram of the CEA-709 modem function implemented using a DSP controller.

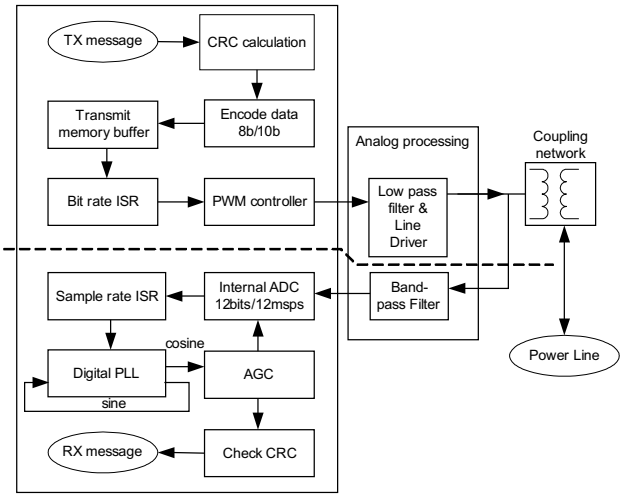

Figure 2. CEA-709 PHY Block Diagram

2 Implementation OF CEA-709 Protocol

The implemented communication protocol is based on the CEA-709 Standard. The complete CEA 709 protocol stack is a substantial topic and beyond the scope of this paper. This paper will primarily discuss the physical layer implementation.

The CEA-709 communication system is defined with a carrier frequency of 131.579 kHz. Each transmitted bit consists of 24 cycles of a sine wave at the carrier frequency, resulting in a baud rate of 5.5 kbps. The phase of each bit field can be set to 0 degrees to encode a “zero” bit or 180 degrees to encode a “one” bit.

Signal Reception: The 131.5 kHz modulated signal is detected by first removing the 50/60 Hz power line voltage at the coupling network and then filtering the signal with a second order active band-pass filter. This filter is constructed using an operational amplifier. The output of the band-pass filter is sampled by one channel of the DSP's analog–to-digital converter. The signal sample sequence is processed by an FIR matched filter and the output of this filter is used to perform timing recovery and data detection.

By sampling the received signal at 115 kHz, which is 21/24ths of the carrier frequency, the signal can be down-sampled from 131.5 kHz to an intermediate frequency of 16.5 kHz. This operation can be described as mixing or multiplying the incoming carrier sine wave signal with the sample rate clock. The multiplication of two sine wave signals results in a signal containing the sum and difference of the frequencies of the two sine waves. Figure 3 shows the manner in which the frequencies "fold" around multiples of the Nyquist frequency.

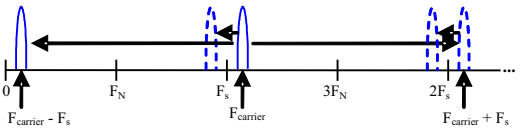

Figure 3. Frequency Effect of Under-Sampling

The resulting digital values from the under-sampled analog-to-digital conversion have a frequency content of 16.5 kHz plus the additive noise from the communication channel.

In operation, the DSP generates an interrupt at the completion of each ADC sample conversion. Each sample is then compared to the output of the digital PLL to estimate the phase of the received signal. At the bit rate, 5.5 kHz, the phase is determined. If the phase is less than ± 90 degrees then a “zero” is assumed to be received, otherwise a “one” is assumed to be received.

The received bit sequence is compared to the known bit pattern for the “bit sync” field which is sent at the beginning of a transmitted data packet. When the bit sync pattern is recognized, the modem then begins looking for the “word sync” pattern. The word sync pattern demarks the start of message data and also defined the polarity of the message data. After the data portion of the packet is determined and each bit has been detected, each 8-bit data byte is decoded from the 11-bit codeword for that byte. The parity bit for each byte is compared to the calculated parity for the transmitted data. The data is passed on from the PHY layer to the MAC layer. If the CRC checksum calculated from the received data agrees with the CRC word that was transmitted, the message is passed on from the MAC/Link layer to the Network layer.

Phase Detection: In order to detect the transmitted signal, “zero” or “one”, the phase of the 16.5 kHz IF signal is detected in the discrete received signal values. This is done by first driving a digital phase-lock-loop (PLL) with the received samples. When the output of the PLL is locked synchronously with the received signal, an estimate of the complex phase between the PLL and the received signal is generated by the PLL module. The real part of the complex phase is the cosine sum and will be either a large positive value when a “zero” has been received or a large negative value when a “one” has been received. The complex part of the phase is the sine sum. This represents the phase error and is fed back to the PLL to adjust the sine output so that it tracks the received signal.

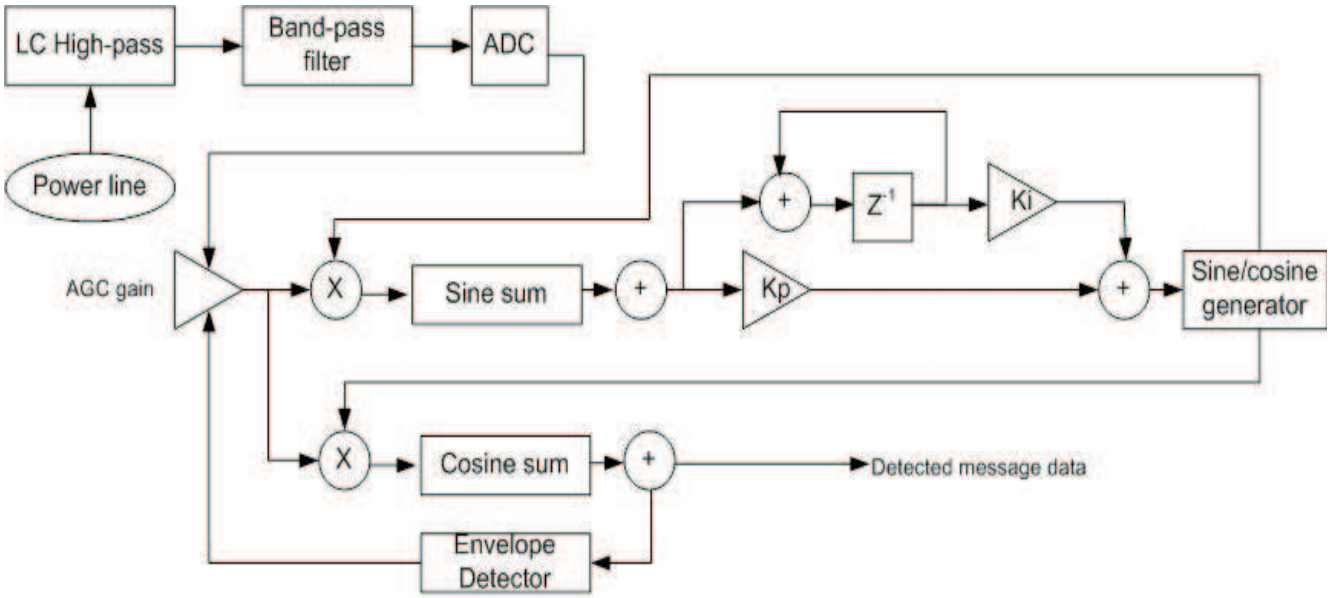

Figure 4. Receive Signal Processing Block Diagram

Figure 4 shows the complete receive signal processing block diagram. An automatic gain control module is also added to increase the robustness of the system. The AGC module applies an applicable gain to the receive signal by detecting the average magnitude of the receive signal.

Signal Transmission: In this application the transmit signal is generated directly using the on-chip PWM module outputs of the DSP controller. Each bit is defined to be 24 cycles, so the PWM controller is allowed to run for 24 cycles and then an interrupt reassigns the PWM outputs based on the polarity of the next bit being transmitted. To generate the transmit waveform, the message data to be transmitted is passed from the Application layer to the Session layer, to the Transport layer, to the Network layer, to the MAC/Link layer, and then to the PHY. At the Link layer the CRC word for the message data is calculated and appended to the data. The MAC layer holds the data until the PHY has determined if the channel is available. This is done by looking for the presence of the preamble pattern on the power line.

PWM Generation for the Transmit Waveform: A tri-level signal waveform is generated by summing two PWM outputs from the DSP controller. This tri-level waveform is then low-pass filtered to produce a sine wave. A tri-level waveform has much lower odd-harmonic energy than a standard two-level square wave.

Different pulse widths will produce different harmonic frequency content. In order to minimize harmonics that the filter needs to remove we need to use the optimum pulse width. This can be found by writing out the formula for the Fourier series for a symmetric pulse where *T* is the fundamental frequency period and w is the pulse width.

$$f(t) \quad \frac{4}{T} \sum_{n=1} \sin\left(\frac{n}{2}\right) \frac{\sin\left(\frac{n\,w}{T}\right)}{\frac{n\,w}{T}} \sin\left(\frac{n2}{T}t\right) \tag{1}$$

The total harmonic distortion (THD) can be expressed as

$$THD \quad \frac{\int_0^T f(t,n=1)^2 dt}{\sum_{n=2} \int_0^T f(t,n)^2 dt} \tag{2}$$

Using these equations and solving for the minimum total harmonic distortion (THD), the optimum pulse width is found to be approximately 37% of the period T. However, this does not take into account the effect of the low pass filtering the waveform. If a second order low pass filter is applied to the waveform a different result is found. The Q of the 2nd order low pass filter used in simulations was set to 2.3. This value is a tradeoff between improved THD and the natural response time constant. With a large Q the THD would be even better but the circuit rings from one transmitted bit time into the next bit time, resulting in inter-symbol interference. Therefore, the optimum design sets the digital positive and negative pulse widths to 1/3 of the pulse period and sets the low pass filter corner frequency to the same frequency as the digital pulse train. The 1/3 pulse width can easily be constructed using a timing clock that is 12 times the transmit waveform frequency. This is shown in Figure 5. The transmit sine wave is obtained from these PWM outputs by utilizing an analog circuit that sums the two signals and then low-pass filters the harmonics.

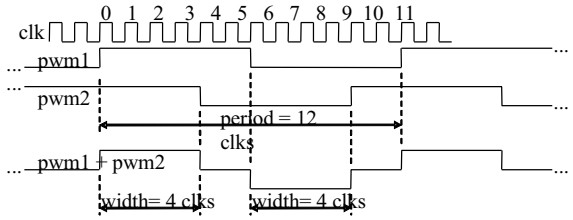

Figure 5. Tri-Level Waveform Construction

Transmit Amplifier: The transmit amplifier is based on a Sallen-Key filter, the transfer function for this circuit can be expressed as:

$$v_{out} \quad \frac{A}{akR^2C^2} \frac{v_a}{s^2 \quad \frac{1 \quad k \quad ak \quad 1 \quad A}{akRC} s \quad \frac{1}{akR^2C^2}} \tag{3}$$

where $R_1 = kR$, $R_2 = R$, $C_1 = C$, $C_2 = aC$

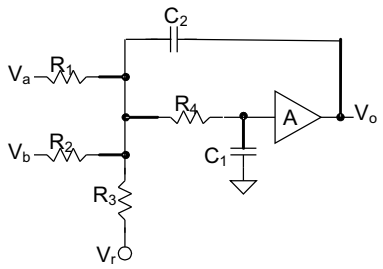

Figure 6. Transmit Low-Pass Filter Amplifier

For an amplifier with a gain of 2, V_{out} can be expressed as follows

$$v_{out} \quad \frac{2 \quad ^{2}v_{a}}{s^{2} \quad \overline{Q}s \quad ^{2}} \tag{4}$$

where $\frac{1}{\sqrt{ak}RC}$, $Q \quad \sqrt{a}\frac{\sqrt{k}}{1 \quad k}$

The peaking in the filter is maximized when Q is maximized and Q is maximized when the quotient $\frac{\sqrt{k}}{1 \quad k} \quad 1$. (**k** is the ratio of R_1 to R_2)

Therefore the resistors R_1 and R_2 in Figure 6 are typically set equal in a Sallen-Key filter circuit and the Q is set by adjusting the ratio of the capacitor values.

The transmit amplifier has two inputs that add and filter the signal from the two PWM outputs of the processor. It is desirable to have a fair amount of peaking at the transmit frequency. The more peaking the amplifier provides at the transmit frequency, the more relative attenuation there will be at the harmonic frequencies. Therefore we want to set the parallel combination of R_1, R_2 and R_3 equal to R_4 so that a large Q can easily be obtained.

Defining, R_4=R, then $\frac{1}{R} \quad \frac{1}{R_1} \quad \frac{1}{R_2} \quad \frac{1}{R_3}$ and $R \quad \frac{R_1R_3}{2R_3 \quad R_1}$

Further, defining the attenuation factor *K* such that $\frac{1}{K} \quad \frac{R_3}{2R_3 \quad R_1}$. This is the attenuation of the input at the first voltage node in the circuit. Then we can define the resistors in terms of *R* and *K*.

$$R_1 \quad KR, \quad R_2 \quad KR, \quad R_3 \quad \frac{K}{K \quad 2}R, \quad R_4 \quad R$$

Defining the capacitors as $C_1 = C$, $C_1 = aC$ we can now express the transmit amplifier transfer function in terms of *A*, *K*, *a*, *R* and *C*

$$v_{out} \quad \frac{A}{KaR^{2}C^{2}} \frac{v_{a}}{s^{2} \quad \frac{2 \quad a1 \quad A}{aRC}s \quad \frac{1}{aR^{2}C^{2}}} \quad \frac{A}{K} \frac{^{2}v_{a}}{s^{2} \quad \overline{Q}s \quad ^{2}} \tag{5}$$

Where $\frac{1}{\sqrt{a}RC}$ and $Q \quad \frac{\sqrt{a}}{2 \quad a\,1 \quad A}$

For a given Q we can solve for the capacitor ratio:

$$a \quad \frac{1 \quad \sqrt{8Q^2 \quad A \quad 1 \quad 1}}{2Q^2 \quad A \quad 1^{\,2}} \quad \frac{2}{A \quad 1} \tag{6}$$

For an amplifier gain of A = 2, and picking the smaller solution for a this reduces to: $a \quad 2 \quad \frac{1 \quad \sqrt{8Q^2 \quad 1}}{2Q^2}$

Finally, at s = ω_0 the transfer function gain is $G\ j\ _0 \qquad j\frac{AQ}{K}$. Now we have all the information we need to define the component values for the transmit amplifier. The filter components are obtained using the above equations to design the analog front end of the modem.

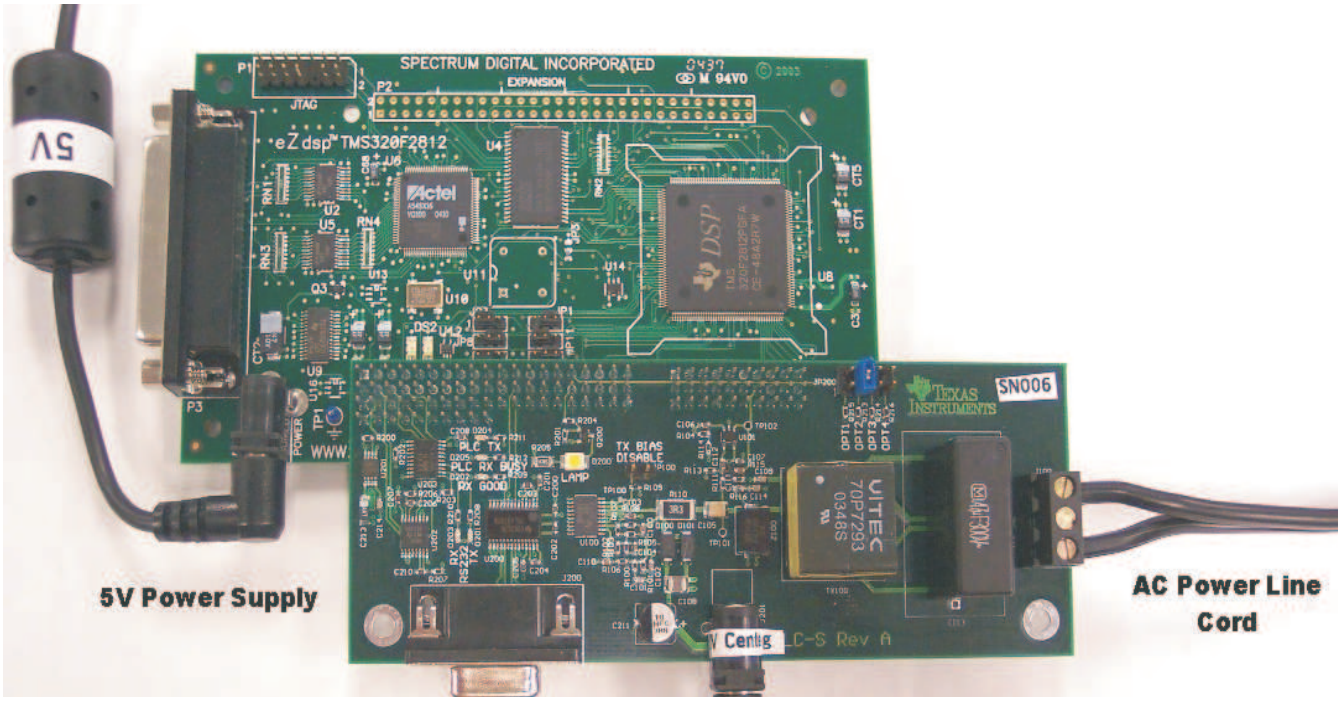

Figure 7. DSP Controller Based Power Line Modem Hardware

3 Experimental Results

A complete power line modem unit based on TMS320F2812 using BPSK modulation was implemented. The prototype is shown in Figure 7. The lower board is the DSP board and the upper board is the analog front end board.

This modem was tested with both 110 V and 220 V power line systems with reliable performance. The complete system code is written in standard “C”. The modem function utilizes 8 KB of program memory and 4 KB of data memory and consumes about 55 MIPS with CRC and AGC modules enabled. Figure 8 shows the received signal with the corresponding de-modulated waveform. The current implementation achieves 5.5 kbps baud rate for the modem functionality.

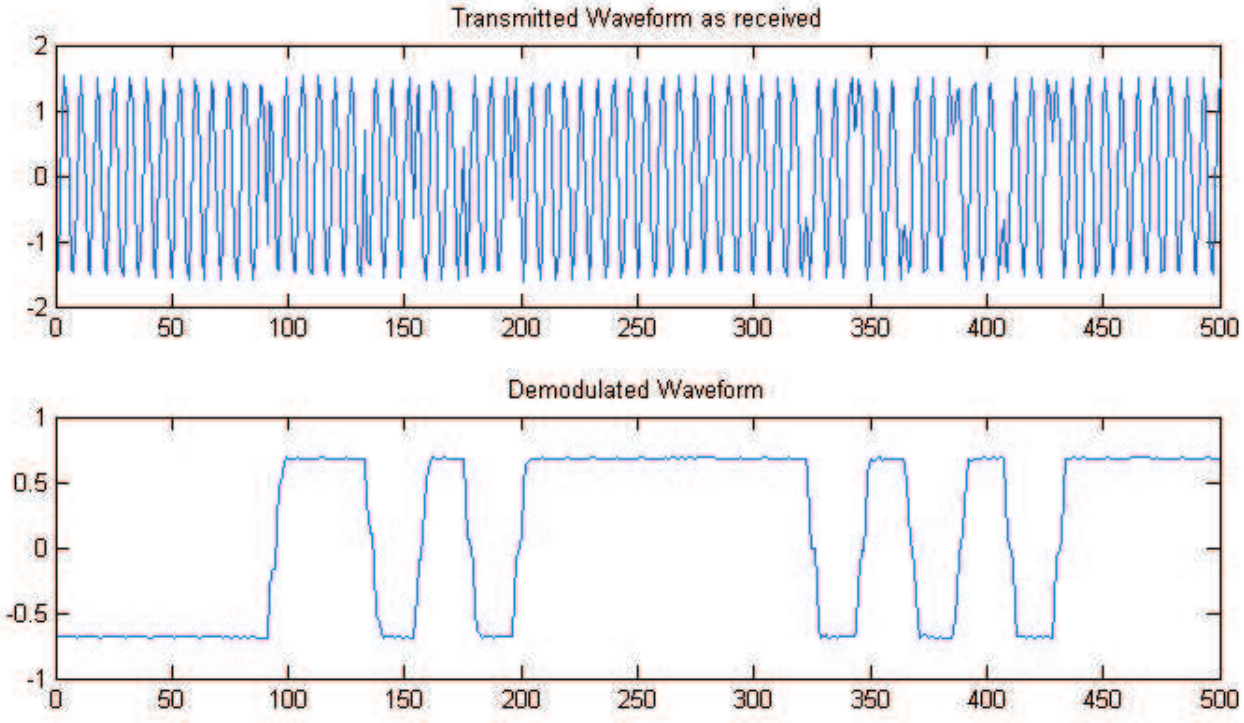

Figure 8. Received Waveform with Corresponding Demodulated Signal

In addition, the system shown in Figure 7 implemented the digital addressable lighting interface (DALI) [4] command structure to show the potential of integrating a complete lighting network using a single DSP controller. The DALI commands are transmitted over the power line to control the intensity of a white LED using an extra PWM output of the DSP controller.

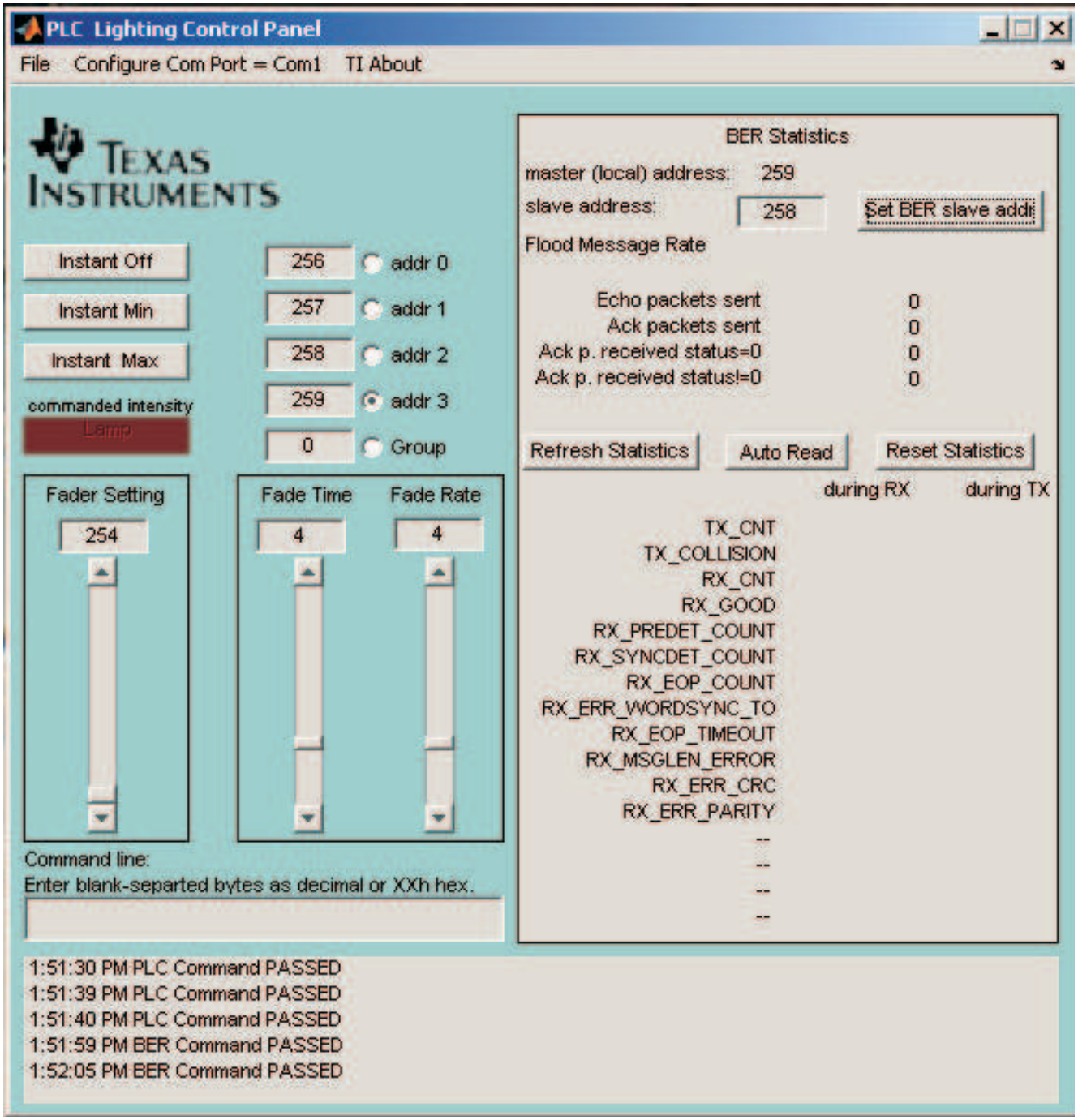

Figure 9. Serial Port GUI for Controlling the Power Line Modem Function

Each DSP modem node also implements a serial port based interface for controlling the network from a PC. The serial communication GUI utilizes the on-chip SCI port of the DSP controller. The GUI PC interface is written using MATLAB[5]. A screen shot of the GUI is shown in Figure 9. A standard PC can be used to control any of these nodes.

4 Conclusions

This paper presented a power line modem implementation with binary phase shift keying modulation technique using a single fixed-point DSP controller. The remaining resources of the same DSP controller are utilized to implement additional functions like a three-phase voltage source inverter, DALI command set, and a serial-port GUI to show the potential of system integration. The actual modem hardware was tested under various power conditions in different parts of the world; the system performance in all cases was robust and reliable.

5 References

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2. ANSI/EIA/CEA-709.1-B-2000 Control Network Protocol Specification http://www.lonmark.org/products/guides.htm#lontalk
3. Texas Instruments TMS320F2812 Data Manual http://focus.ti.com/lit/ds/symlink/tms320f2812.pdf
4. Digital Addressable Lighting Interface Activity Group (DALI AG) of ZVEI, Division Luminaires Stresemannallee 19, D60596 Frankfurt am Main, Germany http://www.dali-ag.org
5. MATLAB is a product of The MathWorks http://www.mathworks.com

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