



**ELECTROSTATIC DISCHARGE SENSITIVITY
MEASUREMENT**

by Microcontroller Division Applications

This application note describes a procedure for determining the susceptibility of microcontroller devices to ESD damage.

1 REFERENCE DOCUMENTS

1.1 REFERENCE DOCUMENTS (INTERNAL ST REFERENCES)

- 0061692 "Reliability Test Specification for Product Qualification"
- SOP2614 "Reliability Procedure for Product Qualification"

1.2 OTHER REFERENCES

- CDF-AEC-Q100-002 "Human Body Model ESD test"
- CDF-AEC-Q100-003 "Machine Model ESD test"
- ESD Association standard draft DS5.3 - 1993 Draft Standard for ESD sensitivity text-Charged Device Model (CDM) Component Testing
- ESD Association standard draft DS5.3.1 - 1996 Charged Device Model (CDM) Non-Socketed Mode
- JEDEC STANDARD JESD22-C101 "Field- induced Charged Device Model"
- JEDEC STANDARD JESD22-A114A "Human Body Model"
- JEDEC STANDARD JESD22-A115A "Machine Model"
- ESD Association standard draft DS5.2 - 1996 "Machine Model"
- ESD Association Standard ESD STM 5.1 - 1998 "Human Body Model"
- EIAJ Provisional Standard EDX-4702 "Charged Device Model"

2 DEFINITIONS

- DUT (Device under test): a product evaluated for its sensitivity to ESD
- ESD (Electrostatic discharge): the transfer of electrostatic charge between bodies at different electrostatic potentials
- Electrostatic Discharge Sensitivity: an ESD voltage level which causes part failure
- ESD simulator: an instrument that simulates the models described in this specification
- Human Body Model (HBM) ESD: an ESD pulse simulating the human body discharge to a device
- Machine Model (MM) ESD: an ESD pulse approximating a pulse from a machine or mechanical equipment
- Maximum Withstanding Voltage: the maximum ESD voltage at which the product passes the failure criteria requirements specified in Section 4.
- PUT: pin under test
- Non-supply Pins: all input, output, bi-directional and clock pins except power pins and non connected pins.
- Power Pins all power supply, external voltage source and ground pins
- Like-named Power Pins: Power Pins with similar names and functions. i.e. VDD1 - VDD2, VCC1 - VCC2, GND1 - GND2.
- Ringing current: the damped high frequency current oscillation usually following the pulse rise time

3 GENERAL

- ESD pulse simulator and DUT
- For HBM see **FIGURE 1**
- For MM see **FIGURE 2**

3.1 MEASUREMENT EQUIPMENT

3.1.1 For HBM and MM

An oscilloscope and current probe with a minimum bandwidth of 350 MHz.

Maximum cable length of current probe is 1 meter.

- Evaluation loads:
 - a) low inductance, 1000 Volt, 500 ohm +/- 1% sputtered film resistor
 - b) tinned copper shorting wire

3.2 EQUIPMENT QUALIFICATION

Must be performed during initial testing for equipment acceptance, after repairs that may affect the waveform and at least once per year, unless different recommendation from Tester Supplier.

For HBM and MM the tester must meet the requirements of **TABLE 1** and **TABLE 2** at all voltage levels on the highest pin count test socket with both the shorting wire and 500Ω load.

3.3 WAVEFORM VERIFICATION

Must be performed every 6 months as a minimum. For CDM the use of 1GHz oscilloscope is allowed.

4 PROCEDURE

- All units must be tested per applicable Data Sheet (Static and dynamic parameters). Sample size according to spec. 0061692 for HBM and MM, minimum sample size 3 devices.
- For HBM and MM each sample shall be stressed at one voltage level using all pin combinations specified in **TABLE 3**, applying 3 positive and 3 negative pulses for each pin combination, unless different requirements in the detail specification. Minimum time between pulses is 1 second.

Note A: for HBM and MM under responsibility of the involved Product Group Q&R Dept. following derogations may be applied in agreement with ESD Associations Standard ESD STM5.1 1998 (February 1998) and JEDEC Standard JESD22- A114A and JEDEC Standard JES22 - A 115 A applying one positive and one negative pulse for each pin combination, unless different requirements in the detailed specification. If more than one pulse is requested, minimum time between pulses is 500 milliseconds.

Note B: For HBM and MM 3 new components may be used at each voltage level or pin combination if desired. This will eliminate any step stress hardening effect, and will reduce the possibility of early failure due to cumulative stress on power pins. However, if a single set of 3 components are stressed at each level, then to avoid missing possible ESD vulnerability windows, it is recommended not to miss any stress step.

- Failure criteria:
 - A product passes a voltage level if all units stressed at that voltage level pass.
 - A unit will be defined as a failure if, after exposure to ESD pulses, it no longer meets the data sheet requirements (static and dynamic parameters).

Note: Cumulative damage effects may be eliminated by retesting at the failure voltage step using a new sample.

ELECTROSTATIC DISCHARGE SENSITIVITY MEASUREMENT

Table 1. Waveform Specification For Human Body Model

Voltage level (V)	I _{peak} for Short I _{ps} (A)	I _{peak} for 500 Ω* I _{pr} (A)	Rise Time for Short t _r (ns)	Rise Time for 500Ω* t _{rr} (ns)	Decay Time for Short t _d (ns)	Ringing Current I _R (A)
1000.00	0.6-0.74	.375-.55	2-10	5-25	130-170	15% of I _{ps} and I _{pr}
2000.00	1.2-1.48	NA	2-10	NA	130-170	15% of I _{ps} and I _{pr}
4000.00	2.4-2.96	NA	2-10	NA	130-170	15% of I _{ps} and I _{pr}
8000.00	4.8-5.92	NA	2-10	NA	130-170	15% of I _{ps} and I _{pr}

* The 500 Ω load is used only during Equipment Qualification as specified in Section 3.2

Table 2. Waveform Specification For Machine Model

Voltage Level (V)	Positive First Peak Current for Short, I _{ps1} (A)	Positive Second Peak Current for Short, I _{ps2} (A)	Major Pulse Period for Short, t _{pm} (ns)	Positive First Peak Current for 500Ω* I _{pr} (A)	Current at 100ns for 500Ω* I ₁₀₀ (A)
200	2.8-3.8	67% to 90% of I _{ps1}	66-90	NA	NA
400	5.8-8	67% to 90% of I _{ps1}	66-90	0.85 to 1.2	0.29 ± 10%

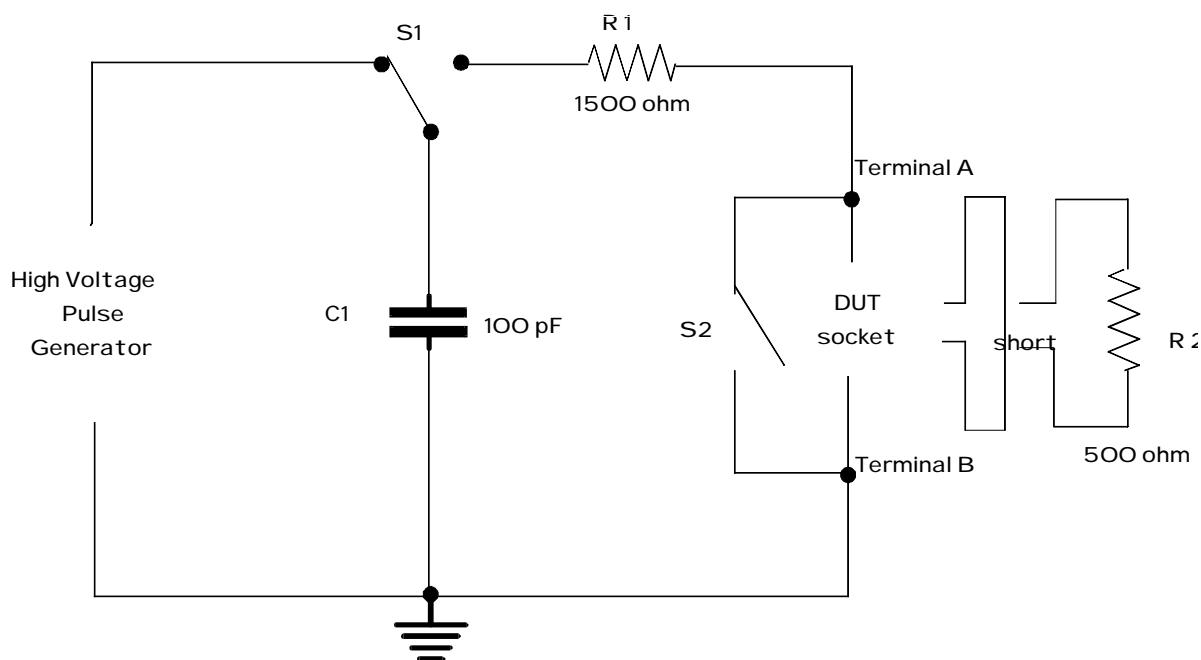
* The 500 Ω load is used only during Equipment Qualification as specified in Section 3.2

Table 3. Pin Combinations For Integrated Circuits (HBM and MM)

Pin combination	Connect Individually to Terminal A	Connect Individually to Terminal B (Ground)	Floating Pins (unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	First power pin(s)	All pins except PUT and first power pin(s)
2	All pins one at a time, except the pin(s) connected to Terminal B	Second power pin(s)	All pins except PUT and second power pin(s)
3	All pins one at a time, except the pin(s) connected to Terminal B	Nth power pin(s)	All pins except PUT and Nth power pin(s)
4	Each Non-supply pin	All other Non-supply pins except PUT	All power pins
5*	Each Inverting input pin	Each corresponding Non-inverting pin	All pins not under test and all power pins

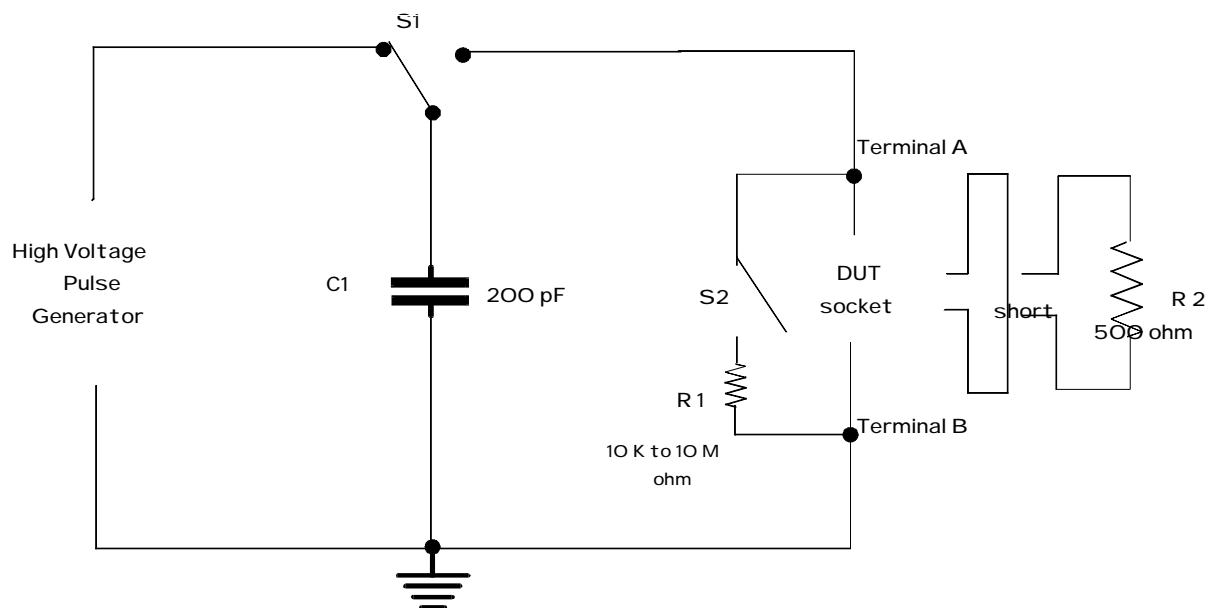
* For Integrated Circuits with operational amplifier functions

Figure 1. Typical Equivalent HBM ESD Circuit

**Notes:**

- The performance of any simulator is influenced by its parasitic capacitance and inductance.
- Precautions must be taken in tester design to avoid recharge transients and multiple pulses.
- R2, **used for Equipment Qualification as specified in Section 3.2** shall be a low inductance, 1000 Volts, 500 resistor with $\pm 1\%$ tolerance.
- **Piggybacking of DUT sockets is permitted if waveform in socket is within spec limits.**
- Reversal of terminals A and B to achieve dual polarity is not permitted.
- S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in charge state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

Figure 2. Typical Equivalent MM ESD Circuit



Note:

- The performance of any simulator is influenced by its parasitic capacitance and inductance.
- Resistor R1, in series with switch S2, ensures a slow discharge of the device.
- Precautions must be taken in tester design to avoid recharge transients and multiple pulses.
- R2, **used for Equipment Qualification as specified in Section 3.2** shall be low inductance, 1000 Volts, 500 resistor with $\pm 1\%$ tolerance.
- **Piggybacking of DUT sockets is permitted if waveform in socket is within spec limits.**
- Reversal of terminals A and B to achieve dual polarity is not permitted.
- S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in charge state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

ELECTROSTATIC DISCHARGE SENSITIVITY MEASUREMENT

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