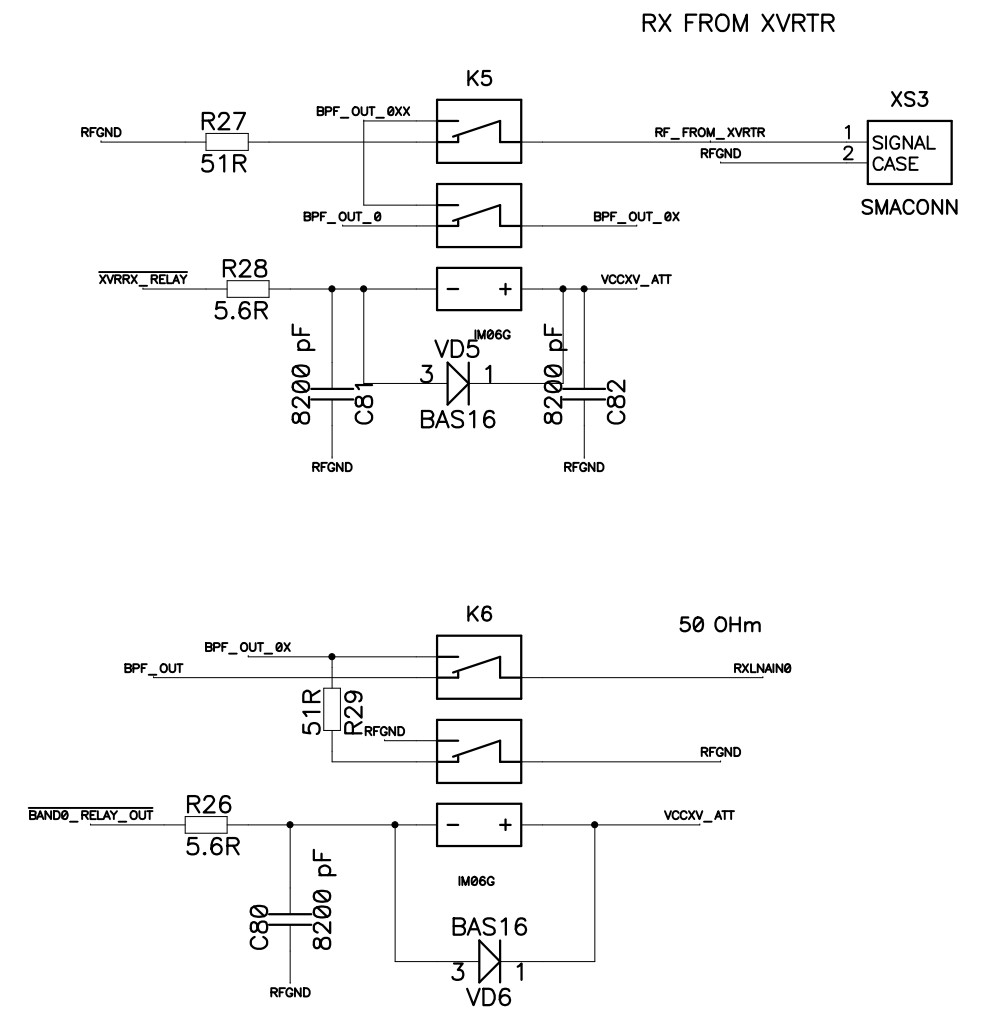
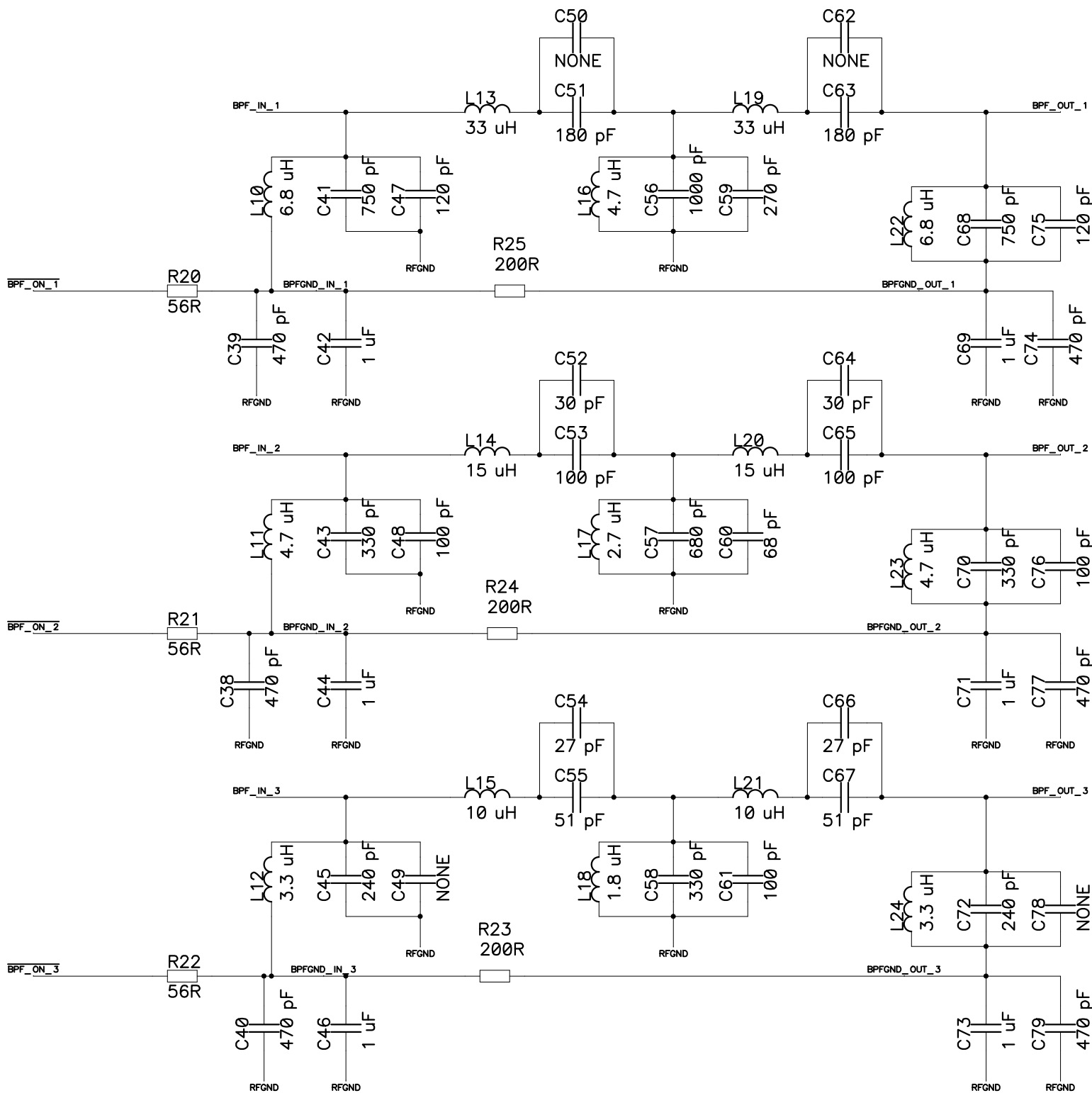


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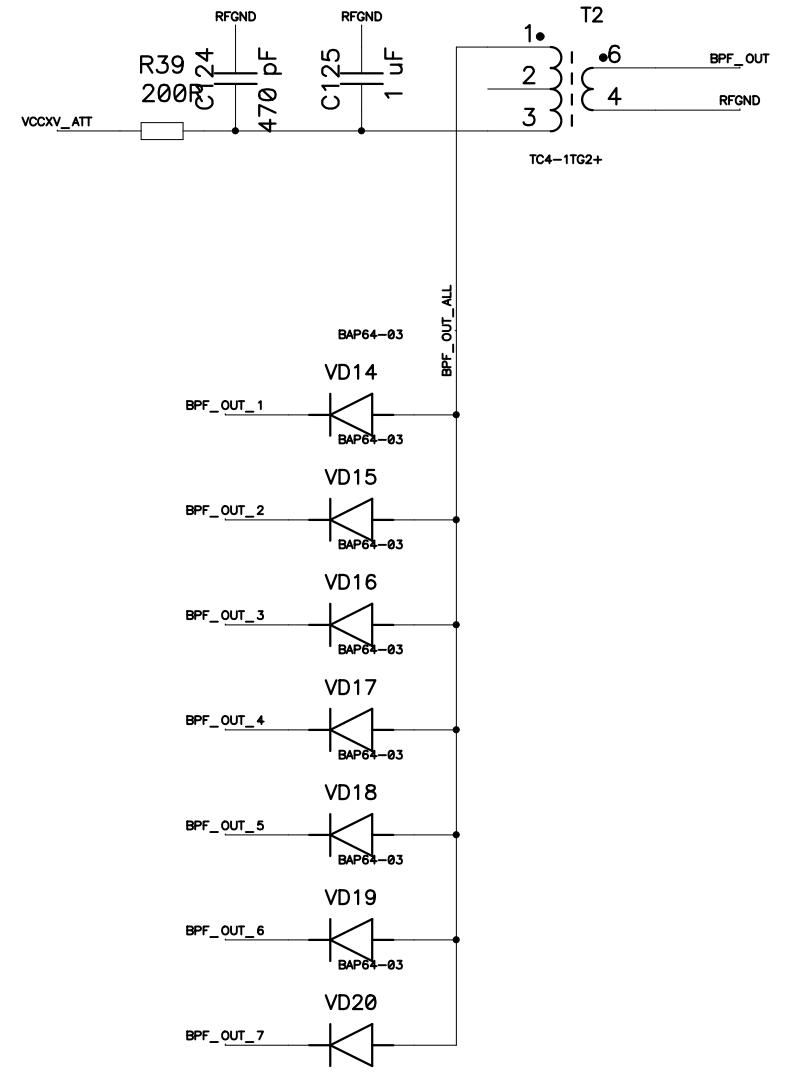
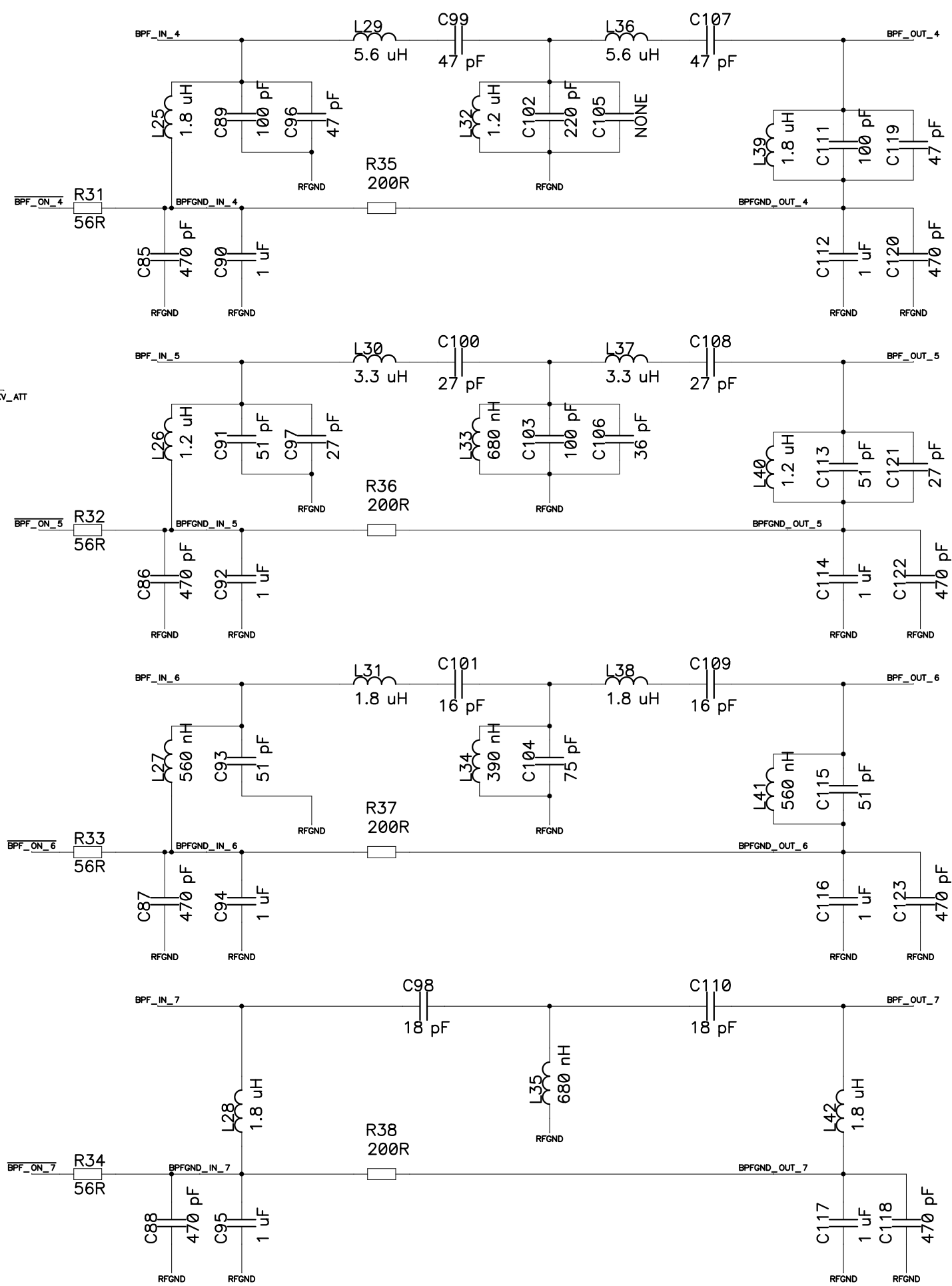
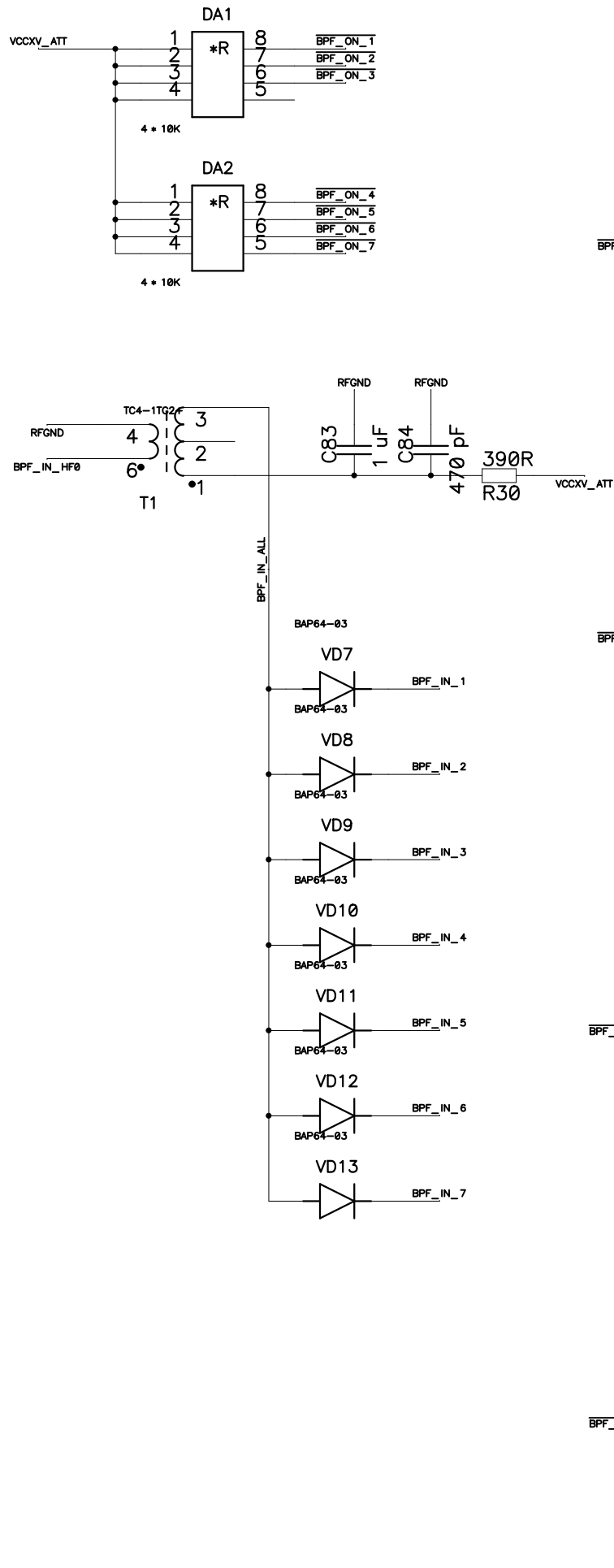
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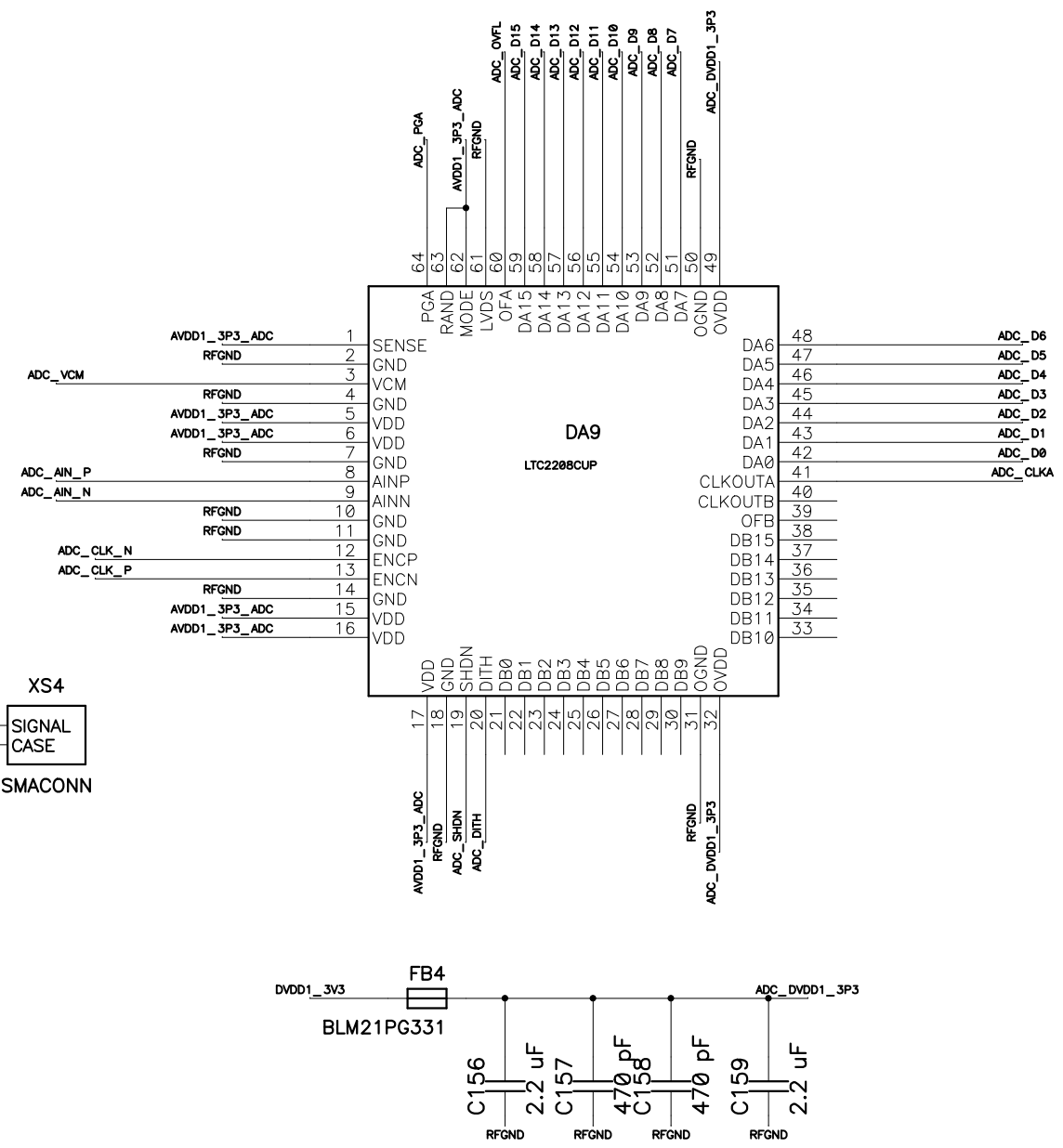
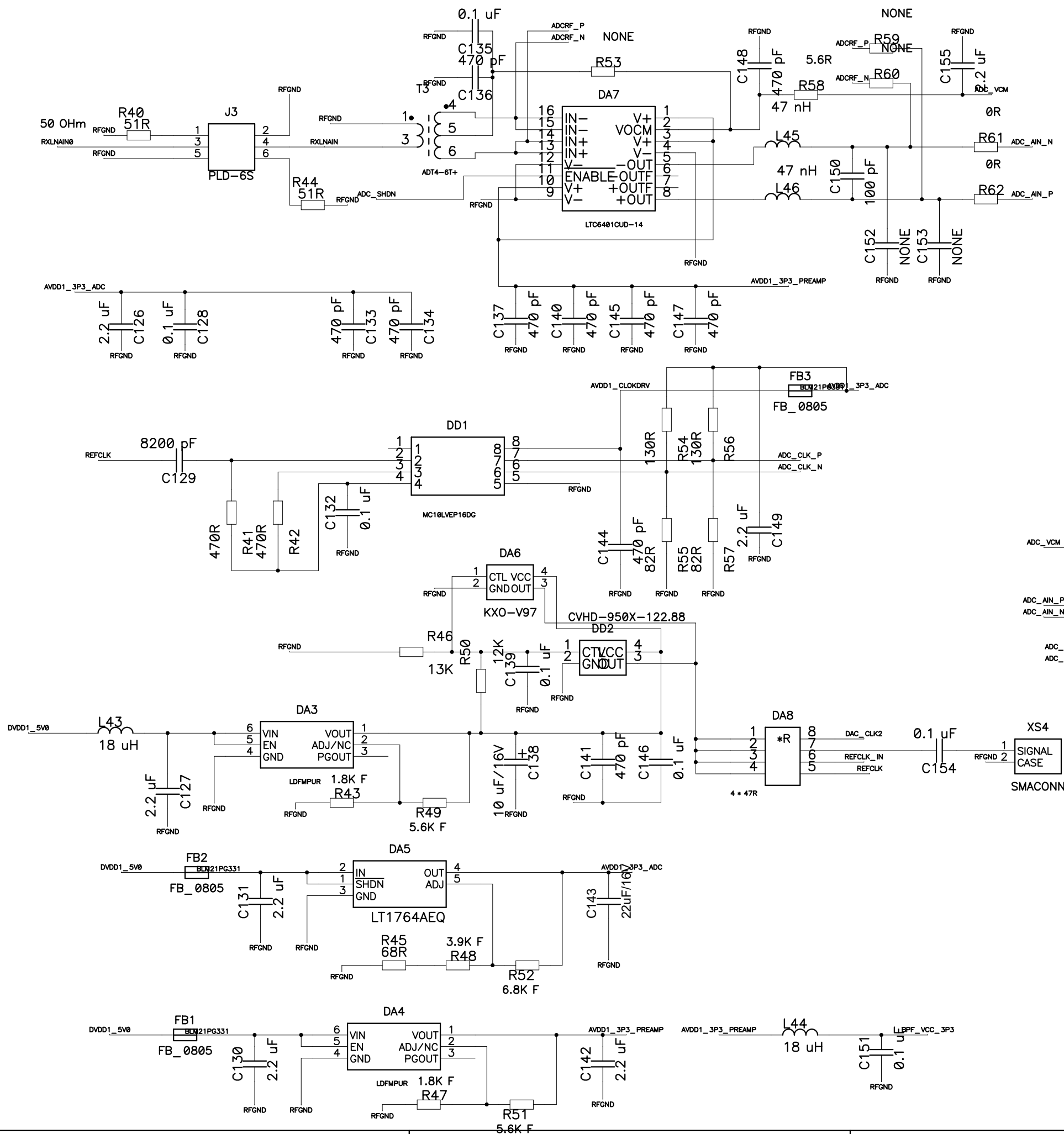
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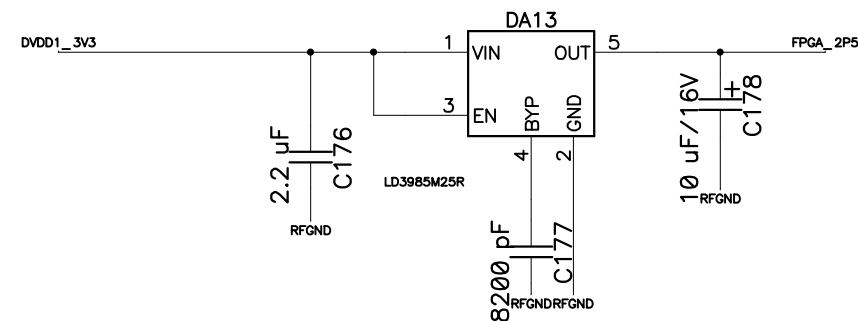
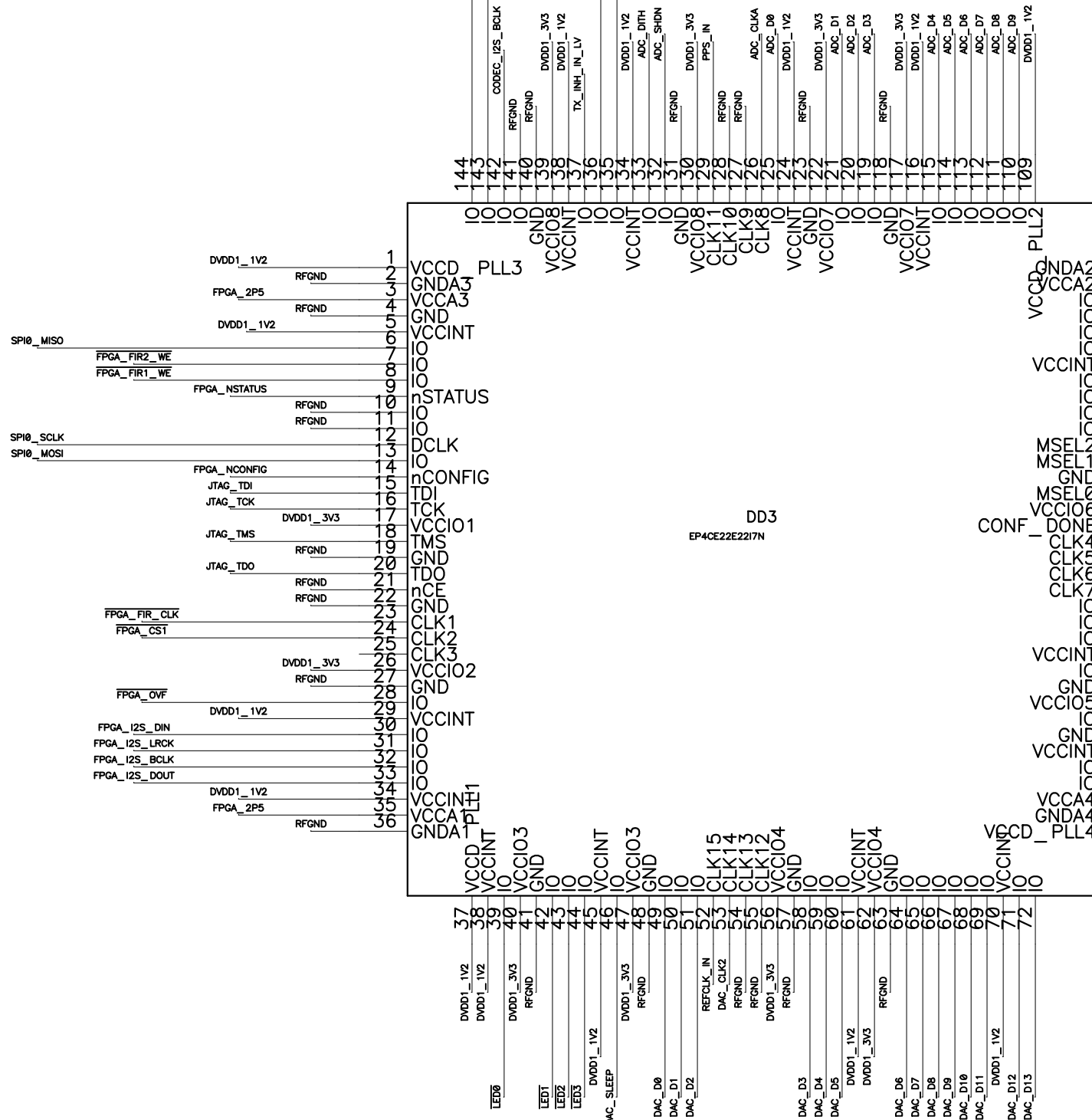
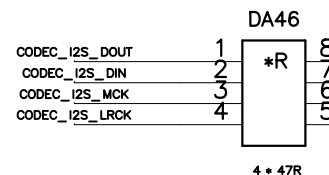
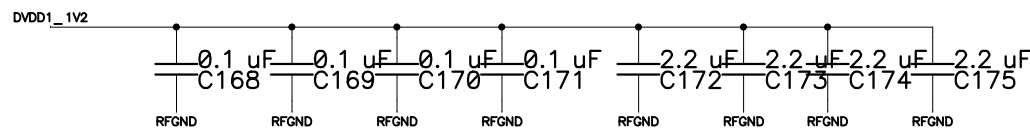
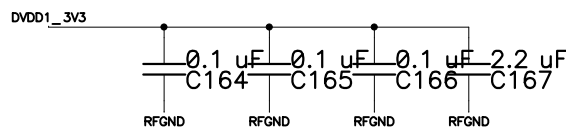
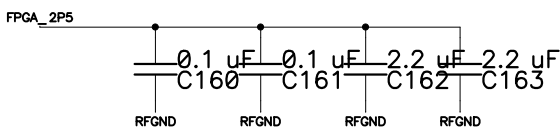
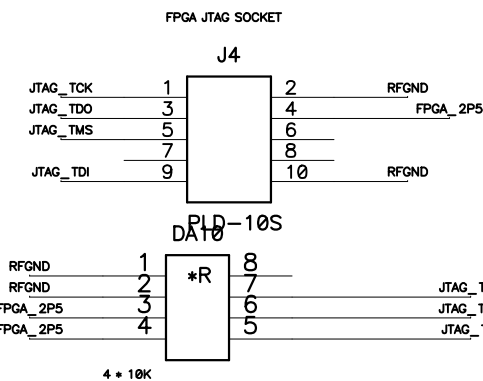
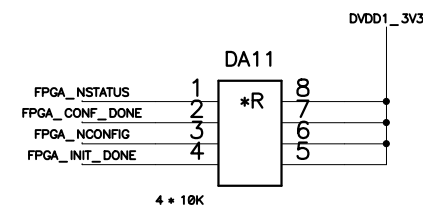
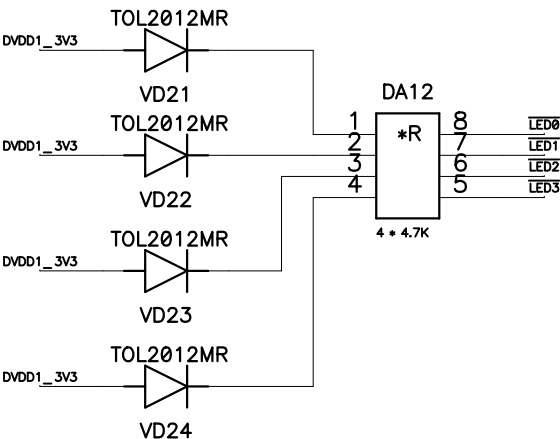
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TO CPU: PASSIVE SERIAL MODE SUPPORT

SPI0\_MISO  
SPI0\_MOSI  
SPI0\_SCLK  
FPGA\_NSTATUS  
FPGA\_NCONFIG  
FPGA\_CONF\_DONE

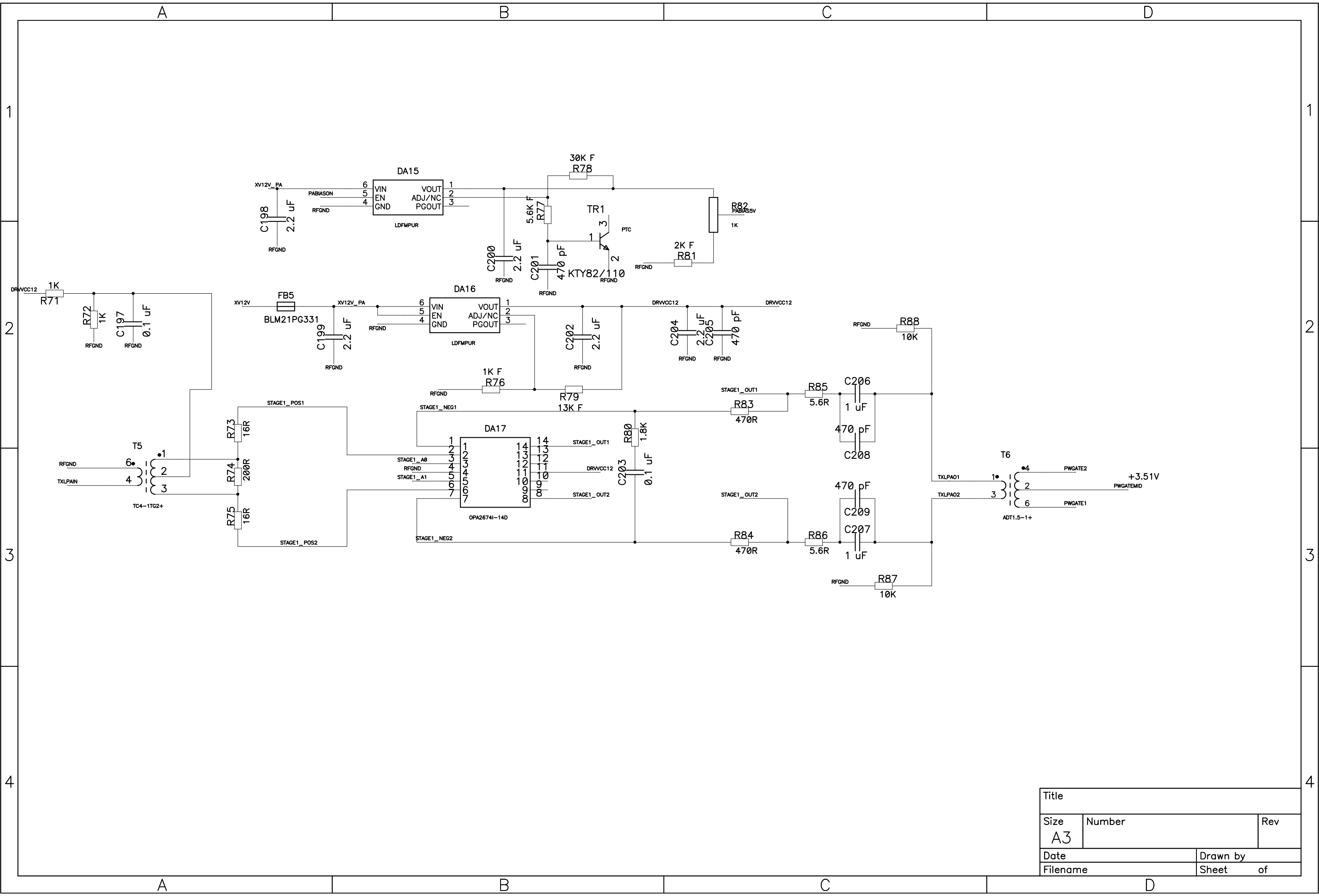


MSEL[2..0]:  
0: PS, POR=STANDARD, 3.3, 3.0, 2.5  
4: PS, POR=FAST, 3.3, 3.0, 2.5  
2: AS, POR=STANDARD, 3.3  
5: AS, POR=FAST, 3.3 (default)  
Note:  
The fast POR time is 3 ms < TPOR < 9 ms  
The standard POR time is 50 ms < TPOR < 200 ms

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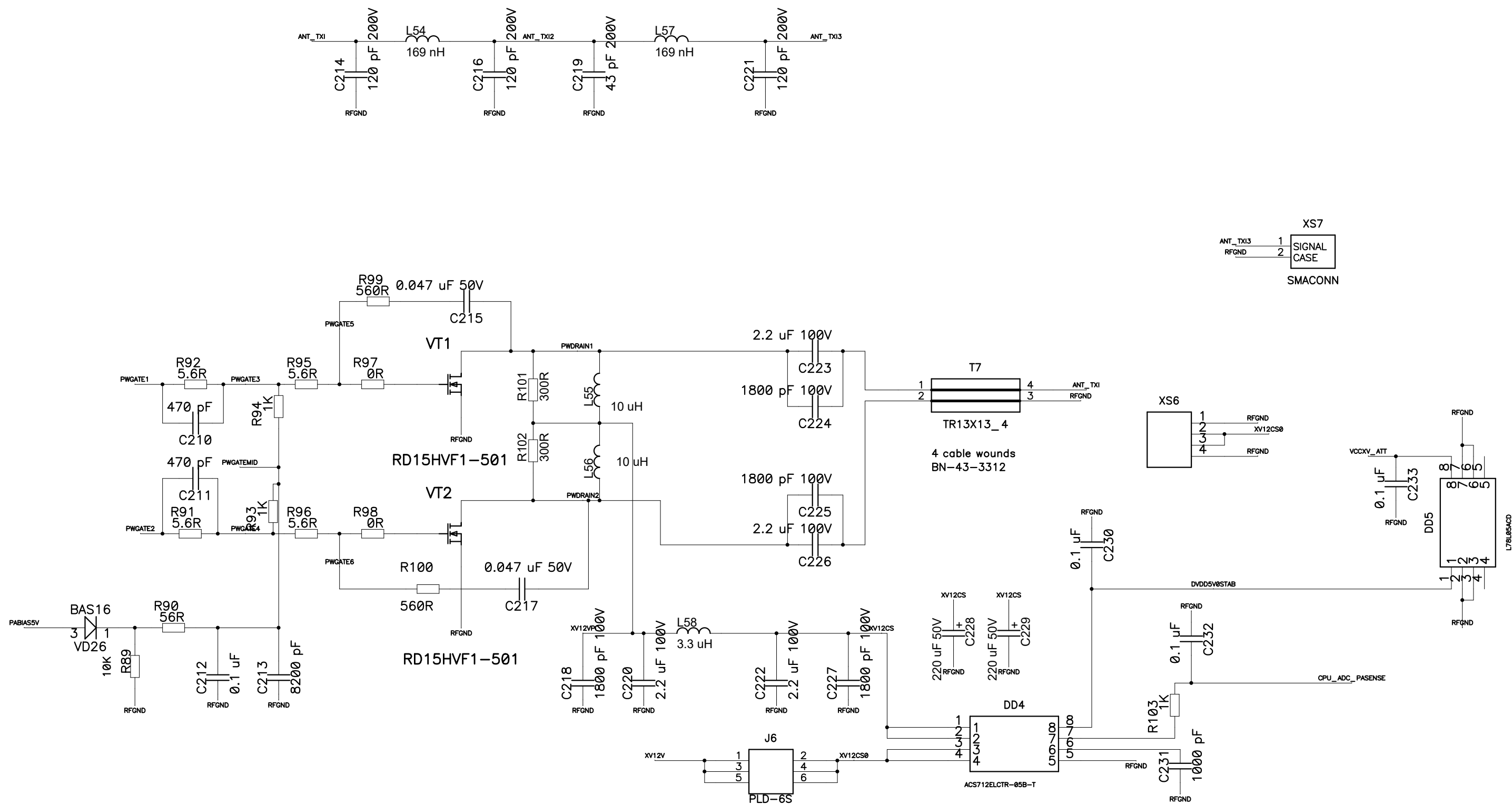




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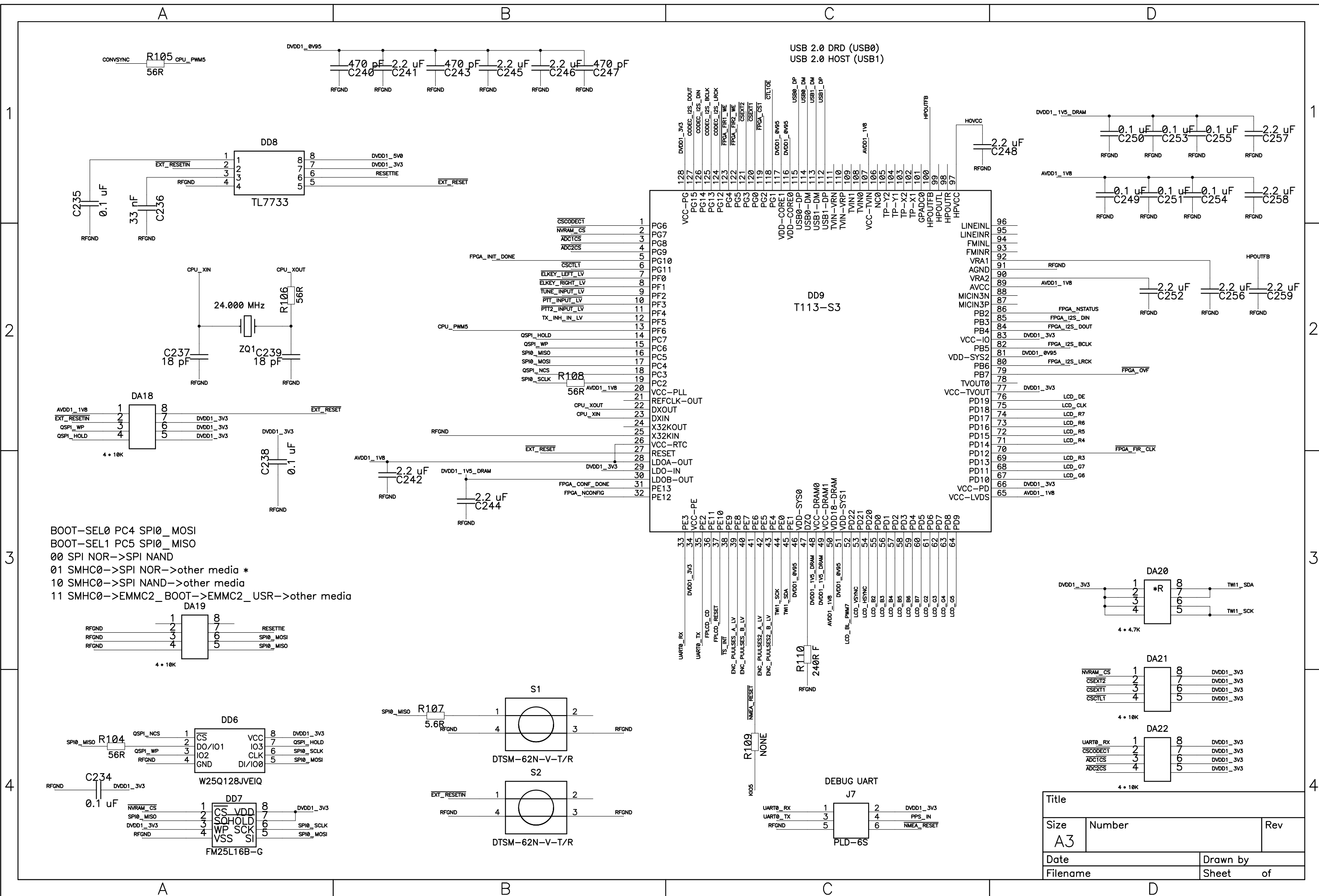
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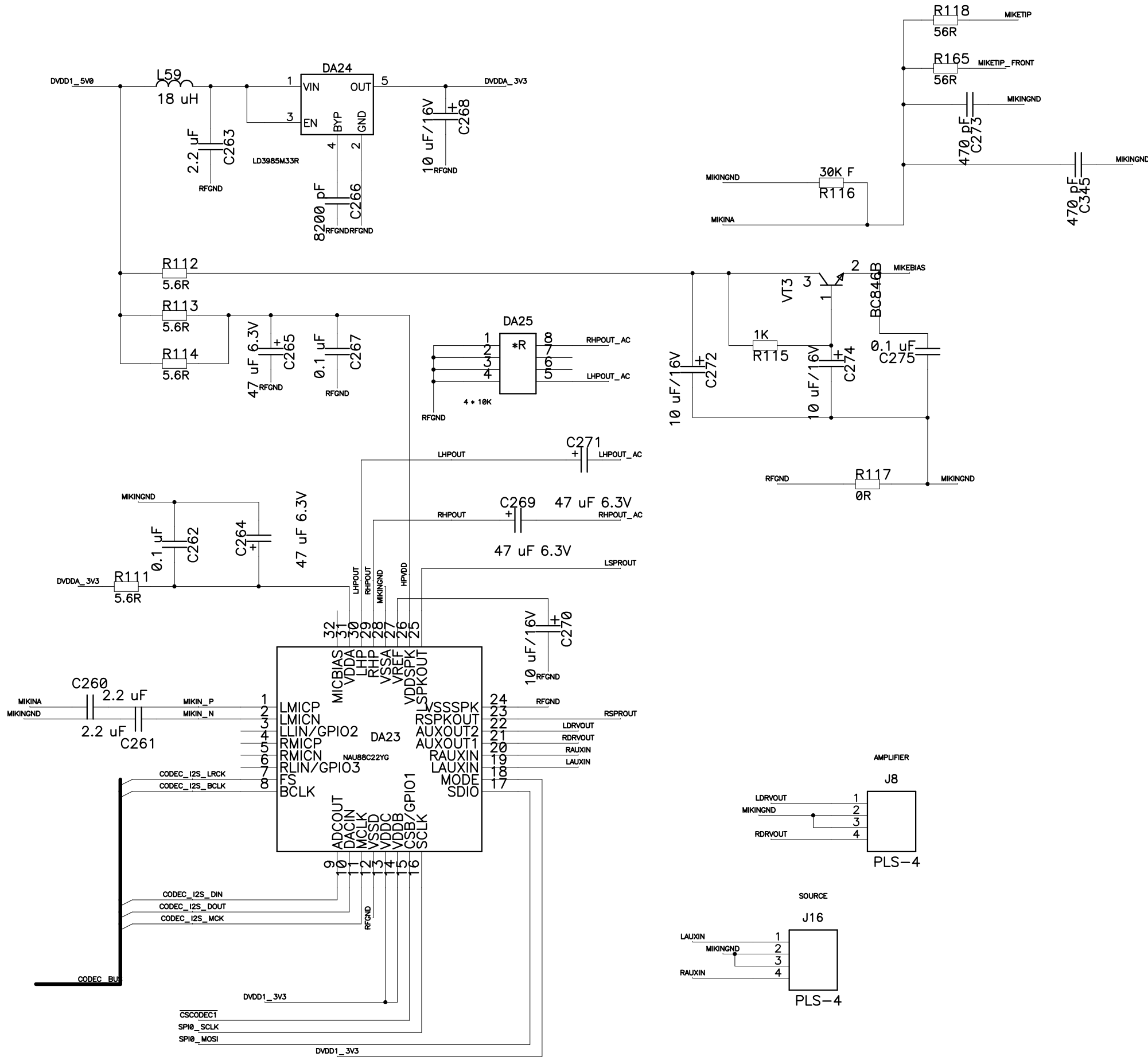
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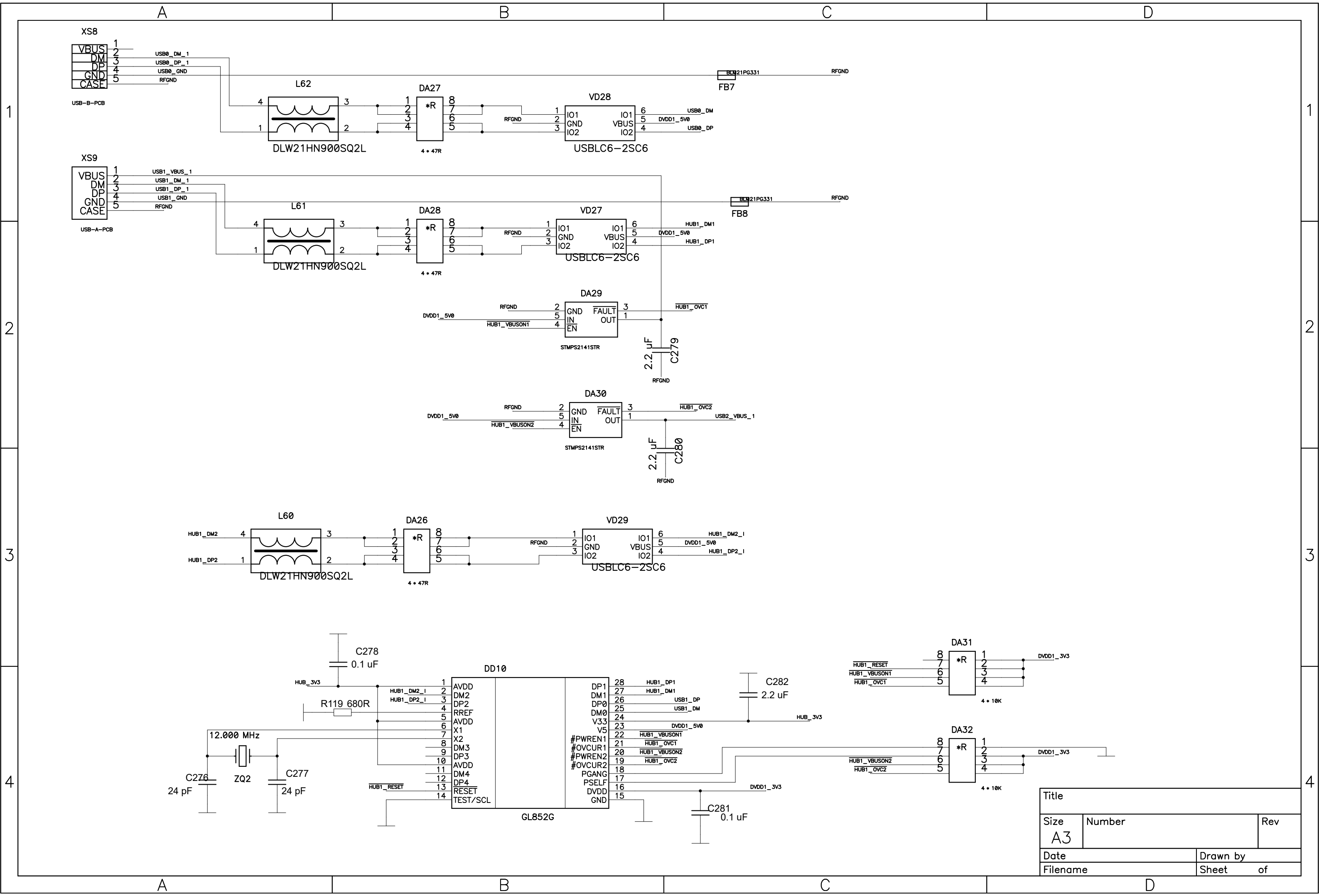
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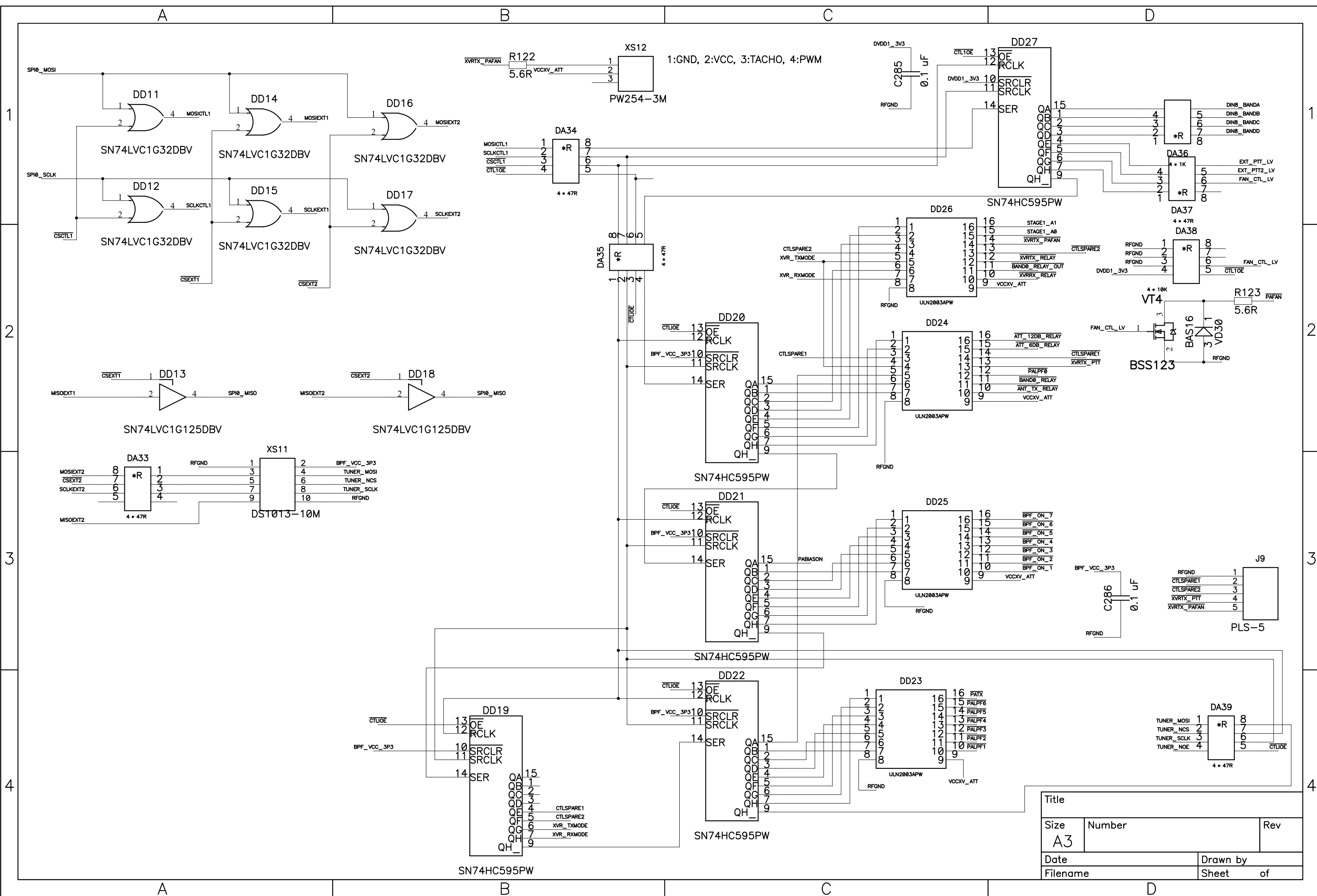




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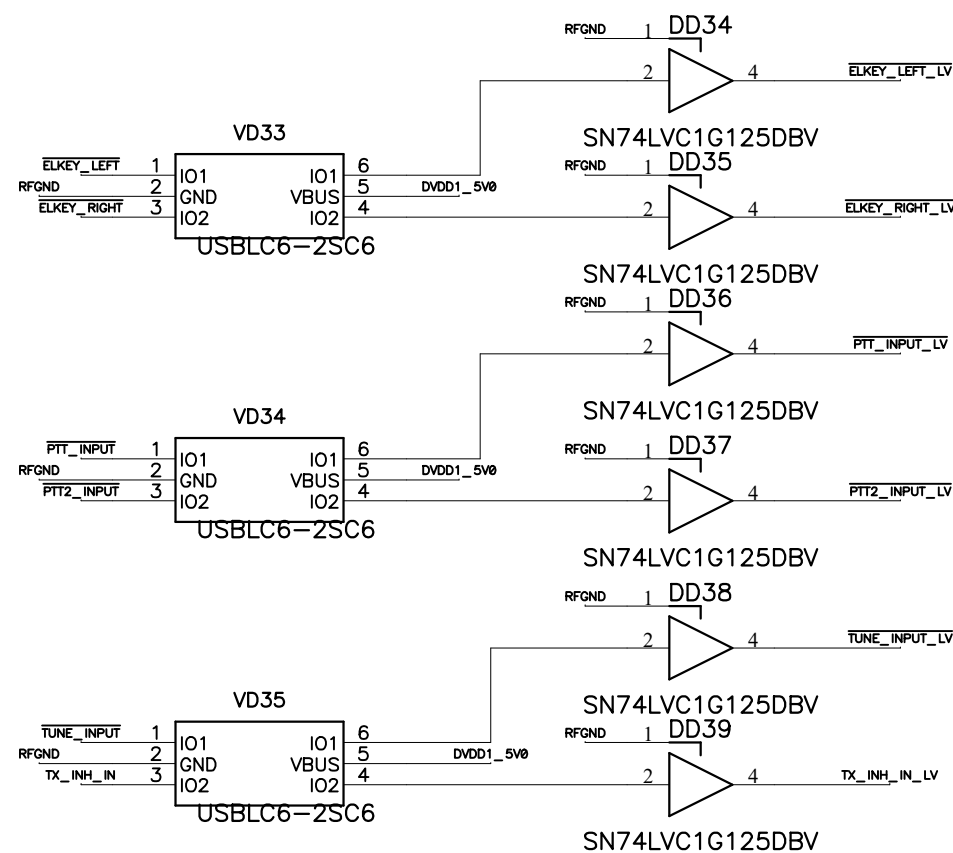
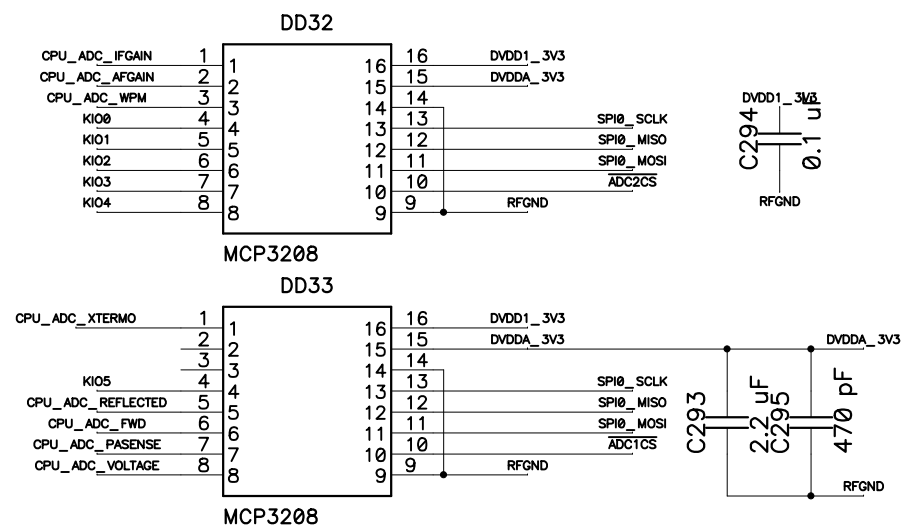
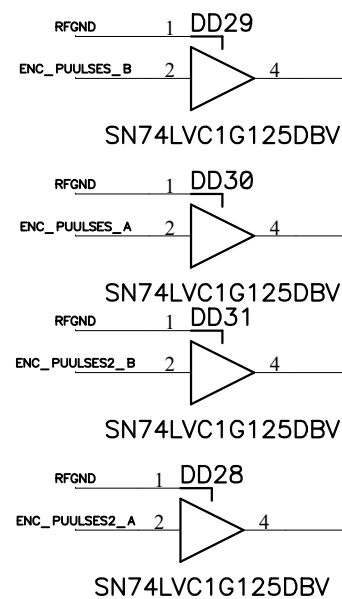
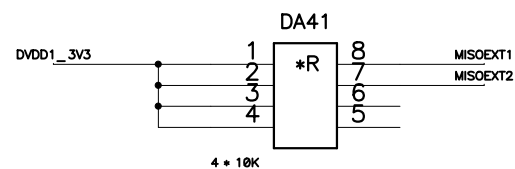
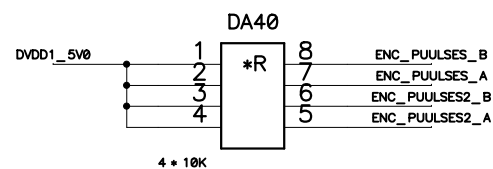
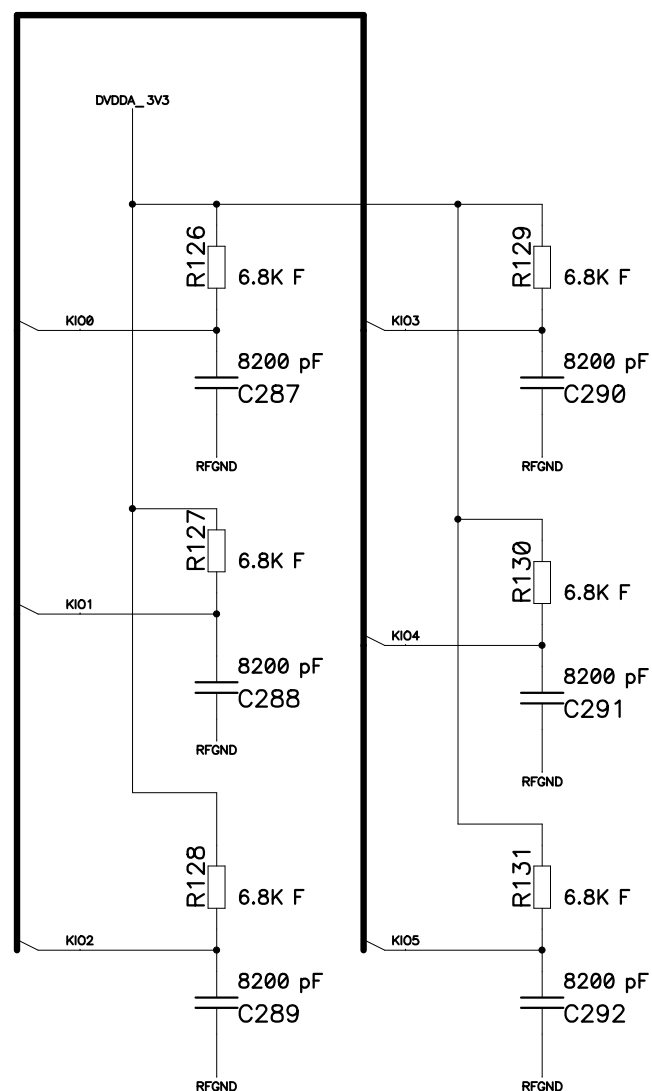
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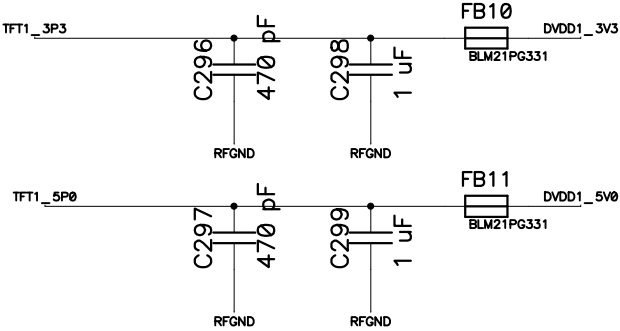
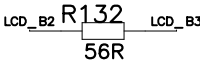
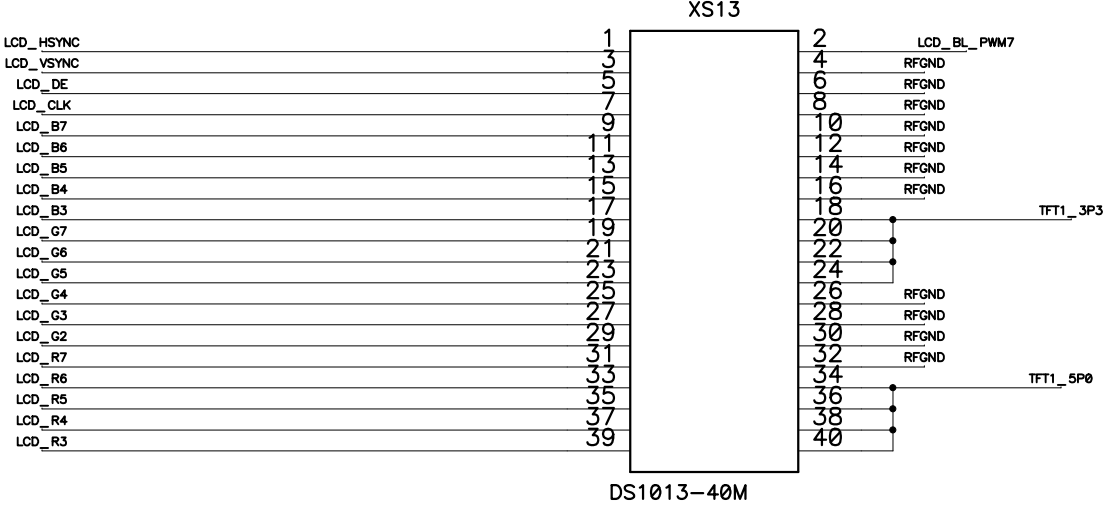
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DE MODE: MODE=1, HSYNC & VSYNC tie high



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