DE0-CV Pin Assignments
Cyclone V 5CEBA4F23C7N

Toggle switches

Switch	SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
Pin#	AB12	AB13	AA13	AA14	AB15	AA15	T12	T13	V13	U13

Pushbuttons

Button	Reset_N	Key3	Key2	Key1	KEY0
Pin#	P22	M6	M7	W9	U7

Red LEDs

LED	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
Pin#	L1	L2	U1	U2	N1	N2	Y3	W2	AA1	AA2

7-Segment displays

Digit	HEX5	HEX4	HEX3	HEX2	HEX1	HEX0
a	N9	U20	Y16	Y19	AA20	U21
b	M8	Y20	W16	AB17	AB20	V21
c	T14	V20	Y17	AA10	AA19	W22
d	P14	U16	V16	Y14	AA18	W21
e	C1	U15	U17	V14	AB18	Y22
f	C2	Y15	V18	AB22	AA17	Y21
g	W19	P9	V19	AB21	U22	AA22

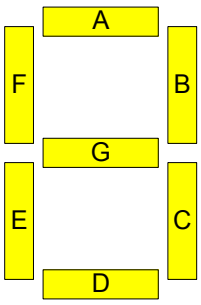

Table 3-6 Pin Assignment of Clock Inputs

Signal Name	*FPGA Pin No.*	*Description*
CLOCK_50	**PIN_M9**	**50 MHz clock input(Bank 3B)**
CLOCK2_50	**PIN_H13**	**50 MHz clock input(Bank 7A)**
CLOCK3_50	**PIN_E10**	**50 MHz clock input(Bank 8A)**
CLOCK4_50	**PIN_V15**	**50 MHz clock input(Bank 4A)**

DE0-CV Pin Assignments

Expansion Headers (board view)

GPIO 0
JP1

N16	1	2	B16
M16	3	4	C16
D17	5	6	K20
K21	7	8	K22
M20	9	10	M21
VCC5	11	12	GND
N21	13	14	R22
R21	15	16	T22
N20	17	18	N19
M22	19	20	P19
L22	21	22	P17
P16	23	24	M18
L18	25	26	L17
L19	27	28	K17
VCC33	29	30	GND
K19	31	32	P18
R15	33	34	R17
R16	35	36	T20
T19	37	38	T18
T17	39	40	T15

Expansion Headers (board view)

GPIO 1
JP2

H16	1	2	A12
H15	3	4	B12
A13	5	6	B13
C13	7	8	D13
G15	9	10	G17
VCC5	11	12	GND
H18	13	14	J18
J19	15	16	G11
H10	17	18	J11
H14	19	20	A15
J13	21	22	L8
A14	23	24	B15
C15	25	26	E14
E15	27	28	E16
VCC33	29	30	GND
F14	31	32	F15
F13	33	34	F12
G16	35	36	G15
G13	37	38	G12
J17	39	40	K16