A 500MSPS 8-bit ADC Card based on Time-interleaving Technique

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Abstract: Time interleaving technique is a significant trend in performance enhancement for high-speed ADC systems. This paper presents an ADC card based on time-interleaving technique. The system uses two 8-bit ADCs in parallel. Each ADC can sample at 250 MHz and the total sampling speed will theoretically becomes 500 MSPS. In an approach to increase the system's performance, a calibration algorithm is developed to suppress spurs due to channel mismatches. This paper is also concerning hardware design features that give the system good performance and practicality. A VGA amplifier provides the system with programmable full scale range adjustment. Up to 1Gbit data buffering solution is applied using a high bandwidth, low cost DDR-SDRAM. And the utility of FPGA, in which LVDS receiver, DDR-SDRAM controller and PCI controller are implemented, simplifies the circuit and brings down power consumption as well as the cost.

Key words: ADC, time-interleave, high speed, high capacity, PCI card

1 Introduction

High-speed analog-to-digital-converter (ADC) systems are needed in many areas, such as physics experiments and telecommunications. It's difficult for a monolithic ADC to have both the features of high bandwidth and high resolution. Existing ADC chip may not meet the requirement of some ultra high-speed A/D convert applications. Furthermore an ultra high-speed ADC chip is costly and asks for highly sophisticated periphery circuits, which also increases cost of system. Time-interleaving technique, one of the applications of multi-order sampling [1], employs the concept of running m ADCs at a sample rate that is $1/m$ of the overall system sample rate. It could be used to achieve high converting rate and high resolution with relative low speed ADC chips at reasonable cost.

Unfortunately, three types of mismatches, gain, offset and sample timing mismatches, between the individual channels of a time-interleaved ADC system cause system degradation. All these mismatches decrease spurious-free dynamic range of the ADC system and degrade the signal to noise and distortion ratio [2][3]. Fine-adjust circuit would reduce the influence of mismatches but increase the design difficult and may be not suitable for ultra high-speed application. Digital signal processing filters [4] can also eliminate the drawback caused by these mismatches. Compared with hardware circuits, digital filters are easier and more flexible to implement

We deduced a two-channel-mismatch-error correcting algorithm based on the architecture of hybrid analysis/Synthesis filterbanks [5][6].And a two-channel interleaved ADC system was constructed. It consists of two 250MSPS 8-bit ADC chips and achieves 500MHz sampling rate. The system is featured with adjustable full-scale range and high-capacity data buffering using DDR-SDRAM. Techniques of high-accuracy clock distributor and LVDS serial-to-parallel convert in FPAG are also used in the system for a better performance.

2 Correcting Algorithm

The algorithm treats the values of three mismatches as the parameters of digital filters to correct the sampling result. Since these mismatches are constants after the Printed Circuit Board is made, we only need to measure them for one time to construct the filters of algorithm.

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First, we concern ourselves about the correction of sampling time mismatches, most complex part. The processing algorithm can be illustrated with Fig.1.

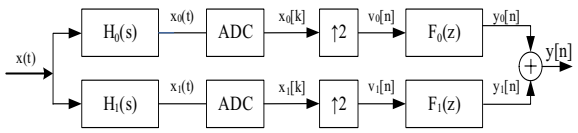


Fig.1 Filterbanks for two-channel timing mismatch correction

Sampling period of each ADC is $2T_s$. Phase difference between two sampling clocks is ideally T_s. In practice it is Δt bigger than T_s. We can use two analysis filters $H_0(j\omega)$ and $H_1(j\omega)$ to model the time-interleaving sampling:

$$H_0(j\omega)=1 \ , \ H_1(j\omega)=e^{j\omega(T_s+\Delta t)} \quad (1)$$

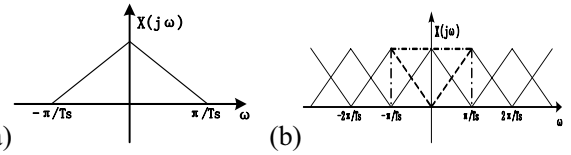
Analog input x(t) passes analysis filters $H_0(j\omega)$ and $H_1(j\omega)$. The output of them, $x_0(t)$ and $x_1(t)$ are sampled by ADC. The digital results are up-sampled by a factor of 2, and then filtered by $F_0(z)$ and $F_1(z)$ which together correct for timing mismatch. Uniformly spaced samples y(n) of the ADC input is given by adding the outputs of $F_0(z)$ and $F_1(z)$.

Consider x(t) as a band-limited signal which is non-zero in 1st Nyquist band, as shown in Fig.2 (a) . Ignoring quantization error, the Fourier transform of the output sequence y(n) can be written as [7]:

$$Y(e^{j\omega})=\sum_{p=-\infty}^{+\infty}T_p(j\omega)X\left(j\omega-j\frac{\pi p}{T_s}\right) \quad (2)$$

where

$$T_p(j\omega)=\frac{1}{2}\sum_{m=0}^{1}F_m(e^{j\omega})H_m\left(j\omega-j\frac{\pi p}{T_s}\right) \quad (3)$$



(a) (b)

Fig.2 (a) A band-limited input signal.

(b) The copies of input signal's frequency spectrum.

As shown in Fig. 2 (b), input signal's frequency spectrum is copied at π p/T_s, p =±1, ±2, … .

In [6] the method of perfect reconstruction filter calculation is given. Apply it to two-channel model, we have

$$\begin{cases} F_0(e^{j\omega})+F_1(e^{j\omega})H_1\left(j\omega+j\pi/T_s\right)=0, & p=-1 \\ F_0(e^{j\omega})+F_1(e^{j\omega})H_1(j\omega)=2, & p=0 \end{cases}, \ -\frac{\pi}{T_s}<w<0 \quad (5)$$

$$\begin{cases} F_0(e^{j\omega})+F_1(e^{j\omega})H_1\left(j\omega-j\pi/T_s\right)=0, & p=1 \\ F_0(e^{j\omega})+F_1(e^{j\omega})H_1(j\omega)=2, & p=0 \end{cases}, \ 0<w<\frac{\pi}{T_s}$$

(6)

For a time-interleaved sampling with timing error, combining (`) and (5), (6) gives us:

$$F_0(e^{j\omega})=\frac{e^{-j\frac{\pi\Delta t}{2T_s}sign(\omega)}}{\cos\left(\frac{\pi\Delta t}{2T_s}\right)} \ , F_1(e^{j\omega})=\frac{e^{-j\omega T_s}e^{-j\omega\Delta t}e^{-j\frac{\pi\Delta t}{2T_s}sign(\omega)}}{\cos\left(\frac{\pi\Delta t}{2T}\right)}, |w|<\pi/T_s \quad (7)$$

(7) is what we need to implement correction algorithm. Their Inverse Fourier transforms:

$$f_0(n)=\frac{2\sin\left(\pi n/2\right)\sin\left(\pi(\lambda-n)/2\right)}{n\pi\sin\left(\pi\lambda/2\right)} \ , f_1(n)=\frac{2\sin\left(\pi n/2\right)\sin\left(\pi(n-\lambda)/2\right)}{\pi(n-\lambda)\sin\left(\pi\lambda/2\right)} \quad (8)$$

where $\lambda=(T_s+\Delta t)/T_s$

Here we complete correction of timing mismatch of two channels. For the gain mismatch and offset mismatch, we can eliminate their influences by simply addition and Multiplication to get the fully correcting algorithm which is shown in Fig.4

$$O=Offset_0-Offset_1, \ G=Gain_0/Gain_1 \quad (9)$$

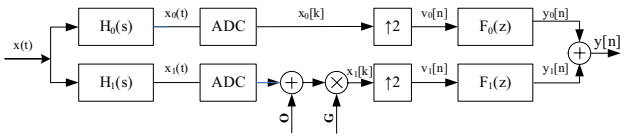


Fig.3 Processing algorithm for two-channel Time-interleaved ADC.

3 Hardware Design

While designing time-interleaved ADC system, we encounter two problems which do not exist in normal ADC design: generating accurate multi-phase clocks for sampling and synchronizing data from different channels to form the right sampling result. Like in normal ADC, high speed data transmission and buffering are still challenges. A solution based on PLL and clock distributor is applied to generate multi-phase clocks. As to data transmission, we turn

to new FPGA deserializing technique to reduce data rate for data transmission rather than deserializer chip, which also dealing with the problem of data synchronization. And DDR-SDRAM solution that is featured with high bandwidth, high density, low power and low cost is applied to data buffering.

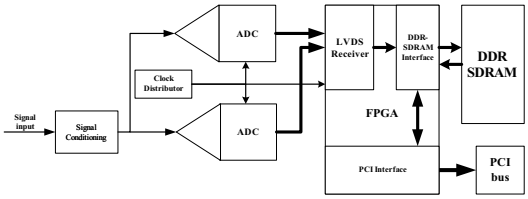


Fig.4 Block diagram of the overall system

Our time-interleaved ADC system consists of two monolithic ADC chips manufactured by ADI Company, AD9480, which is an 8-bit ADC with 250MSPS conversion rate. Two ADC chips operate in time-interleaving way. The digital data is buffered with a DDR-SDRAM and accumulated and then transferred to the computer through PCI interface. Fig.4 is the block diagram of the whole system. There are three main parts besides two ADC chips: signal conditioning, clock distributor and digital data buffering.

1) Signal Conditioning:

A single-ended analog input is driven into three cascaded differential amplifier for signal conditioning. First it is converted to a differential signals by a full differential amplifier. Then it is amplified or attenuated to 1Vpp by a variable-gain-amplifier (VGA) to be suitable for ADC chip's voltage reference. At last it is split to the two ADC chips by an ADC driver. Because of VGA, our system have programmable Full-Scale Range from 0.2V for 2V with acceptable performance.

2) Clock Distributor:

High accurate multi-phase clocks are extremely important for time-interleaved ADC applications. In our application, clock jitter is critical to the system's SNR performance [8] and clock skew to system's SFDR [2]. Though the effect of clock skew can be eliminate by correcting algorithm theoretically, too big a skew cannot be corrected well in practice because it needs high order filters. Therefore we should center our attention on minimizing clock jitter and skew.

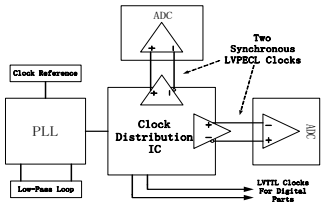


Fig.6 Block diagram of clock distributor

A phase-locked loop (PLL), ADF4360-2, and a clock distribution IC, AD9514, are used to generate multi-phase clocks. The circuit is illustrated in Fig.6 AD9514 divides the 1GHz differential clock generated by ADF4360-2 by a set integer of 4 and provides two 250MHz synchronized LVPECL clocks for two ADC chips. The two LVPECL clocks both have a duty-cycle of 50% and one of them is connected to ADC reversely. So we get two 250MHz sampling clocks with 180-degree phase difference for two-channel time-interleaved ADC system. AD9514 also provides another two LVTTL clocks for digital parts of the system.

The two chips are suited for data converter clocking applications where maximum converter performance is achieved by encoding signals with subpicosecond jitter. During PCB layout, in order to minimize clock skew we match the lengths of two ADCs' clock traces, as well as the two analog signals' trace lengths from ADC driver to ADC chips. Test shows that the timing mismatch between two ADC is about 40.5ps, which can be easily dealt with by correcting algorithm.

3) Data Transmission and Buffer:

A high-speed of 500MByte/s data rate, high-capacity, low cost storage scheme is applied for the system. A FPGA, Altera's CycloneII, and a DDR-SDRAM, Micron's 46V64M16, are chosen to constitute the circuit. In the FPGA, as shown in Fig. three logic components are implemented: LVDS receiver, DDR-SDRAM interface and PCI interface.

First the ADCs' sampling data is fed into LVDS receiver, where the two channels' data is synchronized and ordered. Fig.7 (A) illustrates how this receiver logic works and (B) is the timing diagram of the logic.

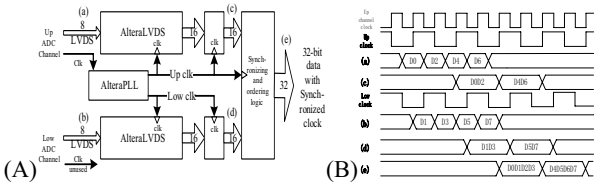


Fig.7 Illustration of LVDS receiver function

Each ADC's 8-bit-parallel output is fed into an AlteraLVDS megafuction for serial-to-parallel convert. The AlteraLVDS outputs 16-bit-parallel data at half the original data rate and maintains its phase. Then a logic is implemented to synchronize the phase-different data of two channels and arrange the data in sampling order. Finally a 32-bit-parallel data with 125MHz rate is ready for buffering. In the part of logic an AlteraPLL megafuction, which drives the PLL integrated in FPGA, is used to get clocks that logic needs.

DDR-SDRAM interface consists of two logic parts, as shown in Fig.8. One is an Altera IP Core, named DDR-Controller. This part handles the complex aspects of using DDR- SDRAM, translating command request from local interface into all the necessary SDRAM command signals. It's called megacore part. The other part offers the megacore part command request and interfaces with other logics of FPGA. It is called local part. In our system the local part exchanges data with LVDS receiver and PCI interface.

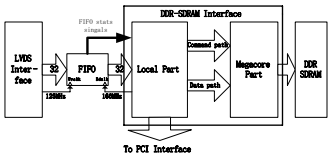


Fig.8 DDR-SDRAM controller logic diagram

The ddr-local's data bus width matches LVDS receiver's 32bit output, while its operation frequency is 166MHz, rather than 125MHz. Since the average data transmission rate should be bigger than 125MHz in order to avoid data lost, the controller's efficiency should be 125/166=75.3% at least. In practice, we write data into DDR-SDRAM with long burst. Under this circumstance the writing efficiency is up to 90%, which makes sure of no data lost. Experiment shows that none error occurs.

4 Test Result

We test the ADC system after it is finished. The frequency spectrums of 50MHz sine wave are shown in Fig.9 (A) is its spectrum without using mismatches-correcting processing algorithm, and (B) with. Additive tones caused by the mismatches are

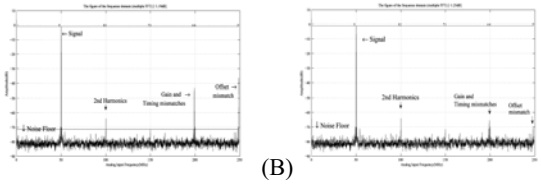


Fig.9 Frequency spectrum of 50MHz sine-wave.(A) original data, (B) is after processing.

depressed after processing. ENOB increases from 5.81 before processing to 7.32 after processing.

According to Fig.10 (A), while frequency of input sine-wave varies, time-interleaved result is almost the same as the worse single-channel result of the two channels. That means the processing algorithm produces desired effects on all signals less than half Nyquist frequency. ENOBs of both channels and overall system are above 7.0 when the sine-wave is below 100MHz, but decrease while sine-wave frequency increases. This is because of poor second and third harmonic distortion characteristics of ADC driver [9] in signal conditioning circuit, as shown in Fig.10 the right. This is a defection of our system and needs to be improved by selecting more suitable amplifiers for signal conditioning.

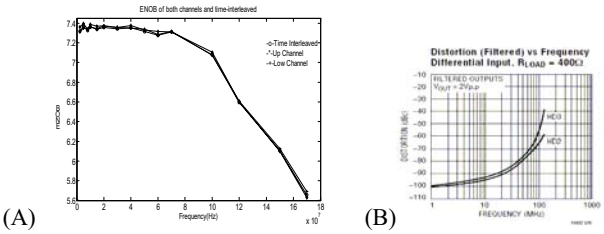


Fig.10 (A): ENOB of each channel and the overall system (B): 2nd Harmonic and 3rd harmonic of ADC diver

5 Conclusion

We succeeded in applying time-interleaving concept in high-speed ADC application and made an

ADC system of 500MHz converting rate out of two ADC chips operating at half of that rate. Our system doesn't suffer the drawback of time-interleaving ADC owing to its corresponding mismatch-error correcting algorithm. High-speed data transmission and high-capacity low-cost data storage techniques are used and the whole system is implemented on a PCI card, which makes the system an applicable one for many areas. It could be a reference for designing higher bandwidth and resolution ADC system beyond monolithic ADC chip restriction.

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Author Biographies

Zhou Hao was born in Sichuan, P.R.China, in 1981. He is currently purchasing the Ph.D. degree in physical electronics at University of Science and Technology of China. His current research interests include theory, design and implementation of high-speed analog to digital converting system and analog and digital signal processing.

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