Track-and-Hold Techniques for Ultra High Speed Time-Interleaved ADCs

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***Abstract*—A hierarchical time-interleaved (TI) track-and-hold (T&H) circuit for an ultra high speed analog-to-digital converter (ADC) is presented. The circuit is designed as a front-end for an 8b 32GS/s 16-way time-interleaved analog-to-digital converters (ADCs) using a 40nm CMOS process. The input and output buffers of the sampled signals are designed in response to the demand of time-interleaving, and the output buffer is a PMOS source-following structure with common mode compensation in order to balance the requirements of bandwidth and common mode. The circuit has an ENOB of 8.77 bits and an SFDR of 55.86 dB at the Nyquist input frequency.**

Keywords—time-interleaved ADCs, hierarchical sampling, track-and-hold circuit, common mode compensation

I. INTRODUCTION

With the continuous development of integrated circuit manufacturing technology and 5G technology, communication systems are demanding higher and higher speed, and the demand for high-performance analog-to-digital converters (ADCs) in military and civil fields is increasing day by day. With the development of integrated circuit processes, the limitations of single-architecture ADCs have become more apparent. To have a faster sampling rate, higher accuracy, and wider input range at the same time, the time-interleaved ADCs scheme is a more ideal choice. When time-interleaved ADCs were first proposed, the sampling rate was only 2.5 MHz. Time-interleaved ADCs of tens of GHz are common today, and it is foreseen that time-interleaved ADCs will continue to be an important research area in the future.

Time-interleaved ADCs are implemented by multiple ADCs being multiplexed in time and running in parallel [1]-[3]. The sample and hold circuit of a time-interleaved ADCs usually has two structures, a simple parallel structure, and a hierarchical time-interleaved structure as proposed in [4]. The performance of interleaved ADCs can be maximized by choosing a suitable interleaved structure. The T&H circuit proposed in this paper uses a two-stage hierarchical time-interleaved structure to achieve a sampling bandwidth of 32 GS/s.

The paper is organized as follows. Section II describes the basic structure of the time-interleaved ADCs circuit; in Section III, the circuit implementation details are presented; Section IV shows the layout and simulation results; finally, Section V draws the main conclusions of this work.

II. BASIC OF TIME-INTERLEAVED ADCS

A. Time-Interleaved ADCs Architecture

The single-channel ADC design has reached its limit with the current process and design level, and the time-interleaved structure is one of the most effective methods to break the ADC conversion rate bottleneck [5], [6]. To break the upper limit of the speed of a single ADC, multiple ADCs can be combined to work in alternating sampling cycles to achieve multiplication of the conversion rate, as shown in Figure 1.

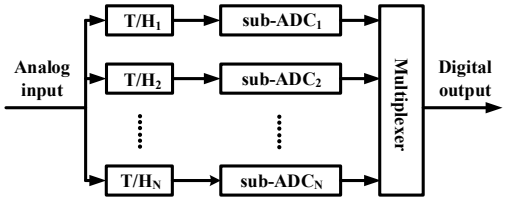

Fig. 1. Time-interleaved ADCs architecture

The timing relationship between two stages in a hierarchical interleaved architecture is very important, where N sub_ADCs are interleaved and sampled sequentially under the control of the clock. The timing diagram of the multiplex ADC is shown in Figure 2. At the falling edge of the master clock, one of the channels goes from tracking mode to hold mode and samples the input signal. The sampling rate of each single channel ADC is f_s, the Mux module uses the output of each single channel ADC as the digital output of the system in order of sampling, and the overall sampling rate of the system is $f_s \times$

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N. This is the basic working principle of Timing-Interleaved ADCs.

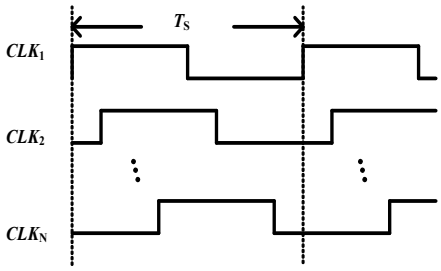

Fig. 2. Timing diagram of a time-interleaved ADCs

B. Mismatches of Time-Interleaved ADCs

If the TI-ADC channels are perfectly matched to each other, the SNDR of the interleaved system does not drop and its operating rate can be increased exponentially. Due to the existence of random mismatch and voltage variations, the sub-ADCs cannot have the same characteristics. There will be parameter mismatch between multiple sub-ADCs of the time-interleaved ADCs architecture, which mainly includes inter-channel mismatch (offset), inter-channel gain error mismatch (gain mismatch), and sampling time interval error (timing skew), as is shown in Figure 3.

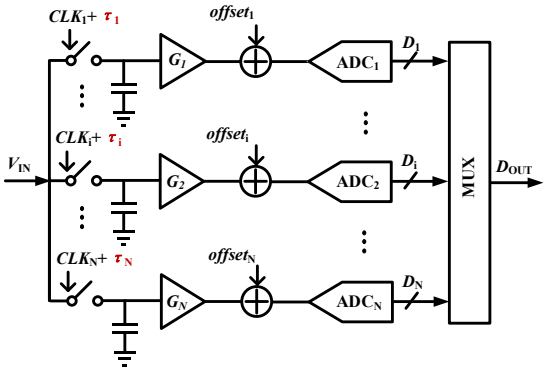

Fig. 3. Mismatch of TI-ADC

The i-th channel has $b_i(n)$ as its detuning, $g_i(n)$as its gain, and τ_i as its sampling time error. then the output of this channel is

$$y_i\hat{}(n)=\sum_{k=-\infty}^{k=+\infty}[x(n)*g_i(n)+o_i(n)]*_i\,\delta(n-kN-\frac{\tau_i}{T_s}) \quad (1)$$

Gain mismatch and offset have been extensively studied [7], [8]. Inter-channel offset and gain mismatch are often referred to as static errors and are ideally independent of the input signal. However, these two errors are affected by the frequency of the ADC input signal in practical applications. In a multi-channel time-interleaved ADCs architecture, the channel-to-channel offset mismatch and gain mismatch fluctuate with the input signal frequency, and the error fluctuation trend varies from channel to channel. This means that each channel may have a different transfer function, which leads to bandwidth mismatch.

III. High-Speed Front-End Sampler Implementation

A. 4×4 Hierarchically Time-Interleaved T&H

In the design of time-interleaved ADCs, the selection of the number of channels and architecture is an important task. When the number of channels is small (≤8), a two-stage interleaving architecture (A×B) is usually used. When the number of channels is high, the number of parallel switches is higher when using two-stage interleaving architecture, which will increase the input capacitance of node Vi and reduce the system bandwidth. In this case, the two-stage interleaving can be changed to three-stage interleaving to reduce the number of parallel switches at the input.

The purpose of this paper is to design a time-interleaved track-and-hold circuit with a 32GS/s sample rate, setting a single channel to operate at a rate of 2GHz. As shown in Figure 4, a differential CMOS structure was chosen for the sampling switch. CMOS sampling switches are fast and can somewhat reduce the charge injection at the moment of switch closure. The sampling transistor size, common mode and input signal swing are optimized for high bandwidth and high linearity across process corners.

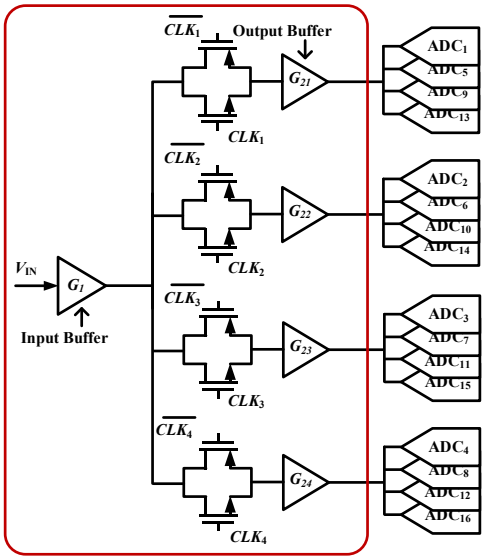

Fig. 4. Architecture of the 4×4 Time-Interleaved T&H

In the case that the single channel rate is determined, the system sampling rate can only be increased by increasing the number of interleaved channels. The design of this paper can be considered as a 2×8 or 4×4 interleaving architecture. In the 2×8 interleaving architecture, the first stage clock frequency is faster and there are only two key clocks with 50% duty cycle; in the 4×4 interleaving architecture, there are four key clocks with 25% duty cycle. The first stage sampling time is 30ps in both architectures, but the sub_ADC has more sampling time in the 4×4 interleaving architecture.

The sampling period of the ADC is $t_s=1/f_s$, where the f_s is the sampling frequency of the ADC. N_1 is the number of sampling switches, $N_{1,c}$ is the number of sampling switches turned on at the same time [9], and $t_{h,d}$ refers to the hold time of the signal before going into the sub_ADC. For the two-stage interleaved structure, the sampling time of the sub_ADC is

$$t_{h,d} = \begin{cases} (N_1 - N_{1,c})t_s & for\ N_1 \geq 2 \\ \frac{1}{2}t_s & for\ N_1 = 1. \end{cases} \quad (2)$$

This design uses a 4×4 interleaved architecture, as shown in Figure 4. Figure 5 shows the working timing of the structure, and it can be seen that the sub_ADC works alternately under the control of the first stage clock to achieve a doubling of the speed.

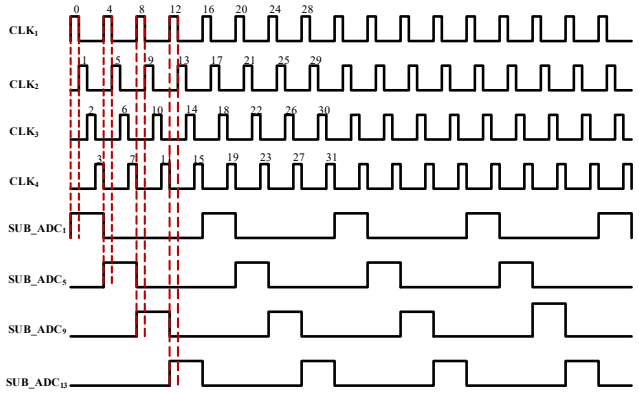

Fig. 5. Timing diagram of the 4×4 TI ADC

B. Buffer Circuit Design

The role of buffer in the design of multi-channel interleaved high-speed ADC systems is critical. In addition to the input buffer usually required between the analog input and the sample switch of the system, the output buffer is also required before the sample signal enters the sub_ADC. The design of the buffer needs to take into account the bandwidth and system common mode requirements.

The input buffer has high requirements for bandwidth, and a source follower structure is used in the design of this paper [10], whose basic structure is shown in Figure 6. The driver circuit usually requires high input impedance and low output impedance to isolate the charge injection from the sampling switch.

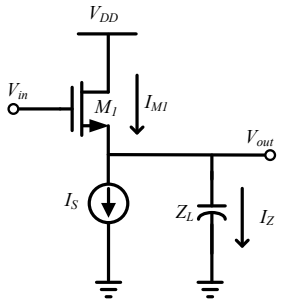

Fig. 6. Basic structure of NMOS source follower

The gain expression is shown in Equation (3).

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m1}(Z_L // r_{ds1})}{1 + g_{m1}(Z_L // r_{ds1})} \quad (3)$$

g_{m1} is the transconductance of M1 and r_{ds1} is the output resistance of M1. The main source of the source follower nonlinearity is the variation of the load current. The current flowing through the source follower is the sum of the DC bias current I_{M1} and the load current I_Z. As the circuit operates in a large signal state, the load current varies with the input signal swing and makes the transfer function correlate with the input signal V_{in}, thus causing nonlinear distortion. To achieve high linearity, the input common-mode of the source follower needs to be raised, while its output common-mode also defines the common-mode of the interleaved sampling switch. This requires the output buffer to coordinate the common-mode of the signals coming into the sub_ADC.

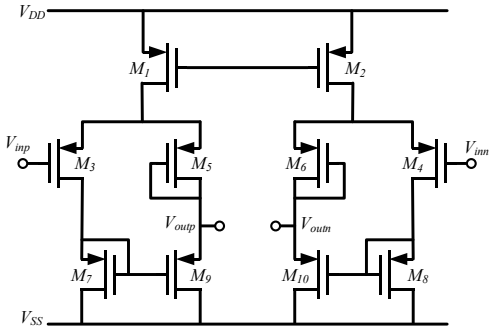

Fig. 7. Source follower with common mode compensation

The output buffer connects the sampled signal and sub_ADC, and it is necessary to adjust the signal common-mode so that it can meet the working conditions of a single channel, provided that its bandwidth meets the working requirements. this paper adopts the PMOS source following structure with common mode compensation, as shown in Figure 7. v_{cm_inp} is the signal common mode at the input of this buffer, v_{cm_outp} is the common mode of the signal at the output of the buffer, V_{GS3} is the gate-source voltage of M3, V_{GS5} is the gate-source voltage of M5, and their relationship is given by Equation(4).

$$V_{CM\_outp} = V_{CM\_inp} + V_{GS3} - V_{GS5} \quad (4)$$

The basic PMOS source-following structure will raise the common mode of the signal. In this design, the common mode compensation circuit is added to reduce the signal common mode, and the change of common mode can be controlled by changing the operating current and MOS size, but this structure will also bring an increase in power consumption.

IV. Layout Design and Simulation Results

The 32GS/s time-interleaved track-and-hold circuit designed in this paper was designed and implemented in 40nm CMOS technology, and the circuit design were done with Cadence Virtuoso software. Figure 8 gives the layout of the designed circuit, which has an area of 0.03 mm^2. In this layout, the differential input signal enters the input buffer from the left side of the chip and passes the signal sequentially to the right.

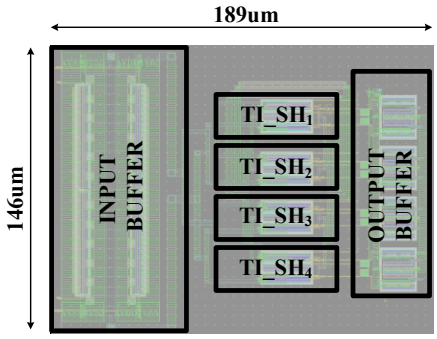

Fig. 8. Layout of the Time-Interleaved T&H

The output buffer, as an important connection circuit in this design, has the ac frequency characteristics shown in Figure 9(a), and a common mode shift of about 150mv between the output signal and the input signal can be seen in Figure 9(b).

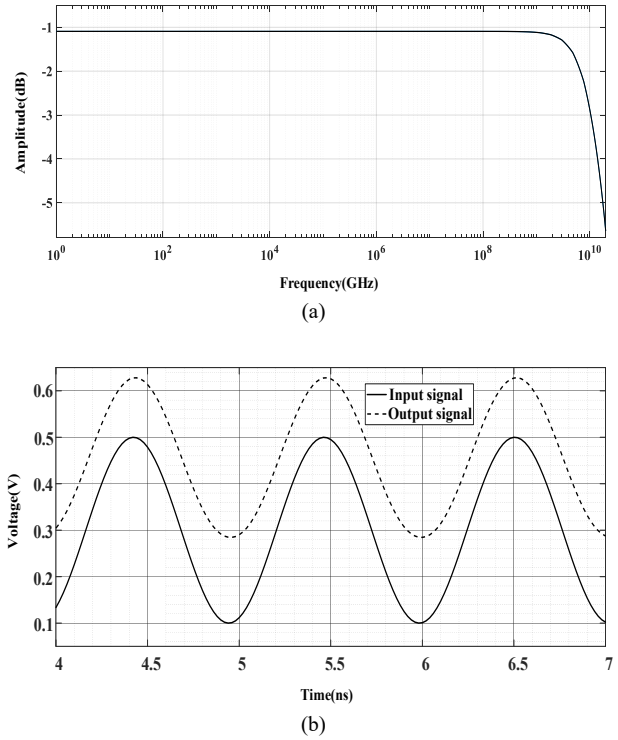

Fig. 9. (a) Ac frequency characteristics (b) Common mode shift

The time-interleaved sampling circuit with a sampling rate of 32GS/s, the input signal swing is 400mVpp. and the output spectrum of the input signal near Nyquist frequency is shown in Figure 10(a), which shows that the ENOB is 8.77 bits and the SFDR is 55.86 dB. The curve of ENOB with the input frequency is shown in Figure 10(b).

Table I shows the comparison between the track-and-hold circuit designed in this paper and other time-interleaved track-and-hold circuits. It can be seen that the circuit designed in this paper has a high sampling rate and good linearity in the same field.

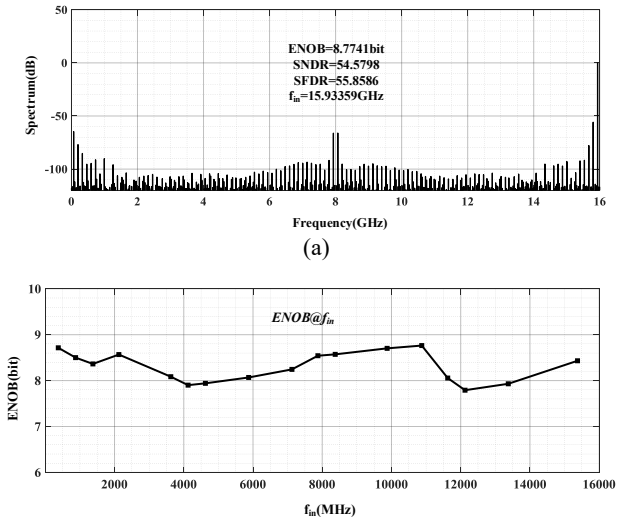

Fig. 10. (a)Output spectra with frequency near Nyquist (b)ENOB vs input frequency.

TABLE I. PERFORMANCE COMPARISON

Reference	[1]	[2]	[3]	This work
Process	45nm CMOS_SOI	65nm CMOS	32nm CMOS_SOI	40nm CMOS
Supply (V)	2.5	3	1.5	1.1
Resolution (bit)	8	6	7	8
Sample Rate (GS/s)	40	32.5	34	32
SFDR (dB@ f_{in}GHz)	55@5	37.42@6	43.8@10	55.86@16

V. CONCLUSION

This paper presents an 8-bit time-interleaved track-and-hold circuit for ultra-high-speed ADCs using 40nm CMOS technology. The sampling frequency is 32 GS/s and the supply voltage is 1.1 V. The input and output buffer of the signal is also designed to meet the requirements of time interleaving, and the output buffer is designed as a PMOS source-following structure with common mode compensation to meet the requirements of bandwidth and common mode. According to the simulation results, the proposed time-interleaved sampling circuit has an ENOB of 8.77 bits and an SFDR of 55.86 dB at Nyquist input frequency, and the track-and-hold circuit has excellent performance at different frequencies with 400 mVpp input signal.

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