A Digital Timing Mismatch Calibration Technique in Time-Interleaved ADCs

Jing Li, *Student Member, IEEE*, Shuangyi Wu, *Student Member, IEEE*, Yang Liu, *Member, IEEE*, Ning Ning, *Member, IEEE*, and Qi Yu, *Member, IEEE*

***Abstract*—A digital calibration scheme is proposed to minimize the timing mismatch in time-interleaved analog-to-digital converters (TIADCs). First, the scheme is to subtract the outputs from adjacent channel ADCs and to utilize the expectations of the absolute value of the subtracted results to represent the actual sampling time interval. The timing mismatch is recognized by comparing these expectations. The obtained information is fed back to adjust variable delay buffers, thus reducing the timing mismatch. The application of this scheme to a 12-bit 1.6 GS/s four-channel TIADC is demonstrated. Simulation results show that with an input signal whose bandwidth is limited to the Nyquist frequency, the proposed timing mismatch calibration scheme is effective and capable of reducing the mismatch to the minimum. Compared with traditional calibration schemes, the proposed scheme is more feasible to implement and consumes less power and chip area.**

***Index Terms*—Digital calibration, time-interleaved analog-to-digital converter (TIADC), timing mismatch.**

I. Introduction

HIGH-RESOLUTION and high-speed analog-to-digital converters (ADCs) are necessary in communication systems such as 3 G/4 G wireless base stations and wideband communication systems. A single ADC with a traditional architecture cannot simultaneously achieve high resolution and high speed because of process limitations. Time-interleaved ADCs (TIADCs) can effectively increase the sampling rate f_s despite technology-imposed speed limitations, while high resolution can be maintained [1]. Hence, the use of TIADCs is an optimal approach in obtaining high-performance ADCs [2]–[8].

Considering process, voltage, and temperature variations, the channels in a TIADC are not identical and the performance of TIADC will be limited by offset, gain, and timing mismatches among the channels [9]. Among the three mismatches, offset and gain mismatches can be solved by digital calibration. However, timing mismatch is difficult to calibrate because of the difficulty to detect and to correct.

A number of recent studies have been conducted on timing mismatch mitigation. One option is to employ a front-end sampler [2]. Using a single sampling switch, the sampling moment of all channels is determined by a global clock, thus completely eliminating the timing mismatch. However, when the sampling rate f_s is in the Giga Hertz range, the speed of the sampling switch will become a bottleneck in normal CMOS processes. In [10] and [11], digital calibration methods were proposed, in which both detection and correction occurred in the digital domain. The calibration shows a negligible effect on the analog circuit, but may require high power and a large chip-area because of the use of finite-impulse response (FIR) filters. In [12], the author detected the timing error by counting the input zero crossings among samples. The calibration is achieved by digital logic at the cost of additional samplers in each channel. The mismatch among additional samplers results in a residual timing error. In [13], the author multiplied the outputs of the channels and utilized the dc component of the product to detect the timing mismatch. The method includes multiplication, which requires a large chip-area and leads to a high power consumption.

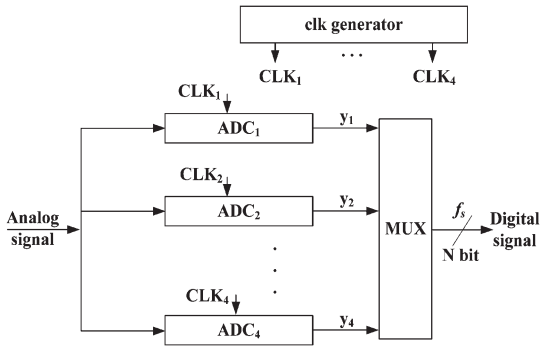

Fig. 1. Time-interleaved ADC block diagram.

In this brief, a digital calibration technique is proposed to detect and calibrate the timing mismatch. This method detects the timing mismatch by identifying the expectation of the absolute difference of the adjacent channel ADCs. Compared with the mean-squared-difference method in [11], this approach has less computational complexity because it does not require multipliers and FIR filters. In the analog field, this calibration maintains the status of the channel ADCs, except for the insertion of a group of delay buffers after the clock generators.

The rest of this brief is organized as follows: Section II introduces the principle of the proposed timing mismatch detection utilized in a four-channel TIADC. Section III describes the complete calibration scheme. Section IV provides the simulation results. Lastly, Section V states the conclusion.

II. Timing Mismatch Detection

To express the principle of the timing mismatch detection, a four-channel TIADC (Fig. 1) without offset and gain mismatches is considered as an example. The sample period and

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The authors are with the State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China (e-mail: yliu1975@uestc.edu.cn; qiyu@uestc.edu.cn).

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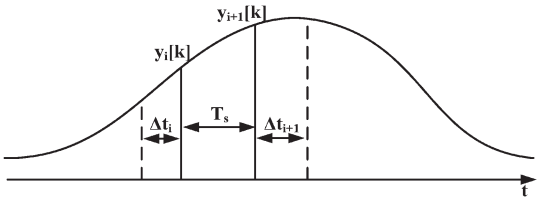

Fig. 2. Part of the sampling waveform of TIADC.

the frequency of the TIADC are T_s and $f_s = 1/T_s$, respectively. The analog input $V_{in}(t)$ is bandlimited from DC to 0.5 f_s and is assumed to be real-valued with zero mean. The output of the i-th channel can be expressed as

$$y_i[k] = V_{in,i}\left((kM+i)T_s + \Delta t_i\right) \tag{1}$$

where Δt_i is the timing mismatch, and the index i refers to the channel number $(\mathrm{i} = 1, 2, 3, \text{ and } 4)$.

As shown in the sampling waveform in Fig. 2, based on a linear approximation, the difference D_i of adjacent channels can be approximated as

$$\begin{aligned} D_i &= y_{i+1}[k] - y_i[k] \\ &= V_{in}\left((kM+i+1)T_s + \Delta t_{i+1}\right) - V_{in}\left((kM+i)T_s - \Delta t_i\right) \\ &\approx \left(T_s + \Delta t_{i+1} - \Delta t_i\right) \cdot V'_{in,i} \end{aligned} \tag{2}$$

where the lead time Δt_i is defined as negative; the delay time Δt_{i+1} is defined as positive; $T_s + \Delta t_{i+1} - \Delta t_i$ is the actual sampling time interval of adjacent channels; and $V'_{in,i}$ is the derivative of the input signal. The expectation of the absolute value of the differences A_i can then be derived as

$$\begin{aligned} A_i &= \lim_{N\to\infty} \frac{1}{N} \sum_{k=1}^{N} \left| y_{i+1}[k] - y_i[k] \right| \\ &\approx \lim_{N\to\infty} \frac{1}{N} \sum_{k=1}^{N} \left| \left(T_s + \Delta t_{i+1} - \Delta t_i\right) \cdot V'_{in,i} \right| \\ &= \left(T_s + \Delta t_{i+1} - \Delta t_i\right) \cdot \lim_{N\to\infty} \frac{1}{N} \sum_{k=1}^{N} \left| V'_{in,i} \right| \\ &= \left(T_s + \Delta t_{i+1} - \Delta t_i\right) \cdot E\left(\left|V'_{in,i}\right|\right). \end{aligned} \tag{3}$$

For a bandlimited signal with zero mean, the expectation of the absolute value of the signal $E(|V_{in}|)$ is constant, similar to the expectation of the derivative $E(|V'_{in}|)$ of the signal. When N increases toward infinity, the outputs of the channel ADCs exhibit the same statistical characteristics as those of the TIADC. This can be written as

$$E\left(\left|V'_{in,i}\right|\right) \approx E\left(\left|V'_{in,j}\right|\right) \approx E\left(|V'_{in}|\right) \tag{4}$$

where both i and j refer to the channel number and $\mathrm{i} \neq \mathrm{j}$.

By combining (3) and (4), the expectation A_i is proportional to the time interval of the adjacent channels. At the absence of timing mismatches $(\Delta t_i = 0)$, A_i will be equal for each channel. Otherwise, Ai will increase or decrease relative to the time interval as a result of the timing mismatch.

The scheme of using the expectation A_i to detect the timing mismatch is explained below. The timing mismatch detection scheme according to (3) is shown in Fig. 3. The expectation A_i is calculated depending on the output of the channel ADCs.

At the absence of timing mismatches $(\Delta t_i = 0)$, the differences D_i as shown in Fig. 4(a), will be close to one another. The

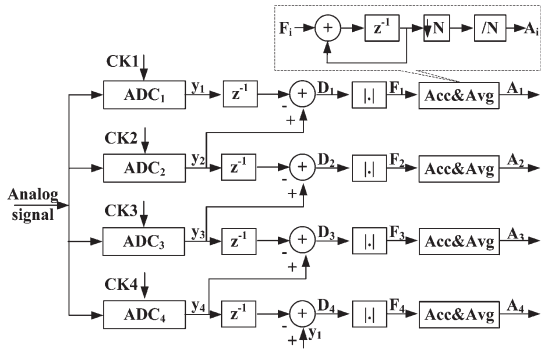

Fig. 3. Proposed timing mismatch detection scheme.

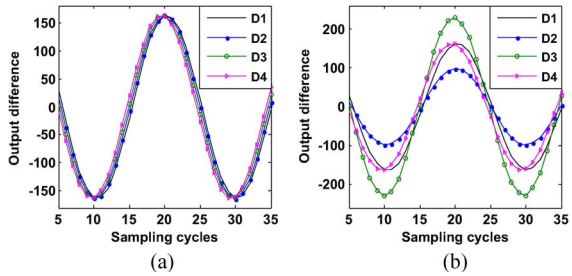

Fig. 4. Digital output difference as a function of sampling cycles: (a) without timing mismatch and (b) with timing mismatch in the third channel.

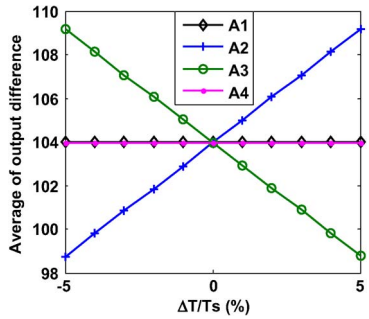

Fig. 5. Simulated expectations as a function of timing mismatch.

expectations A_i of the absolute value of the differences will be equal, as mentioned by (3).

At the presence of a timing mismatch ($\Delta t_3 = \Delta T$, ΔT is negative), the sampling instant of the third channel will occur before the ideal sampling instant. As a result, the time interval T_2 between the second and third channel will be less than that between the third and fourth channel. The other two time intervals, T_1 and T_4, remain unchanged. Consequently, the output difference D_2 is "skewed" because of ΔT, whereas D_3 is "skewed" in the opposite direction.

The simulation result with $\Delta T/T_s = 0.4$ is shown in Fig. 4(b). When comparing Fig. 4(a) to Fig. 4(b), it can be seen that the output differences of D_2 and D_3 are deviating from their nominal value due to the mismatch ΔT. The expectation A_2 will decrease whereas A_3 will increase, which is consistent with (3).

In Fig. 5, the expectations A_i are plotted as a function of $\Delta T/T_s$. When ΔT is zero, the expectations A_i are equal to each other, as analyzed above. Otherwise, when ΔT is negative or positive, A_2 and A_3 will change proportionally to ΔT in opposite directions.

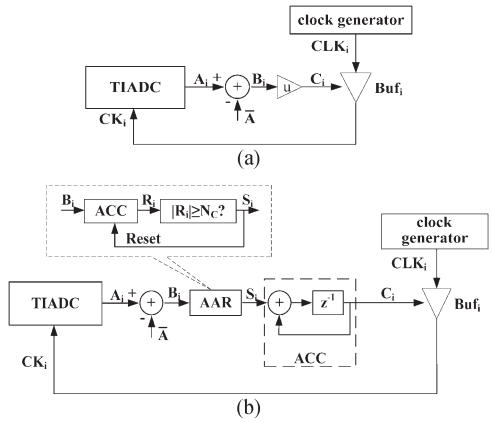

Fig. 6. Timing mismatch calibration loop: (a) Direct calibration loop and (b) Proposed calibration loop.

Thus, by calculating the expectations A_i based on the outputs of the channels, the timing mismatches can be determined.

III. Four-Channel Timing Mismatch Calibration

The expectation A_i is calculated based on the outputs of the ADC channels $y_i[k]$. With A_i as a function of the time interval of the adjacent channels, the sum of A_i represents one complete sampling cycle of four channels. In considering the mean value of expectations

$$\bar{A} = \frac{1}{4}\sum_{i=1}^{4} A_i \approx \frac{1}{4}E\left(|V'_{in}|\right)\cdot\sum_{i=1}^{4}(T_s + \Delta t_{i+1} - \Delta t_i). \quad (5)$$

As $\sum_{i=1}^{4}(T_s + \Delta t_{i+1} - \Delta t_i) = 4T_s$ for the TIADC, the mean value $\bar{A}$ can be simplified as

$$\bar{A} \approx T_s \cdot E\left(|V'_{in}|\right). \quad (6)$$

$\bar{A}$ is thus proportional to the standard time interval T_s, but uncorrelated with the timing mismatch Δt_i.

According to (3) and (6), the relevant timing mismatch between adjacent channels can now be extracted according to

$$B_i = A_i - \bar{A} \approx (\Delta t_{i+1} - \Delta t_i)\cdot E\left(|V'_{in}|\right). \quad (7)$$

Generally, if B_i is multiplied by a gain factor u, $u \cdot B_i$ can be fed back directly to the variable delay buffers to regulate the delay in real time, as shown in Fig. 6(a). The sampling clock CK_i will be adjusted to be advanced or delayed to reduce the timing mismatch. To ensure stability of the timing mismatch calibration loop, the first channel is not calibrated by signal C_1, but uses CK_1 directly as a reference clock.

This method achieves fast regulation at the cost of steady-state accuracy and power consumption. As previously discussed, the values of A_i equal each other according to (3). In a practical application, the values of A_i may not be completely the same because of statistical errors (caused by a finite number of observations), even at the absence of timing mismatches. B_i will always exhibit small variations, which will result in continuous, noisy regulation. In this way, B_i will behave as an additional random jitter on the sampling clock and will consequently affect not only the calibration accuracy but also the performance of the TIADC.

To reduce the effects of statistical errors, B_i is transmitted through an accumulation-and-reset (AAR) block, as shown in Fig. 6(b) [12]. The AAR block works as a low-pass filter. The output status of the AAR block only changes when $|R_i| \geq N_C$ (N_C is a positive integer). If the timing mismatch ΔT occurs in the third channel, B_2 and B_3 will contain the mismatch information, where B_2 will become negative and B_3 positive. Given the accumulation in the AAR, R_2 will continue to decrease until $-R_2 \geq N_C$, and the AAR will generate a negative value on S_2. R_3 will continue to increase until $R_3 \geq N_C$ and the AAR will generate a positive value on S_3. The calibration signals C_2 and C_3 are then updated by

$$\begin{cases} C'_2 = C_2 - 1 \\ C'_3 = C_3 + 1. \end{cases} \quad (8)$$

Correspondingly, Buf_2 reduces the delay time and advances clock CK_2. Buf_3 increases the delay time and delays CK_3. The time intervals of the adjacent channels are thus updated by

$$\begin{cases} T'_2 = T_2 - g_t \cdot \Delta C_2 + g_t \cdot \Delta C_3 \\ T'_3 = T_3 - g_t \cdot \Delta C_3 + g_t \cdot \Delta C_4 \end{cases} \quad (9)$$

where g_t is the delay time step of the buffers and $\Delta C_i = C'_i - C_i$. Consequently, the time interval T_2 increases, whereas T_3 decreases. After several calibration cycles, the timing mismatch ΔT will be reduced to the minimum.

Normally, the mismatches are not integer multiples of the time step g_t, such that the mismatch cannot perfectly reach zero. However, if the time step g_t is sufficiently small, the timing mismatch will approximate zero after calibration. In practice, it has been shown that minimum time steps of approximately 0.2 ps are feasible [8], [14].

The variable delay buffer is the bridge between the digital circuit and the analog circuit. It is normally used in timing mismatch compensation system [8], [12], [14]. Each variable delay buffer is composed by cascaded CMOS inverters. It may suffer from power supply noise and thermal noise, both of which will deteriorate jitter performance of the sampling clocks. However, the thermal noise jitter can be reduced by proper design and power supply noise jitter is mitigated by providing the power and ground line off chip. Thus, the impact of the variable delay buffers on jitter performance can be controlled to not be the main contribution.

The complete timing mismatch detection and calibration scheme is shown in Fig. 7. A clock generator is used to generate the 4 clocks $(\mathrm{CLK}_i, i = 1, 2, 3, 4)$ for the TIADC. The phase spacing of the adjacent clocks is 90°. The four-channel ADCs quantize the input signal and output the digital sequences y_i. Based on the digital sequences y_i, the proposed timing mismatch detector quantizes the time interval as A_i. By subtracting A_i from the standard time interval $\bar{A}$, the relevant timing mismatch B_i of each channel is derived. The AAR block is utilized to reduce the impact of statistical errors to improve calibration performance. Eventually, the calibration signals C_i (except for C_1) are fed back to the variable delay buffers to regulate the delay time of the corresponding sampling clock and subsequently achieve the calibration.

IV. Simulation Results

A behavioral model of a four-channel TIADC based on the proposed timing mismatch detection and calibration is designed

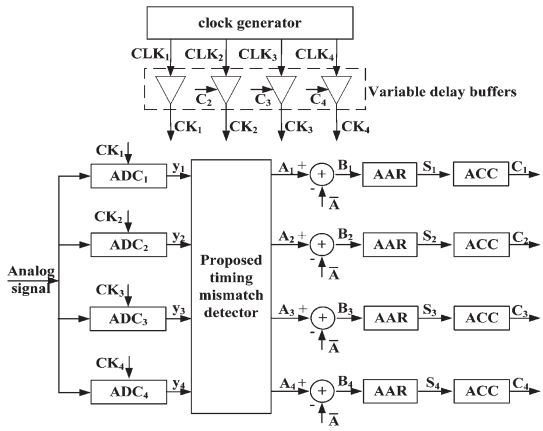

Fig. 7. Timing mismatch calibration loop for four channels.

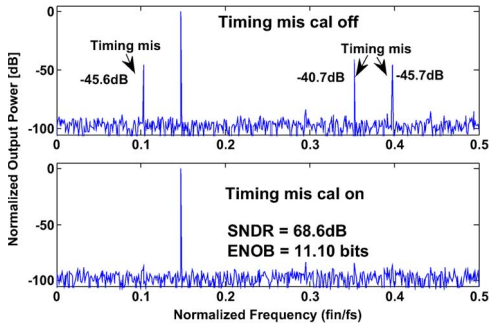

Fig. 8. Output spectrum of the TIADC.

and simulated using MATLAB. The sampling frequency of the TIADC is 1.6 GS/s, and the designed resolution is 12 bits. The sampling frequency of each channel ADC is 400 MS/s. The channel ADC is formed by a pipelined ADC with a sample-and-hold (S/H) circuit, four 2.5-bit multiplying- digital-to-analog converter (MDAC) stages, and a 3-bit flash ADC. Thereafter, $3‰$ random mismatches are added to the capacitors in all MDAC stages. The parasitic capacitor at the input node of the MDACs is set to be a quarter of the sampling capacitor. The DC gain of the amplifier in the S/H and in the first MDAC stage is designed to be 80 dB, and other MDAC stages are scaled down in sequence. The rms jitter of the sampling clock is set to 0.2 ps. The calibration scheme is ineffective in the presence of offset mismatch and gain mismatch. It is thus assumed that this method is applied after the calibration of offset mismatch and gain mismatch, for instance based on methods like [5]. To evaluate the performance of the proposed calibration method, it is assumed that there is no gain and offset mismatches between the channels in this work. For single-tone tests, the timing mismatch among the channels is assumed to have a standard deviation of $0.01T_s(T_s = 625$ ps).

The output spectra of the TIADC are shown in Fig. 8. The input signal is a full-scale 236 MHz sine wave. When the calibration is off, the distortions caused by timing mismatch appear at frequencies $(f_s/4 \pm f_{in})$ and $(f_s/2 - f_{in})$, limiting the signal-to-noise-and-distortion-ratio (SNDR) of the TIADC to 38.5 dB. After calibration, the distortions due to timing mismatch are minimized, and the SNDR is improved to 68.6 dB, which is close to the desired value of 68.8 dB when the timing mismatches are disabled.

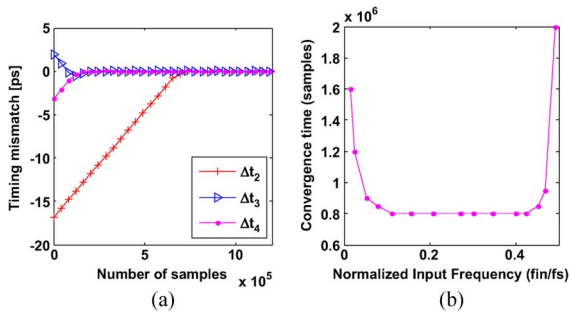

Fig. 9. Timing mismatch convergence time: (a) at $f_{in} = 236$ MHz and (b) versus input frequency f_{in}.

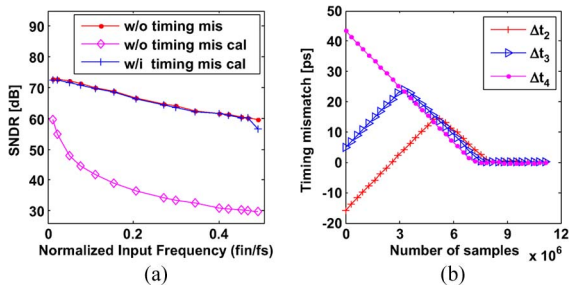

Fig. 10. (a) SNDR versus input frequency f_{in}; (b) Timing mismatch convergence time with phase-shift keying input signal.

The timing mismatch convergence process is shown in Fig. 9(a). With the clock of the first channel set as the reference clock, only the clocks of the other three channels are calibrated. Initially, the timing mismatches of the channels are at the maximum. During calibration, the timing mismatches are gradually reduced and reach their minimum after approximately 8×10^5 samples. Fig. 9(b) shows the convergence time versus the input signal frequency. For most frequencies, the convergence time is approximately 8×10^5 samples. The maximum time is approximately 2×10^6 samples and occurs when the input frequency is close to Nyquist.

Fig. 10(a) shows the SNDR versus the input frequency with the same timing mismatch as before. The first line shows the performance without timing mismatch. As a result of the sampling clock jitter and the nonlinearity in the S/H and MDACs, the SNDR decreases from 72.8 dB to 59.6 dB with increasing input frequency from DC up to Nyquist.

Fig. 10(a) also shows the performance in the presence of timing mismatch, both before and after calibration. Before calibration, the SNDR is inversely proportional to the input signal frequency as the timing mismatch has more influence for higher input frequencies. When the input signal frequency approaches Nyquist, the SNDR decreases to 28 dB.

When the timing mismatch calibration is enabled, the proposed scheme is able to compensate the timing errors. The SNDR remains close to the situation without timing mismatch in the entire Nyquist frequency range. When the input frequency is close to the Nyquist frequency, the calibration loop is still stable and able to minimize the timing mismatches. However, while A_i converges to $\bar{A}$, a residual error is remained due to statistical errors. This residual error can be neglected at lower frequencies, but results in a maximum static phase error of about 1 ps around the Nyquist frequency. Even so, after

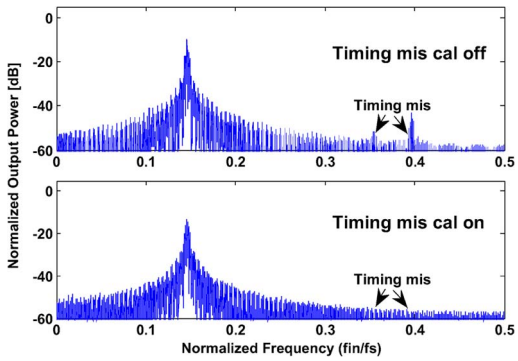

Fig. 11. Output spectrum of the TIADC with phase-shift keying input signal.

TABLE I
PERFORMANCE COMPARISON

	[10]	[11]	[13]	[15]	This work
Channels	4	16	2	2	4
Mismatch types	Gain, timing	Gain, offset, timing	Timing	Timing	Timing
Filter (taps)	82	/	0	31	0
# of adders	/	10^6	1	2	23
# of multipliers	/	10^6	2	2	0
Gate count	/	85k	/	/	5.3k
Convergence time (# of samples)	10^5	10^5	1.5×10^7	5×10^4	8×10^5
Area	2.9mm^2	2mm^2	/	/	0.075mm^2

calibration, the SNDR has been improved from 28 dB to 57 dB at Nyquist, which is only 2.6 dB lower than the ideal situation.

Furthermore, the proposed calibration scheme is verified with a modulated phase-shift keying input signal, as a realistic example of an actual application. The maximum timing mismatch is set to $0.1T_s$ to clarify the benefits of the algorithm. The input signal can be expressed as

$$V_{in}(t) = A \cdot cos(2\pi \cdot f_{in} \cdot t + 2\pi \cdot Anoise) \qquad (10)$$

where A is the amplitude of the signal; f_{in} is the carrier frequency (set to 236 MHz); $Anoise$ is a sequence of uniformly distributed pseudorandom numbers which are normalized to 2 bits (taking values 0, 1/4, 1/2 or 3/4). The update rate or symbol rate of $Anoise$ is set to 8.12 MHz. The timing mismatch convergence process is shown in Fig. 10(b). It is similar to Fig. 9(a) and proper calibration is achieved. The convergence time is approximately 1.1×10^7 samples. The output spectra of the TIADC are shown in Fig. 11. The noise floor is raised and the distortions induced by the timing mismatch are partially drowned by the noise floor. But similar with Fig. 8, the distortions caused by timing mismatches are minimized.

Table I summarizes the performance of this work as well as other references. The area and gate count of the proposed calibration logic are estimated with a 65 nm CMOS process.

In [10], [11], and [15], the authors use FIR filters to reconstruct the output signal and to reduce the timing mismatch. Although they may achieve a faster convergence time, a high number of taps is necessary in these filters as they determine the calibration resolution. In this brief, the timing mismatch is detected by identifying the expectation of the absolute difference and the compensation is realized in the analog domain. Complex signal processing is not required, and all logic operations depend on the addition operation. The method in [13] seems consuming less hardware but it is for two channels. It will be at the same level with ours for four-channel TIADC.

Without using filters and multipliers, the proposed calibration scheme consumes less chip area. The estimated area is 0.075 mm^2. The convergence time is approximately at 8×10^5 samples, which is at the same level as that of other calibration methods.

V. CONCLUSION

A digital calibration scheme is proposed to minimize the timing mismatch in TIADCs. By subtracting the output of the adjacent channels, the timing mismatch is determined and calibrated by digital logic. The proposed calibration technique depends on the output of the channel ADCs and avoids the influence on the analog circuit in ADC. The proposed scheme is effective within frequency range of 0–$0.47 \cdot f_s$. It may provide an area-efficient background calibration technique for timing mismatch in TIADC.

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