

Interleaving ADC Technique for Super-sampling using FPGA.

Proposal ideas.

This project aims to explore the operation and characteristics of the interleaving ADC technique in FPGA hardware for super-sampling, a critical requirement when digitizing analog signals (ADC) at rates beyond the capabilities of conventional hardware. The interleaving ADC technique is a promising approach that leverages parallelism to enhance the speed and accuracy of analog-to-digital conversion, making it well-suited for demanding applications in signal processing and data acquisition.

The goal of this project is to implement FPGA firmware to demonstrate the operation and characteristics of the interleaving ADC technique, commonly seen in modern high-speed applications that demand very high sample rate. For example, the RF-ADC module in RFSoc hardware interleaves four single-ADC to achieve a high sample rate at Gigahertz.

At the high-level architecture, the technique combines the output of multiple ADC modules, operating simultaneously, to effectively achieve a higher sample rate at the output. The first section of this study will address the benefits of the interleaving ADC technique in terms of hardware parallelism, higher sampling rate, and better data resolution.

The subsequent section of this study will analyze of the characteristics of this technique. Particularly, this section will explore the optimal configuration in terms of the appropriate number of input ADC dies and interleaving factor based on the hardware clock rate and the desired output rate. In addition, it will address how time and phase alignment affect the output data in terms of errors and interleaving spurs. Methodological approaches to overcome such error and noise effects are also included within this section of the study.

Procedures, Experiments.

An experiment will be conducted to demonstrate the process and success of this project. This experiment will implement an FPGA firmware that perform interleaving technique on 2 input ADC and provides the output sampling rate as doubled of the input rate. Each input ADC will be configured to sample at $f_{ADC_{in}} = 100MHz$, and the expected output is $f_{ADC_{out}} = 200MHz$. It is also expected to see some errors and interleaving spurs at the output signal, and such characteristics will be used for evaluating the effectiveness of this technique. This experiment will be conducted in Vivado simulation environment.

Conclusion.

In conclusion, the project should be able to address the operation and characteristics of interleaving ADC technique based on the theory analysis and experiment results. It should demonstrate the advantage of utilizing this technique. The output sampling rate should be the combined sampling rate of the input ADC dies, and the data resolution should be improved. In contrast, the noise and spur characteristics should also be discussed based on its effects to the output data. Lastly, the study will outline potential future work of this project such as increasing the number input ADC dies or analyzing the technique in an actual FPGA hardware.