Interview questions for Electrical Engineers

Contents

Introduction

Hello! You must be a recent graduate looking for a new job in high-tech? Or you just like to solve some interesting engineering problems.

This booklet contains typical interview design questions for junior hardware engineers, which arouse during interviews in numerous high-tech companies. The solutions to all of the questions appearing in this booklet are made by recent university graduates who have experienced most of the questions by themselves.

All the questions are divided for four categories. The first one contains design questions for logic design and verification engineers. The second category is suitable for circuit design engineers. The third category contains logic questions, which could be asked in all interviews. The last category contains several questions for RF and DSP engineers.

The designs in this booklet are not always ideal, but they should work. If you find any errors, please write to the following email address.

hardware_qu@yahoo.com.

Logic Design and Verification Engineer interview questions

Q:

Implement D- latch from

a) RS flip flop;

b) multiplexer

A:

a)

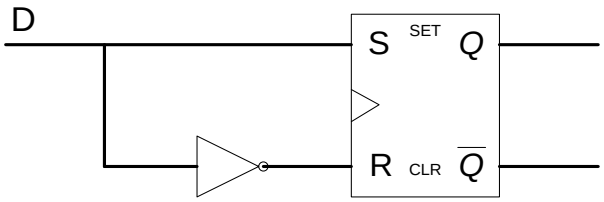


Figure 1

b)

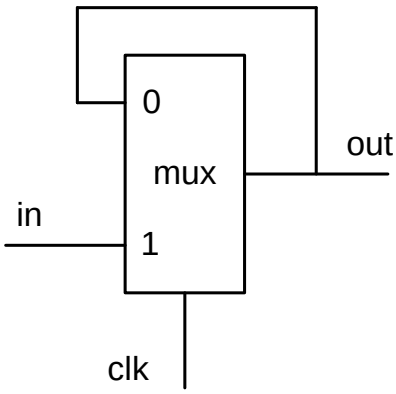


Figure 2

This is a 2-input **mux** implements D-latch. It works this way:

At every clock =1 out=in,

When clock =0 out= last in

Q:

How to convert D-latch into JK-latch and JK-latch into D-latch?

A:

Compare the truth tables of D-latch and JK-latch accordingly:

Clk	D	Q
+	0	0
+	1	1

Clk	J	K	Q
+	0	0	hold
+	0	1	0
+	1	0	1
+	1	1	Switch to opposite

Using these truth tables it is easy to convert JK-latch into D-latch.

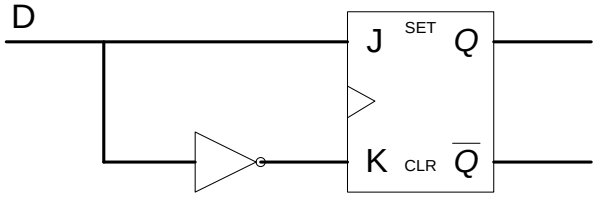


Figure 3

To convert D-latch into JK-latch some extra logic is required.

The following table shows the relation between J, K and D

J	K	Q
0	0	Q
0	1	0
1	0	1
1	1	!Q

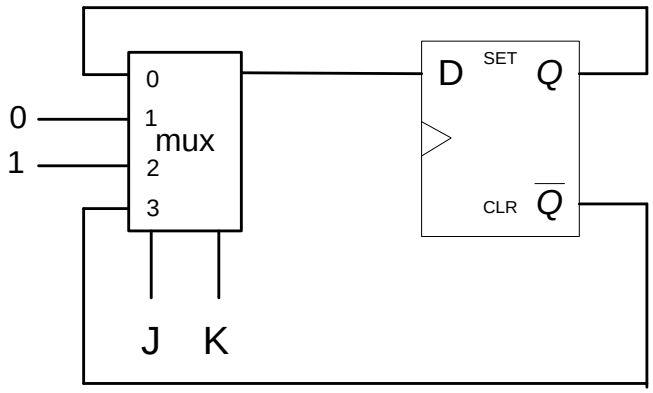


Figure 4

Looking at the drawing and the table it is not a problem to implement block A.

Probably the easiest way is to use a MUX.

J and K are control signals and 1,0,Q,!Q are data inputs.

Q:

Design a simple circuit based on combinational logic to double the output frequency.

A:

The buffer propagation delay should be a quarter of a clock cycle.

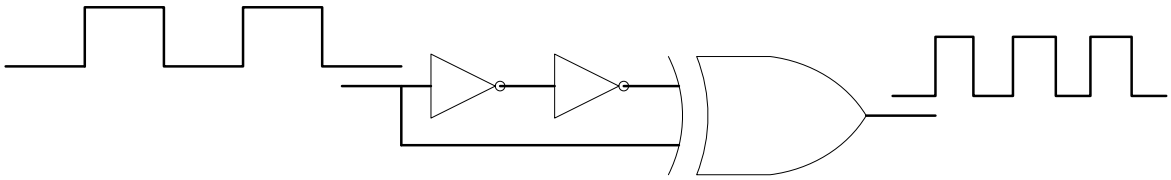


Figure 5

Q:

Design 1-bit full adder using decoder and 2 "or" gates?

A:

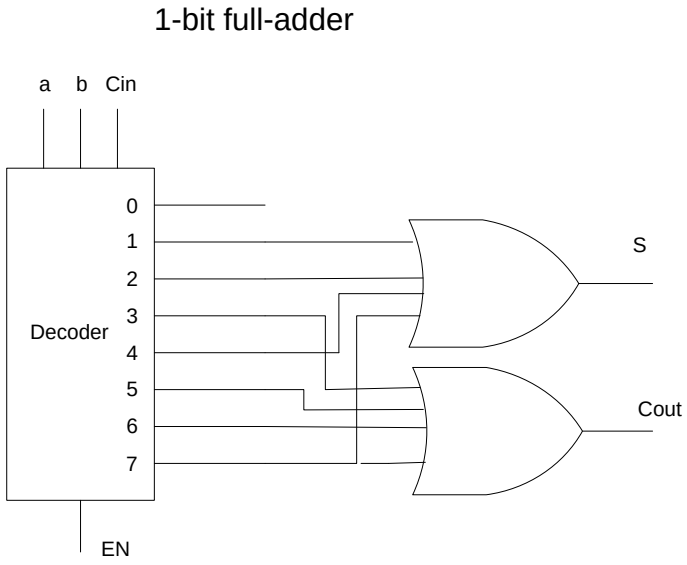


Figure 6

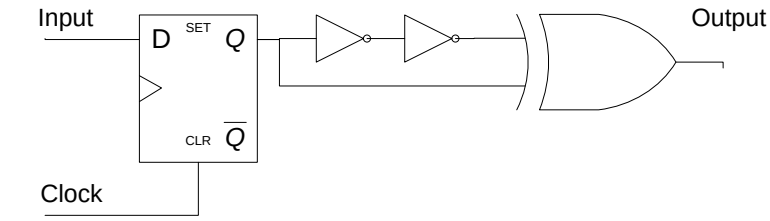
Decoder: - give 1 from the fit place and 0 from all others

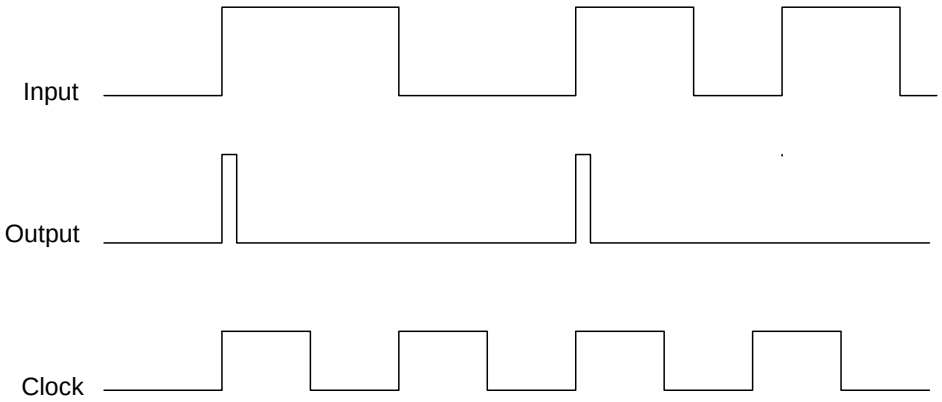
Need to write table a,b,Cin ---- SUM, Cout (when you get SUM=1 or 0, Cout=1 or 0)... easy...

Q:

Design a signal rising edge differentiator (receives any duration signal and outputs only one pulse at the low-to-high level signal transition).

A:





Q:

Design a system which is able to identify a single person entering a room or exiting from. The system consists of a counter, two light sensors and control block, which should be built. When a sensor identifies a person passing across, it outputs logic '1', and when there is none passing the sensor, its output is logic '0'. It may be assumed, that there is a certain area under the sensor for which the sensor outputs logic '1'.

A:

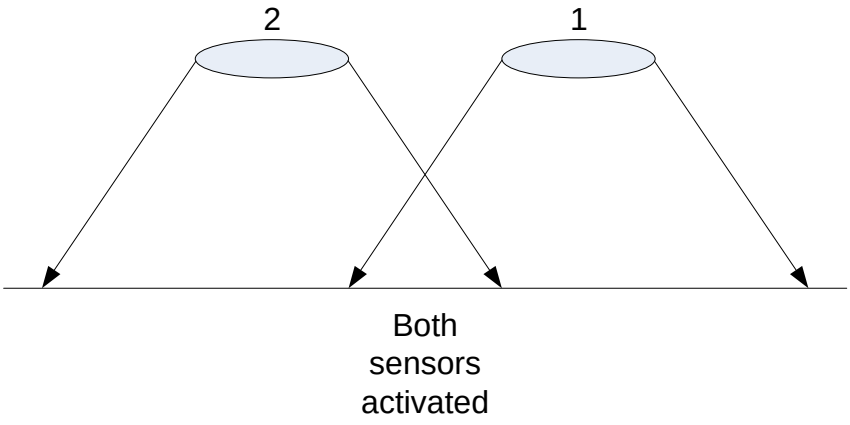


Figure 7

The solution is based on, that there is a region covered by both sensors. In other words, both sensors output logic '1', when a man standing in this region. We build a FSM which gets input signals from the sensors and outputs signals to the counter.

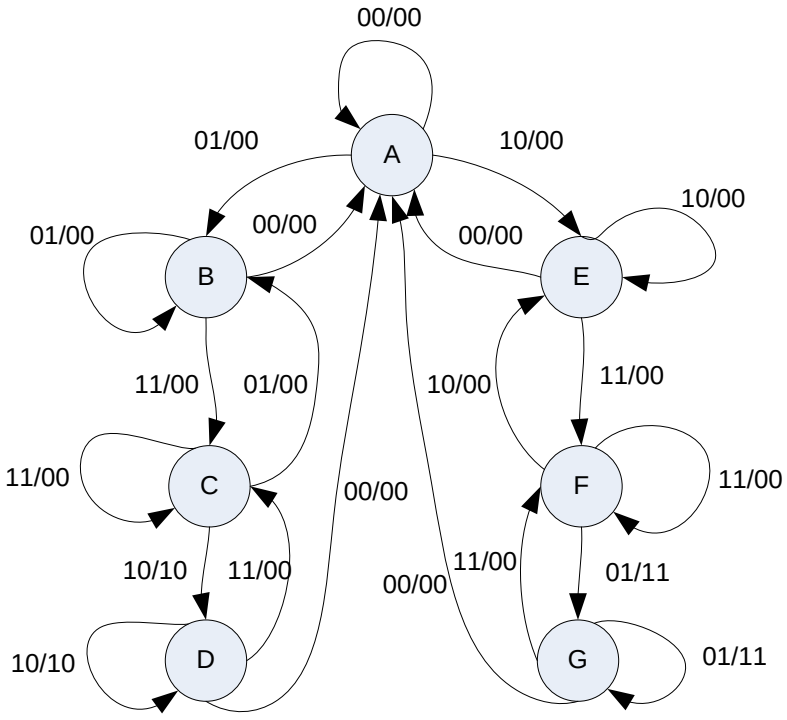


Figure 8

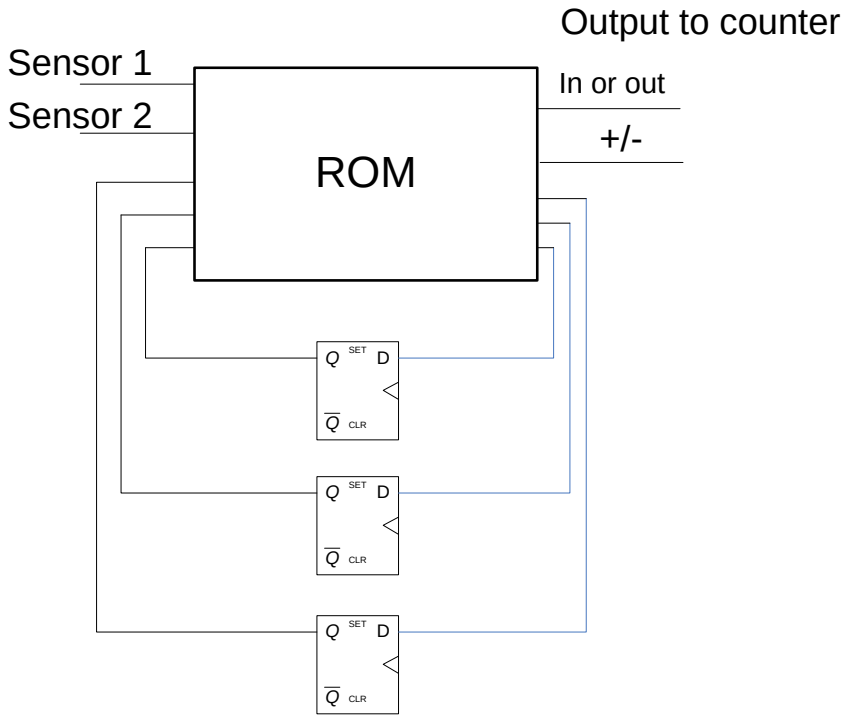


Figure 9

Q:

Design a system which gets a series of '1' s and '0's, and identifies errors in series of '0' or '1'.

If there is even series of '0'

If there are odd series of '1'

If the system identifies an error it outputs logic '1', otherwise it outputs logic '0'.

For example:

input	000011111000001
output	000010000100000

A:

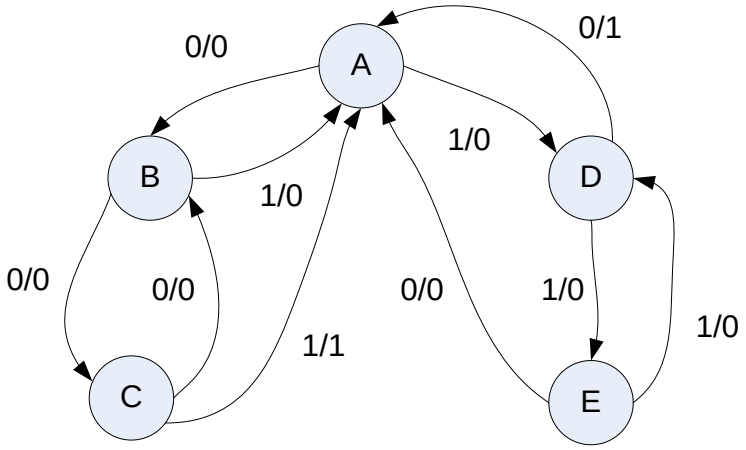


Figure 10

A- start

B- until this moment, there is an odd number of zeros

C- until this moment, there is an even number of zeros

D- until this moment, there is an odd number of ones

E- until this moment, there is an even number of ones

Q:

Design a system, which implements a Fibonacci series: 1 1 2 3 5 8 13 …

$X_n = X_{n-1} + X_{n-2}$. You can use memory components and arithmetic gates.

A:

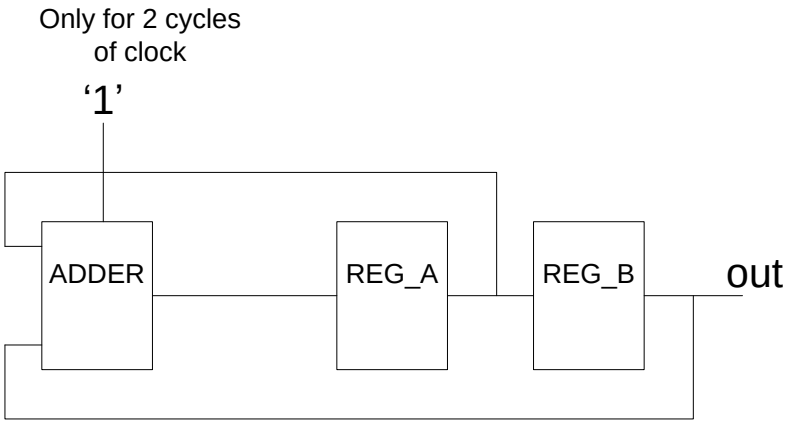
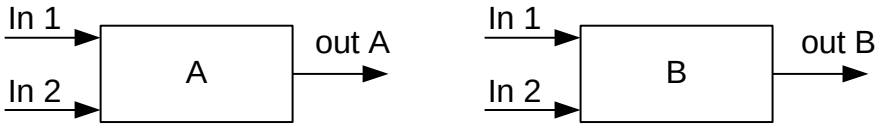


Figure 11

Q:

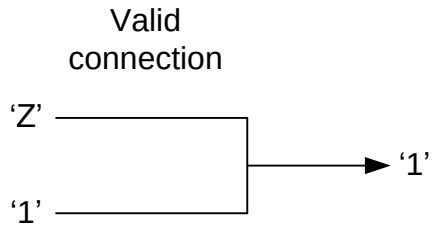
You have to components with the following true table:

Input 1	Input 2	Out 1	Out 2
0	0	1	Z
0	1	Z	Z
1	0	Z	Z
1	1	Z	0



Z is a High Impedance state (open circuit approximation) and can be an input to an every component.

When there is an intercept of two outputs where one is in High Z state and the other is in legitimate logic state, the output gets the logic state. For example:



Build a XOR gate using A and B components.

A:

We can implement a XOR gate using NOT and AND gates or NOT and OR gates.

$$X \otimes Y = X \cdot Y' + X'Y = \left(\left(X \cdot Y' \right)' \cdot \left(X' \cdot Y \right)' \right)'$$

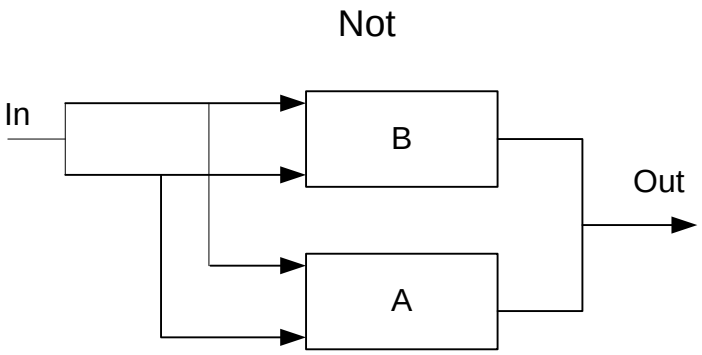


Figure 12

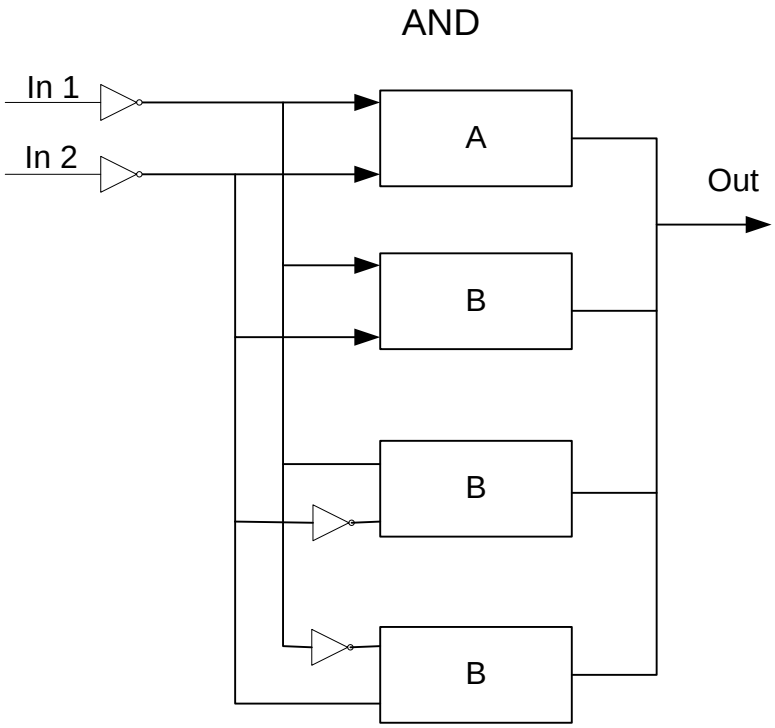


Figure 13

Q:
A seven bits Bus is given. Design a system which can count the number of logic ones in this bus. For example: if the bus value is 00101101, then the system outputs $(100)_2 = 4$. You can use adders, subtractors and other logic gates.

A:
In order to implement the system we use 2 bit full adders.

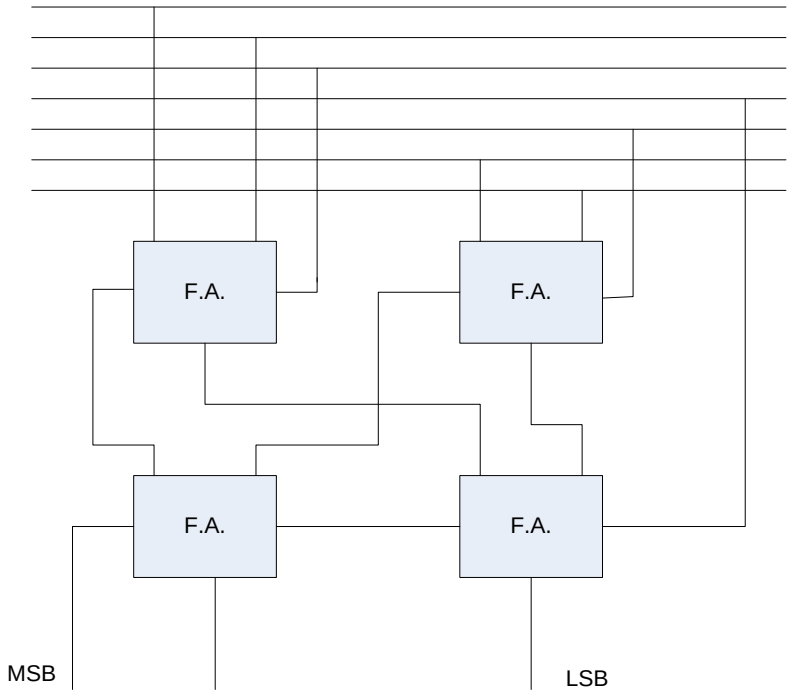


Figure 14

Q:

The ALU component can implement only basic logical operations –AND ,OR ,NOR , NAND and XOR. X and Y register are loaded by x and y operands accordingly. Describe the SWAP operations, in other words switching the registers content. At the end, the Y register must contain x operand and X register the y operand. The description must contain the LOAD and SEL lines and the registers content at every clock cycle.

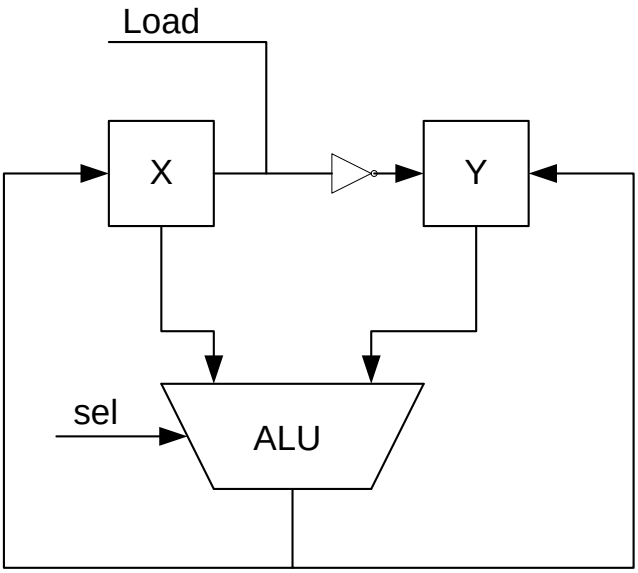


Figure 15

A:

STATUS	X	Y	LOAD	SEL
0	X	Y	0	0
1	$X \otimes Y$	Y	1	XOR
2	$X \otimes Y$	$Y \otimes (X \otimes Y) = X$	0	XOR
3	$X \otimes (X \otimes Y) = Y$	X	1	XOR
END	Y	X		

Q:

A system with one bit input and output is given.

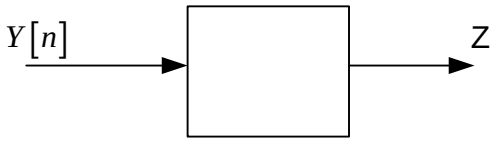


Figure 16

Here is the system input and output signals:

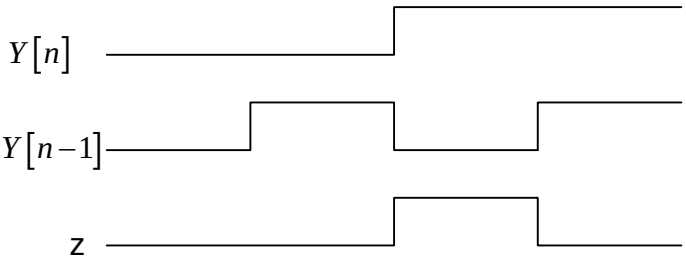


Figure 17

Describe the systems structure using logic gates and Flip-Flops.

A:

$Y[n]$	$Y[n-1]$	z
0	0	0
0	1	0
1	0	1
1	1	0

$$z = Y[n] \cdot \overline{Y[n-1]}$$

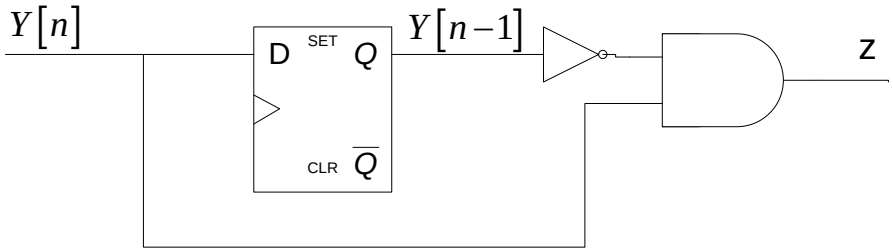


Figure 18

Q:

Design a system which gets 2 numbers and outputs the bigger among them. You can use memory, arithmetic components and logic gates.

Figure 19

A:

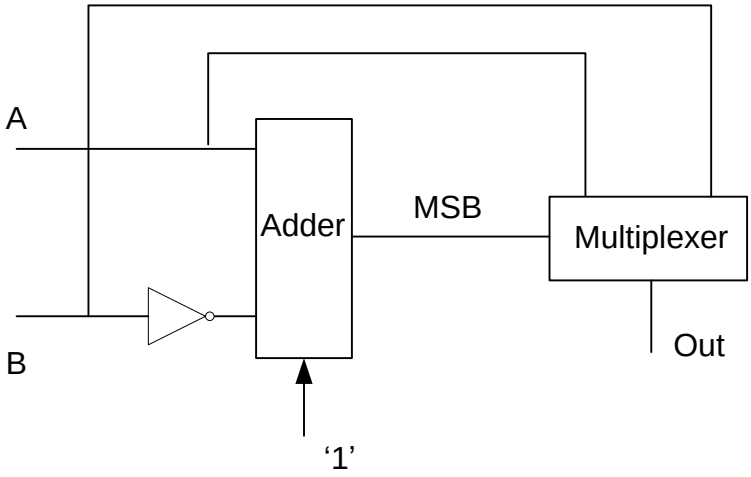
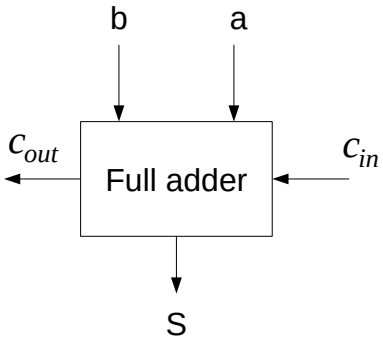


Figure 20

Q:

Design a single bit full adder and using it, build a four bit Full adder.

A:



$$S = a \oplus b \oplus c_{in}$$
$$c_{out} = ab + ac_{in} + bc_{in}$$

Figure 21

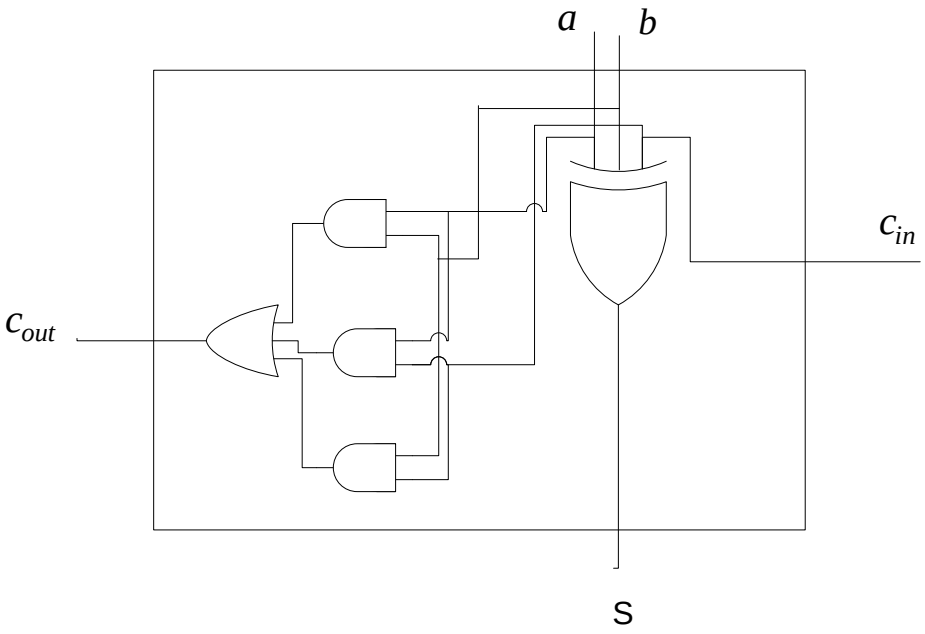


Figure 22

Q:

Design a selector 2×4 using selectors 1×2.

A:

We build a table of input and output signals:

x	y	f
0	**0**	**a**
0	**1**	**b**
1	**0**	**c**
1	**1**	**d**

From the table can be concluded that the desired circuit is

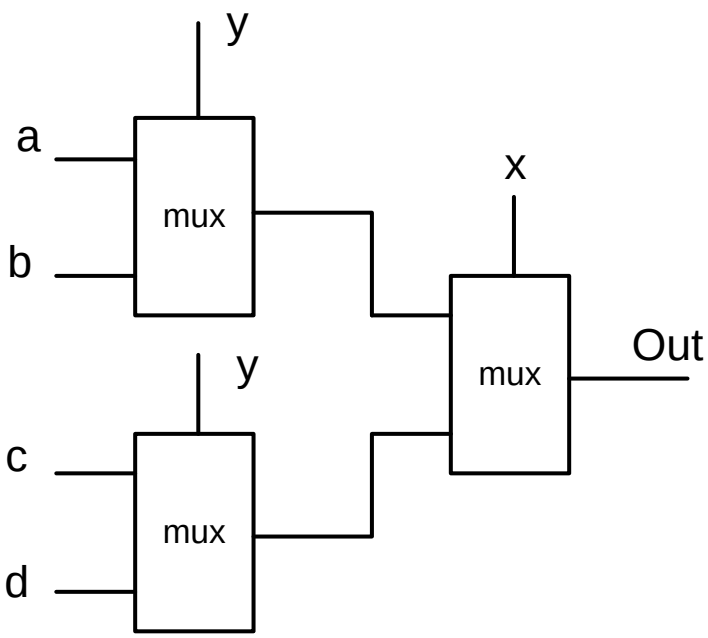


Figure 23

Q:

Design XOR using four NAND gates.

XOR= ab'+a'b=((ab')'(a'b)')'=((a(b'+a'))'(b(a'+b'))')'=((a(ab)')' (b(ab)')')' ➔ 4 NAND's

A:

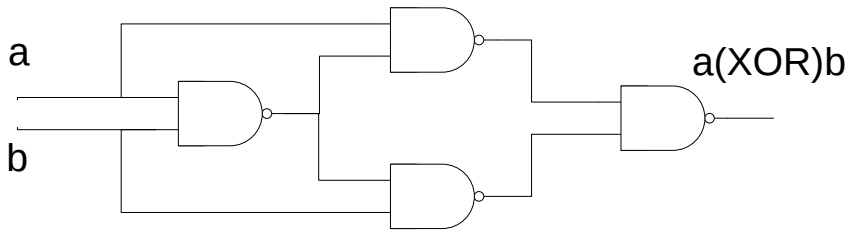
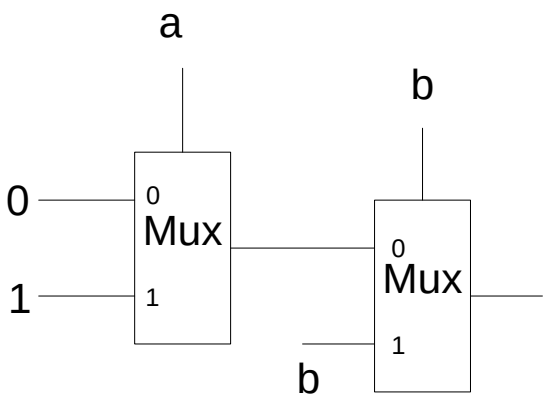


Figure 24

Q:

Design XOR using 2 **mux** components 2×1.

A:



Mistake

Figure 25

Q:

Design a system which outputs two pulses when gets the following input.

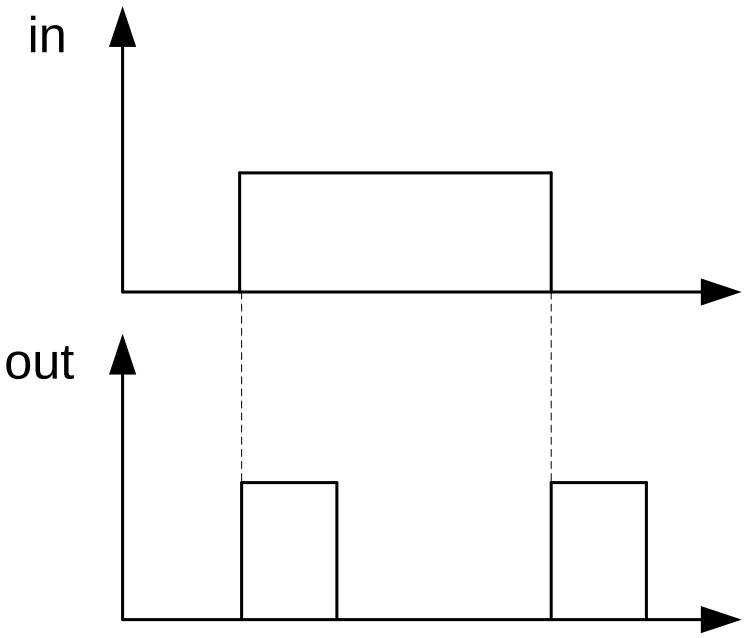


Figure 26

A:

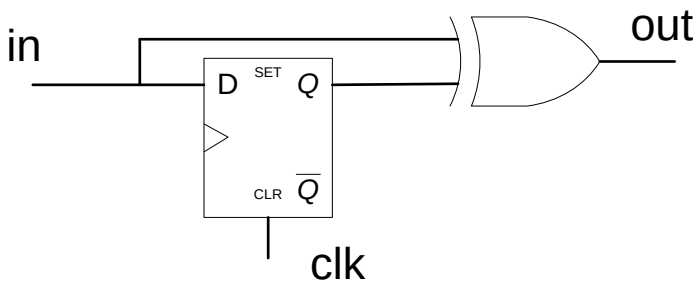
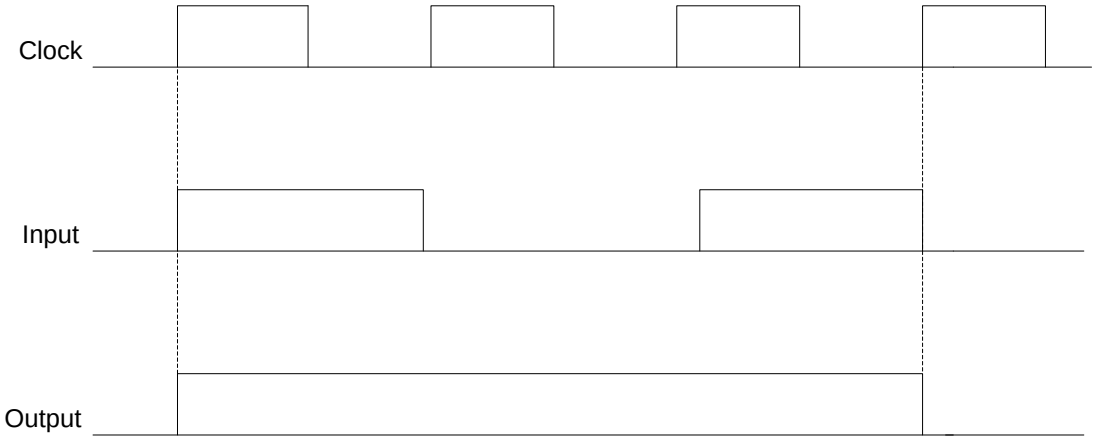


Figure 27

Q:

Design a simple circuit based on combinational logic witch input and output are depicted below.



A:

First implementation:

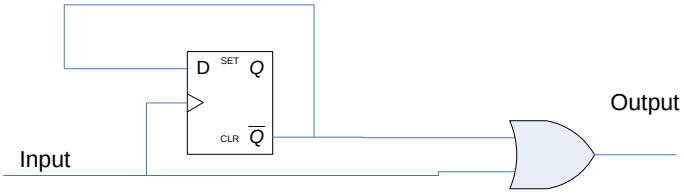
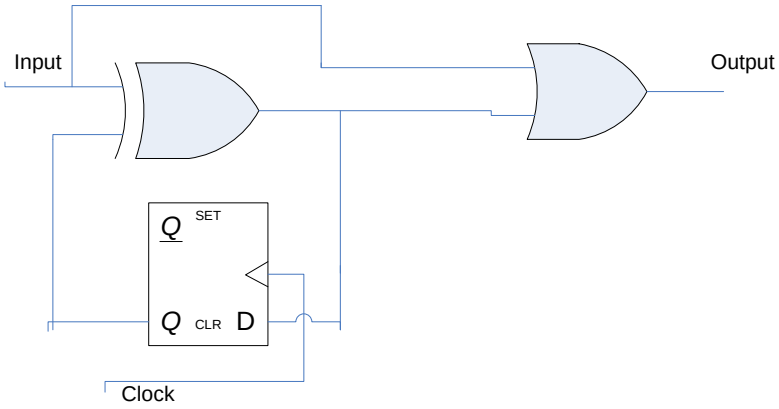


Figure 27

Second implementation:



x	y	Y
0	0	0
0	1	1
1	0	1
1	1	0

Figure 28

Q:

Input of a circuit is a bit string. Build a state machine of a divide-by-5 counter with equal duty cycle?

A:

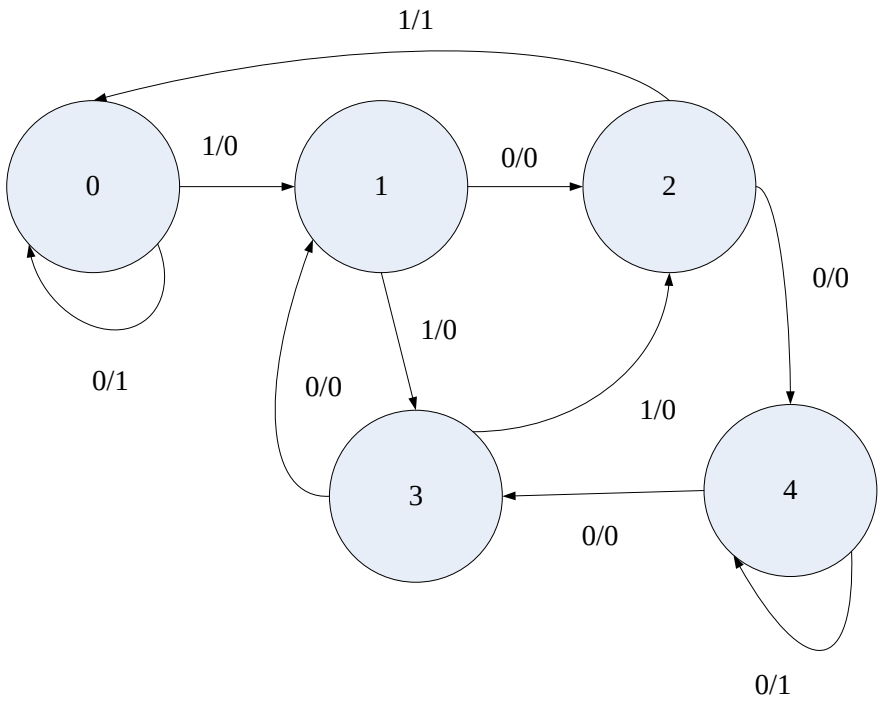


Figure 29

Q:

Design a hardware circuit according to these two VHDL codes given?

Code 1:

```
if a=b then x;
   elseif a=c then y;
      elseif a=d then z;
 else w;
```

Code 2:

```
if a=b then x;
if a=c then y;
if a=d then z;
else w;
```

A:

Implementation of Code 1:

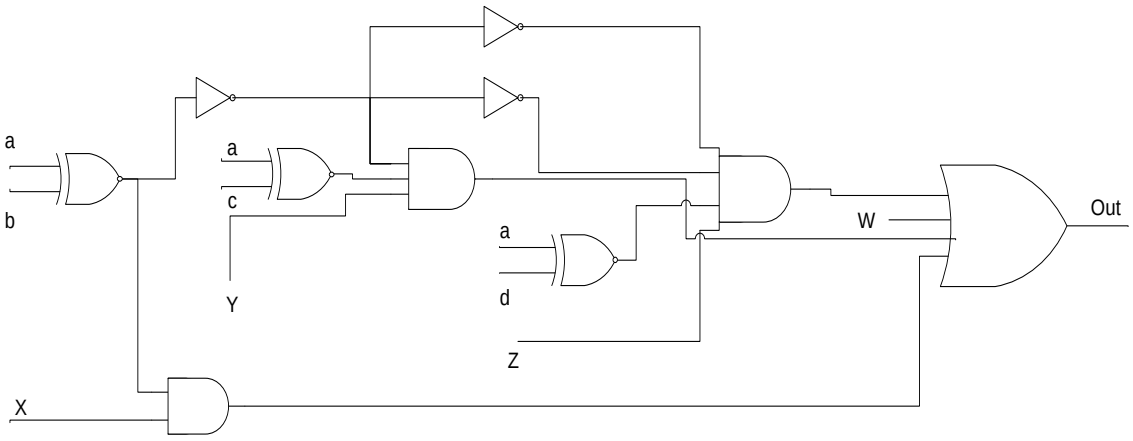


Figure 30

Implementation of Code 2:

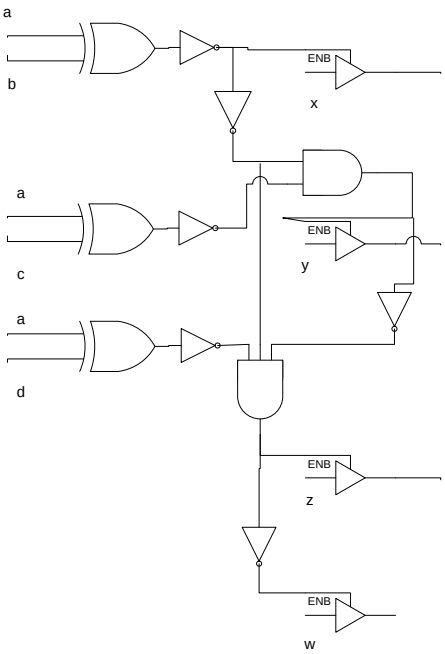


Figure 31

Q:

Design a simple circuit based on combinational logic witch input and output are depicted below.

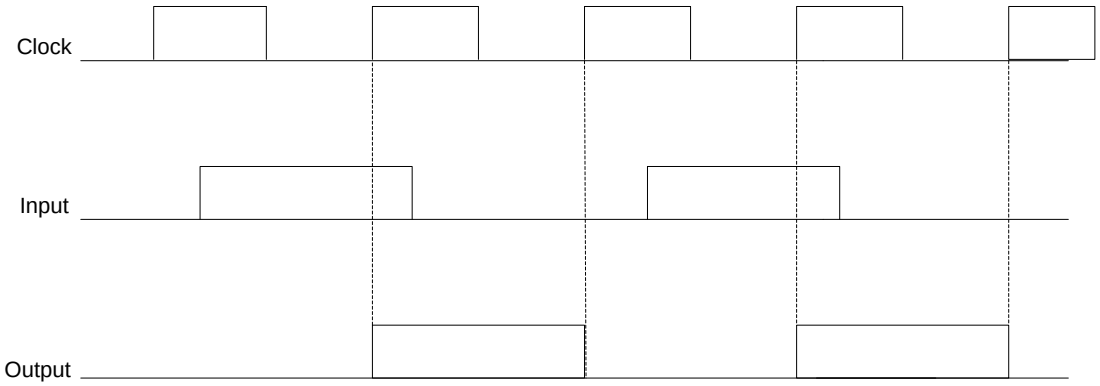


Figure 32

A:

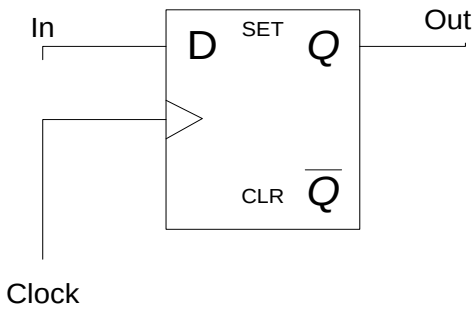


Figure 33

Q:

Design a simple two bit counter circuit based on combinational logic, using only D-Flip Flops.

A:

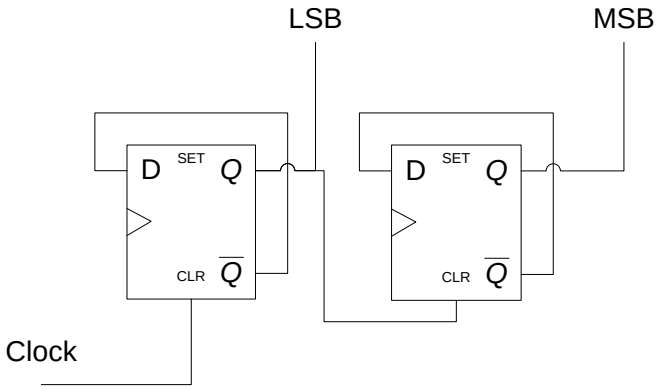


Figure 34

Q:

Design a simple circuit based on combinational logic witch input and output are depicted below.

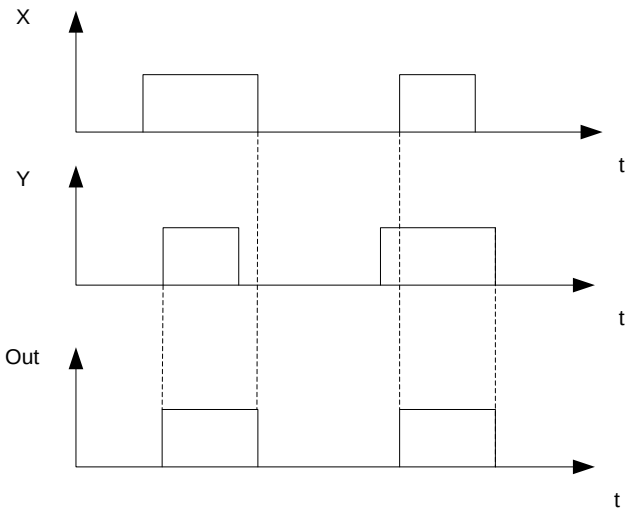


Figure 35

A:

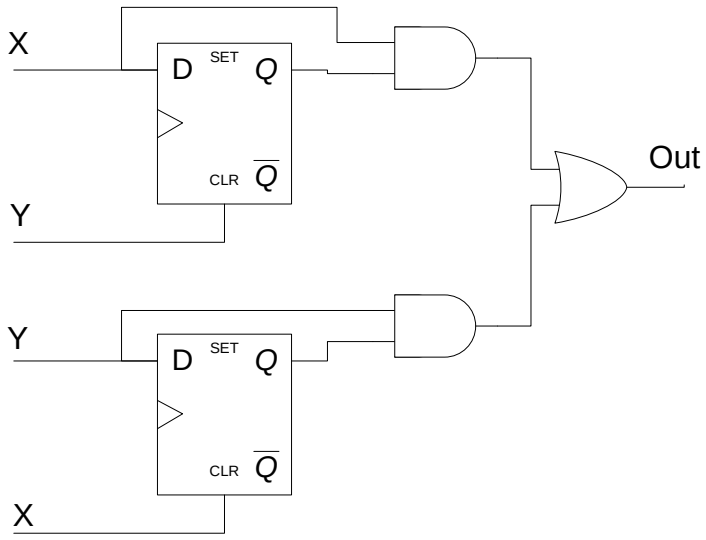
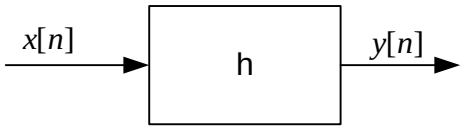


Figure 36

Q:

Build digital filter FIR:



$$y[n]=\sum_{n=0}^{100} h[n]\cdot x[n]$$

$x[n]$ and $y[n]$ are 16 bits numbers including a sign bit.

a) What is the minimal register size to store the result?

b) Build a system which implements this filter.

A:

a)

$$h[n]\cdot x[n]\rightarrow 15\text{bit}+15\text{bit}+1\text{bit}=31\text{bit}$$

101: 31,31,31…….31;
51: 32,32,32……32;
26: 33,33,33.....33;
13: 34,34,34.....34;
7: 35,35,35.....35;
4: 36,36,36,36;
2: 37,37;
1: 38 ⟵ $y[n]$

b)

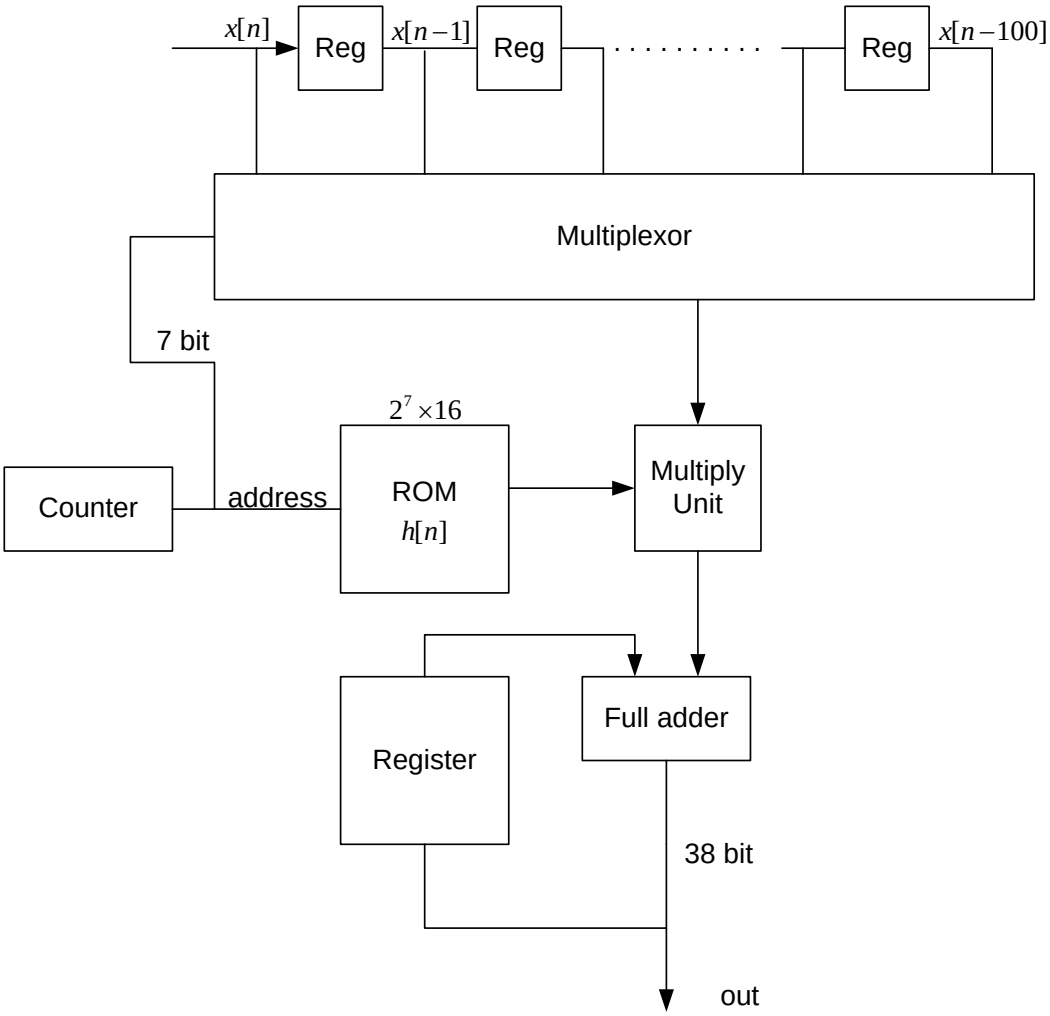

x[n]
Reg
x[n−1]
Reg
. . . . . .
Reg
x[n−100]
Multiplexor
7 bit
2^7 ×16
Counter
address
ROM
h[n]
Multiply
Unit
Register
Full adder
38 bit
out

Figure 37

Q:

Design a shift register of 3 bits, which adds zeros from the left.

A:

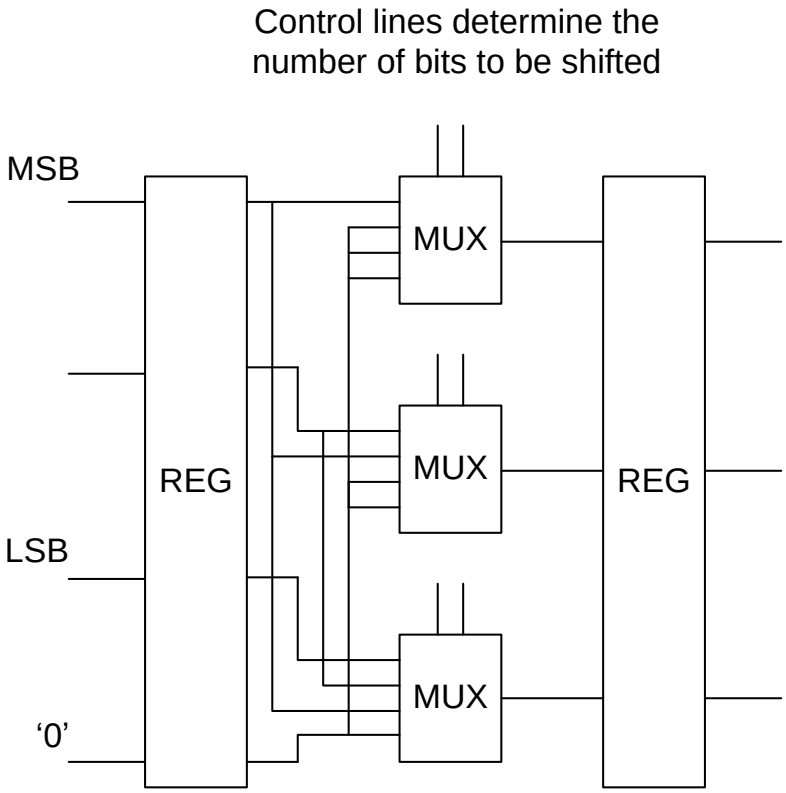


Figure 38

Q:

You have been given two signals A and B each n bits long. Implement $C = \frac{A+B}{2}$ when it is known that $B = A+2$.

A:

You have to pay attention that if A number is even, then B is also an even number. On the other hand, if A is odd, also B is odd.

For example:

If A and B are even, then

$$\begin{array}{l} 000100 \rightarrow A \\ \underline{000110 \rightarrow B} \\ 000101 \rightarrow C \end{array}$$

If A and B are odd, then

$$\begin{array}{l} 000011 \rightarrow A \\ \underline{000101 \rightarrow B} \\ 000100 \rightarrow C \end{array}$$

We can see that if A is even, then the result is obtained when the LSB of A is substituted with '1'. ON the other hand if A is odd, then the result is obtained when the LSB of B is substituted with '0'.

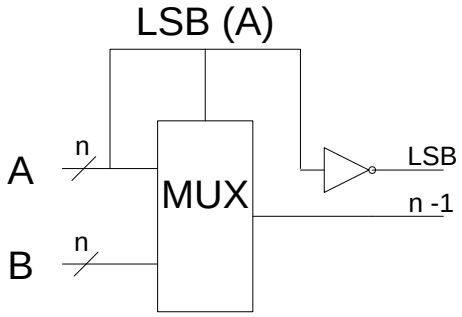


Figure 39

Q:

You are given a system with 8 bits input and output:

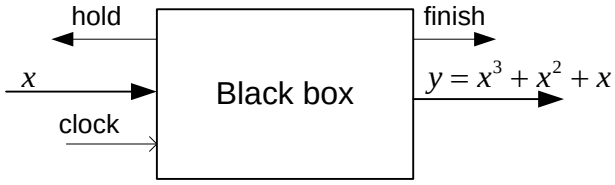
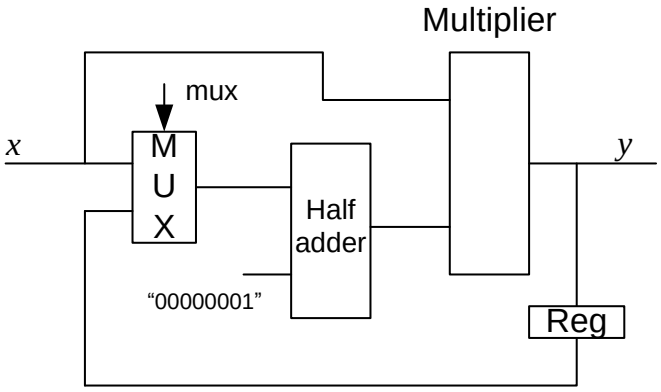


Figure 40

Design a system, which implements the mathematical function using minimum hardware and also design a controller which gets two control signals 'finish' and 'hold'.

A:

$y = x^3 + x^2 + x = x(x^2 + x + 1) = x(x(x+1)+1)$



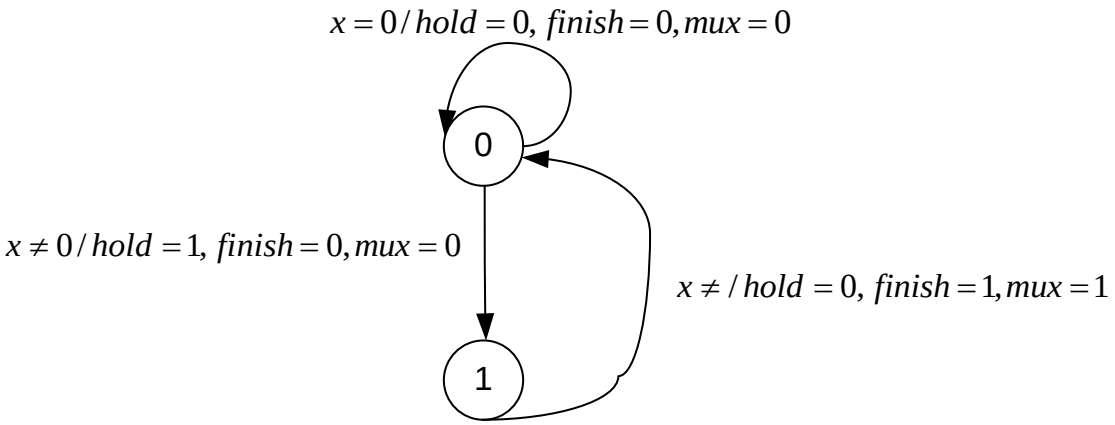


Figure 41

Q:

A circuit which has an analog output is given below:

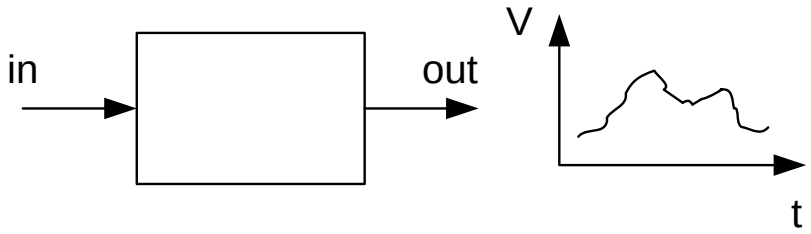


Figure 42

Design a digital system, which reduces the DC voltage from the circuit's output. Use minimum hardware and A/D of 8 bits.

A:

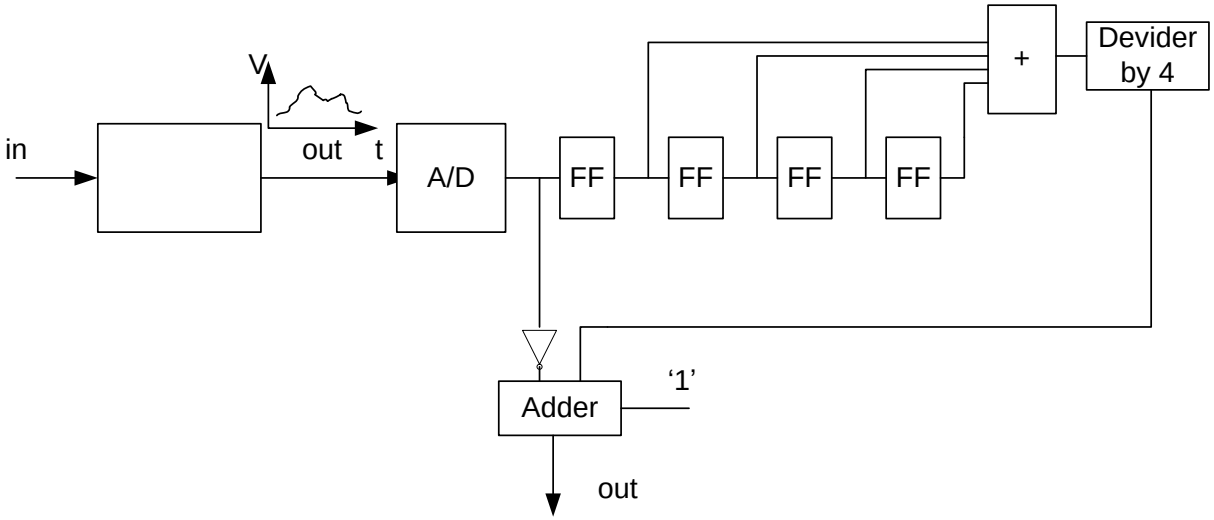


Figure 43

In order to implement this system with minimum hardware, we use number of FFs, which is a power of two. The division may be implemented by connecting wires in required order, instead of using right shift register.

Q:

Design a synchronous circuit, which gets two input signals X and Y and outputs a signal Z, as depicted below:

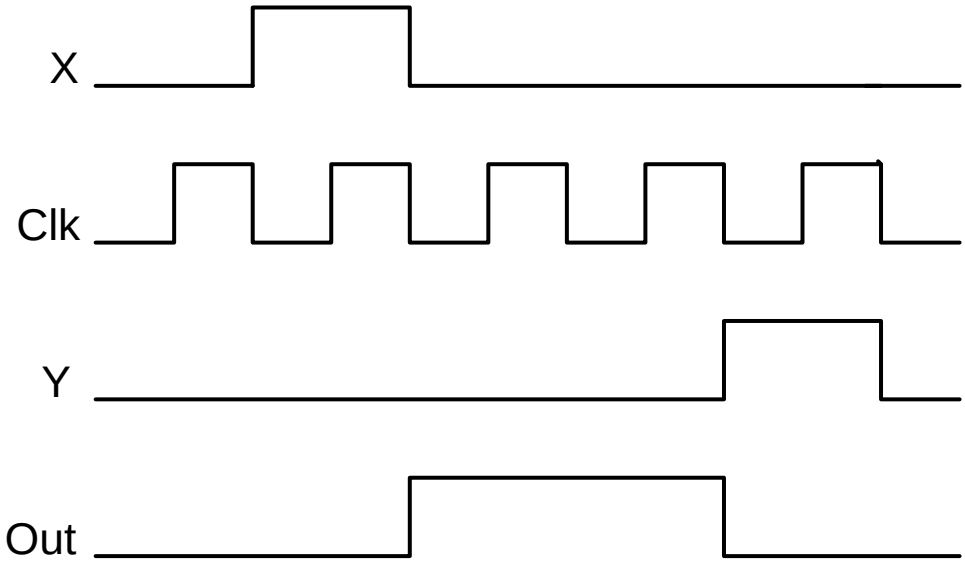


Figure 43

A:

In order to implement this circuit, we use Negative triggered D-Flip-Flop.

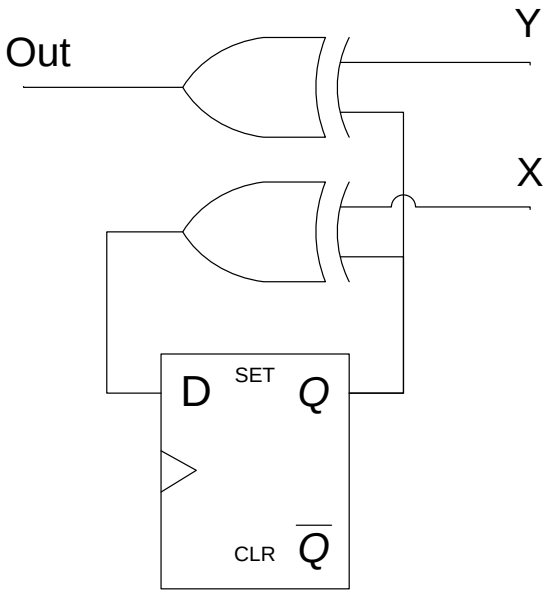


Figure 44

Q:

Add a circuit to a counter of 4 bits, so that the counter will count till 11 and reset itself to zero.

A:

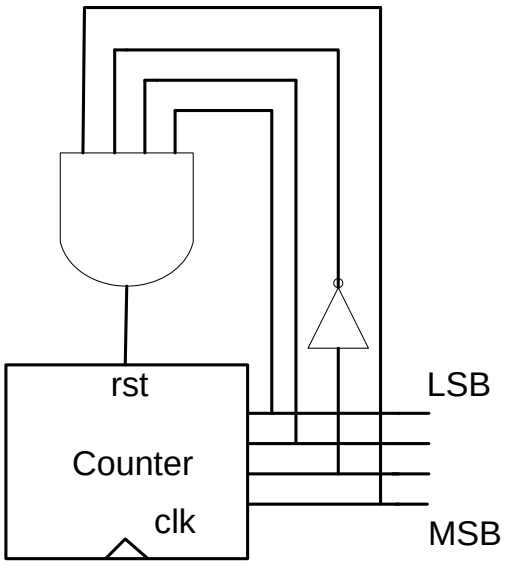


Figure 45

Q:

You have got a system, which includes a counter of 4 bits and some logic. In addition an input of 4 bit is given. When a value in the input equals the counters output the counter should be reset and must restart counting from zero. Design the required logic.

A:

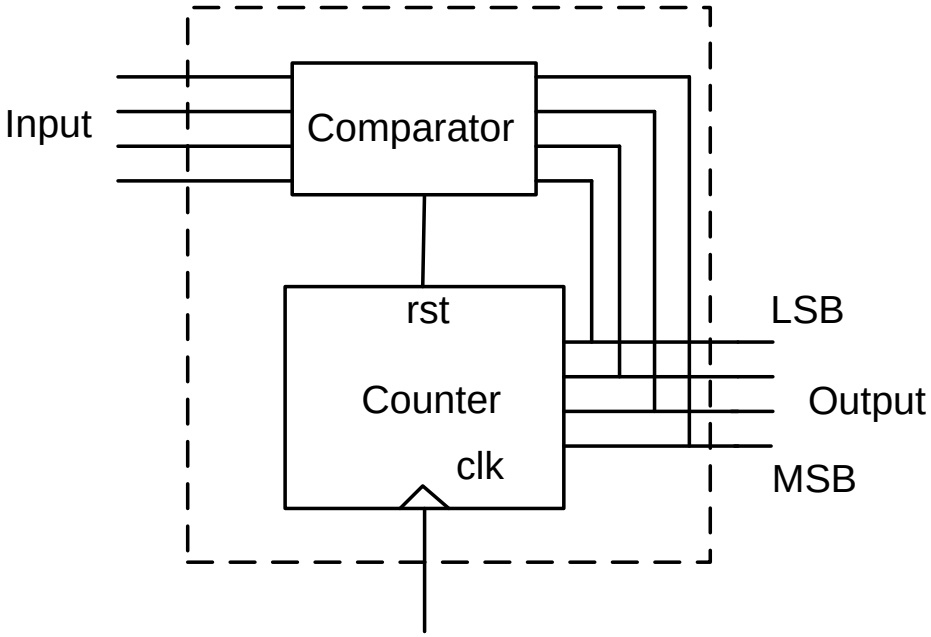


Figure 46

Q:

Design a system, which gets a clock, binary numbers n and m, and outputs a signal as depicted below:

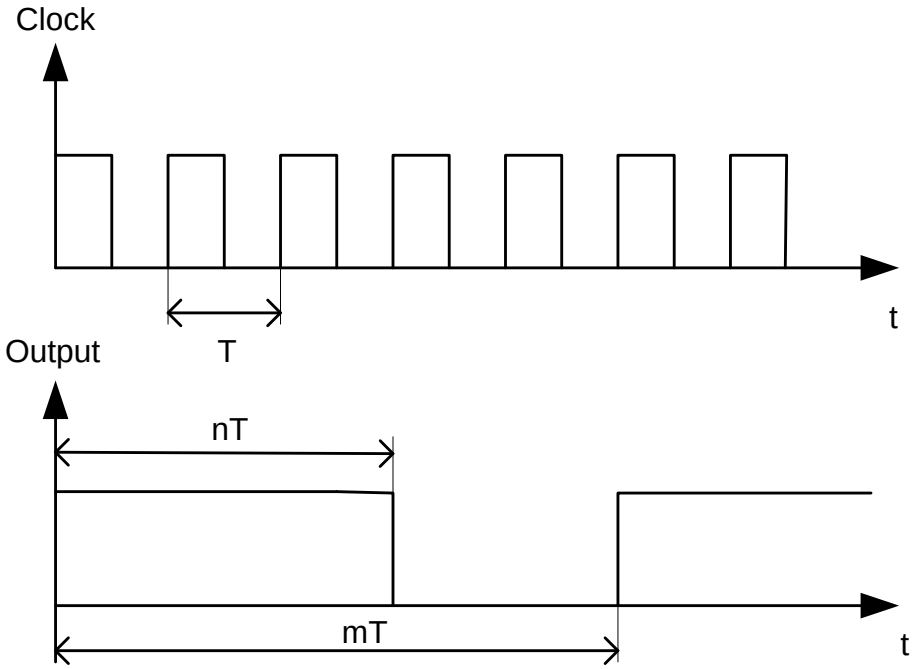


Figure 47

A:

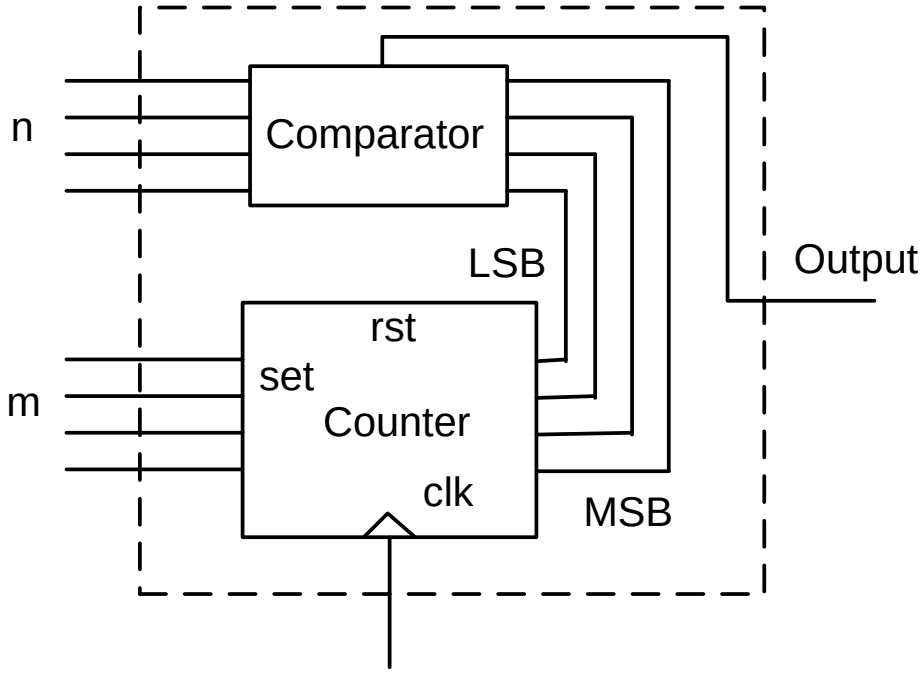


Figure 48

The counter input determines the counters maximal output, after which its output would be reset to zero. In this case the counter will count until m. The comparator outputs '1' when its input is less than n, and outputs '0', when its input is larger then m.

Q:

A disk is given. One half of the disk is transparent and the other one is not. A lamp is set above the disk and under the disk two light sensors are set. Check the picture below.

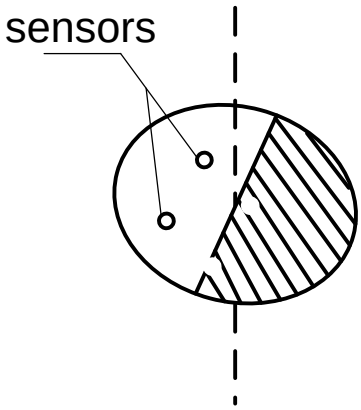


Figure 49

Design a system which determines the direction of rotation of the disk.

A:

We call a signal from the first sensor **a** and from the second **b**. We draw how those signals change if the disk is rotating. It can be clear from the graphs, that there is a constant phase between the signals.

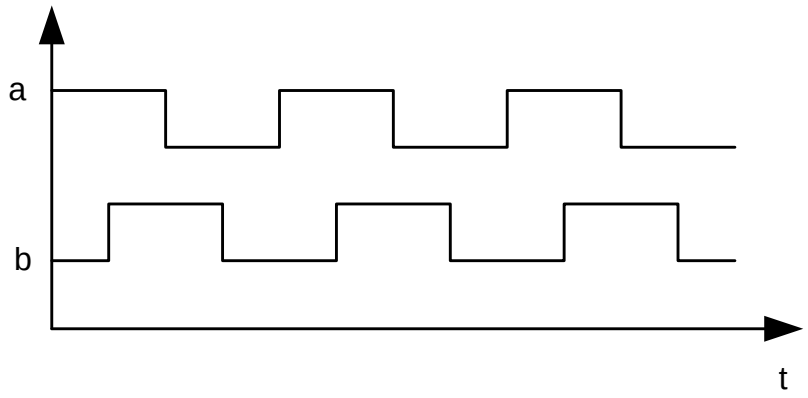


Figure 50

Finally, we use a single D-Flip Flop in the following configuration to determine the rotation direction.

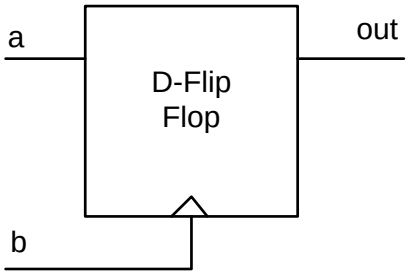


Figure 51

In this configuration the output of the FF depends on the phase difference between the two input signals, which depends on the direction of rotation. As a result the circuit outputs '1' or '0', constantly.

Q:

You have been given a block, which can sort two input numbers.

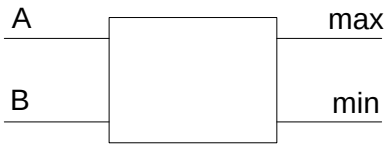


Figure 52

Use any number of those block and sort four and six numbers.

A: Sort four numbers:

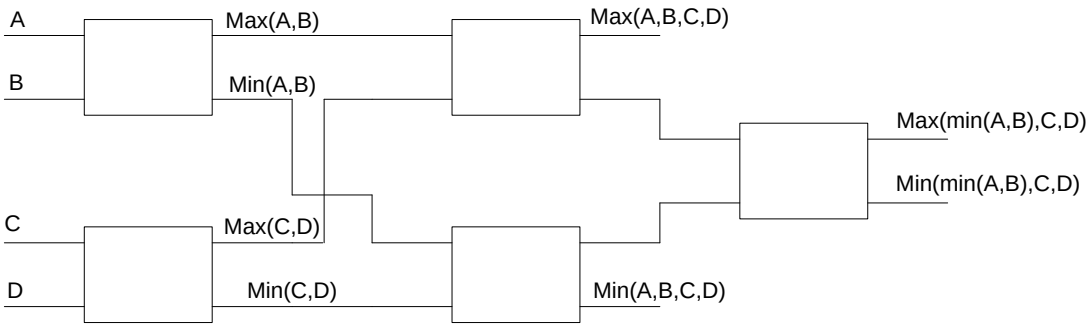


Figure 53

Sort six numbers:

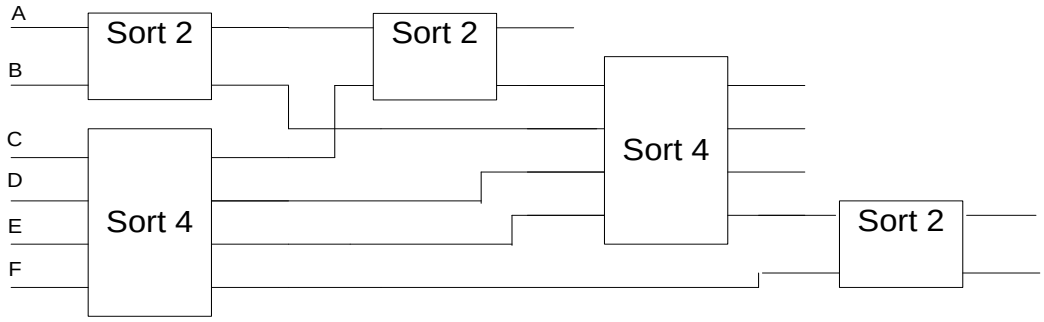


Figure 54

Q:

Design a circuit, which implements $\log_2 M\big|_{\text{int}}$. M is a binary number of n bits and an input to the circuit.

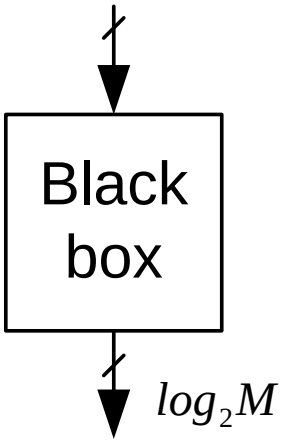


Figure 55

A:

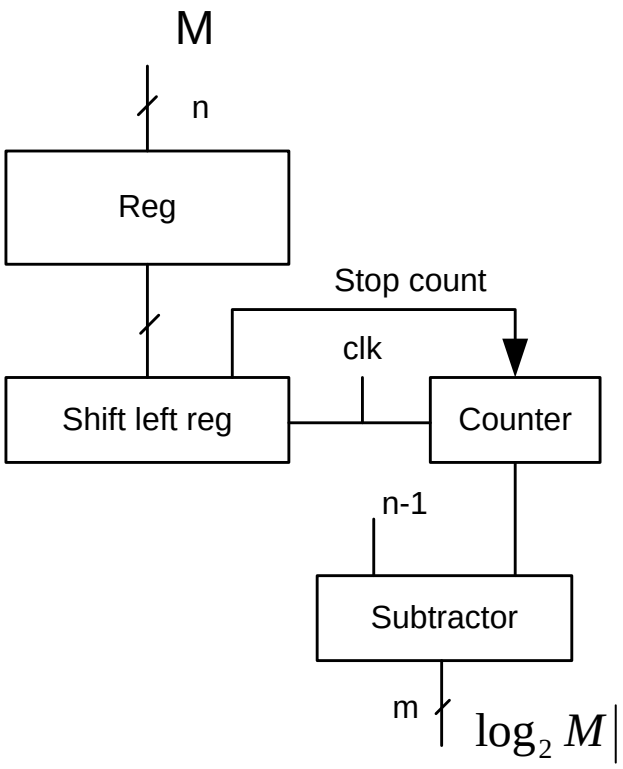


Figure 56

$2^3 2^2 2^1 2^0$	$\log_2 M$
0001	000
0010	001
0011	001
0100	010
0101	010
0110	010
0111	010
1000	100

Q:

How efficiently to transfer data from 8 bit bus to 7 bit bus,

without loosing any data?

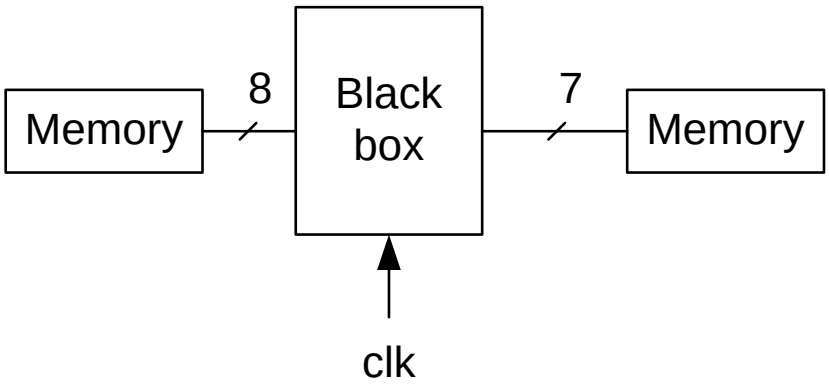


Figure 57

A:

Description of the black box:

The black box should contain 14 registers and a final state machine to implement the following steps:

Step 1: Load 8 bit of data to the first 8 registers

Step 2: Output data of the first seven registers

Step 3: The data in the eighth register is shifted to the first register.

Step 4: Load of next 8 bits into registers 2 to 9.

Step 5: Output data of the first seven registers

Step 6: The data in the eighth and ninth registers is shifted to the first two registers

.

.

.

The process is continued until the first six registers are full.

Step 7: Another 8 bits are loaded into the last registers and now all of the 14 registers are full.

Step 8: The black box outputs the data from first seven registers

Step 9: The remaining 7 bits are shifted to the top of the register

Step 10: The black box outputs the first 7 bits.

Now, the registers are empty and all the steps are gone through all over again.

Q:

Design a circuit which input is 10 bits and the output is the numbers of how many time each input number appeared.

A:

The first circuit is not optimal; it is rather a straight forward design. The second circuit (with RAM) is more optimal.

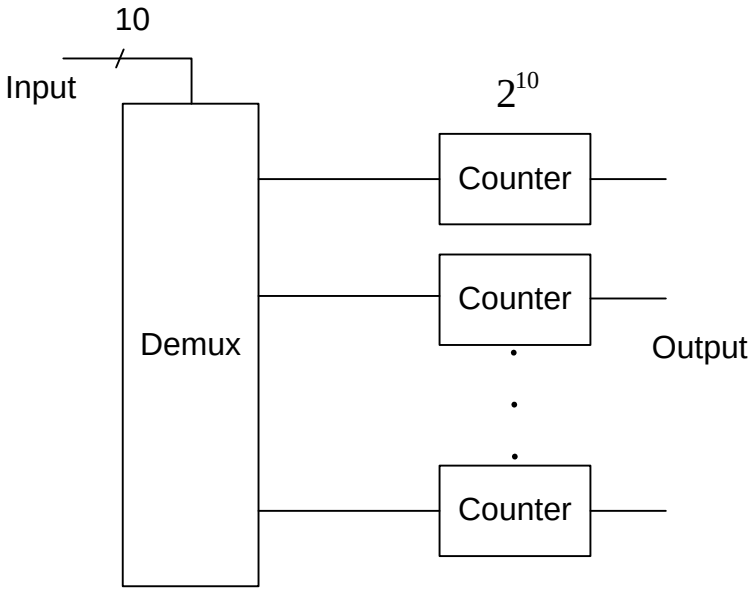


Figure 58

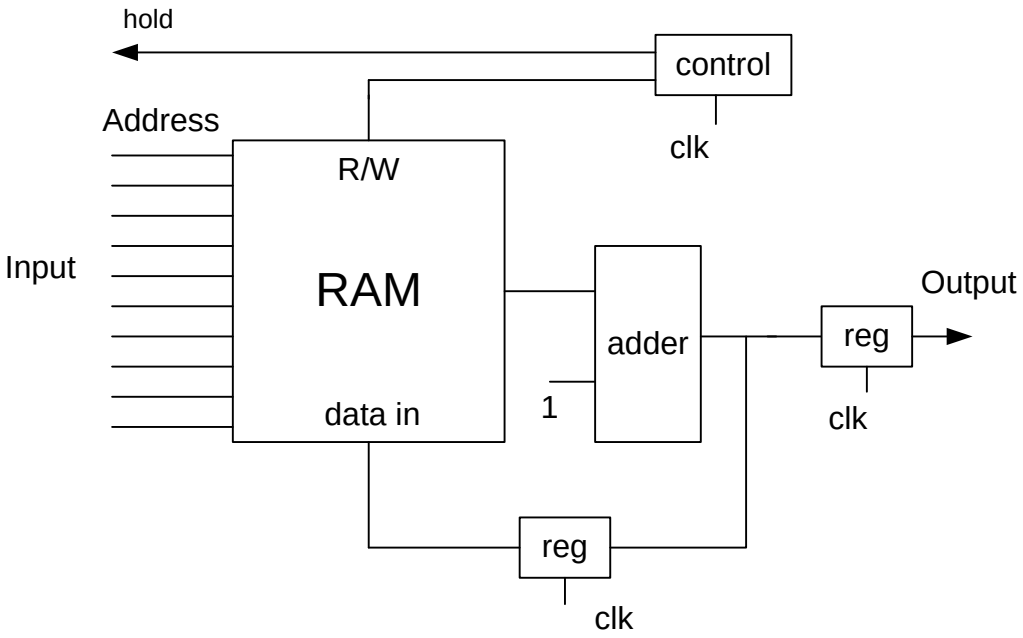


Figure 59

Q:

You have a system which builds a picture 1000 pixel×100 pixel. Each pixel consists of 8 bits. What you should do in order to make a zoom to the picture, but only to the Y axis. Finally you should get a picture 1000 pixel by 200 pixels. Build the block, which enables you to perform the required zoom. You may use a buffer 1000×8 bits and other logic.

A:

In order to implement the zoom, we have to add another line between every two existing lines in the picture. To do so, we make an average between every two lines and insert the new line between them.

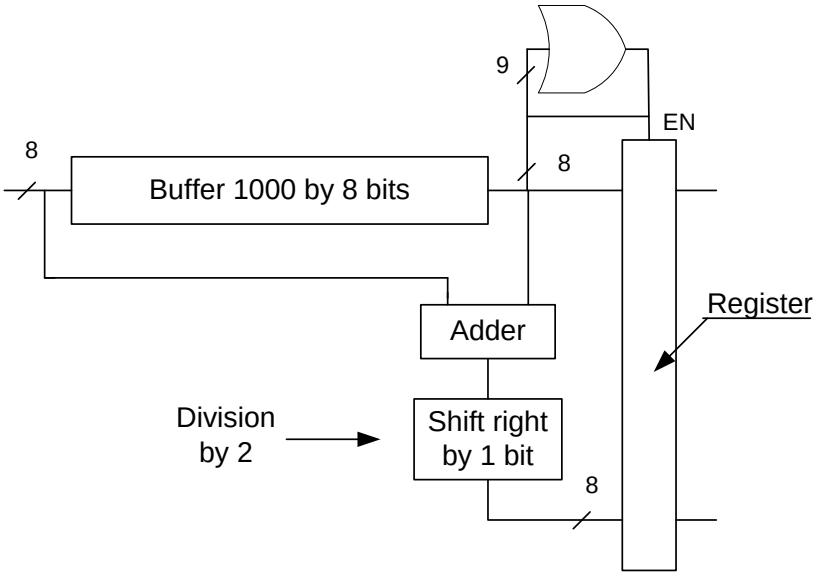


Figure 60

Q:

You get 16 bits word. You have to build a block which outputs the word but with all the ones shifted to one side.

For example: the word is 0010100111000100, so the output should be: 1111110000000000.

A:

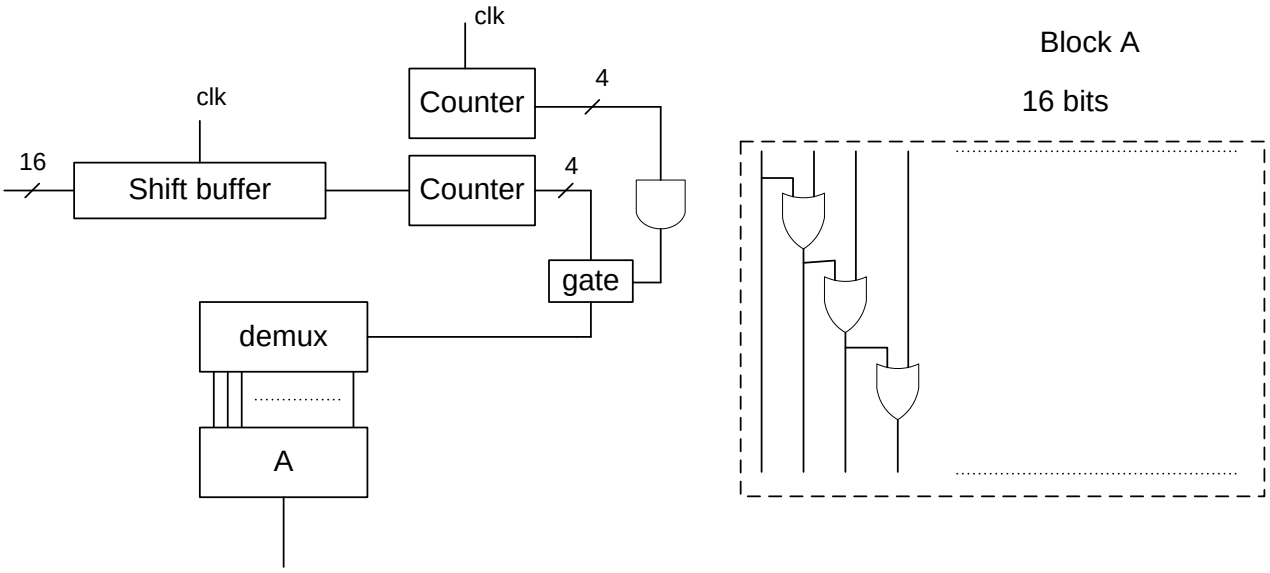


Figure 61

Q:

You get 30 numbers. You should build a block that outputs them in reverse order.

A:

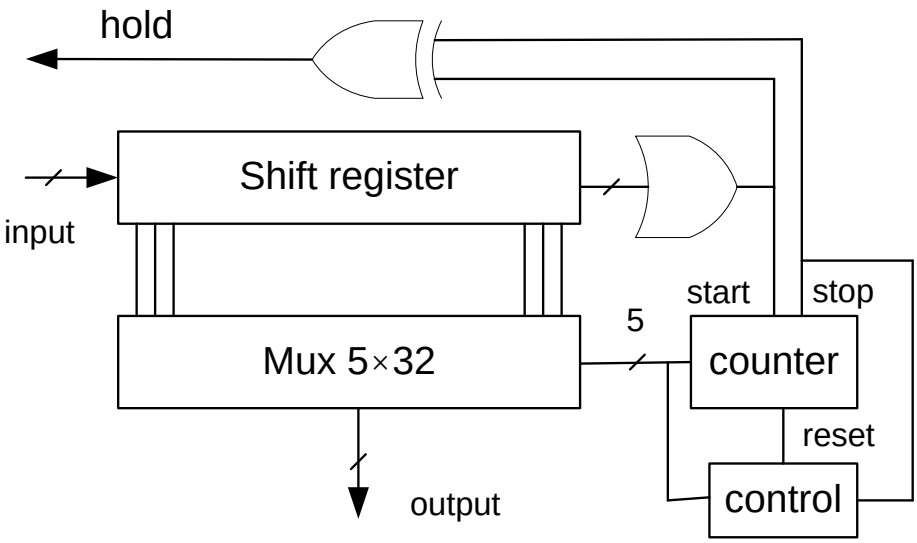


Figure 62

The control block resets the counter when its output is 30, and turns off the hold signal.

Q:

You should implement a system, which inputs are integers 1,2,3,4…. and its outputs are the square values of the inputs: 1,4,9,16… You should build the system using minimum hardware.

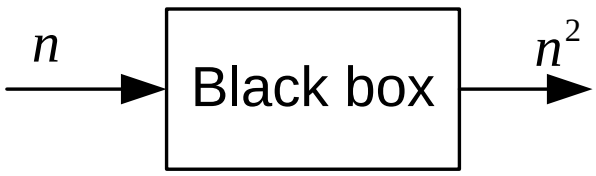


Figure 63

A:

$(n+1)^2 = n^2 + 2n + 1$

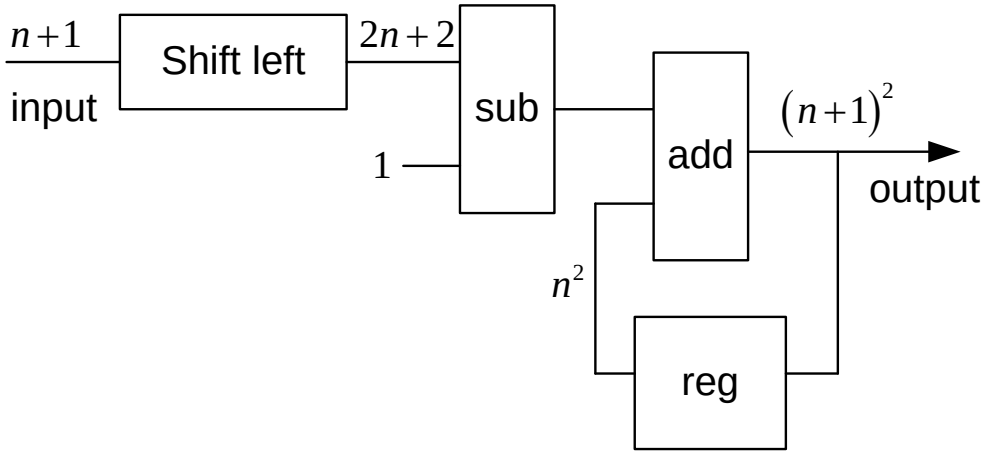


Figure 64

Q:

Design a circuit in accordance with the given signal diagram.

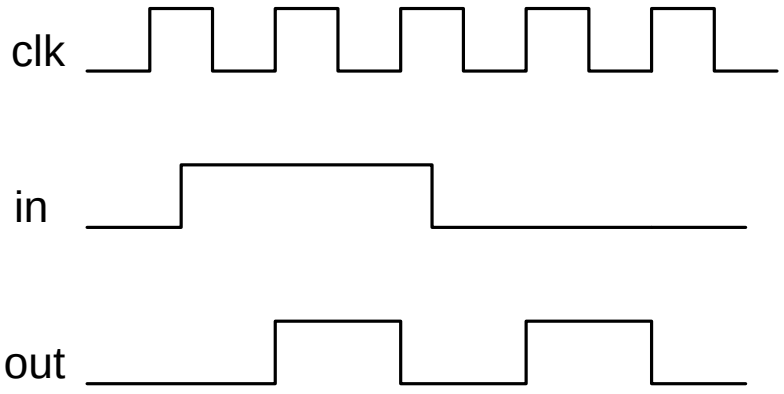


Figure 65

A:

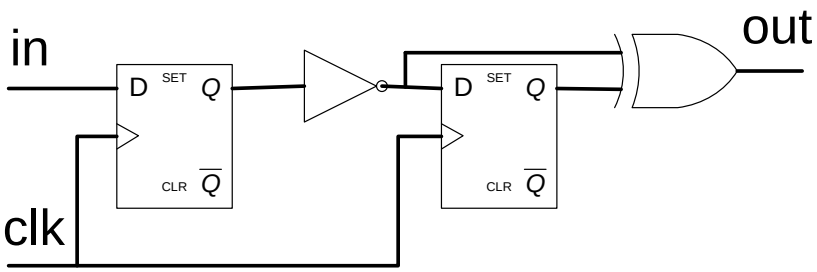
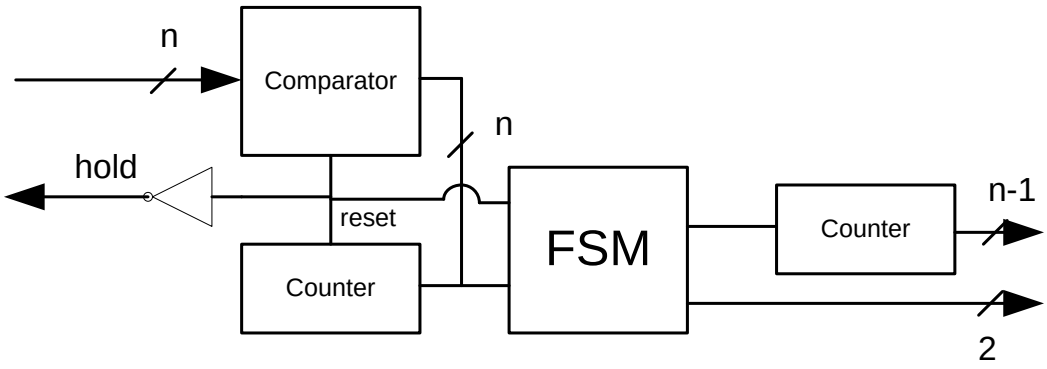


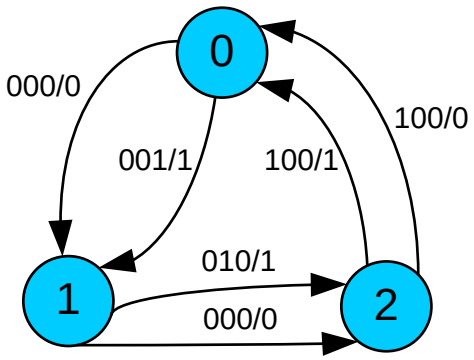
Figure 66

Q:
Design a system, which can divide a number by 3 and return the result + the residue.

A:



The implementation of the FSM is



PS	in	NS	out
Q1 Q2	x	D1 D2	a b c
00	0	01	000
00	1	01	001
01	0	10	000
01	1	10	010
10	0/1	00	100

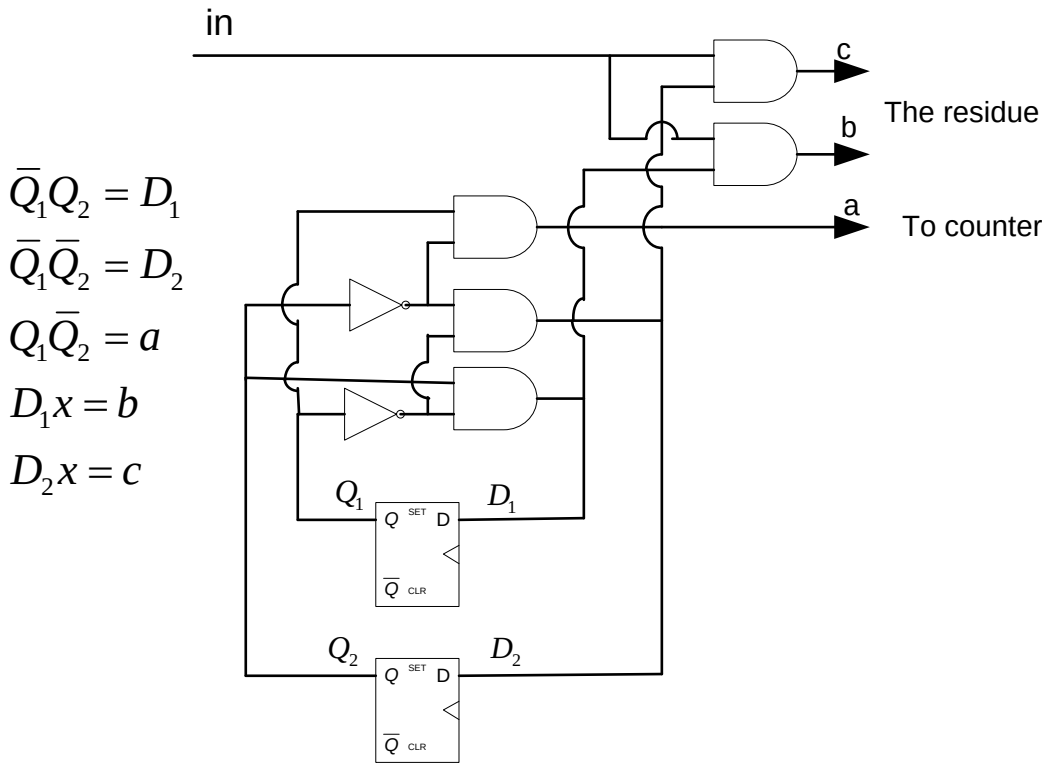


Figure 67

Q:

What limitations are imposed on the clock period to enable the circuit to operate normally?

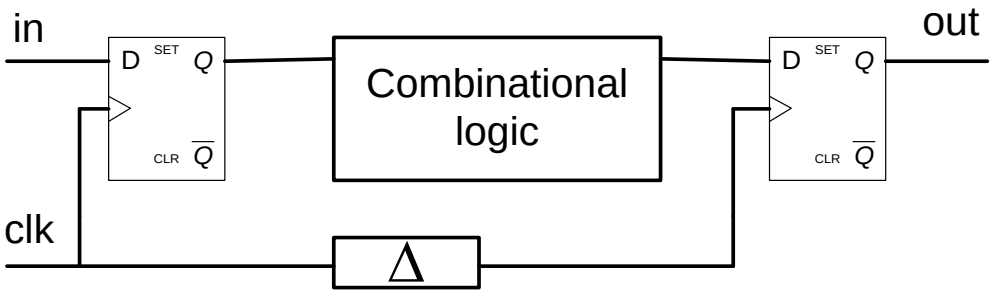


Figure 68

A:

$$t_{pd}(CL) + t_{pd}(FF_1) + t_{setup}(FF_2) < T_{clk} + \Delta$$

$$t_{hold}(FF_2) + \Delta < t_{cd}(FF_2)$$

Q:

You have four comparators of two bits each and several logic gates. Use those comparators and implement four bit comparator.

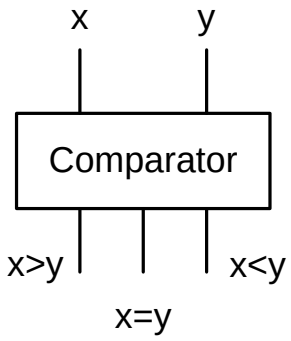


Figure 69

A:

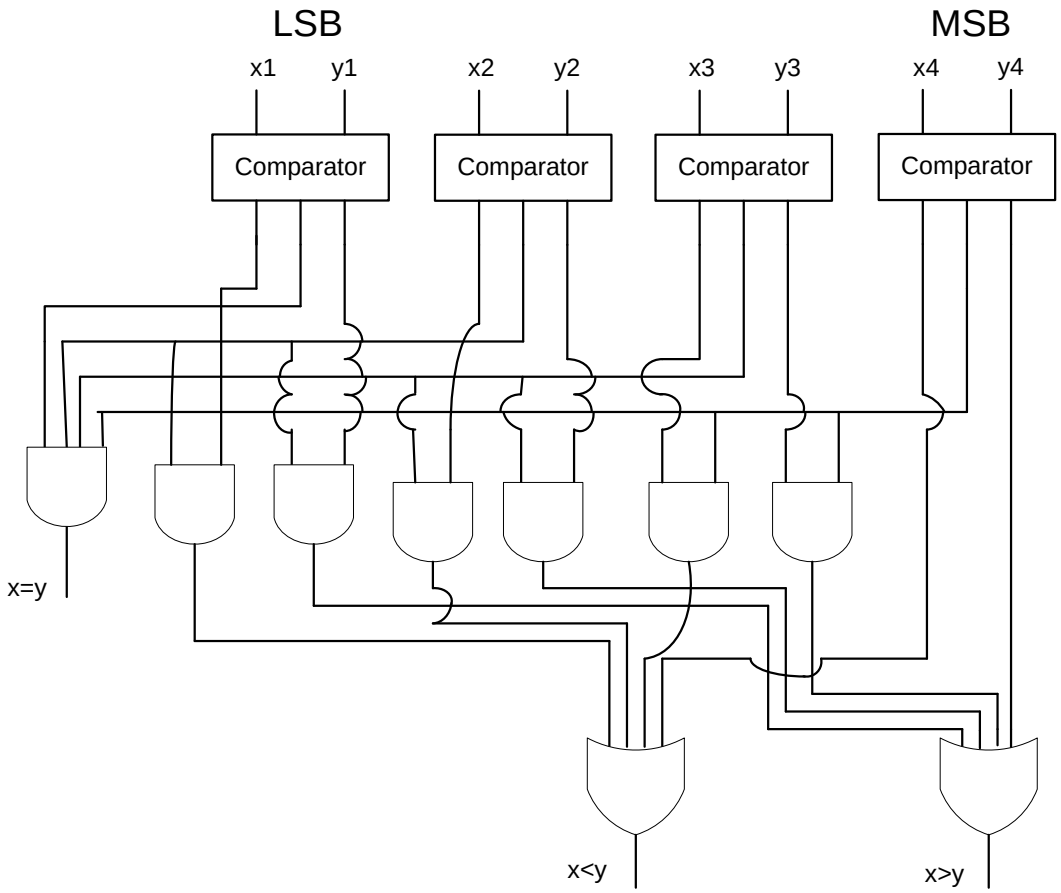


Figure 70

Q:

You have to implement a 2's complement of a four bit number + a sign bit using the following component:

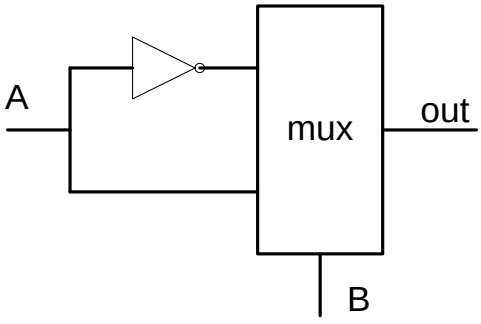
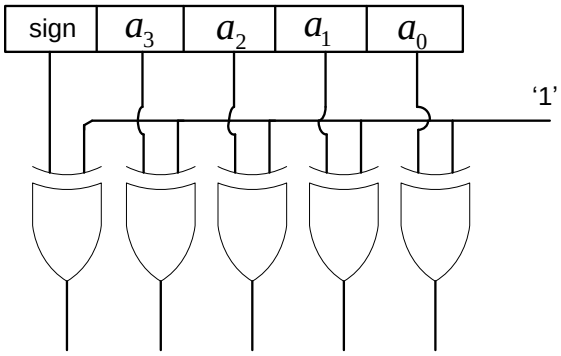


Figure 71

A:

If we analyze this component, we can come to a conclusion that this component implements a XOR gate.



Then, '1' should be added. **Mistake**

Figure 72

Q:

Implement a four bits D/A and A/D devices.

A:

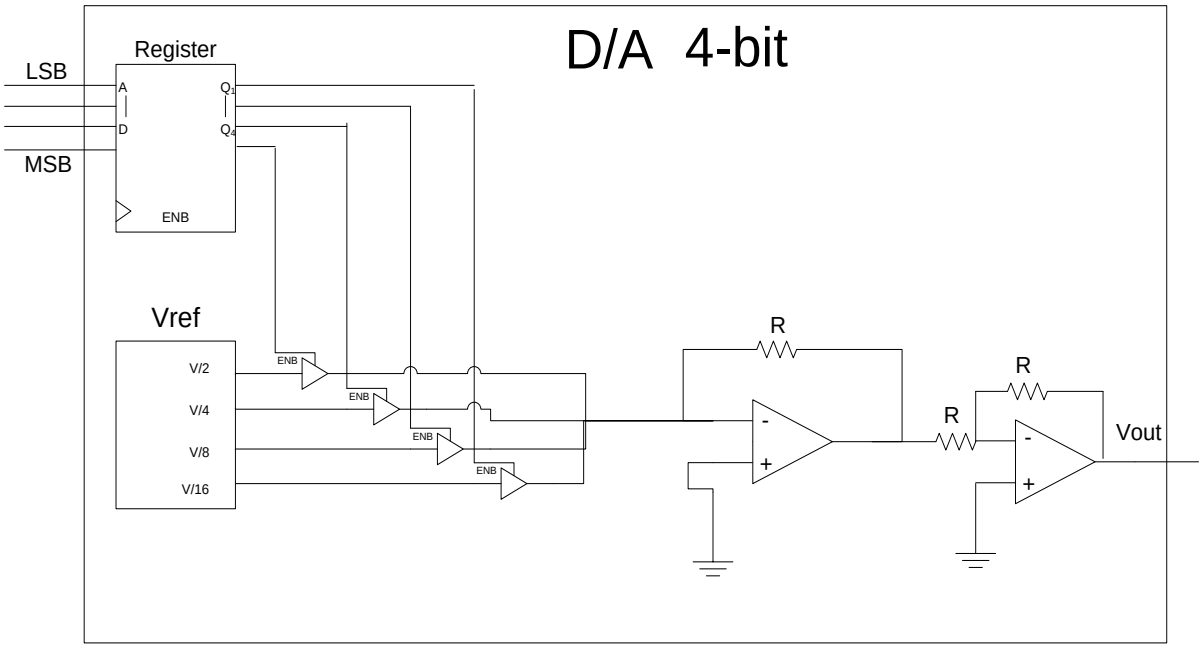


Figure 73

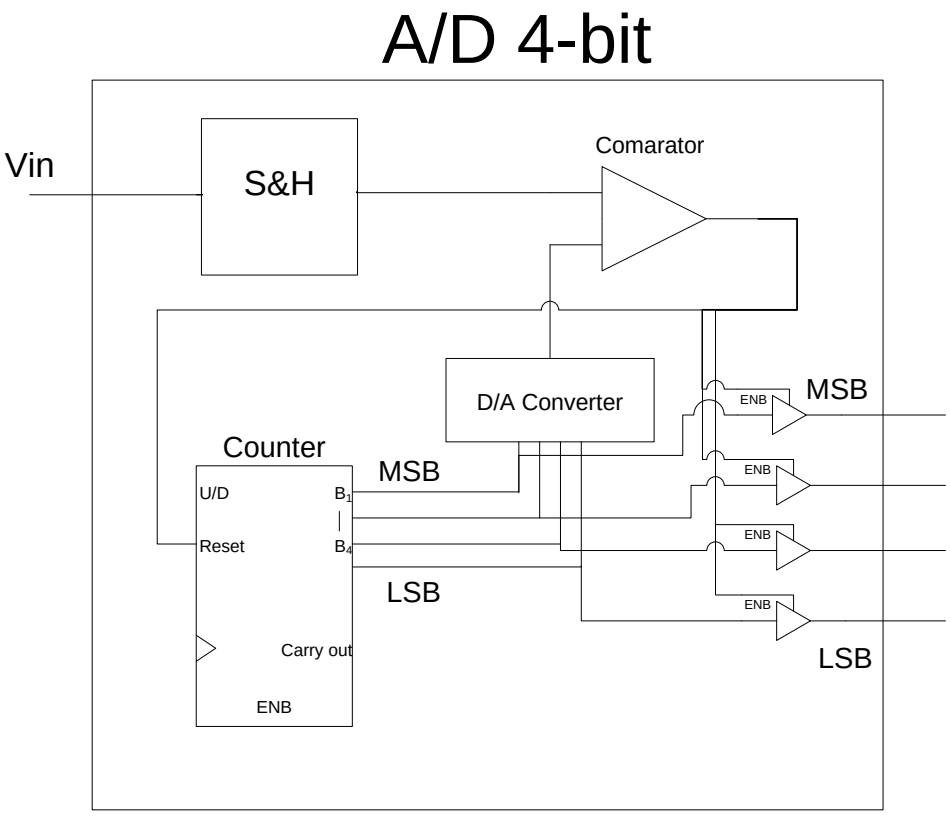


Figure 74

Q:

Design a clock divider by 3.

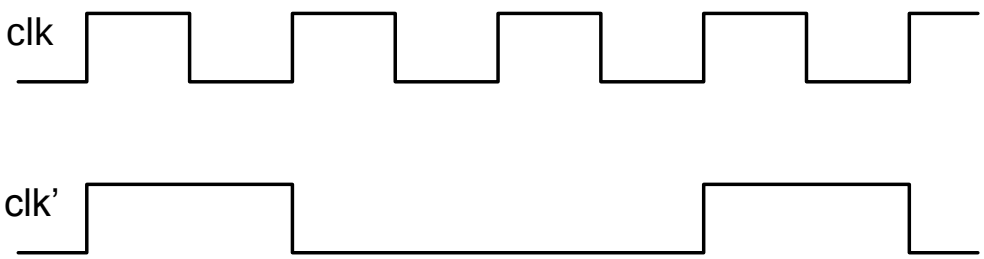


Figure 75

A:

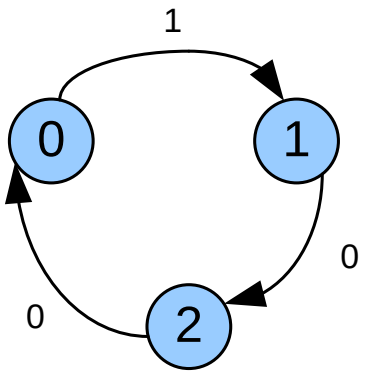


Figure 76

PS	**NS**	**out**
Q1Q2	D1D2	out
00	01	1
01	10	0
10	00	0

$$Q_2 = D_1$$
$$\overline{Q}_1\overline{Q}_2 = \left(Q_1 + Q_2\right)' = D_2$$
$$out = D_2$$

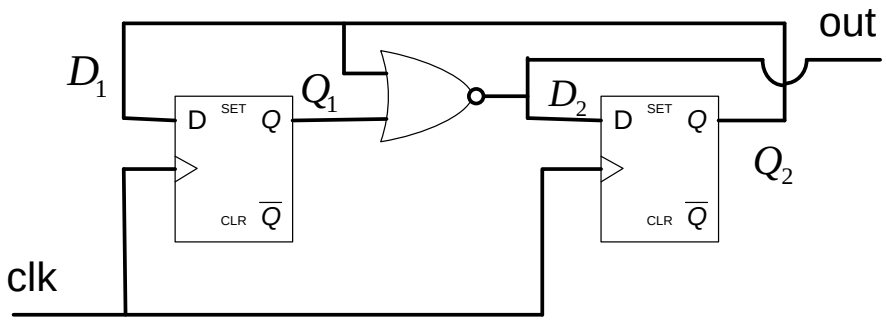


Figure 77

Q:

Design a circuit which gets a series of bits and outputs '1' when the series 101101 is present.

A:

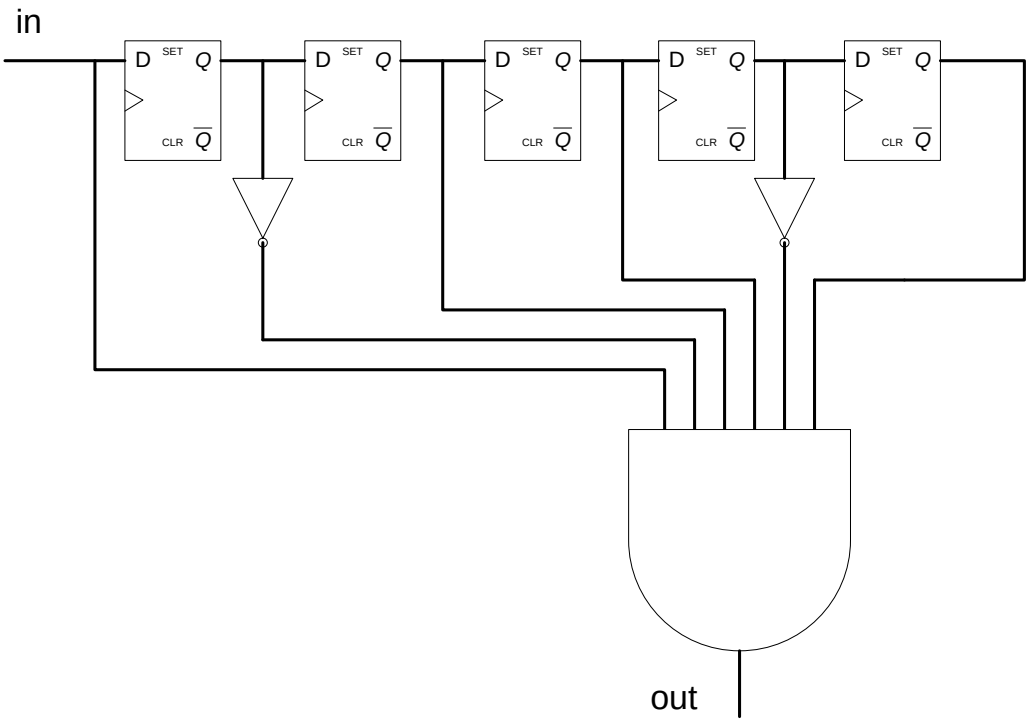


Figure 78

Circuit Design interview questions

Q:

A CMOS inverter is given. What should you in the transistors (NMOS and/or PMOS) parameters in order to shift the inverter curve right/left?

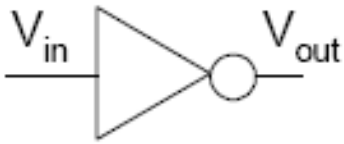


Figure 79

A:

If we strengthen the PMOS transistor by enlarging the PMOS W/L ratio, we strengthen the charging circuit as a result and the inverters curve shifts right and we obtain skewed high (SH) inverter. On the contrary, if we enlarging the W/L ratio of the NMOS transistor, while keeping the PMOS transistor unchanged. We make the inverters curve to shift left and as a result we obtain skewed low (SL) inverter.

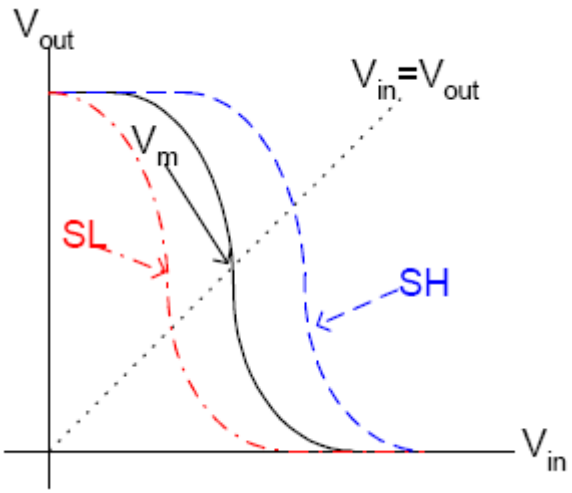


Figure 80

Q:

You have to implement a XOR using four transistors.

A:

$a \quad xor \quad b = a'b + ab'$

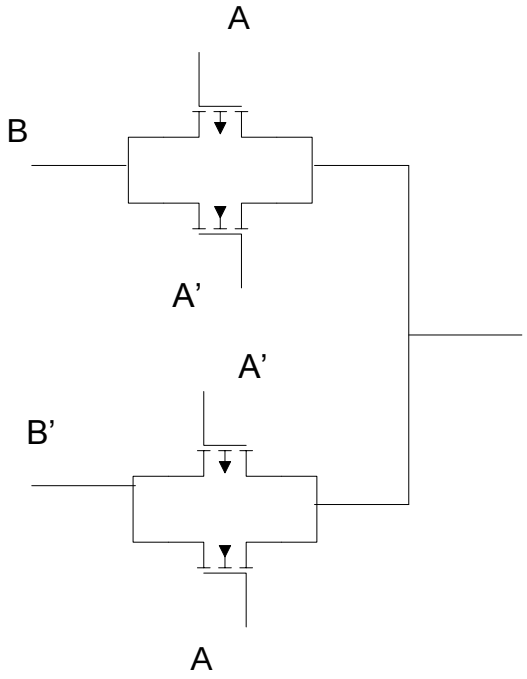


Figure 81

Q:

You have the following circuit. What is the condition that there will be no current through the R5 resistor?

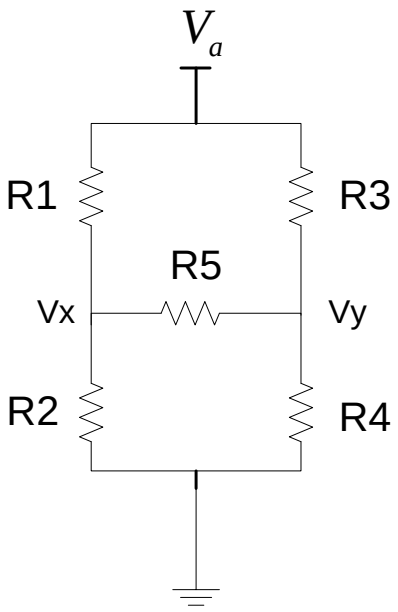


Figure 82

A:

If we are interested in, that there will be no current through R_5. We should demand that Vx=Vy.

$$V_x = \frac{R_2}{R_1 + R_2} \cdot V_a$$

$$V_y = \frac{R_4}{R_3 + R_4} \cdot V_a$$

$$\frac{R_2}{R_1 + R_2} = \frac{R_4}{R_3 + R_4}$$

$$R_1 R_4 + R_2 R_4 = R_2 R_3 + R_2 R_4$$

$$R_1 R_4 = R_2 R_3$$

$$\boxed{\frac{R_1}{R_2} = \frac{R_3}{R_4}}$$

Q:

How does it work? What is the circuit? What are the problems that may occur? How they can be fixed?

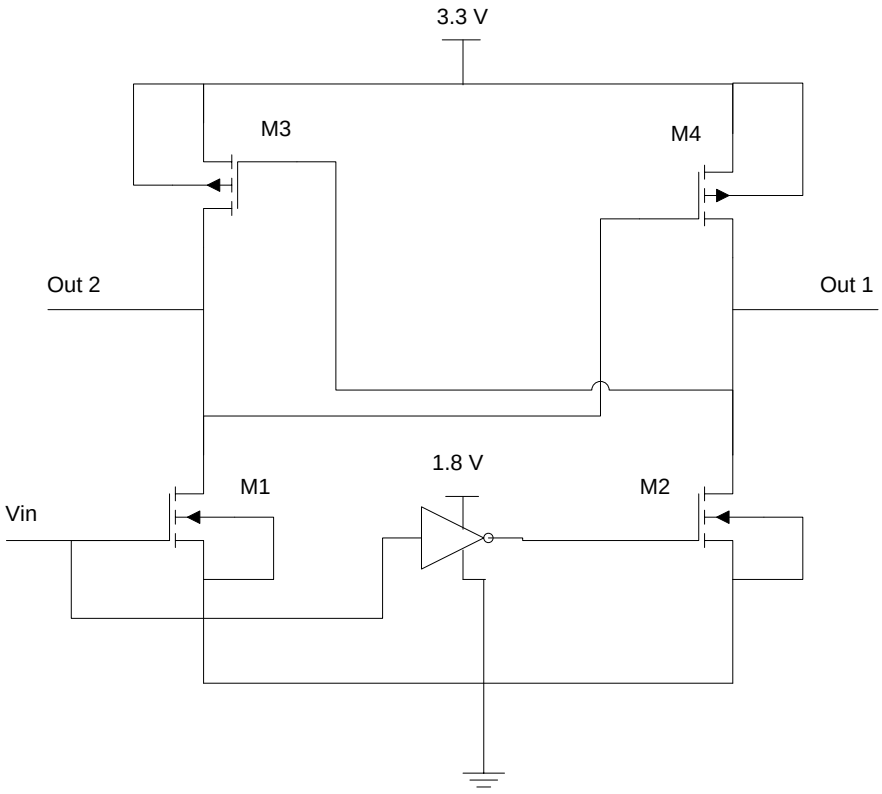


Figure 83

A:

If the input is high (1.8V), then the M1 transistor is on and the M2 transistor is off. We assume that consequently Out 2 is low and the M4 PMOS transistor is on, therefore the Out 1 is high (3.3V). As a result the M3 PMOS is off.

The circuit is a **level shifter**, which can make compatible systems with different logic voltages (1.8V to 3.3V).

In order that the circuit will work properly, the NMOS transistors must be stronger then PMOS ones, in other words W/L ratio of NMOS must be larger the W/L of PMOS.

Q:

Draw the voltages in the circuit versus time, when the input is a short pulse $(\Delta t << RC)$.

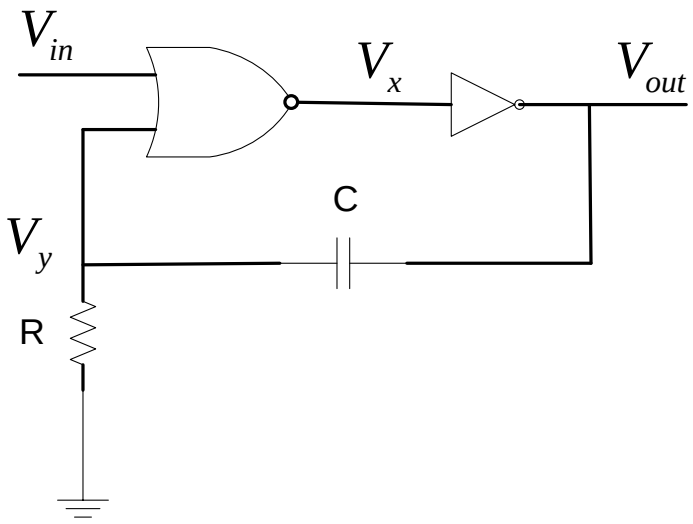


Figure 84

Assume that an inverter with EN input is connected to the second input of the NOR gate, as show below. How does the inverter change the circuit voltages?

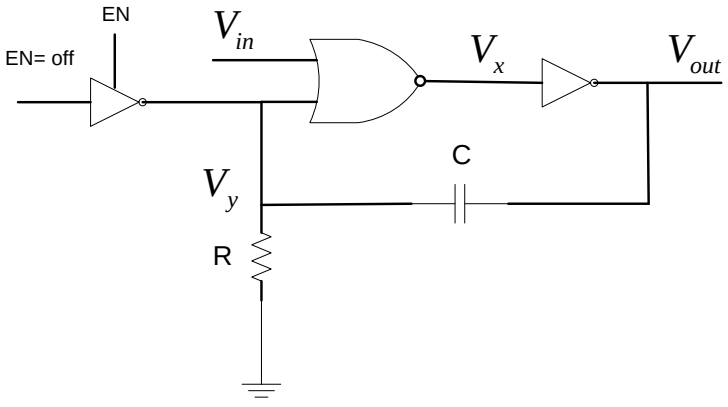


Figure 85

A:

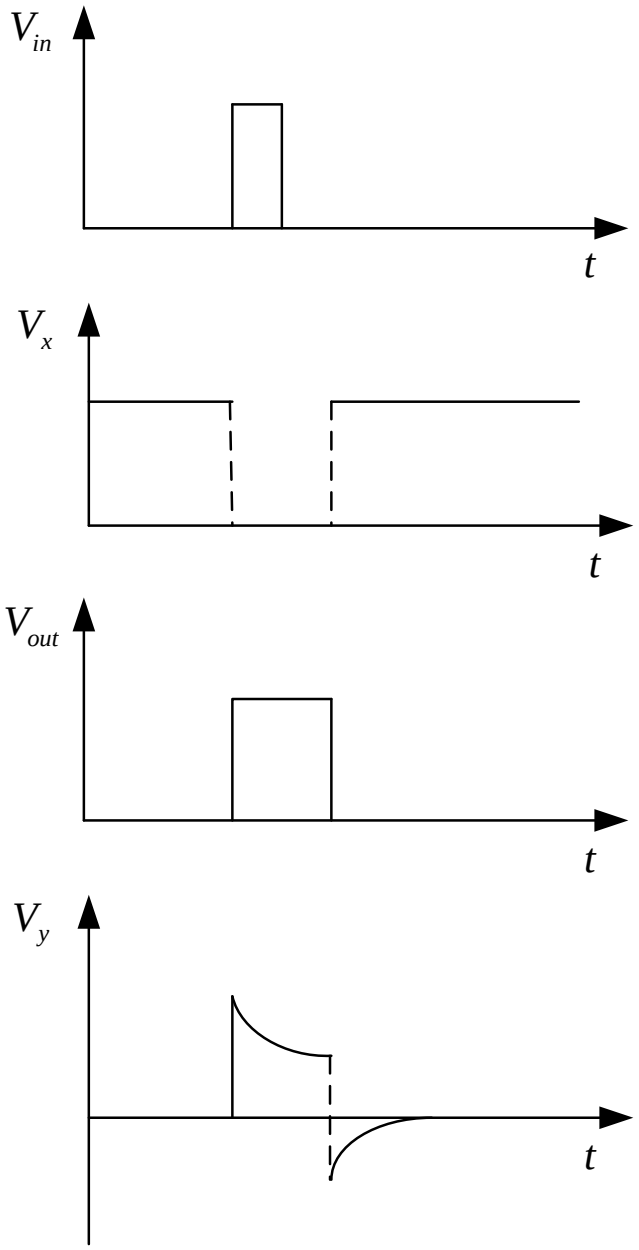


Figure 86

If we connect the inverter with the gate EN is off, as can be seen, the bottom NMOS transistor will conduct when Vy voltage is negative. The conductance occurs through the transistor channel and through the source bulk, since the source bulk diode is on, when the source potential is negative. As a result of the conductance the Vy voltage will return to zero potential faster, than if there is no input inverter.

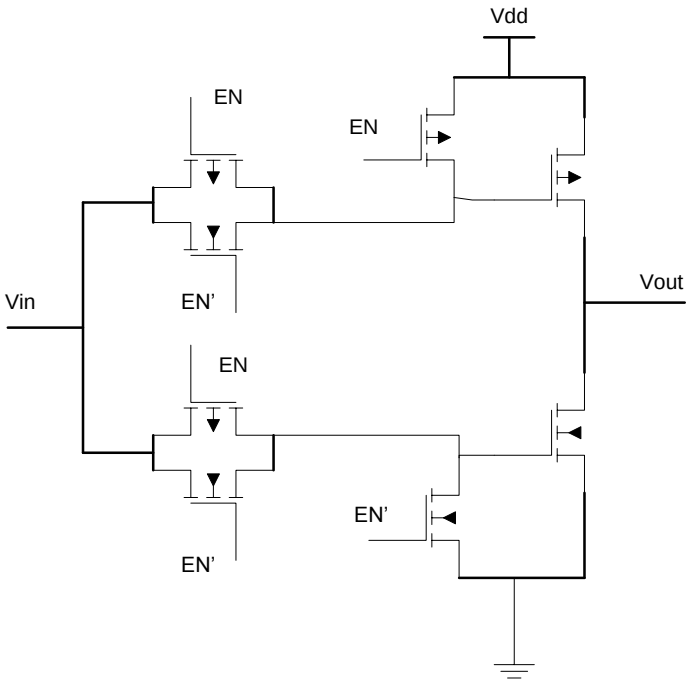


Figure 87

Q:

Draw the CMOS inverter on the wafer and draw the connection to the well and the bulk. Explain what parasitic elements can be formed in the inverter. Sketch them and explain the work principles.

A:

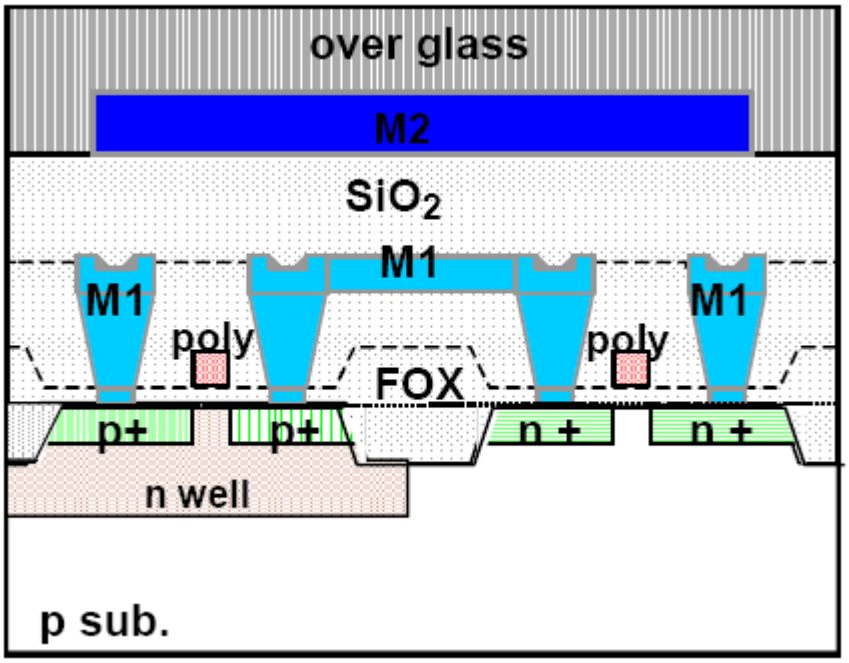


Figure 88

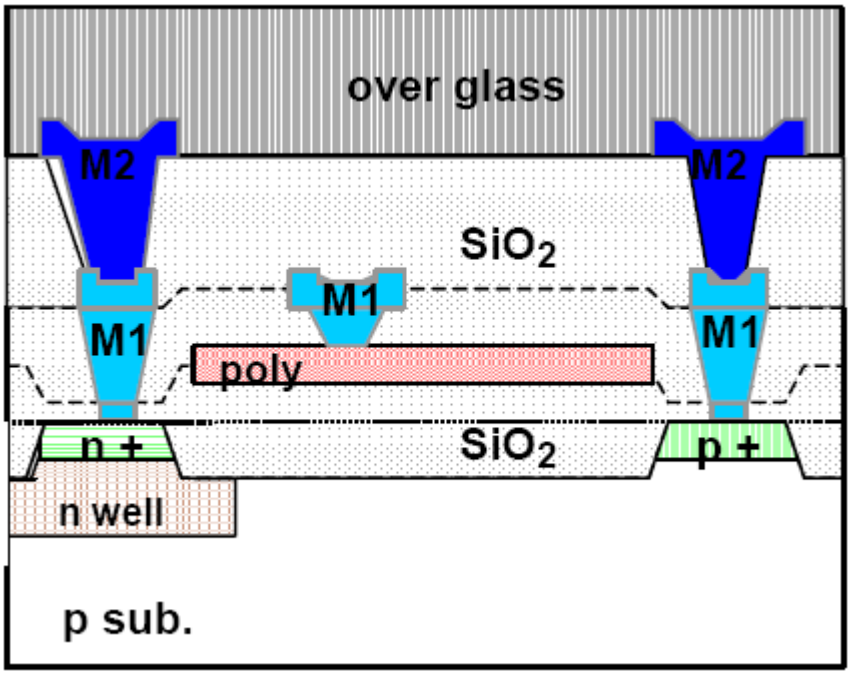


Figure 89

The parasitic element that is formed in the inverter is the SCR (pnpn) element, which can be formed of two bipolar transistors, pnp and npn.

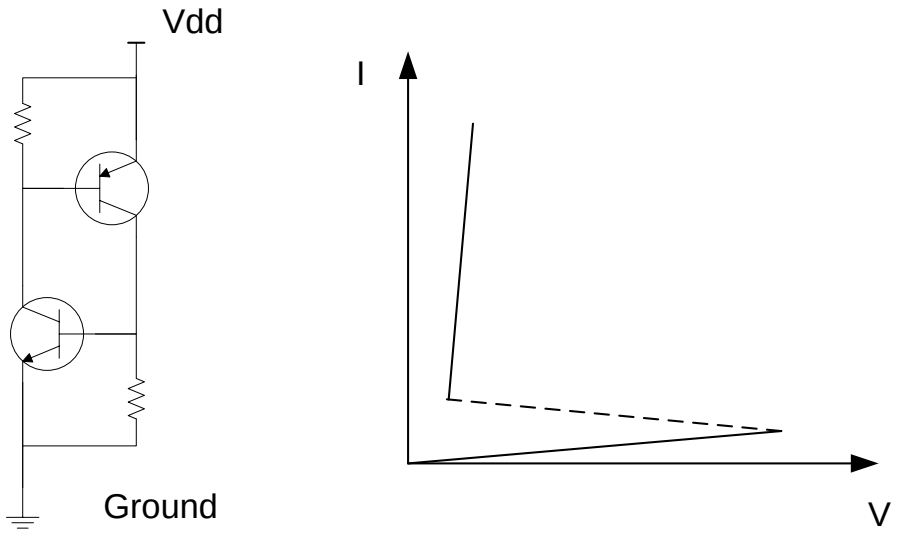


Figure 90

Q:

Design a black box which output capacity is C, 2C, 3C….10C in accordance with the input control bits.

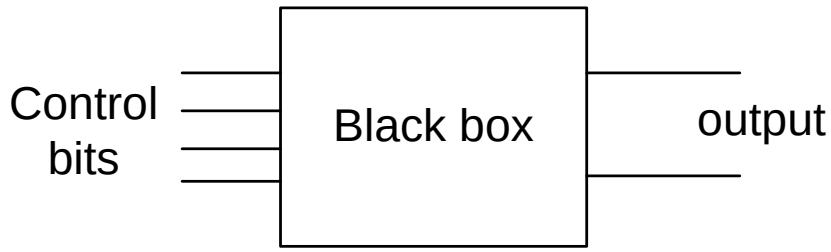


Figure 91

A:

We have to use capacitance reference block set such as depicted below:

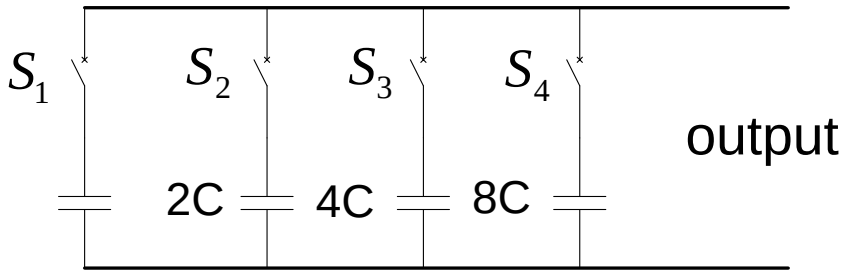


Figure 92

To achieve the desired output capacitance the control bits should be as follow:

Output capacitance	S_4	S_3	S_2	S_1
C	0	0	0	1
2C	0	0	1	0
3C	0	0	1	1
4C	0	1	0	0
5C	0	1	0	1
6C	0	1	1	0
7C	0	1	1	1
8C	1	0	0	0
9C	1	0	0	1
10C	1	0	1	0

Q:

The following circuit is given:

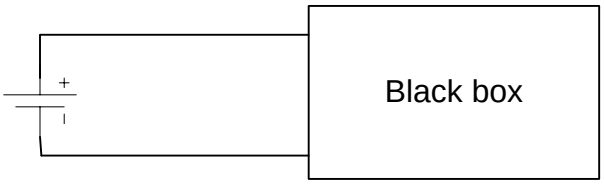


Figure 93

Design a system, which can measure the current that the system consumes (No ampere meter can be used).

A:

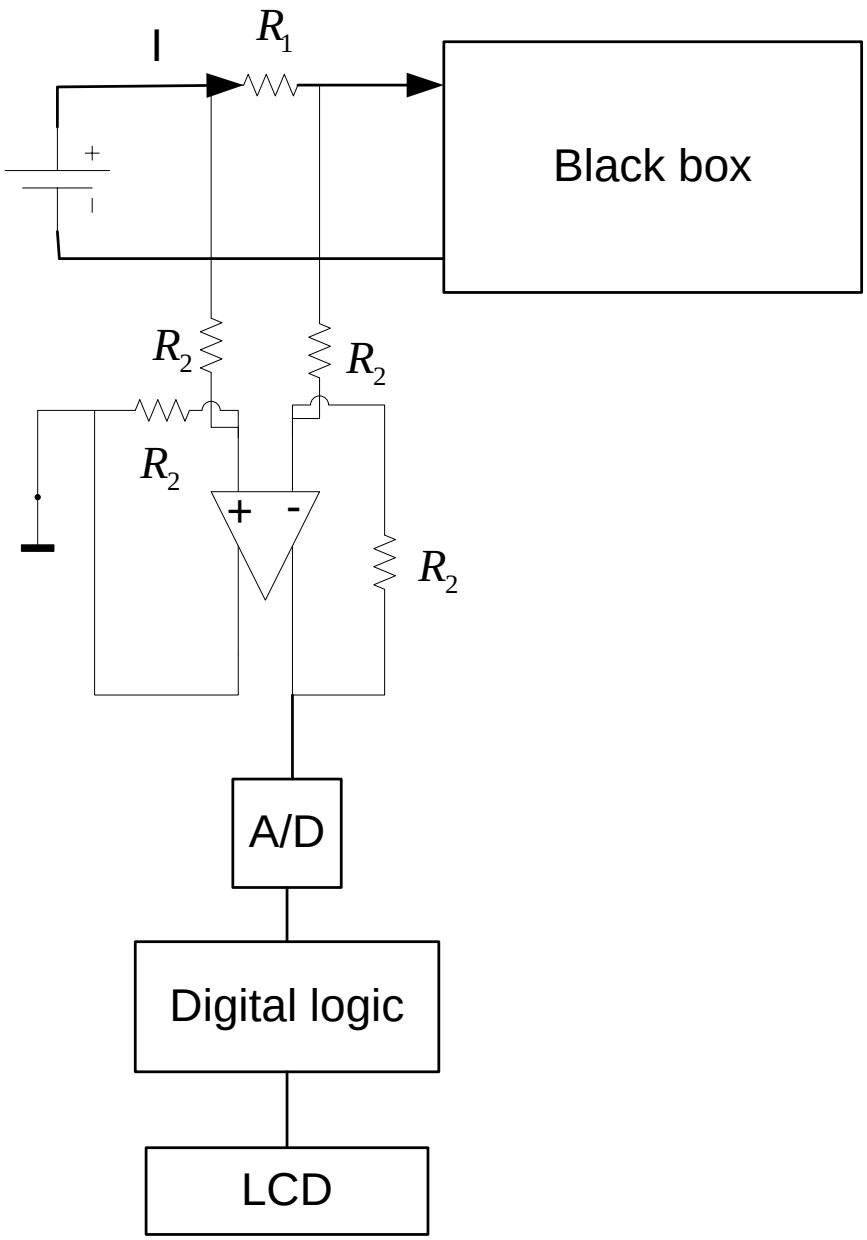


Figure 94

Q:

A diode bridge is given:

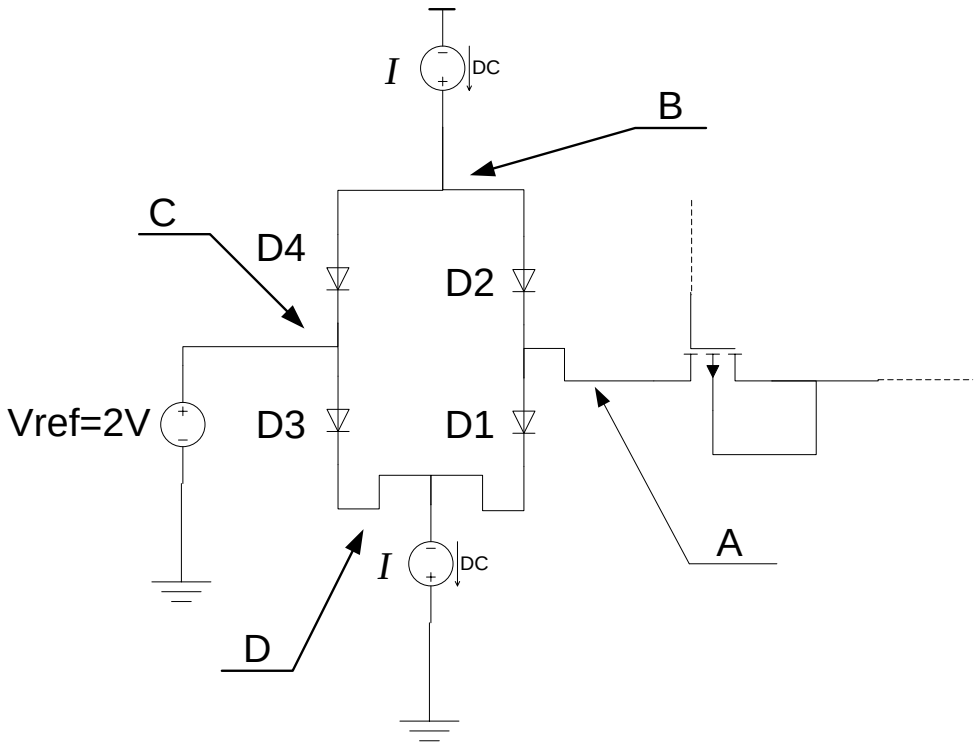


Figure 95

The voltage at the A junction is measured and the result is $V_{measured} = 2.5V$. We would like to determine, which diode branch the current flows through.

A:

Since the A junction voltage is 2.5 V, the B junction voltage is ought to be 3.2V in order the D2 diode to conduct. However, since the reference voltage is only 2V, the B junction voltage would be 2.7V. As a result the D2 diode will not conduct, but D4 diode will do.

Let's analyze the D junction. In order the D1 diode to conduct the voltage at the D junction ought to be 1.8V. On the other hand, for the D3 diode to conduct the voltage at the D junction should be 1.3V. Consequently, the D1 diode will conduct, whereas the D3 diode will not.

Q:

The following circuit is given:

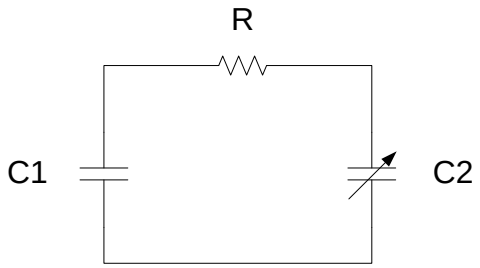


Figure 96

When $t = 0^-$

$C_1 = C_2 = C$
$Q_1 = Q_2 = Q$
$V_1 = V_2 = V$

At time $t = 0^+$ the capacitance C_2 is reduced by 3. Draw the voltage on C_2 capacitor versus time.

A:

$\frac{1}{3}C_1 = C_2 = \frac{1}{3}C$
$Q_1 = Q_2 = Q$
$V_2' = \frac{Q_2}{\frac{1}{3}C} = 3V$
$V_1 = V_1' = V$

At time $t = 0^+$ a current starts flowing from C_2 capacitor to C_1 capacitor.

When $t \to \infty$, voltage on both capacitors is the same and no current will flow through the resistor.

$$V_{final} = \frac{Q_{total}}{C_{total}} = \frac{2Q}{C + \frac{1}{3}C} = \frac{3}{2}V$$

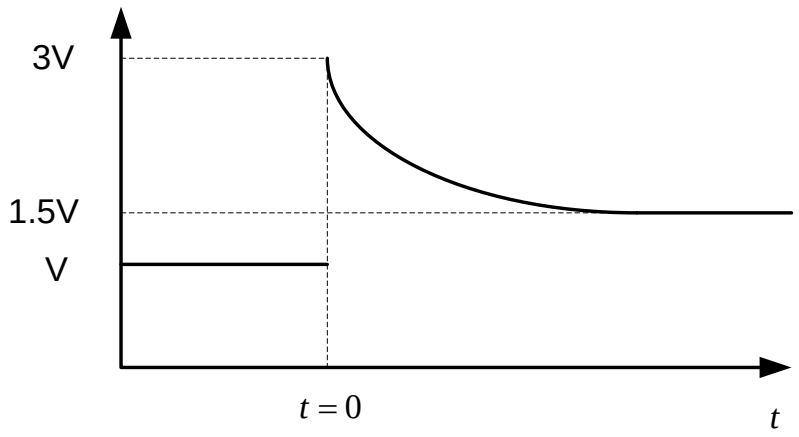


Figure 97

Q:

How does an oscilloscope work? Explain its principals of action.

A:

The main part of an oscilloscope is s tube. The angle of electrons ray is determined by applying a potential between two pairs of plates on both sides of the tube. One pair of plates is for controlling the vertical ray deviation and the other pair is for controlling horizontal deviation. In the oscilloscope the vertical axis is for presenting the input voltage and the horizontal axis is for presenting time. In order to present a n input signal versus time, the vertical plates get a potential proportional to the input potential, whereas the horizontal plates acquire a saw like signal from a generator. See picture below. It is possible to change the voltage scale by attenuator installed at the oscilloscope input. The time scale can be changed by changing the generators signal period.

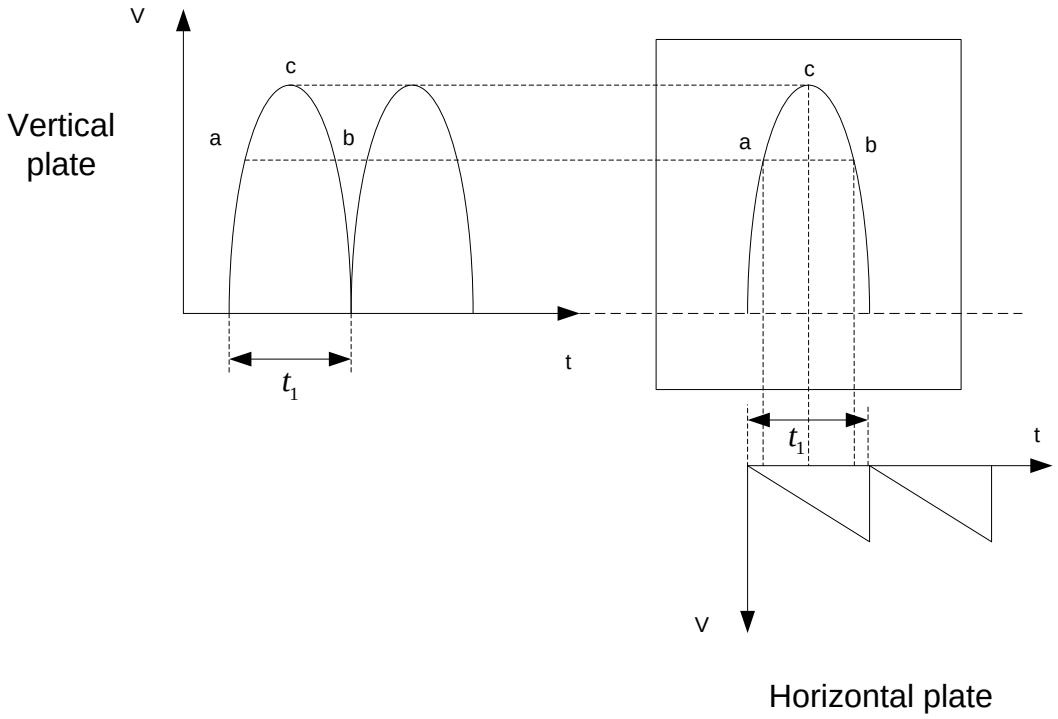


Figure 98

Q:

a) What is the voltage on the capacitors if the switch is on.

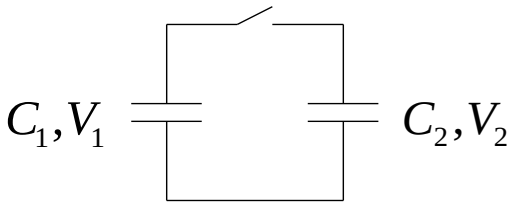


Figure 99

b) What is the Vx when $t \to \infty$

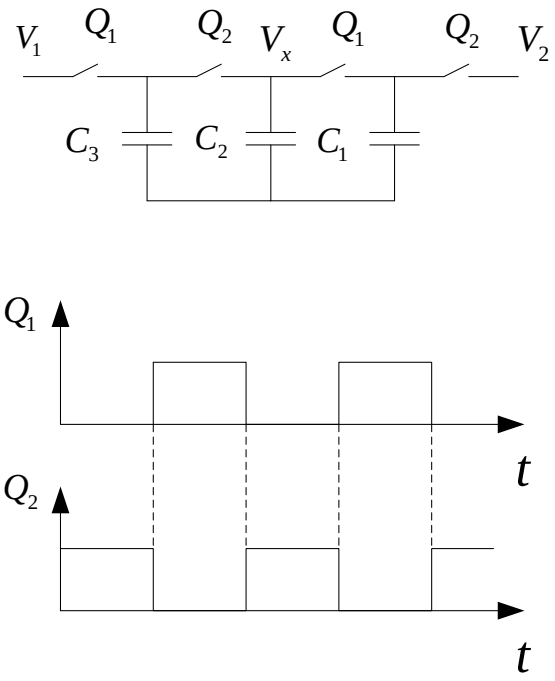


Figure 100

A:

a)

$$V_{final} = \frac{Q_{total}}{C_{total}} = \frac{C_1V_1 + C_2V_2}{C_1 + C_2}$$

b)

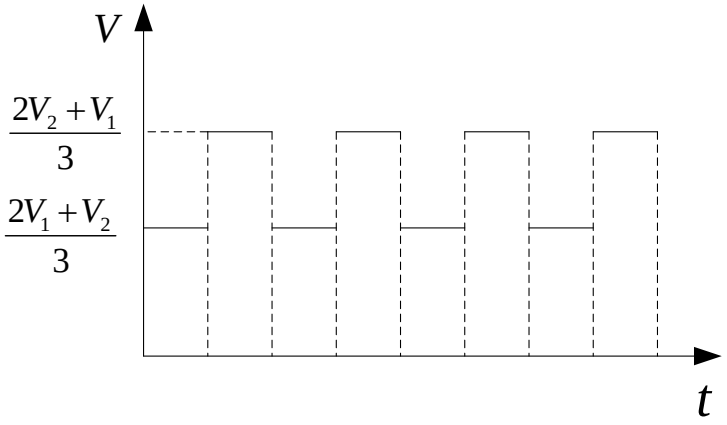


Figure 101

Q:

A CMOS inverter is given, when the n-channel transistor's width is larger by 2 times, than the p-channel transistor's width. Complete the following graphs.

Assume the electron mobility is larger by factor two, than holes mobility.

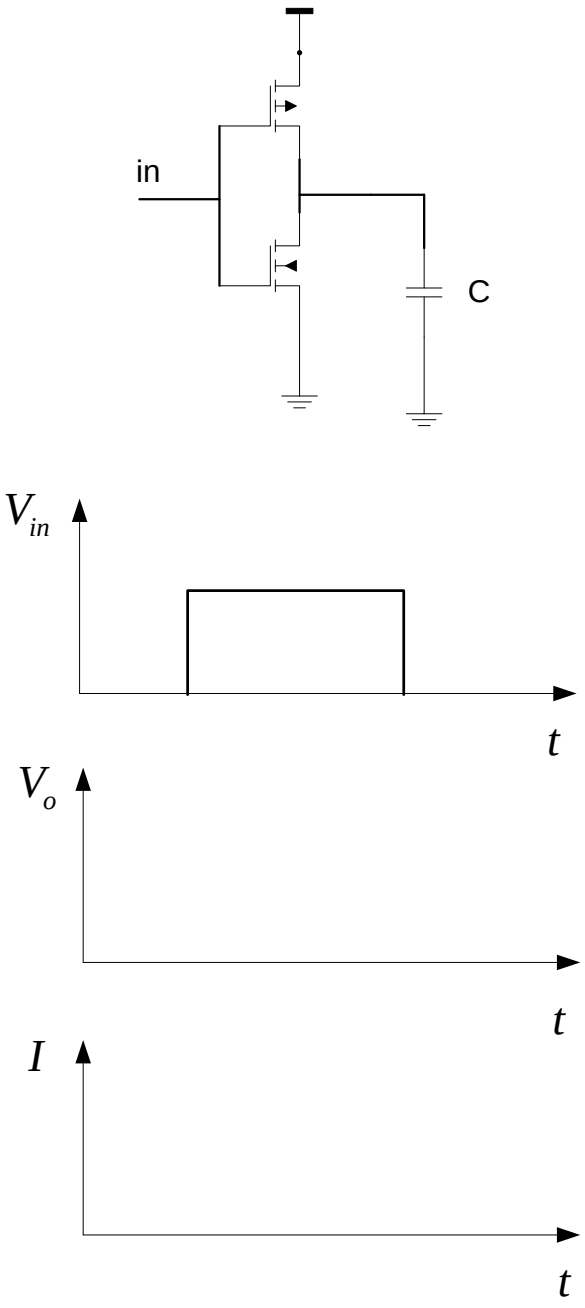


Figure 102

A:

$$I = \frac{K}{2}\left[2\left(V_{GS} - V_T\right)V_{DS} - {V_{DS}}^2\right]$$

$$\frac{1}{R_{eff}} = \frac{dI}{dV_{DS}} \approx K\left(V_{GS} - V_T\right)$$

$$R_{eff} = \frac{1}{K\left(V_{GS} - V_T\right)} = \frac{1}{K\left(V_{DD} - V_T\right)}$$

$$\tau(NMOS) = R_{eff}(NMOS)C = \frac{C}{C_{ox}\mu_e \frac{2W}{L}\left(V_{DD} - V_T\right)}$$

$$\tau(PMOS) = R_{eff}(PMOS)C = \frac{C}{C_{ox}\mu_h \frac{W}{L}\left(V_{DD} - V_T\right)}$$

$$\Rightarrow \tau(NMOS) = \frac{1}{4}\tau(PMOS)$$

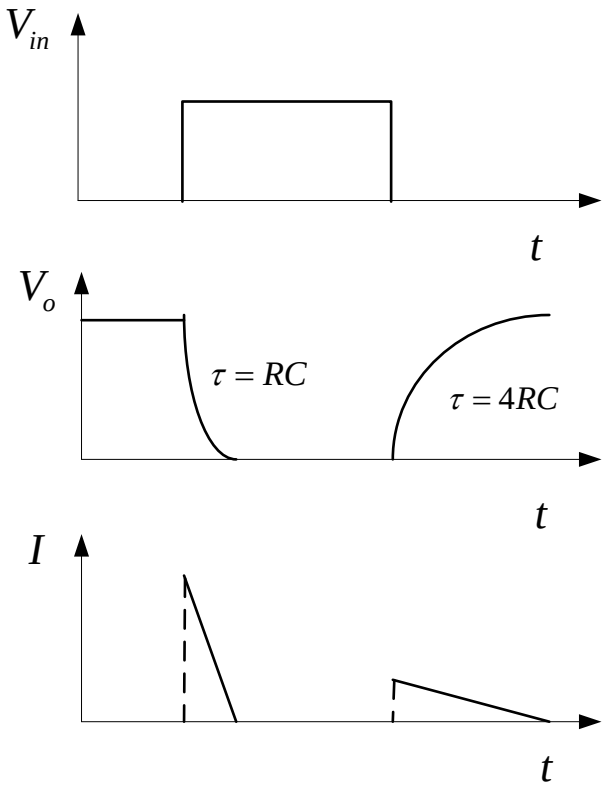


Figure 103

Q:

The following circuit is given:

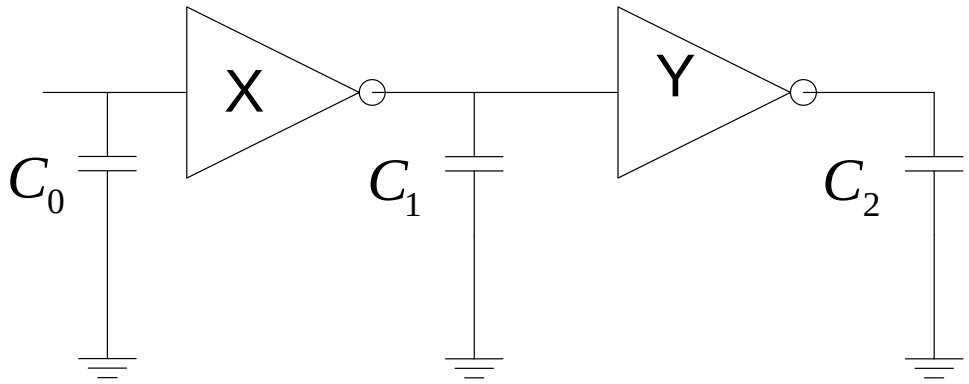


Figure 104

The X invertor's channel is constant. Draw the time delay versus the Y invertor channel's width.

A:

$$d_{abs} = \tau\left(f_1 + f_2\right) = \tau\left(h_1 g_1 + h_2 g_2\right)$$

$$g_1 = g_2 = 1$$

$$d_{abs} = \tau\left(h_1 + h_2\right) = \tau\left(\frac{c_1}{c_0} + \frac{c_2}{c_1}\right)$$

$$c = \left(1 + b\right) W L C_{ox}$$

$$d_{abs} = \tau\left(\frac{W}{W_0} + \frac{W_2}{W}\right)$$

If derive the delay with W and compare to zero, we obtain the W for minimal delay.

$$W_{opt} = \sqrt{W_0 W_2}$$

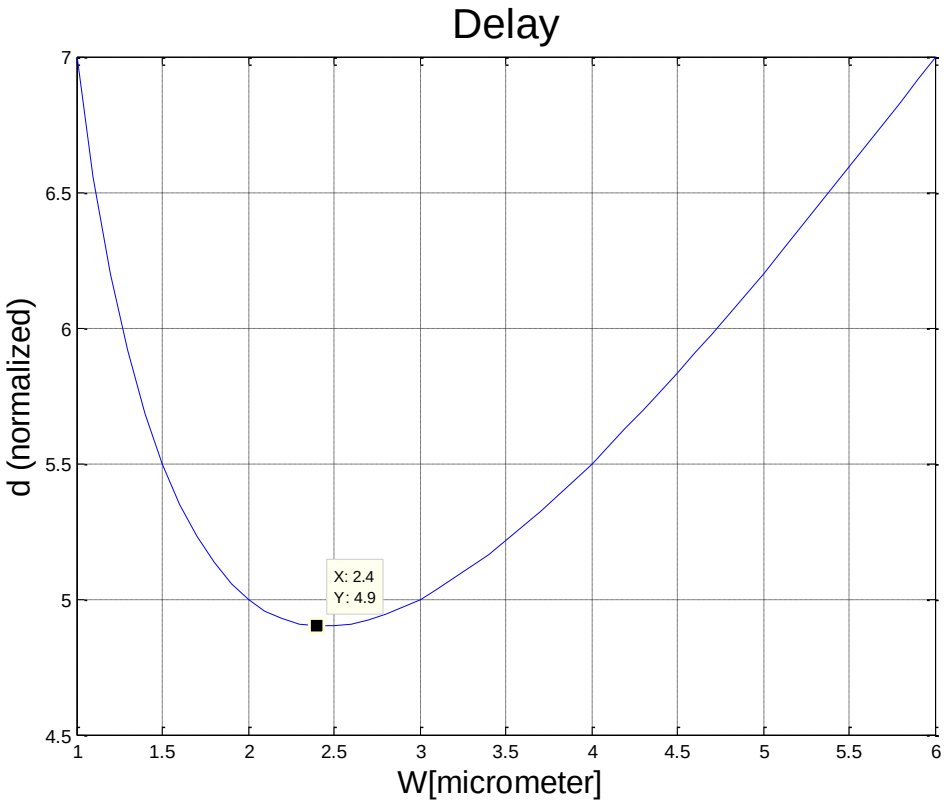


Figure 105

Q:

A transmission line with characteristic impedance of 50Ω is given:

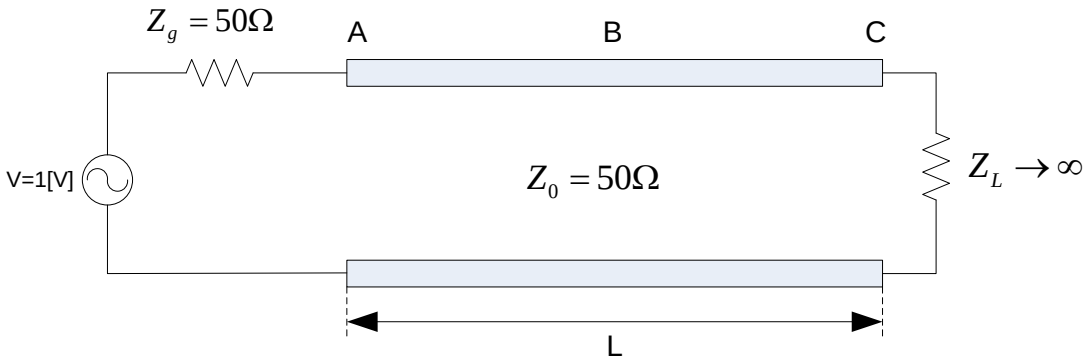


Figure 106

The propagation time from the beginning of the transmission line to the end is 2T. The A point is located at the left edge of the line, the B point is in the middle of

the line and the C point is at the right edge of the line. Draw the voltage propagation through the transmission line versus time.

A:

Since the load to the transmission line is infinitive, the reflection coefficient at the load is 1.

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} = 1$$

In other words the wave returns with the same phase and amplitude.

$$V(t=0) = \frac{Z_0}{Z_g + Z_0} V_{in} = \frac{50}{50+50} V_{in} = \frac{1}{2}[V]$$

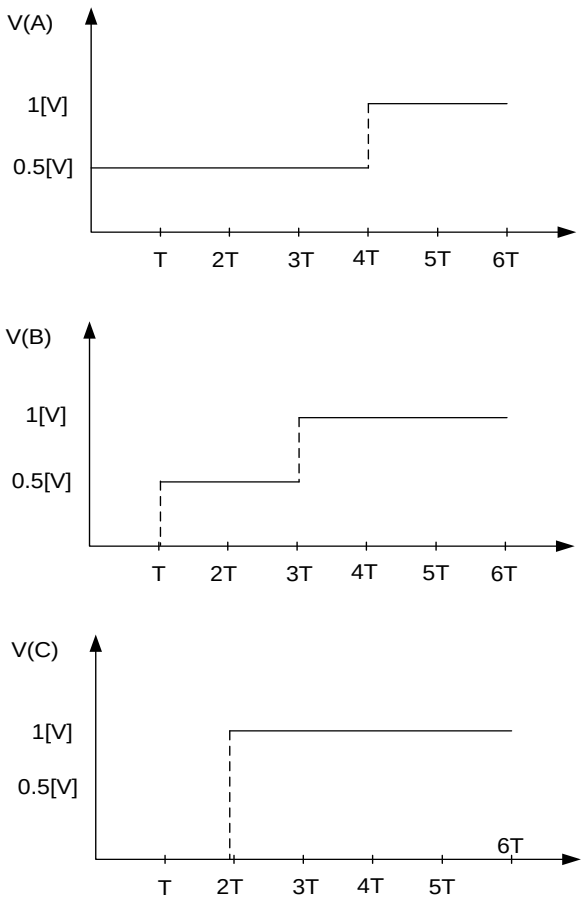


Figure 107

Q:

The parameters of the circuit depicted above are:

V=100[V]
The current measured is 200A,

The copper wires have length of $L = 1m$ and resistance given by $R_w = \rho \frac{L}{S}$.
The maximal current that the wire is capable to conduct is 20A. An unknown resistance is given.

a) Compose a circuit to measure the unknown resistance.
b) Calculate the unknown resistance.

A:
a)

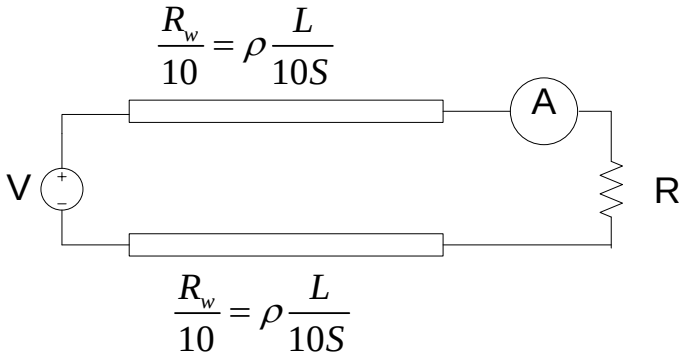


Figure 108

b)

$$V = I \cdot \left[R_w + R_w + R \right] = I \cdot \left[\rho \frac{L}{10S} + \rho \frac{L}{10S} + R \right] = I \cdot \left[\rho \frac{L}{5S} + R \right]$$

$$R = \frac{V}{I} - \rho \frac{L}{5S} = \frac{1}{2} = \rho \frac{1}{5S}$$

Q:

The following circuit is given:

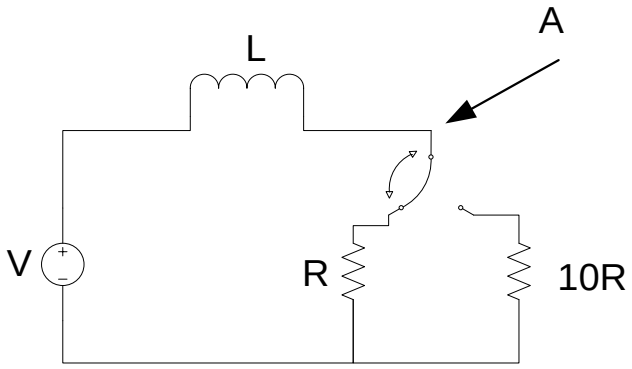


Figure 109

Draw the voltage and the current before and after the switching.

A:

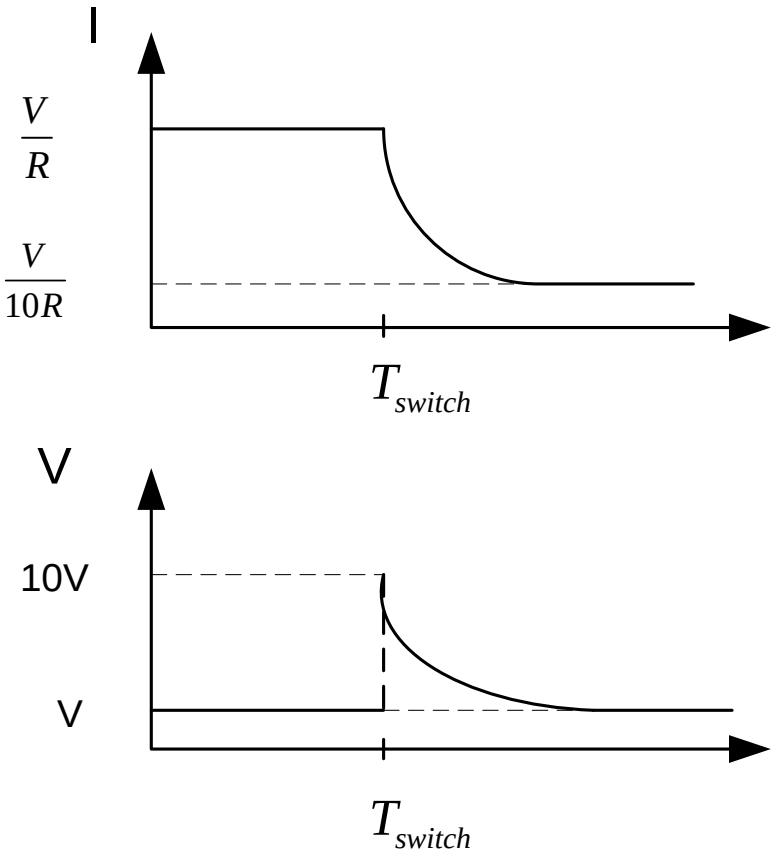
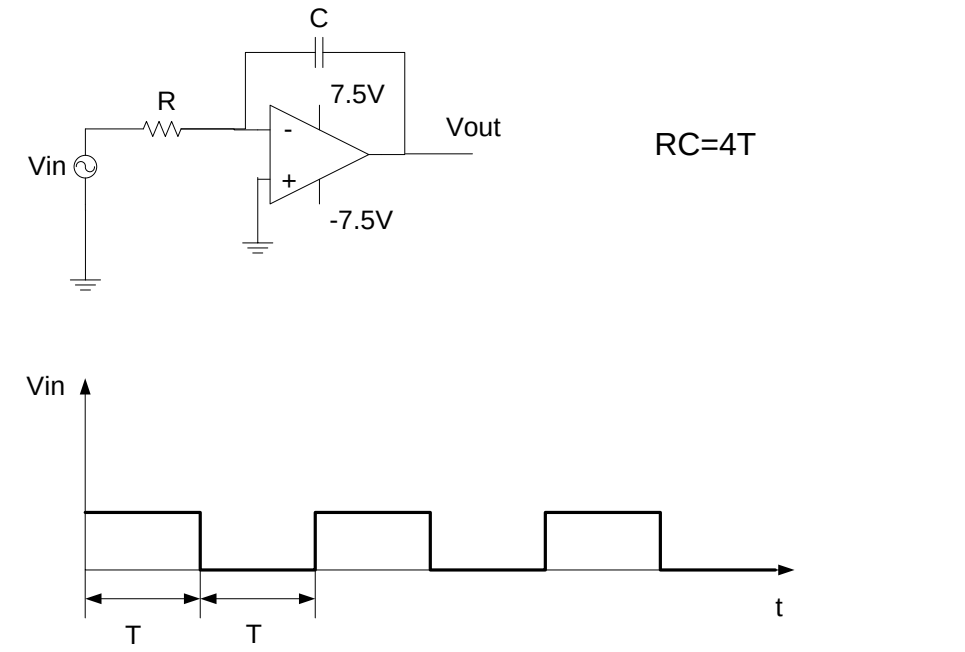


Figure 110

Q:

What is the output of the integration circuit? The input V_{in} is as depicted below with amplitude of 10[V]. Look at the drawing below:



A:

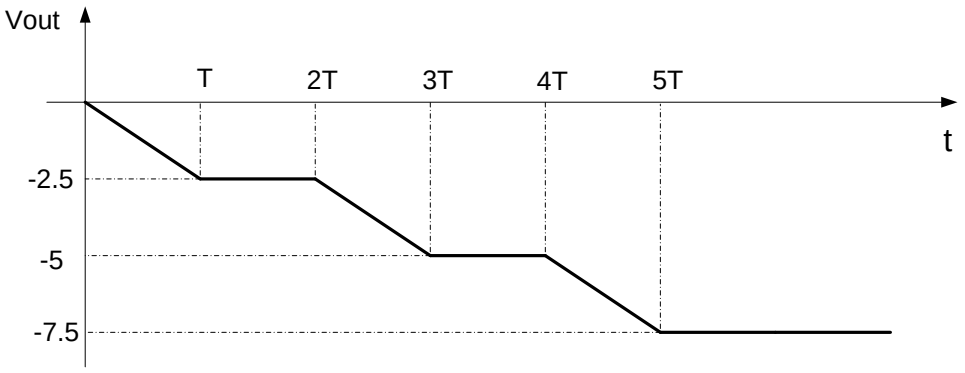


Figure 111

Q:

Design a circuit whose input is two sinusoidal signals and output is DC voltage. The amplitude of the voltage should be a function of phase difference between these two input signals.

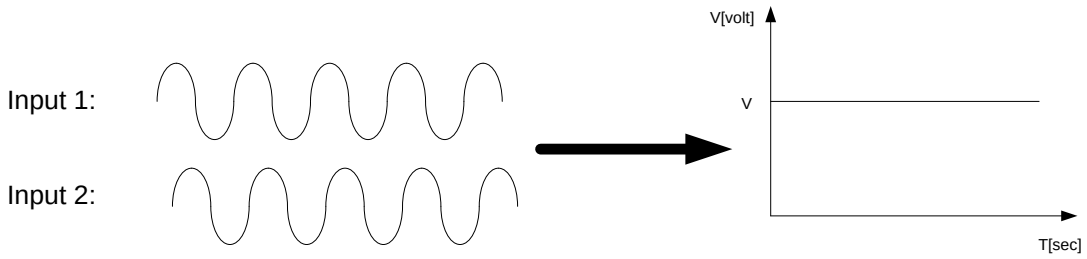
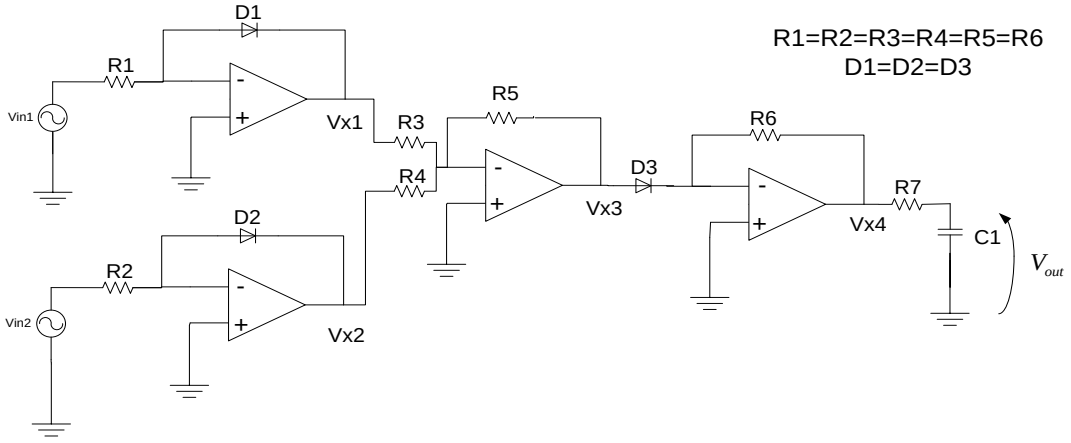


Figure 112

A:



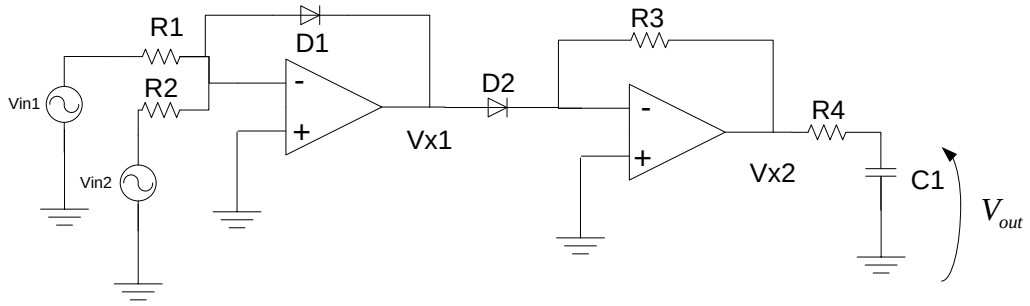
$$V_{x1}=-\frac{KT}{q}Ln\left[\frac{V_{in1}}{RI_0}+1\right]\approx-\frac{KT}{q}Ln\left[\frac{V_{in1}}{RI_0}\right];\ V_{x2}=-\frac{KT}{q}Ln\left[\frac{V_{in2}}{RI_0}+1\right]\approx-\frac{KT}{q}Ln\left[\frac{V_{in2}}{RI_0}\right]$$

$$V_{x3}=\frac{KT}{q}Ln\left[\frac{V_{in1}V_{in2}}{R^2{I_0}^2}\right];\ V_{x4}=-RI_0\left(e^{\frac{qV_{x3}}{KT}}+1\right)\approx-\left[\frac{V_{in1}V_{in2}}{RI_0}\right]=-\left[\frac{{V_0}^2}{RI_0}\right]\left(\sin(\omega t)\cdot\sin\left(\omega t+\phi\right)\right)$$

$$V_{x4}=-\left[\frac{{V_0}^2}{RI_0}\right]\left(\sin(2\omega t+\phi)+\sin\left(\phi\right)\right);\ Vout=-\left[\frac{{V_0}^2}{RI_0}\right]\left(\frac{\sin(2\omega t+\phi)}{j\omega R_y C+1}+\sin\left(\phi\right)\right)$$

Figure 103

Another implementation is:



$$V_{x1} = -\frac{KT}{q} Ln\left[\frac{V_{in1}}{RI_0} + 1\right] - \frac{KT}{q} Ln\left[\frac{V_{in2}}{RI_0} + 1\right] \approx -\frac{KT}{q} Ln\left[\frac{V_{in1}V_{in2}}{R^2 {I_0}^2}\right]$$

$$V_{x2} = RI_0\left(e^{\frac{qV_{x1}}{KT}} + 1\right) \approx \left[\frac{V_{in1}V_{in2}}{RI_0}\right] = \left[\frac{{V_0}^2}{RI_0}\right]\left(\sin(\omega t)\cdot\sin\left(\omega t + \phi\right)\right)$$

$$V_{x2} = \left[\frac{{V_0}^2}{RI_0}\right]\left(\sin(2\omega t + \phi) + \sin\left(\phi\right)\right);\ Vout = -\left[\frac{{V_0}^2}{RI_0}\right]\left(\frac{\sin(2\omega t + \phi)}{j\omega R_4 C + 1} + \sin\left(\phi\right)\right)$$

Figure 104

Also a mixer and LPF can be used:

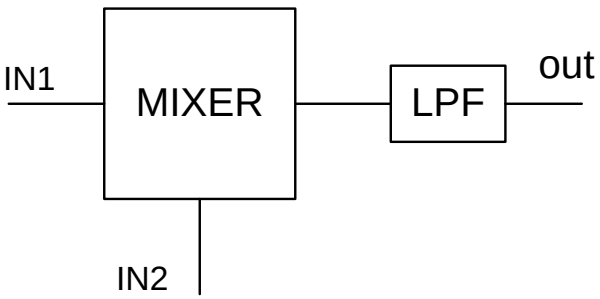


Figure 105

Q:

What is the output of the following circuit, when the input is a pulse? Look at the drawing below:

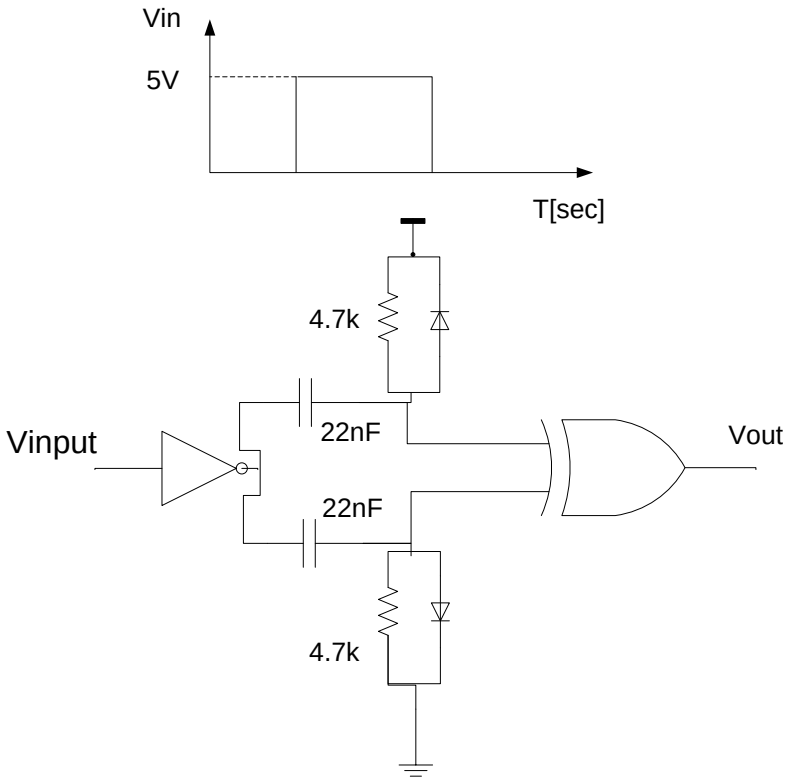


Figure 106

A:

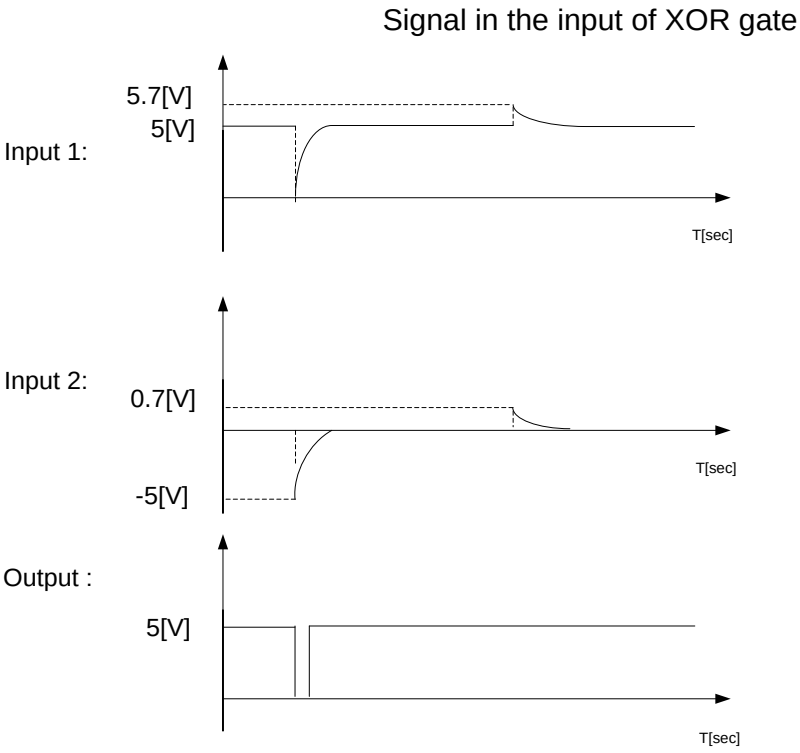


Figure 107

Q:

Design a circuit, so that you could measure the following pulse. Look at the drawing below:

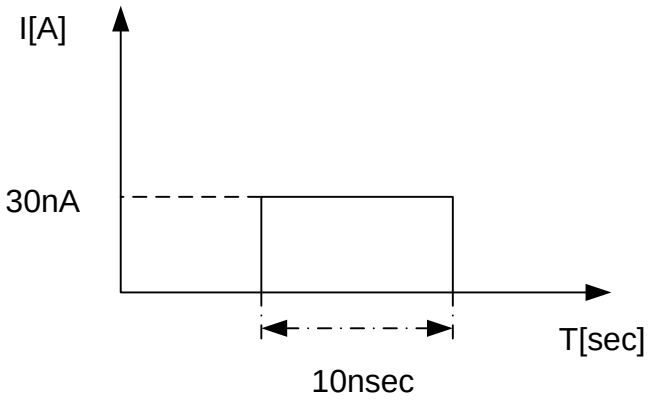


Figure 108

A:

Input capacitance of an amplifier is C=2pF

Bandwidth of an amplifier is BW=50MHz

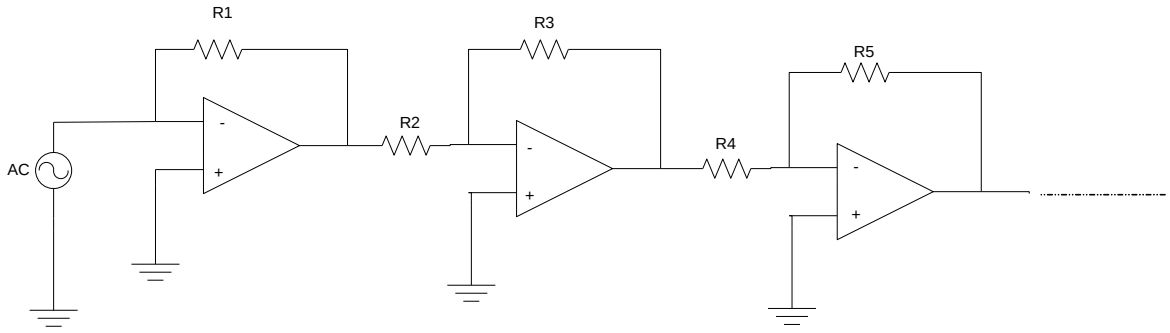


Figure 109

$V_1 = -R_1 I_{in}$

$10[n\sec]/N = R_1 C_{amp} \xrightarrow{N=5} R_1 = 1k\Omega$

$V_1 = 1k\Omega \times 30nA = -30\mu V$

The same considerations lead us to values of and $R_3 = 1k\Omega$ $R_5 = 1k\Omega$

$$V_2 = -\frac{R_3}{R_2} V_1$$

We'll take $R_2 = 250\Omega$ => $V_2 = \frac{1k\Omega}{250\Omega} 30\mu V = 120\mu V$

$$V_{out} = 4^{(N-2)} \times V_2 = 64 \cdot 120\mu V = 7.68mV$$

Q:

Design a CMOS circuit, which implements $\overline{(A+B)\cdot C}$ logic function.

A:

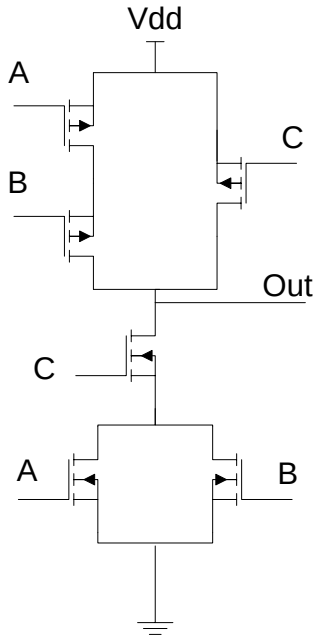


Figure 110

Q:
You have the following circuit:

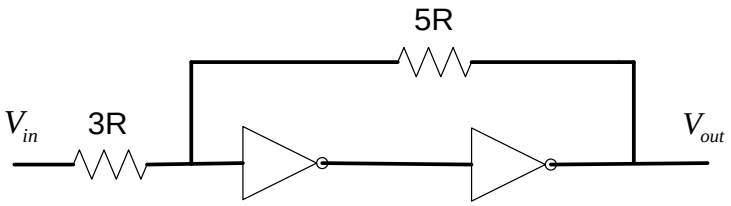


Figure 111

Those two inverters are ideal with the following curve:

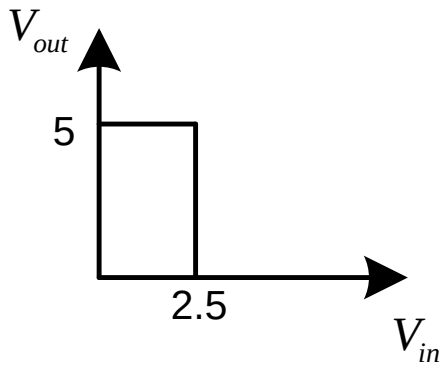


Figure 112

A:

We rise gradually the input potential V_{in} and when the V_x potential reaches 2.5V, the output voltage rises to 5V.

$$V_x = \frac{5R}{3R+5R}V_{in} = \frac{5}{8}V_{in}$$

$$V_{in} = \frac{8}{5}V_x = \frac{8}{5}\cdot 2.5 = 4[V]$$

On the other hand, when we decrease gradually the input potential, the output voltage drops only when the V_x potential reaches 2.5 V.

$$V_x = \frac{3R}{3R+5R}\left(V_{out} - V_{in}\right) + V_{in} = \frac{3}{8}\left(V_{out} - V_{in}\right) + V_{in}$$

$$V_x = \frac{3}{8}V_{out} - \frac{5}{8}V_{in}$$

$$V_{in} = \frac{8}{5}\left[\frac{3}{8}V_{out} - V_x\right] = \frac{3}{5}V_{out} - \frac{8}{5}V_x = \frac{3}{5}\cdot 5 - \frac{8}{5}\cdot 2.5 = 1[V]$$

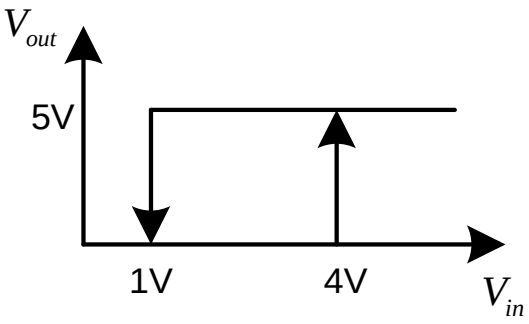


Figure 113

Q:

Implement D-latch using CMOS technology.

A:

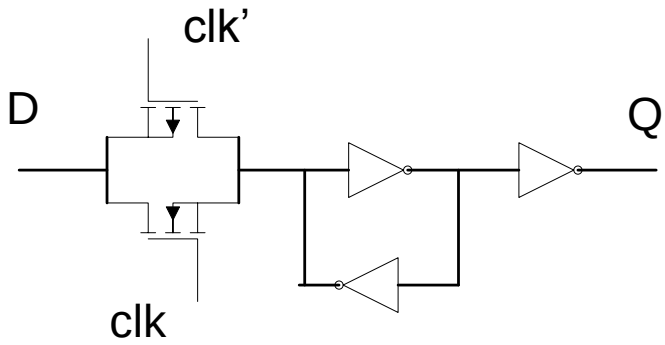


Figure 114

Q:
Implement a HPF and LPF using capacitor with resistor network and inductor with resistor network.

A:

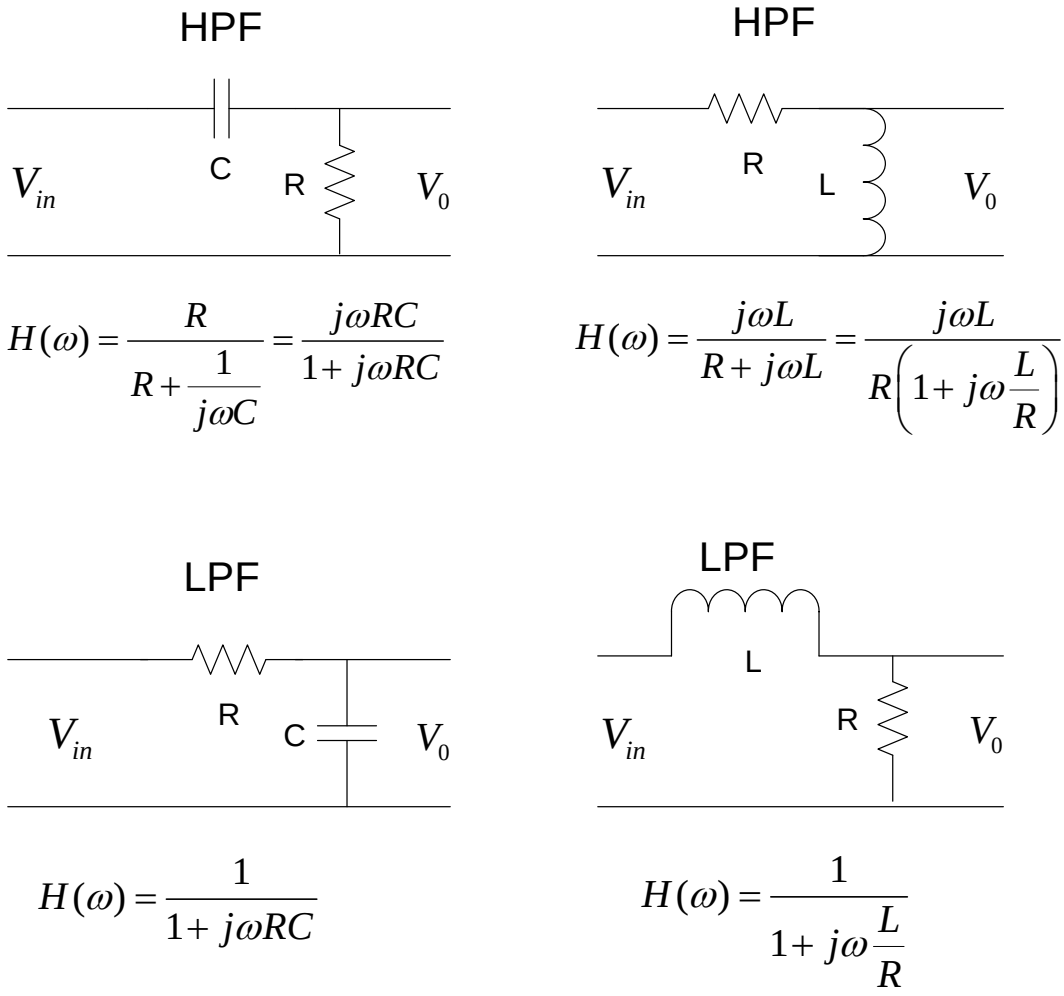


Figure 115

Q:
What does the circuit do? Draw the voltages marked versus time.

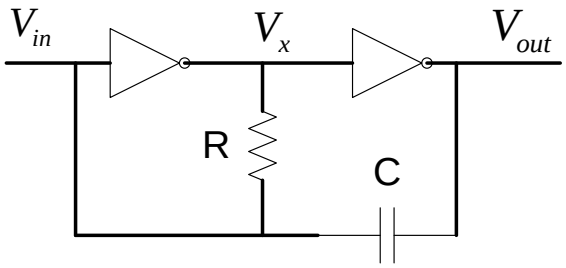


Figure 116

A:
The circuit implements a multivibrator.

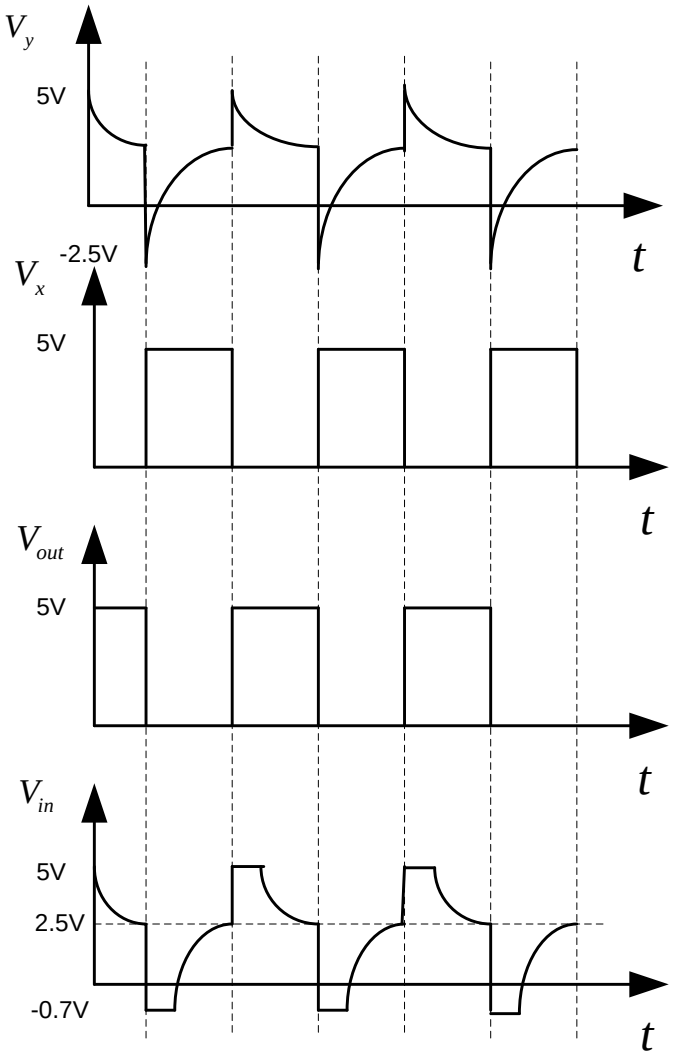


Figure 117

Q:

What the following circuit does?

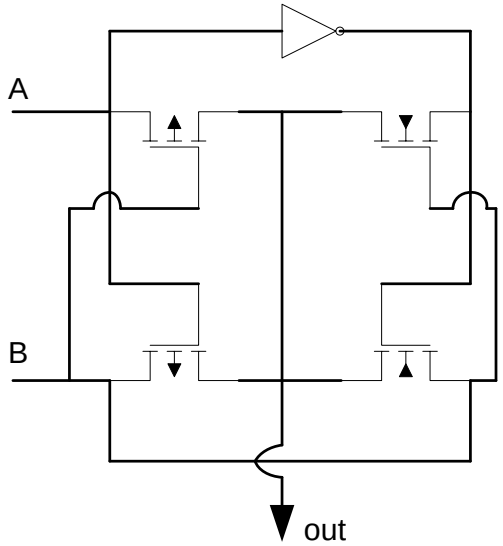


Figure 118

A:

A	B	out
0	0	0
0	1	1
1	0	1
1	1	0

From the table, we can conclude, that the circuit above implements a XOR gate.

Q:

What logic function the following circuit does?

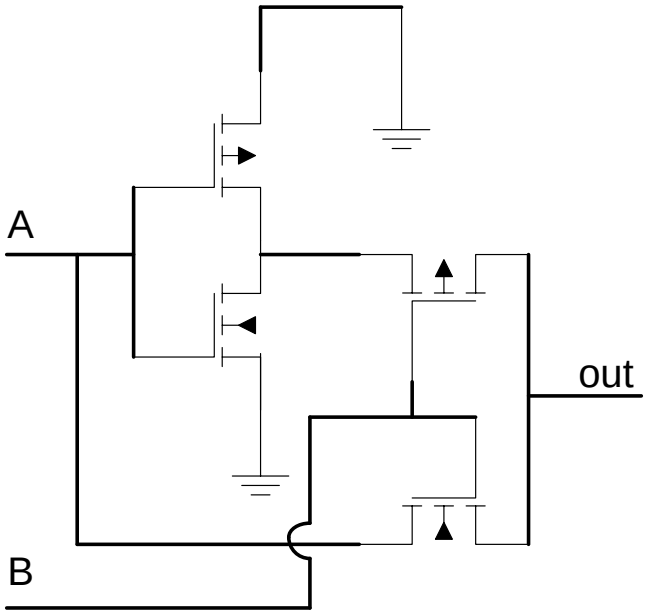


Figure 119

A:

A	B	out
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

From the table, we can conclude, that the circuit above implements a not(XOR) gate.

Logic Questions

Q:

There are 100 lamps. At the beginning all of them are switched off. There are 100 men and all of them go over the lamp array pushing the switch buttons.
The first man pushes the switch buttons of 1,2,3,4,5…….100 lamps.
The second man pushes the switch buttons of 2,4,6,8……100 lamps, and so on…

3,6,9,12….99
.
.
.
n,2n,4n…. N

Answer, what lamps, finally, will be on?

A:

We solve this problem for ten lamps and trying to see some dependence. We can come to conclusion that lamps which were turned on/off odd number of times will stay on. We can see that the lamps number $1^2;2^2;3^2;4^2;5^2;6^2;7^2;8^2;9^2;10^2$ will stay on.

Q:

You have 100 black balls, 100 red balls and two boxes. You have to distribute them in such a way that the probability to take out a black ball will be maximal. The probability to take a ball from both boxes is equal.

A:

We check some cases.

Red balls	Black balls	probability
100	100	$P=\frac{1}{2}\cdot 1+\frac{1}{2}\cdot 0=\frac{1}{2}$
100+100	0	$P=\frac{1}{2}\cdot\frac{1}{2}+\frac{1}{2}\cdot 0=\frac{1}{4}$
100+50	50	$P=\frac{1}{2}\cdot\frac{1}{3}+\frac{1}{2}\cdot 1=\frac{2}{3}$
100+99	1	$\boxed{P=\frac{1}{2}\cdot\frac{99}{199}+\frac{1}{2}\cdot 1=\frac{149}{299}\approx\frac{3}{4}}$

The last case is optimal.

Q:

9 coins, one of them is fake. Use a balance to weigh them not more than 3 times and find the fake. A fake coin is not necessarily lighter.

A:

We divide 9 coins into 3 groups of 3 coins. At first we weight two of the three groups (3:3). If one of the coin groups is heavier or lighter, then the fake coin is in the group. If their weight is equal then the fake coin is in the third group. Then we weight two coins out of the group (1:1) and determine which one is fake, otherwise the remaining coin is fake. Consequently, we have to use the balance at most 2 times.

Q:

A point is chosen at random from within a circular region. What is the probability that the point is closer to the center of the region than it is to the boundary of the region.

A:

The probability is proportional to the area of the circular region.

$$p = \frac{\pi r^2}{\pi R^2}\bigg|_{r=\frac{1}{2}} = \frac{1}{4}$$

Q:

You have 2 candles. Every candle lights for 60 minutes. You have to find the way to measure 45 minutes.

A:

At first we set on fire two ends of a candle and one end of the second candle. When the first candle is burned after 30 minutes, we set on fire the second end of the second candle, which burns out after 15 minutes.

Q:

A man went down to the river with two jugs, one of three-liter capacity and one of five-liter capacity. Using just these, how did he bring back exactly four liters?

A:

A man fills the five-liter jug with water and pours three liter of water into the three-liter jug, so only two liters of water remain in the five liter jug. Then, he empties the three-liter jug and fills it with the two liter of water left in the five liter jug. Now, he can fill the five liter jug to the top, and pour 1 liter to the three-liter jug in order to fill

it up. Consequently, only four liters remain in the five liter jug.

Q:

You have 10 sacks of coins. Only one sack has fake coins. The fake coins are heavier than ordinary coins. Determine which sack has fake coins by using weighing machine only once.

A:

You should take one coin from the first sack, two coins from the second and so on. We assign to the normal coin mass as X and for the fake coin the mass is Y. Now, the total mass that is supposed to be on the weighing machine is

$$x+2x+3x+4x\cdots 10x=10\cdot\frac{x+10x}{2}=55x$$

However, we obtain another result which is bigger than the calculated one, since the fake coins mass is bigger. At this stage we can calculate the number of fake coins which equals the sack number. Suppose we got the total mass of the weighed coins such as Z. Than the sack number is

$$\#=\frac{Z-55x}{y-x}$$

Q:

Find four similar parts in the given figure.

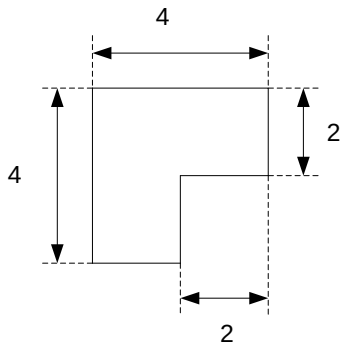


Figure 120

A:

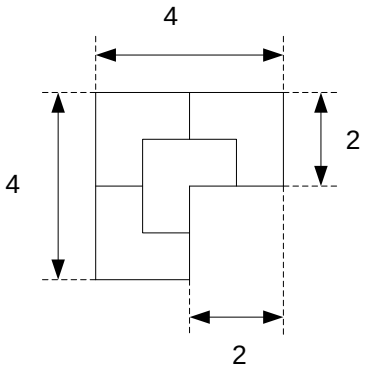


Figure 121

Q:

You are given five squares with the side length of 1 cm.

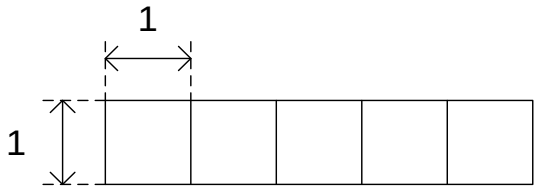


Figure 122

Use those squares (cut, past…) and compose a single square.

A:

We cut those squares in this way.

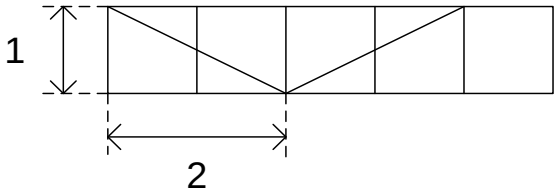


Figure 123

And compose a new bigger square with the side of $\sqrt{5}$ cm

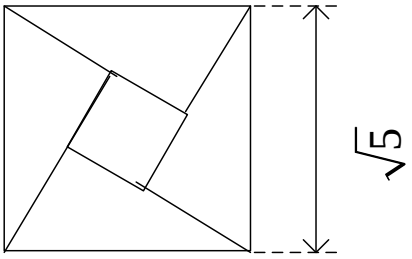


Figure 124

Q:

There are 10 coins each having different value. What is the maximal sum that can be composed using those coins, so that any value from 1 to the maximal value can be composed?

A:

Those coins are: 1,2,4,8,16,32,64,128,256,512 and the sum is 1023.

Q:

There 10 engineers. A delegation must be send abroad with unknown number of men (from 1-10). How combinations are possible?

A:
Each engineer can stay or go, so there are 2 options. There are 10 engineers therefore the number of combinations possible is 2^{10}. However, we have to distinguish between similar combinations. Therefore, the number of combinations possible is

$$\sum_{k=1}^{10}\binom{10}{k}=\sum_{k=1}^{10}\left(\frac{10!}{(10-k)!\cdot k!}\right)$$

Q:
You have three boxes. One of them contains apples, the other oranges, and the third contains both apples and oranges. Each of the boxes has a label on it. The order of labels is changed in cyclic order, so that, each box has a label that does not belongs to it. How can you determine the content of each box if you are permitted to open one of the boxes?

A:
Assume we open a box with a label which says "apples" and discovered oranges, therefore the box containing oranges got a label which says "apples and oranges", and the box containing apples and oranges got a label "oranges".

Other questions

Q:

You have to sample an analog signal using minimal hardware. The signal spectrum is given:

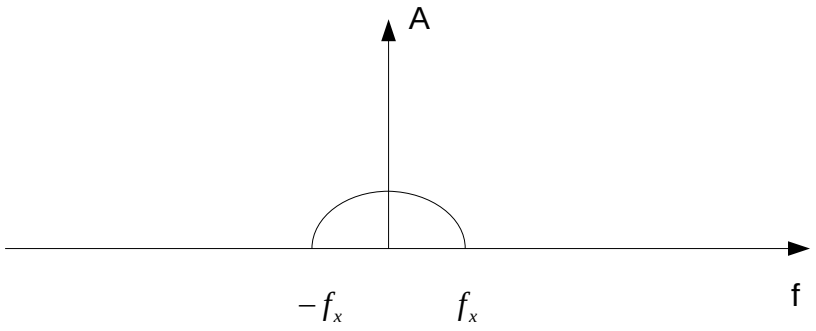


Figure 125

A:

We use an A/D converter for sampling with the minimal sampling frequency, which enables signal recovering.

$$X(f) * \frac{2\pi}{T} \sum_{k=-\infty}^{k=\infty} \delta(f - \frac{k}{T}) = \frac{2\pi}{T} \sum_{k=-\infty}^{k=\infty} X(f - \frac{k}{T})$$

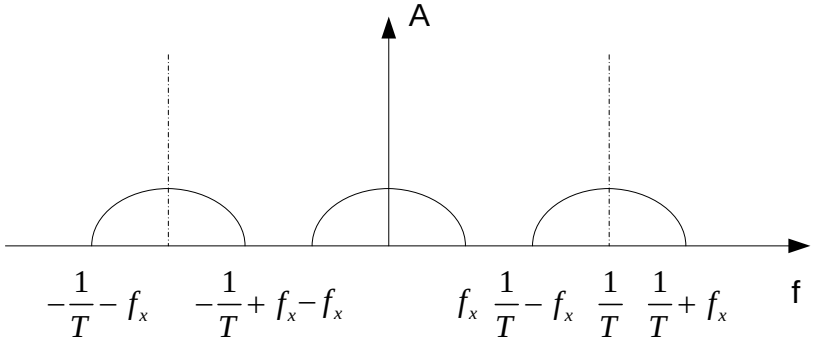


Figure 126

In order to be able to recover the signal, we have to demand, that there will be no alignment between the spectrum components. This demand leads to the following condition $\frac{1}{T} \geq 2 f_x$.

Q:

You have an analog signal. You have to sample it and filter it using LPF. What sampling frequency should you use?

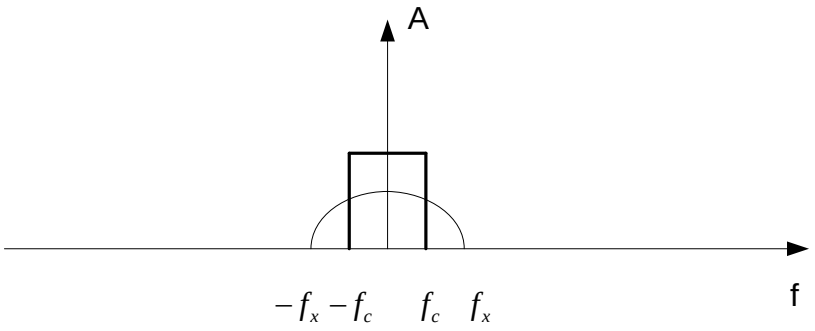


Figure 127

Can you reduce the sampling frequency beyond that one used before?

A:

After sampling we obtain the following spectrum picture.

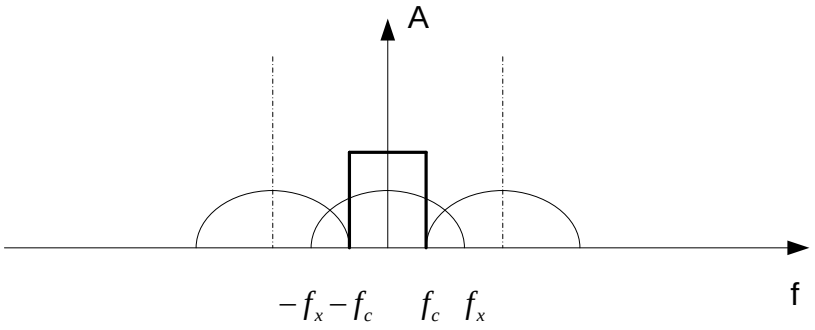


Figure 128

In other words, we can permit alignment such as $\frac{1}{T} = f_c + f_x$ and still be able to recover the original signal.

Q:

How Spectrum analyzer works? Draw block diagram and explain the work principals.

A:

Spectrum analyzer presents a signal's spectrum of the input signal and the power of each spectral component. One way to build such a device is to implement Fourier transform (FFT) of the input signal.

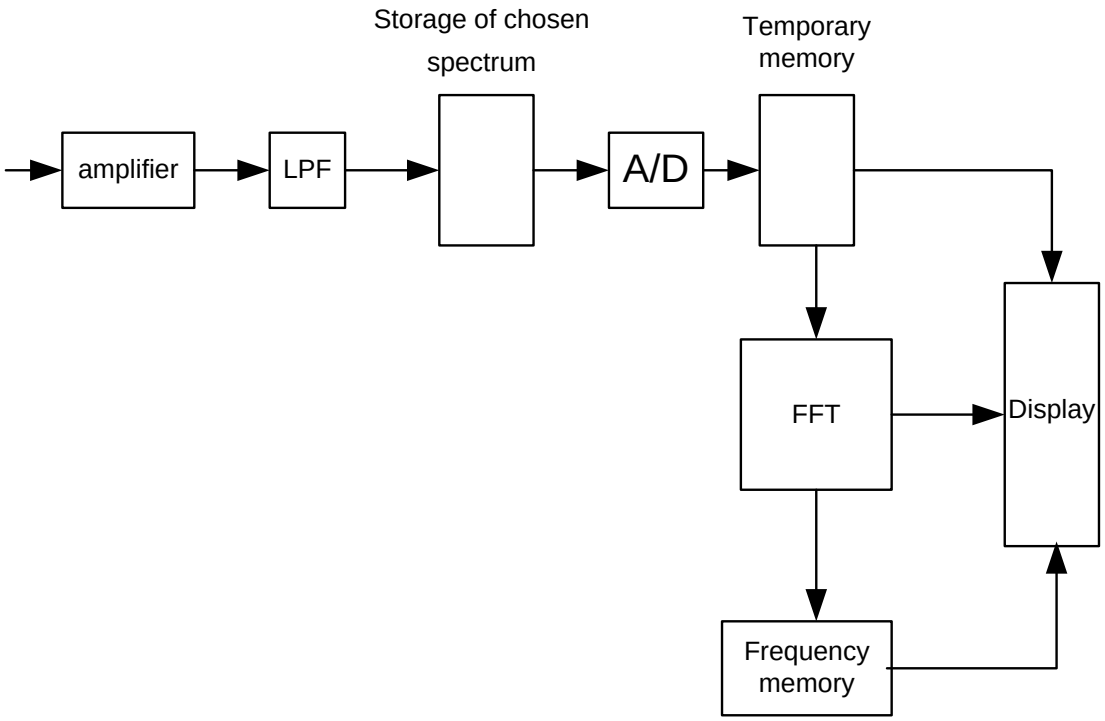


Figure 129

Such an implementation has a drawback, because the maximal frequency of the spectrum analyzer is limited by the A/D maximal sampling frequency.

Q:

How Super Heterodyne works? Draw the block diagram and describe the work principles of the device.

A:

Super Heterodyne enables convertion of an unknown modulated RF frequency f_{RF} to known IF frequency f_{IF}**.** This circuit is very widespread in radio receivers.

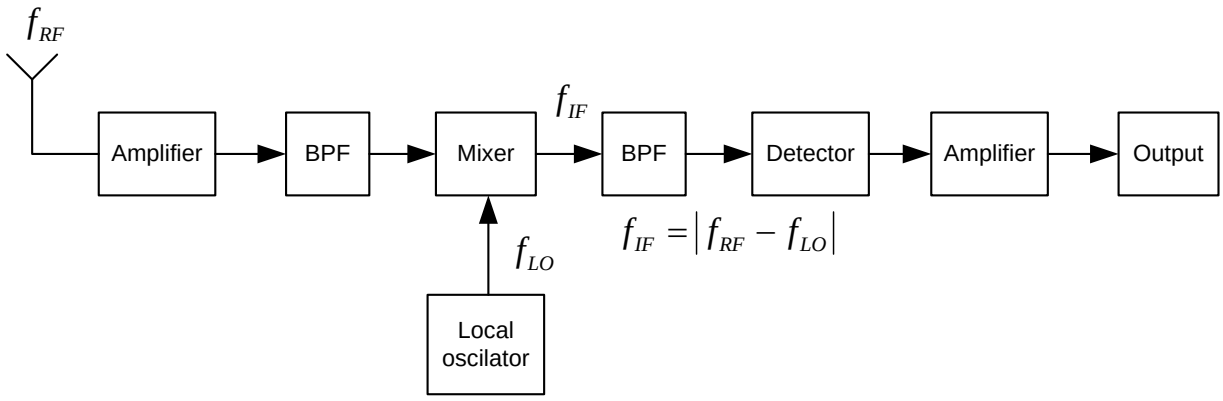


Figure 130

Q:

For the AM signal of Figure 127:

a) Determine the modulation index.

b) If the carrier frequency is 45kHz, what must be the modulation frequency

c) If the input impedance of the AM detector circuit shown is 500-Ω, calculate the carrier power and the total power delivered to the detector.

d) Determine the average value of V_{av}, the detector output voltage.

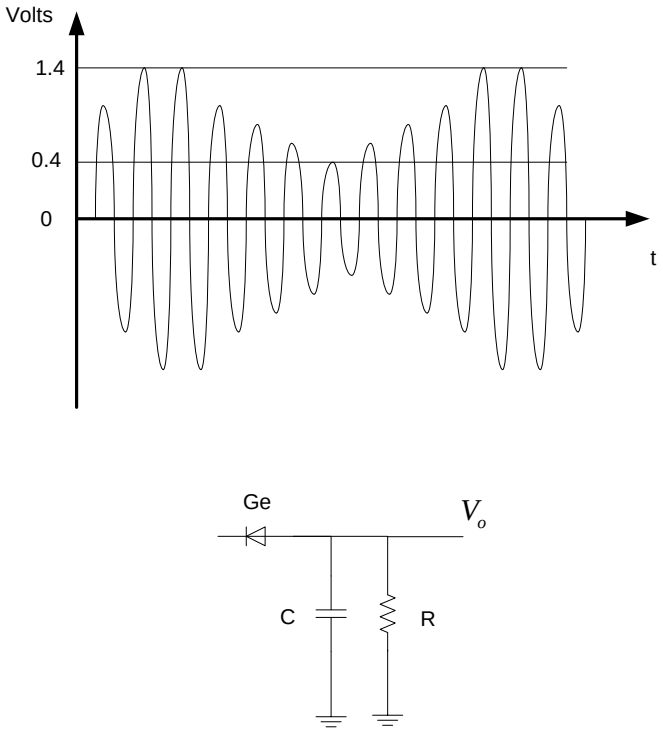


Figure 131

A:

a) First we calculate the modulation index:

A and B are taken from the Figure 127 indicating the maximum and minimum amplitude values.

$$A = E_c + E_m = 1.8V;$$
$$B = E_c - E_m = 1V$$
$$A + B = 2E_c = 1.8V$$
$$A - B = 2E_m = 1V$$
$$m_a = \frac{E_m}{E_c} = \frac{A-B}{A+B} = \frac{1}{1.8} = 0.555$$

b) The modulation frequency is determined from figure 127 by counting the number of peaks in the AM envelope. The number is nine, therefore the modulation frequency is calculated as follows:

$$f_m = \frac{f_c}{9} = \frac{45kHz}{9} = 5kHz$$

c) The power of unmodulated carrier is

$$E_c = \frac{A+B}{2} = \frac{1.4+0.4}{2} = 0.9V$$
$$P_c = \frac{E^2{}_c}{2R} = \frac{0.9^2}{2 \cdot 500} = 0.81mW$$

Calculation of the power in a single sideband is

$$P_{m_{SB}} = \frac{m_a}{4} P_c = \frac{0.555}{4} \cdot 0.81$$
$$P_{m_{SB}} = 0.112mW$$

The total power delivered to the detector is

$$P_t = P_{m_{SB}} + P_c$$
$$P = 0.11mW + 0.81mW = 0.93mW$$

d) The average value of V_{av}, at the detector output voltage is

$$V_{av} = \frac{(-1.4+0.2)+(-0.4+0.2)}{2}$$
$$V_{av} = \frac{-1.2-0.2}{2} = \frac{-1.4}{2} = -0.7V$$

Q:

A receiver has a 6dB noise figure. Determine the gain required to improve the noise figure to 4dB if a preamplifier with a 2dB noise figure is used.

A:

In order to improve the system noise figure we have to use a pre-amplifier.

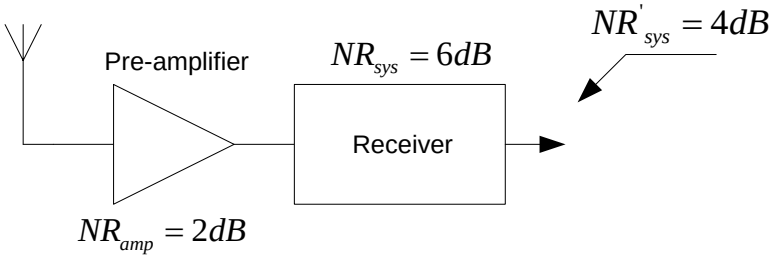


Figure 132

$$NR'_{sys} = NR_{amp} + \frac{NR_{sys} - 1}{G_{amp}}$$

$$G_{amp} = \frac{NR_{sys} - 1}{NR'_{sys} - NR_{amp}}$$

$$NR_{sys} = 6dB = 3.98$$

$$NR'_{sys} = 4dB = 2.51$$

$$NR_{amp} = 2dB = 1.58$$

$$G_{amp} = \frac{3.98 - 1}{2.51 - 1.58} = 3.2 = \boxed{5.06dB}$$

Q:

The mixer is followed by two amplifiers with 20dB gain each and noise figure (NF) of 15dB. Determine:

a) The system noise figure.
b) The noise temperature.

A: $G_1 = G_2 = 10dB = 10$

$NF_1 = NF_2 = 4dB = 2.51$

$G_3 = G_4 = 20dB = 100$

$NF_3 = NF_4 = 15dB = 31.62$

$G_m = -6dB = 0.25$

$NF_m = 8dB = 6.31$

a) $$NF = NR_1 + \frac{NR_2 - 1}{G_1} + \frac{NR_m - 1}{G_1 G_2} + \frac{NR_3 - 1}{G_1 G_2 G_m} + \frac{NR_4 - 1}{G_1 G_2 G_m G_3}$$

$$NF = 2.51 + \frac{2.51-1}{10} + \frac{6.31-1}{100} + \frac{31.62-1}{25} + \frac{31.62-1}{2500} = 3.95$$

$NF = 5.96dB$

b) $T_{eq} = T_0 (NF - 1)$

$T_{eq} = 290 \cdot (3.95 - 1) = 855.5K$

Q: What is the noise figure (NF) of an amplifier? Explain.

A:
A noise figure it is a parameter, which characterize, how much noise the amplifier adds to the output signal. A NF is determined as

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_0}{G \cdot S_{in}/(G \cdot N_0 + \Delta N)} = 1 + \frac{\Delta N}{G \cdot N_0}$$

When:
G - the amplifier's gain

S_{in} - the input signal
N_0 - the input noise
ΔN - the noise added by the amplifier