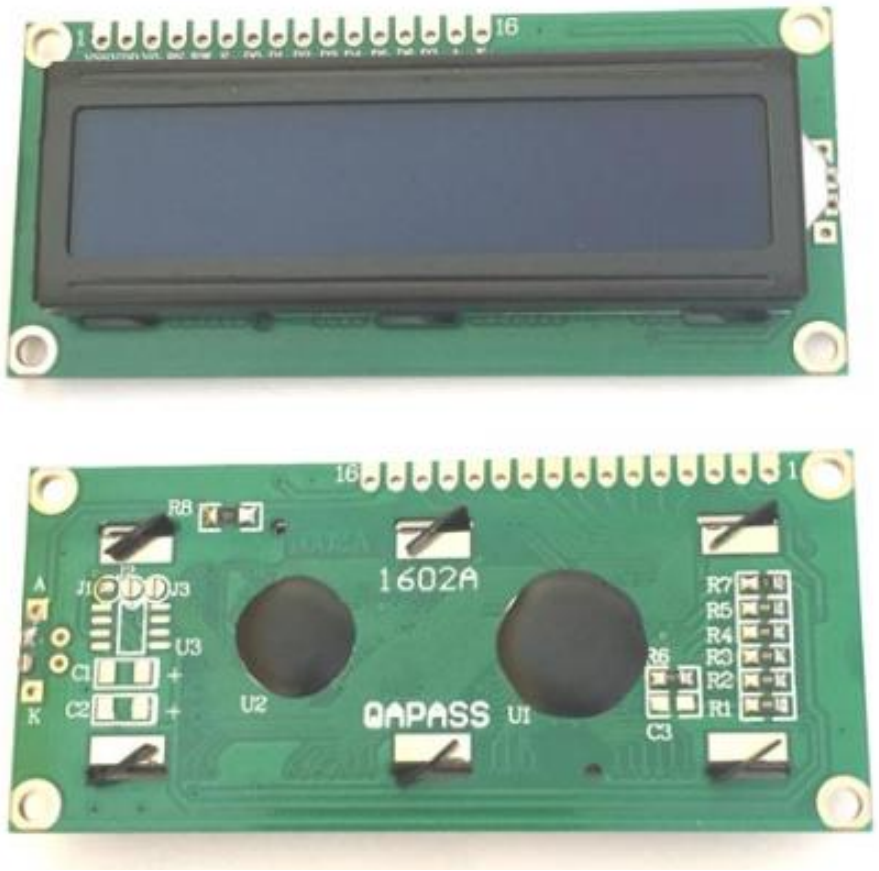
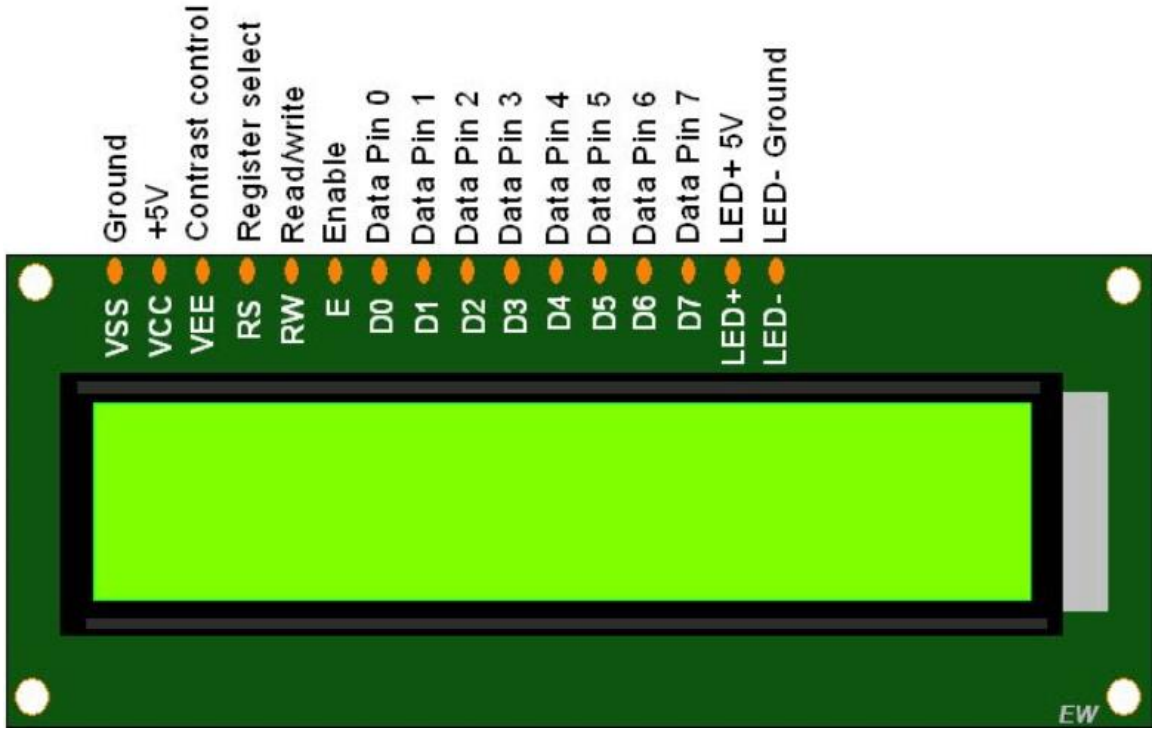
DESCRIPCIÓN DE USO DE UN LCD

APLICACIÓN PARA PIC18F46K22

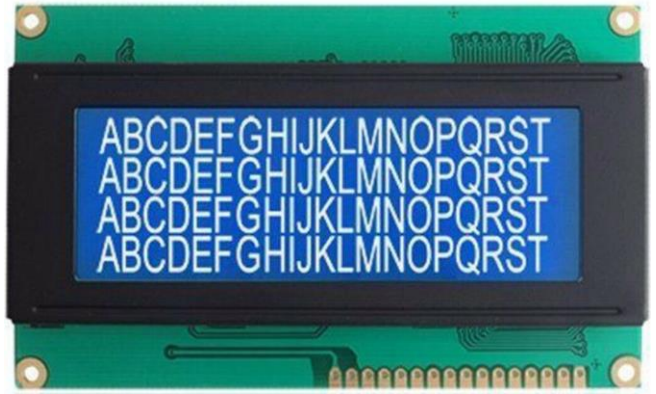
Ing. Benjamín Pérez Clavel

Forma genérica





Forma genérica



Código ASCII

ASCII	Hex	Symbol
0	0	NUL
1	1	SOH
2	2	STX
3	3	ETX
4	4	EOT
5	5	ENQ
6	6	ACK
7	7	BEL
8	8	BS
9	9	TAB
10	A	LF
11	B	VT
12	C	FF
13	D	CR
14	E	SO
15	F	SI

ASCII	Hex	Symbol
16	10	DLE
17	11	DC1
18	12	DC2
19	13	DC3
20	14	DC4
21	15	NAK
22	16	SYN
23	17	ETB
24	18	CAN
25	19	EM
26	1A	SUB
27	1B	ESC
28	1C	FS
29	1D	GS
30	1E	RS
31	1F	US

ASCII	Hex	Symbol
32	20	(space)
33	21	!
34	22	"
35	23	#
36	24	$
37	25	%
38	26	&
39	27	'
40	28	(
41	29	)
42	2A	*
43	2B	+
44	2C	,
45	2D	-
46	2E	.
47	2F	/

ASCII	Hex	Symbol
48	30	0
49	31	1
50	32	2
51	33	3
52	34	4
53	35	5
54	36	6
55	37	7
56	38	8
57	39	9
58	3A	:
59	3B	;
60	3C	<
61	3D	=
62	3E	>
63	3F	?

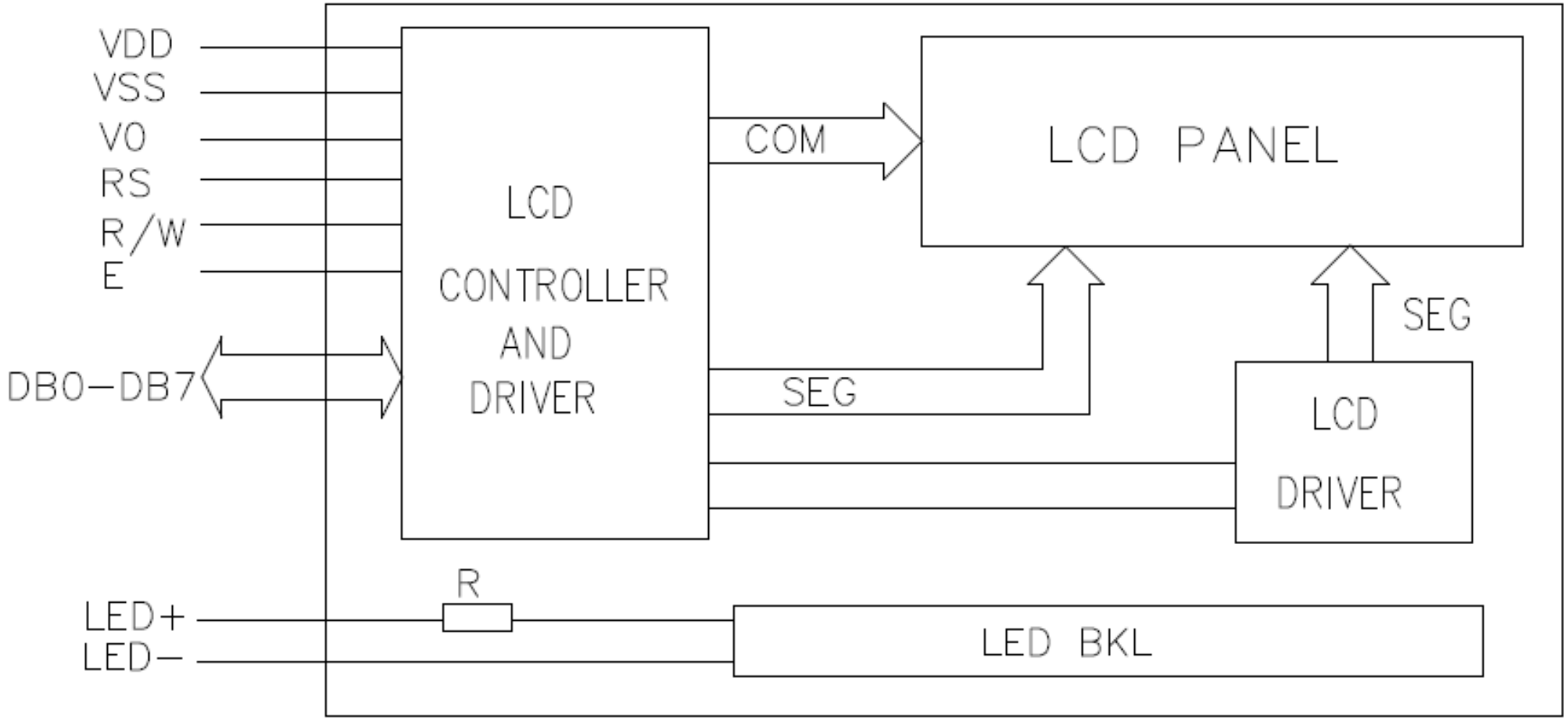
ASCII	Hex	Symbol
64	40	@
65	41	A
66	42	B
67	43	C
68	44	D
69	45	E
70	46	F
71	47	G
72	48	H
73	49	I
74	4A	J
75	4B	K
76	4C	L
77	4D	M
78	4E	N
79	4F	O

ASCII	Hex	Symbol
80	50	P
81	51	Q
82	52	R
83	53	S
84	54	T
85	55	U
86	56	V
87	57	W
88	58	X
89	59	Y
90	5A	Z
91	5B	[
92	5C	\
93	5D	]
94	5E	^
95	5F	_

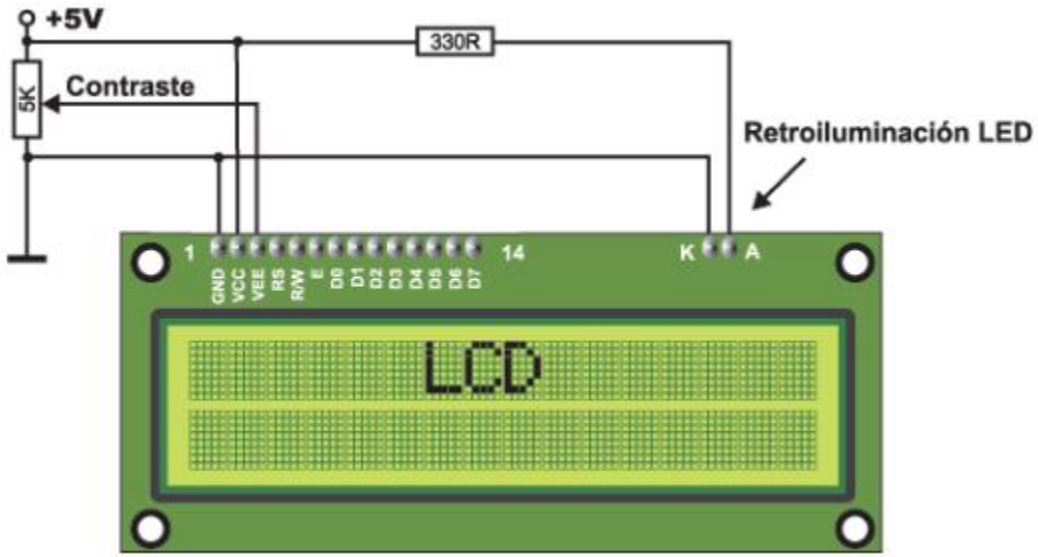
ASCII	Hex	Symbol
96	60	`
97	61	a
98	62	b
99	63	c
100	64	d
101	65	e
102	66	f
103	67	g
104	68	h
105	69	i
106	6A	j
107	6B	k
108	6C	l
109	6D	m
110	6E	n
111	6F	o

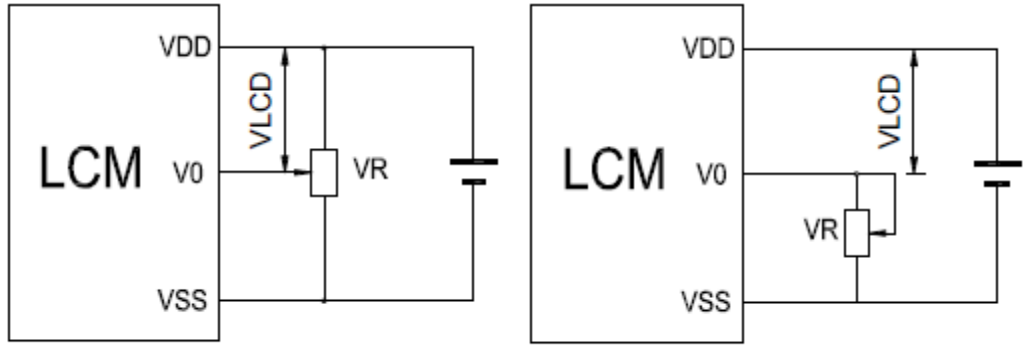
ASCII	Hex	Symbol
112	70	p
113	71	q
114	72	r
115	73	s
116	74	t
117	75	u
118	76	v
119	77	w
120	78	x
121	79	y
122	7A	z
123	7B	{
124	7C	|
125	7D	}
126	7E	~
127	7F	

Diagrama a bloques interno



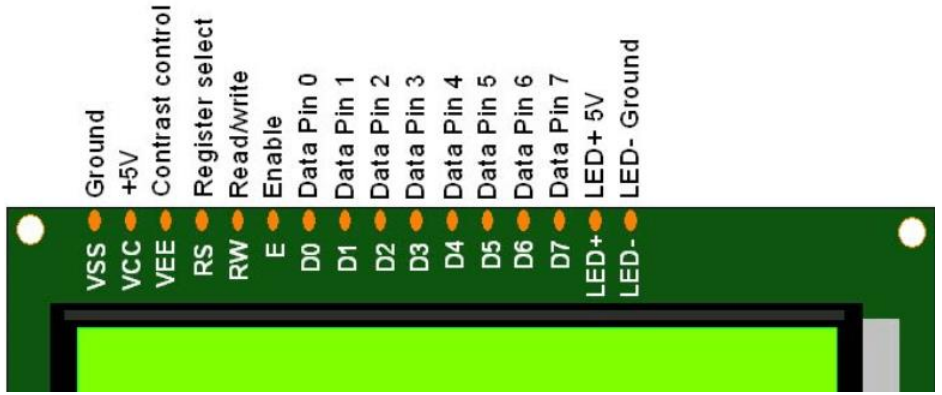
Ajuste de contraste





V_{DD}-V_0: LCD Driving voltage VR: 10k~20k

Descripción de pines



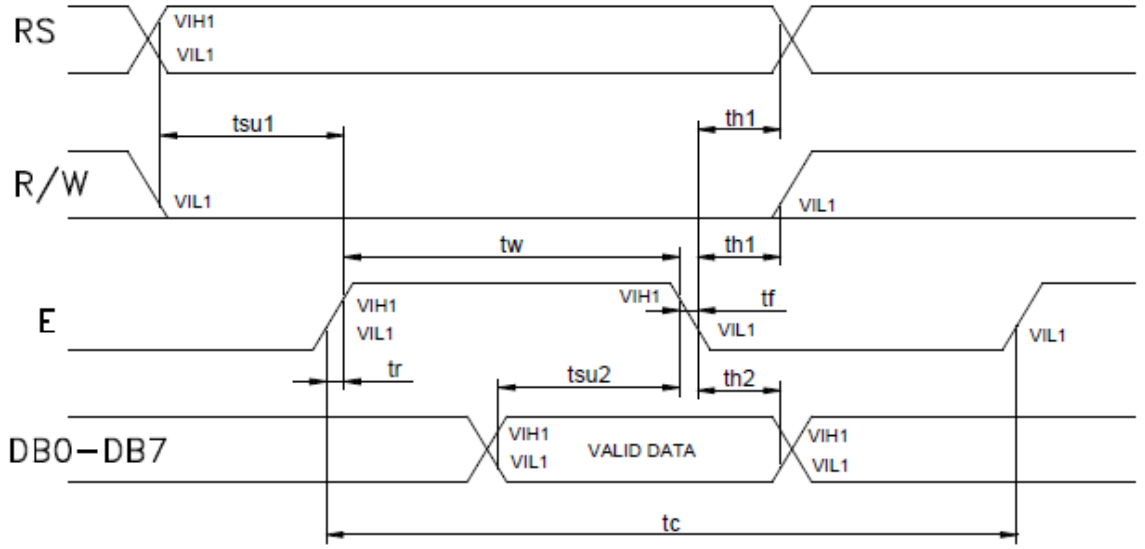
Pin no.	Symbol	External connection	Function
1	Vss	Power supply	Signal ground for LCM
2	V_{DD}		Power supply for logic for LCM
3	V_0		Contrast adjust
4	RS	MPU	Register select signal
5	R/W	MPU	Read/write select signal
6	E	MPU	Operation (data read/write) enable signal
7~10	DB0~DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
11~14	DB4~DB7	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
15	LED+	LED BKL power supply	Power supply for BKL
16	LED-		Power supply for BKL

Diagramas de tiempos (escritura)

Write cycle (Ta=25℃, VDD=3.3V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t_c	E	500	-	-	ns
Enable pulse width	t_w		300	-	-	
Enable rise/fall time	t_r, t_f		-	-	25	
RS; R/W setup time	t_{su1}	RS; R/W	100	-	-	
RS; R/W address hold time	t_{h1}	RS; R/W	10	-	-	
Read data output delay	t_{su2}	DB0~DB7	60	-	-	
Read data hold time	t_{h2}		10	-	-	

Write mode timing diagram

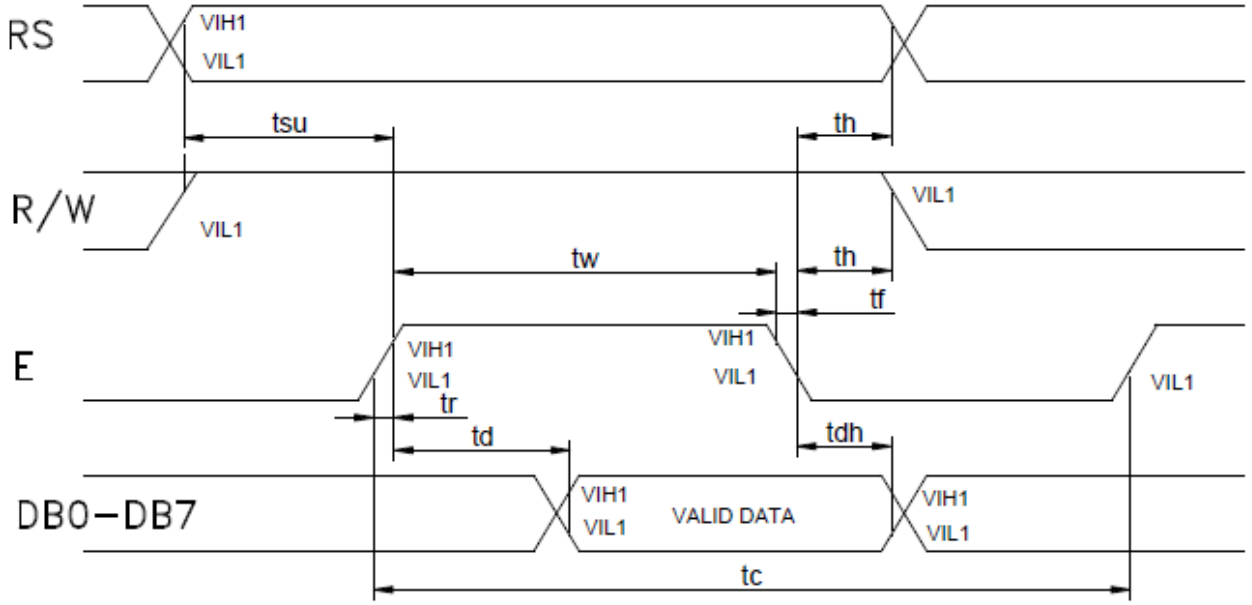


Diagramas de tiempos (lectura)

Read cycle (Ta=25℃, VDD=3.3V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t_c	E	500	-	-	ns
Enable pulse width	t_w		300	-	-	
Enable rise/fall time	t_r, t_f		-	-	25	
RS; R/W setup time	t_{su}	RS; R/W	100	-	-	
RS; R/W address hold time	t_h	RS; R/W	10	-	-	
Read data output delay	t_d	DB0~DB7	60	-	90	
Read data hold time	t_{dh}		20	-	-	

Read mode timing diagram

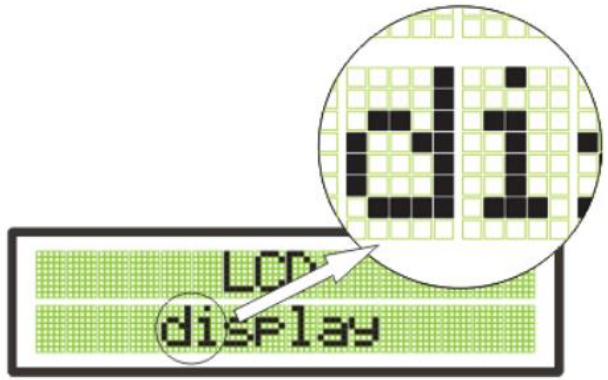


Tipos de memoria en un LCD

El LCD dispone de tres bloques de memoria:

- **DDRAM Display Data RAM (RAM de datos de visualización)**
- **CGRAM Character Generator RAM (generador de caracteres RAM)**
- **CGROM Character Generator ROM (generador de caracteres ROM)**

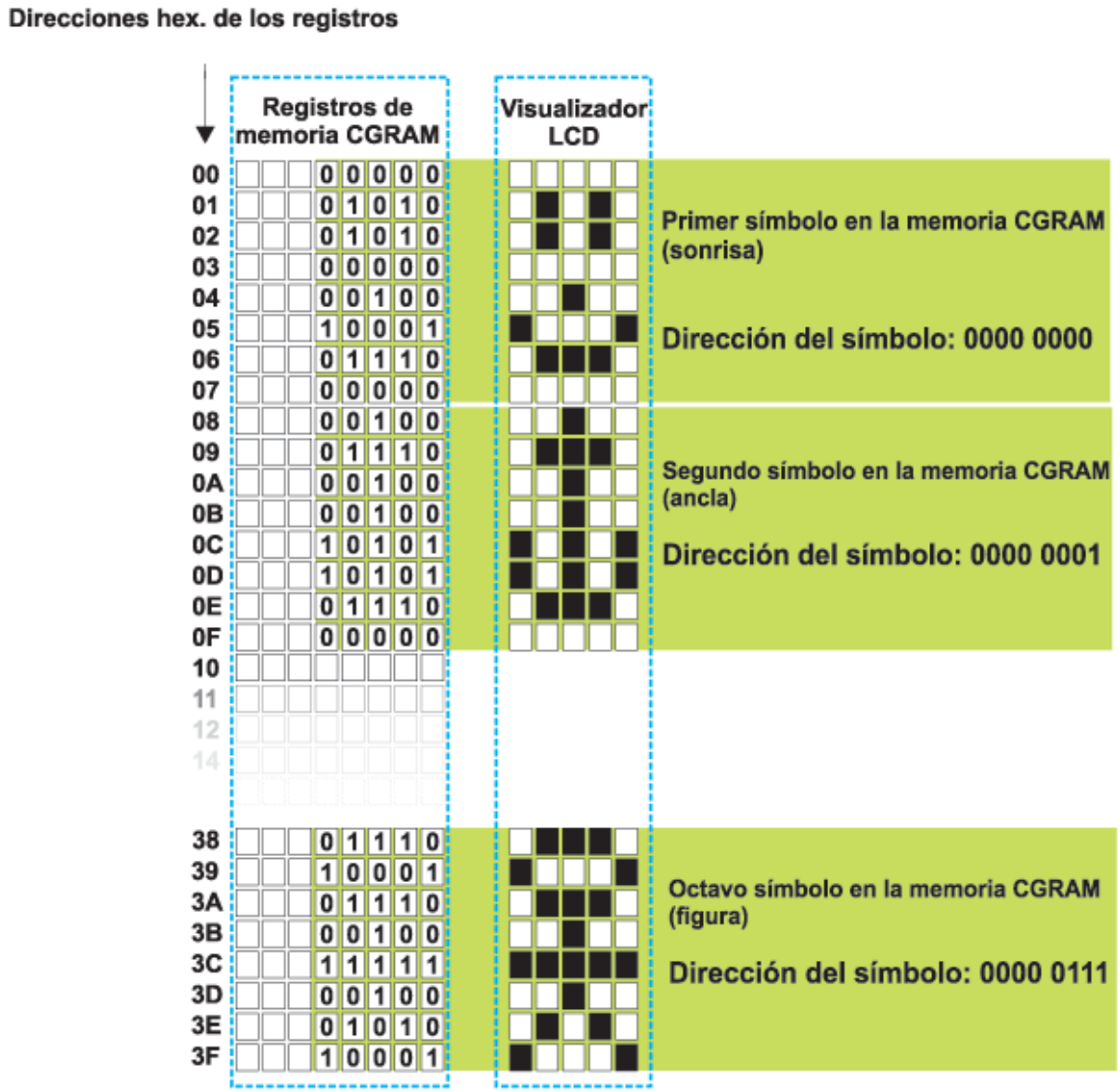
Representación de caracteres CGROM



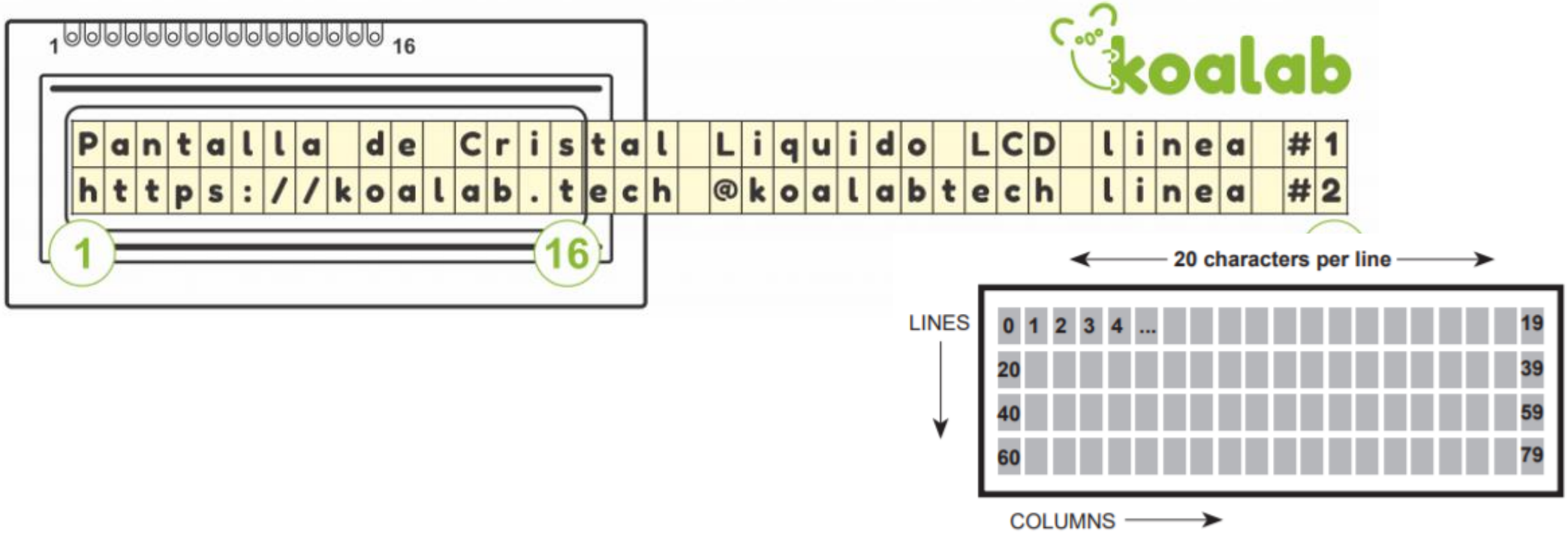
4 bits más bajos de la dirección	4 bits más altos de la dirección															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX 0000	CG RAM (1)			0	@	P	`	p				ー	タ	ミ	α	p
XXXX 0001	CG RAM (2)			!	1	A	Q	a	q			。	ア	チ	ム	ä	q
XXXX 0010	CG RAM (3)			"	2	B	R	b	r			「	イ	ツ	メ	ß	θ
XXXX 0011	CG RAM (4)			#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
XXXX 0100	CG RAM (5)			$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
XXXX 0101	CG RAM (6)			%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
XXXX 0110	CG RAM (7)			&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
XXXX 0111	CG RAM (8)			'	7	G	W	g	w			ァ	キ	ヌ	ラ	g	π
XXXX 1000	CG RAM (1)			(	8	H	X	h	x			ィ	ク	ネ	リ	ɾ	x̄
XXXX 1001	CG RAM (2)			)	9	I	Y	i	y			ゥ	ケ	ノ	ル	ᵑ	y
XXXX 1010	CG RAM (3)			*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
XXXX 1011	CG RAM (4)			+	;	K	[	k	{			ォ	サ	ヒ	ロ	ˣ	万
XXXX 1100	CG RAM (5)			,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
XXXX 1101	CG RAM (6)			-	=	M	]	m	}			ュ	ス	ヘ	ン	Ł	÷
XXXX 1110	CG RAM (7)			.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
XXXX 1111	CG RAM (8)			/	?	O	_	o	←			ッ	ソ	マ	°	ö	▓

	4 bits más altos								
	0000	0001	0010	0011	0100	0101	0110	0111	
XXXX 0000	CG RAM (1)			0	@	P	`	p	
XXXX 0001	CG RAM (2)			!	1	A	Q	a	q
XXXX 0010	CG RAM			"	2	B	R	b	r

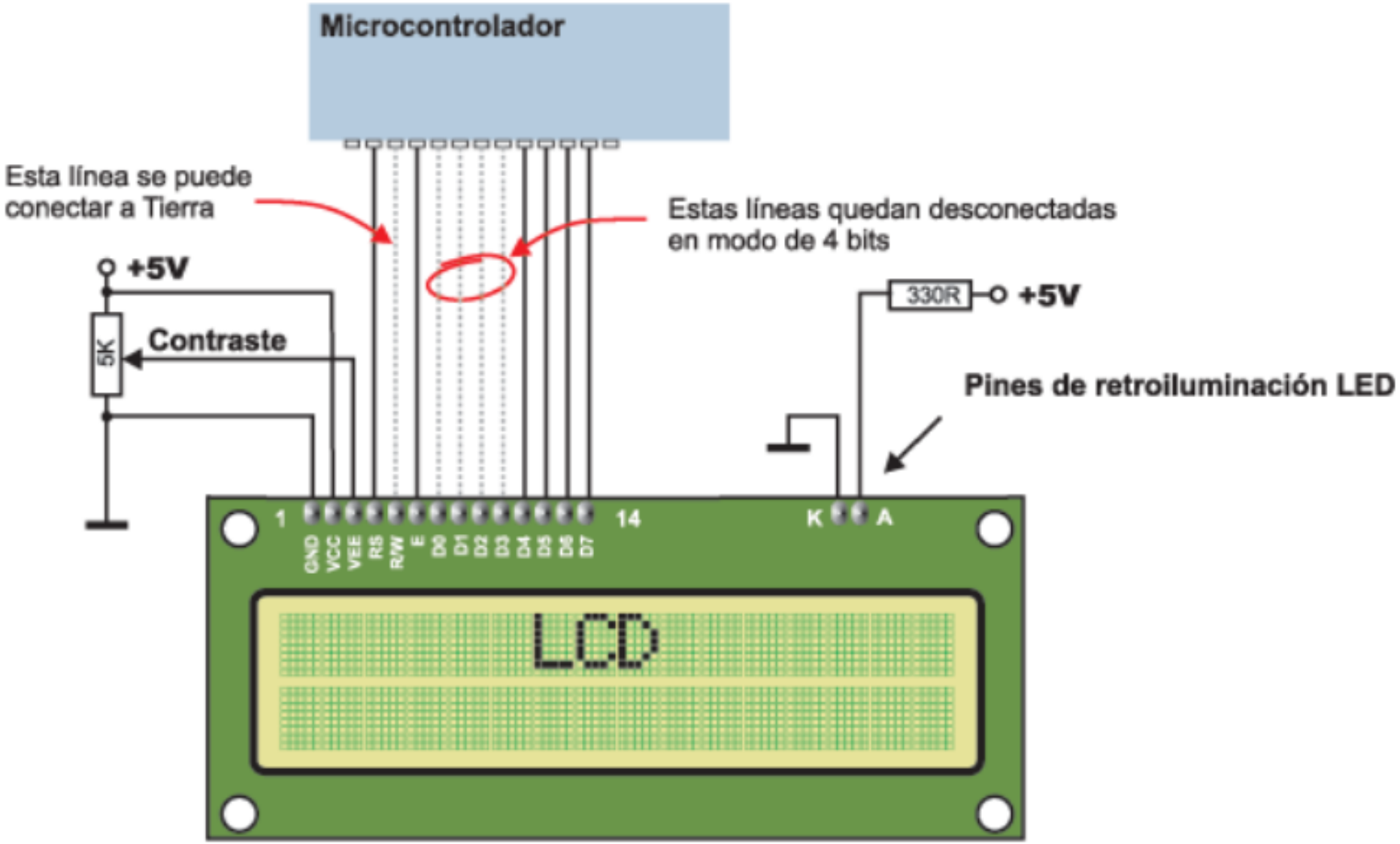
Representación de caracteres CGRAM



Mapa de memoria DDRAM



Conexión de 4-bit



Comandos al LCD

Instruction	Code RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{osc} is 270 kHz)
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.	37 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 µs
Set CGRAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.	37 µs
Set DDRAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.	37 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

I/D = 1: Increment
I/D = 0: Decrement
S = 1: Accompanies display shift
S/C = 1: Display shift
S/C = 0: Cursor move
R/L = 1: Shift to the right
R/L = 0: Shift to the left
DL = 1: 8 bits, DL = 0: 4 bits
N = 1: 2 lines, N = 0: 1 line
F = 1: 5 × 10 dots, F = 0: 5 × 8 dots
BF = 1: Internally operating
BF = 0: Instructions acceptable

Comandos al LCD

Instruction	Code RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
Write data to CG or DDRAM	1	0	Write data								Writes data into DDRAM or CGRAM.	37 µs t_{ADD} = 4 µs*
Read data from CG or DDRAM	1	1	Read data								Reads data from DDRAM or CGRAM.	37 µs t_{ADD} = 4 µs*

Note: — indicates no effect.

* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

DDRAM: Display data RAM
CGRAM: Character generator RAM
ACG: CGRAM address
ADD: DDRAM address (corresponds to cursor address)
AC: Address counter used for both DD and CGRAM addresses

Execution time changes when frequency changes
Example:
When f_{cp} or f_{OSC} is 250 kHz,

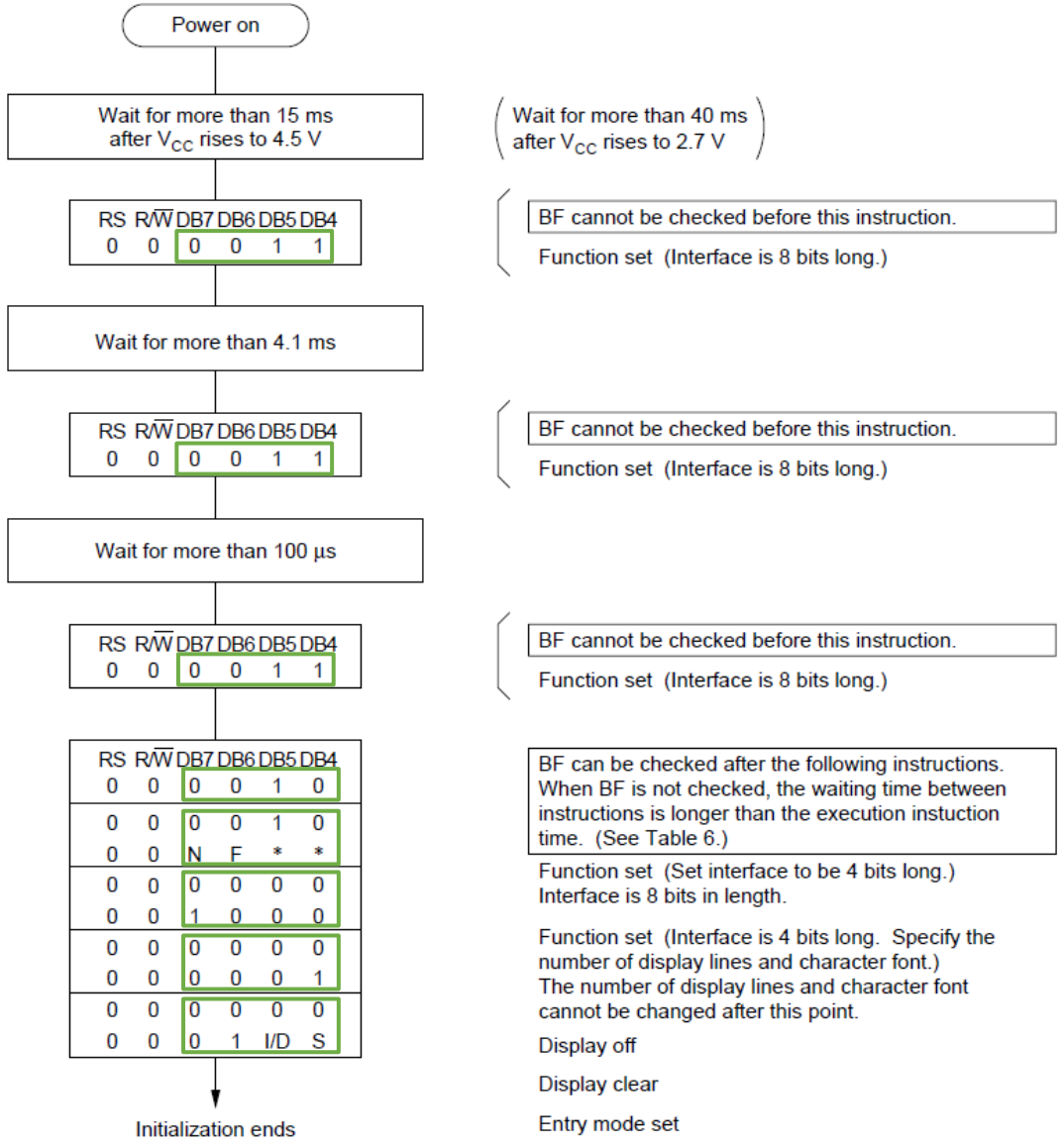
$$37\ \mu s \times \frac{270}{250} = 40\ \mu s$$

Comandos al LCD

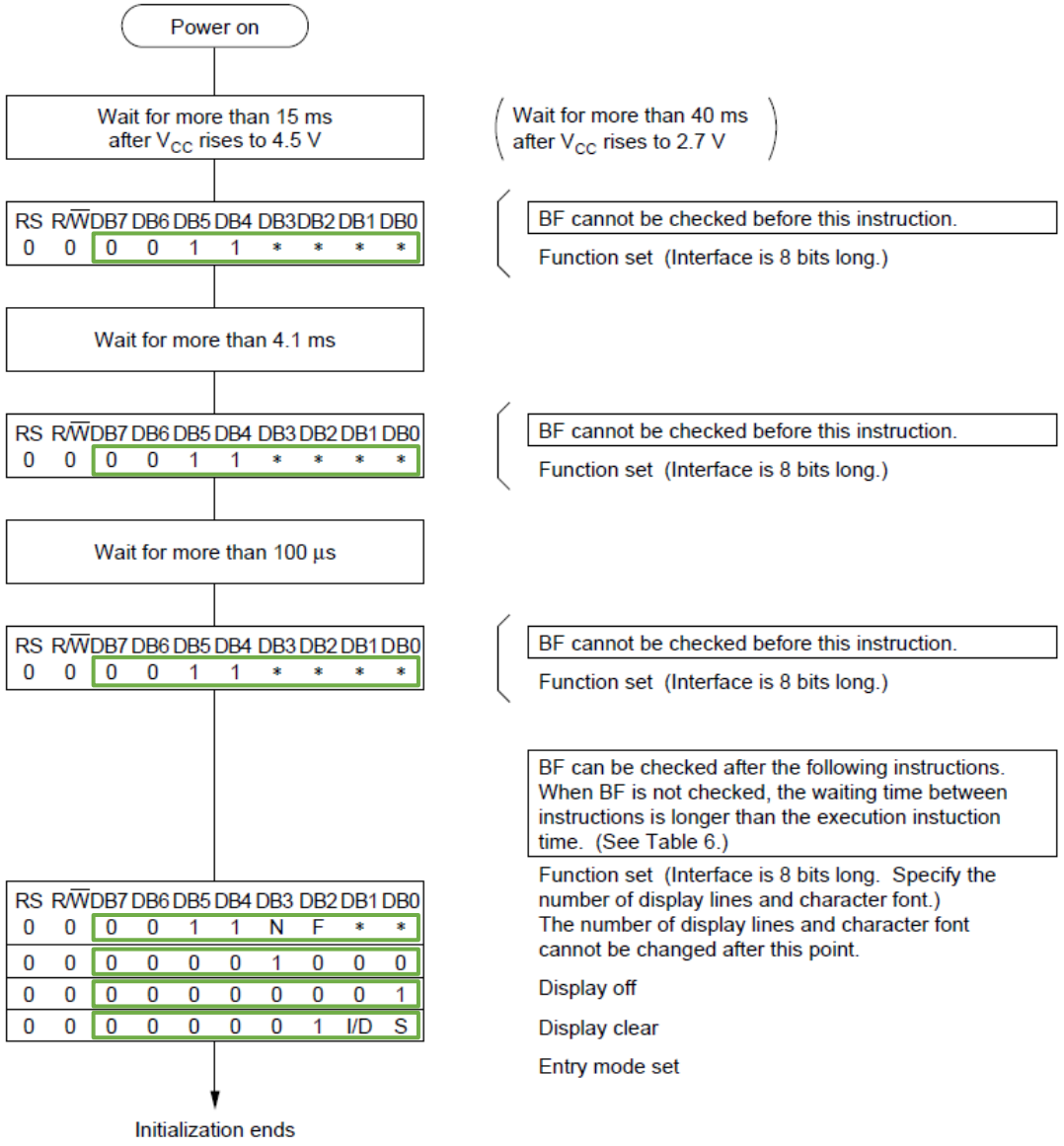
Instrucción	RS	R|W	D7	D6	D5	D4	D3	D2	D1	D0	Descripción
Borrar display	0	0	0	0	0	0	0	0	0	1	Borrar el contenido del display.
Cursor a inicio	0	0	0	0	0	0	0	0	1	X	Lleva el cursor a la posición inicial.
Modo de funcionamiento	0	0	0	0	0	0	0	1	I|D	S	Dirección movimiento del cursor y desplazamiento de pantalla.
Control on/off	0	0	0	0	0	0	1	D	C	B	Encendido de display, encendido de cursor, parpadeo de cursor.
Desplazamiento cursor/display	0	0	0	0	0	1	S|C	R|L	X	X	Desplazamiento de pantalla o cursor y su dirección.
Modo de transferencia	0	0	0	0	1	DL	N	F	X	X	Bus de datos a 8 o 4 bits, numero de lineas y tamaño del carácter.
Acceso a memoria CGRAM	0	0	0	1	Dirección en CGRAM						Se ubica en la dirección de memoria.
Acceso a memoria DDRAM	0	0	1	Dirección en DDRAM							Se ubica en la dirección de memoria.
Lectura de dirección y ocupado	0	1	BF	Contador de dirección							Bandera de display ocupado.
Escritura de datos en memoria	1	0	Dato a escribir								Escribe un dato en la memoria DDRAM o CGRAM.
Lectura de datos en memoria	1	1	Dato leído								Lee un dato en la memoria DDRAM o CGRAM.

Secuencia para envío de datos/comandos

Secuencia de inicio 4-bit



Secuencia de inicio 8-bit



Generando una frase

CARACTER	CÓDIGO BINARIO	CÓDIGO HEX	CÓDIGO DEC
H	0100 1000	48	72
o	0110 1111	6F	111
l	0110 1100	6C	108
a	0110 0001	61	97
M	0100 1101	4D	77
u	0111 0101	75	117
n	0110 1110	6E	110
d	0110 0100	64	100
o	0110 1111	6F	111
Flecha derecha	0111 1110	7E	126