Modules

IN3160 Oblig 6, Spring 2022

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Readme

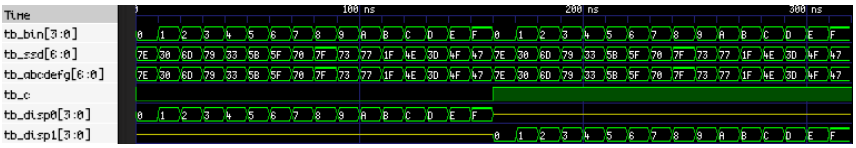
I made a major scheduling miscalculation with this assignment … I did not see the warning, and subsequently expected a similar workload to previous assignments. Compounded with some frustrating debugging, I was not able to complete all exercises in time. But hopefully it's enough for a second attempt!

I did not get far enough to warrant actually programming a Zedboard in the lab, so I have no `.do` files to offer. I use GHDL and GTKWave on my personal computer. If you do too, you can use:

```
ghdl analyze --std=08 bin2ssd.vhd seg7model_ent.vhd \
                      seg7model_beh.vhd tb_bin2ssd.vhd \
                      seg7ctrl.vhd tb_seg7ctrl.vhd
ghdl elaborate --std=08 tb_bin2ssd
ghdl elaborate --std=08 tb_seg7ctrl
ghdl run --std=08 tb_bin2ssd --wave=tb_bin2ssd.ghw
ghdl run --std=08 tb_seg7ctrl --wave=tb_seg7ctrl.ghw
```

Exercises

a) Sample `tb_bin2ssd.vhd` run:



b) I chose to alternate the displays at at least 50 Hz. I then need to calculate the number of 100×10^6 Hz cycles fit in 50 Hz, which is given by

$$\frac{100 \times 10^6 \,\text{Hz}}{50 \,\text{Hz}} = 2 \times 10^6.$$

The appropriate amount of bits is given by $\lfloor \log_2 2 \times 10^6 \rfloor = 20$, I round down get a faster (rather than slower) counter. More precisely, this gives a refresh rate of ≈ 95 Hz.

A possible schematic of the entity `seg7ctrl` is shown in figure 1.

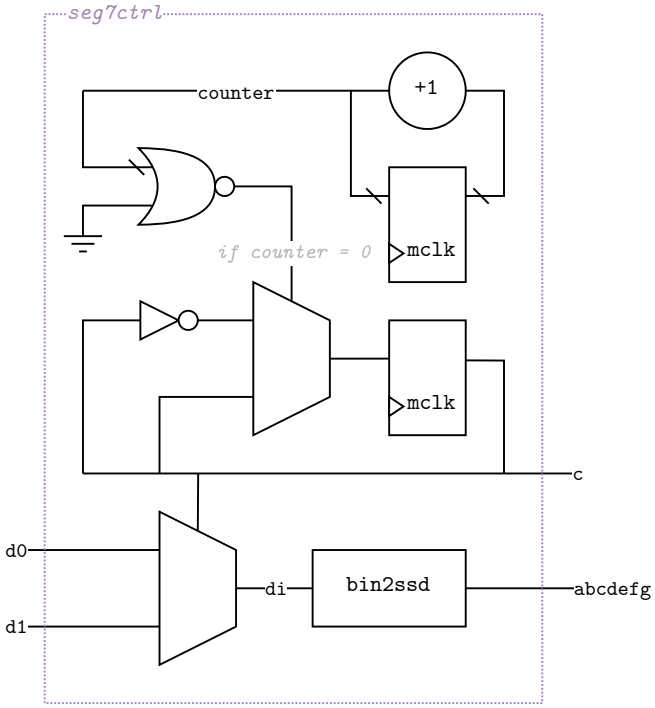
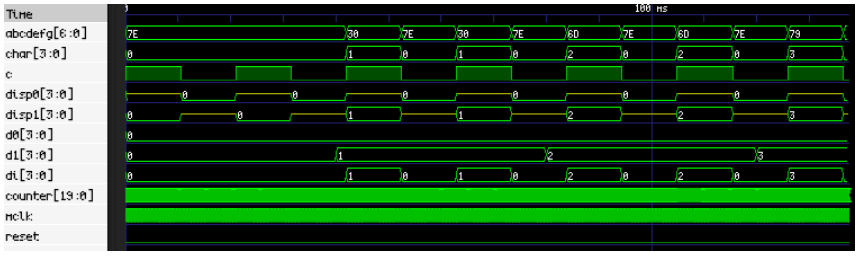


Figure 1: Possible schematic of `seg7ctrl`. Reset functionality is not illustrated.

Sample `tb_seg7ctrl.vhd` run:



c) `TODO!`

d) `TODO!`