Oblig 2

VHDL

IN3160 / IN4160

Version 1.4/19.01.2021

The goal of this exercise is generally described in Oblig 1, and also to get started designing using VHDL.

a)

In this exercise, you will design a 2-to-4 bit decoder. Use a **case** statement in a process to achieve this. The outputs on the decoder should be active low, see truth table below. The decoder shall be implemented on the test board. Use SW1 and SW2 as input, and LD1, LD2, LD3 and LD4 as output.

Test all the possible options for the switches in the simulator (modelsim/Questa). Create a script (.do file) that runs the simulation and displays the waveform.

SW2	**SW1**	**LD4**	**LD3**	**LD2**	**LD1**
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

Approval:

VHDL design file, do file for test, and display of waveform, as well as XDC file.

The exercise must be demonstrated to the laboratory supervisor for approval (except during covid).

b) Create separate files for the entity and architecture. Create another architecture that implements the decoder in a concurrent statement using the **select** statement. Make exactly one deliberate change in the LED output, and make a comment for it in the VHDL architecture. Modify the .do file to compile the newest files and display the new waveform.

Approval:

VHDL design files, modified .do file, waveform.