Q4)

1. and **$t2**, $s1, $s2
2. sub $s4, **$t2**, $s3
3. or $s7, $s6, **$t2**
4. add $t7, $t2, $t5
5. beq $t2, $s8, exit
6. sw $s9, 100($t2)

Data hazards will occur at instruction (2) and (3) because their register "$t2" depend on the preceding "and" instruction.

Control hazards will occur at instruction (6).

instruction (2)	instruction (3)
EX hazard	MEM hazard
EX/MEM.RegWrite = true EX/MEM.RegisterRd ≠ 0 EX/MEM.RegisterRd = ID/EX.RegisterRs	MEM/WB.RegWrite = true MEM/WB.RegisterRd ≠ 0 MEM/WB.RegisterRd = ID/EX.RegisterRt