HW#7 (CSC390) **Due: 03/23/2018 by 11:00PM on Blackbaord**

Q1. (Read chapter#3 (pages 178-182) of your text book before you solve the following questions)

(a) MIPS assembler generates an exception error when overflow occurs in mathematical operation of signed numbers. Write a MIPS assembly language program that will check overflows during the element by element addition between the array elements (signed numbers) of two vectors A and B and store the results in C vector. If overflow occurs the code will store $0xFFFFFFFF_{hex}$ in the corresponding memory location of the C vector, otherwise store the actual addition results.

Consider the following vectors A and B and store the results C vectors in your coding:

A = [1000000000, 2000000000, 2000000000, -1000000000, -2000000000];

B= [1000000000, -1000000000, 1000000000, -1000000000, -1000000000];

C=[. . . …. …. …];

(b) Write a MIPS assembly language program that will check overflows during the element by element addition between the array elements (unsigned numbers) of two vectors A and B and store the results in C vector. If overflow occurs the code will store 0x00000000 in the corresponding memory location of the C vector, otherwise store the actual addition results.

Consider the following vectors A and B and store the results C vectors in your coding:

A = [1000000000, 2000000000, 2000000000, 1000000000, 2000000000];

B = [3000000000, 3000000000, 1000000000, 4000000000, 2000000000];

C=[. . . …. …. …];

Note: Please turn in your Code on the Blackboard by 03/23/2018 by 11:00PM

Q2. The following Circuit performs the multiplication of two 32-bit unsigned binary numbers and produces a 64-bit result. Figure 1 shows the three steps multiplication algorithm that the circuit performs to produce the result. Suppose, you are assigned to design a 5-bit multiplier circuit which will perform the multiplication of the two 5-bit unsigned numbers A=$(11011)_2$ and B=$(10011)_2$ and produce a 10-bit result. Draw the necessary hardware and show the results produced in each iteration of your algorithm. Hints: see figure 3.6 (page 187) of our text book.

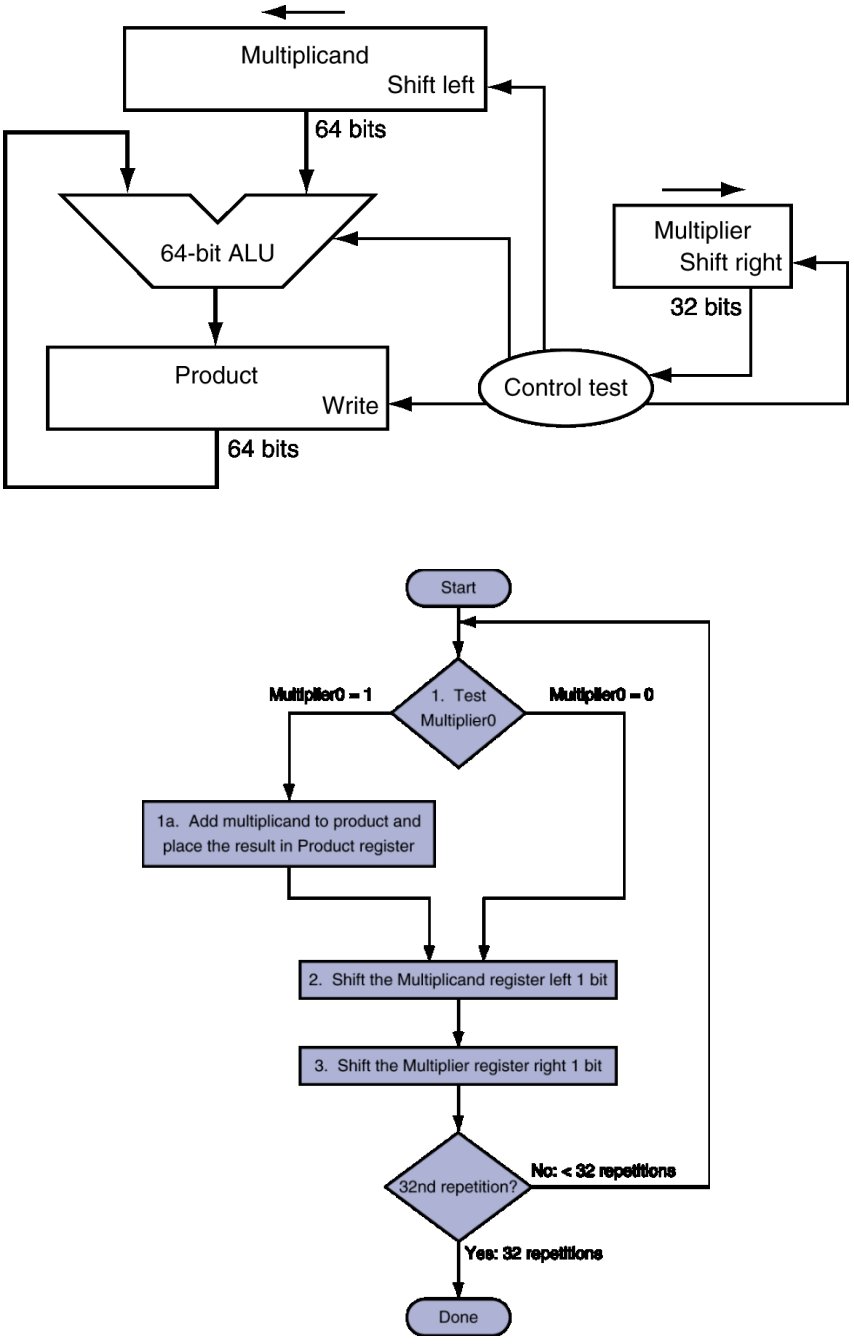

Figure 1

Q3 (a). The optimized version of the hardware and its corresponding algorithm is shown in figure 2. Note that the right half of the product register is now initialized with the multiplier.

Suppose, you are assigned to design a 5-bit multiplier circuit which will perform the multiplication of the two 5-bit signed numbers A=$(11011)_2$ and B=$(01011)_2$ and produce a 10-bit result. Draw the necessary hardware and show the results produced in each iteration of your algorithm. Hints: see slide 13 of the Chapter_03.ppt posted on the Blackboard.

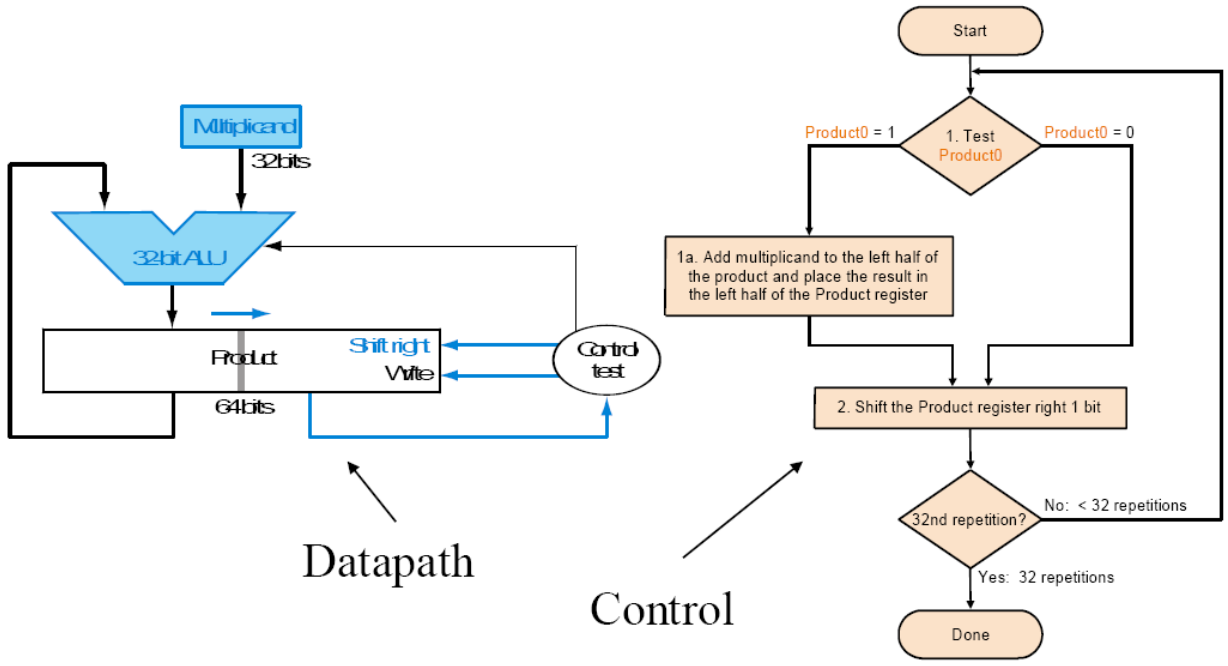

Figure 2

Q3 (b). Verify that the above can also be used to perform the multiplication of the two 5-bit **unsigned** numbers A=$(11011)_2$ and B=$(01011)_2$ and produce a 10-bit result. Show the results produced in each iteration of your algorithm

Q4. To improve the execution speed of the above multiplier circuits, a Fast Multiplication Hardware, as shown in figure 3, is designed using (n-1) adder circuits, which perform the multiplication of two n-bit numbers and produces the 2n-bit result. Suppose, you are assigned to design a 5-bit Fast Multiplication Hardware circuit which will perform the multiplication of the two 5-bit unsigned numbers A=$(11011)_2$ and B=$(10011)_2$ and produce a 10-bit result. Draw the necessary hardware and show the results produced in step of the multiplication process.

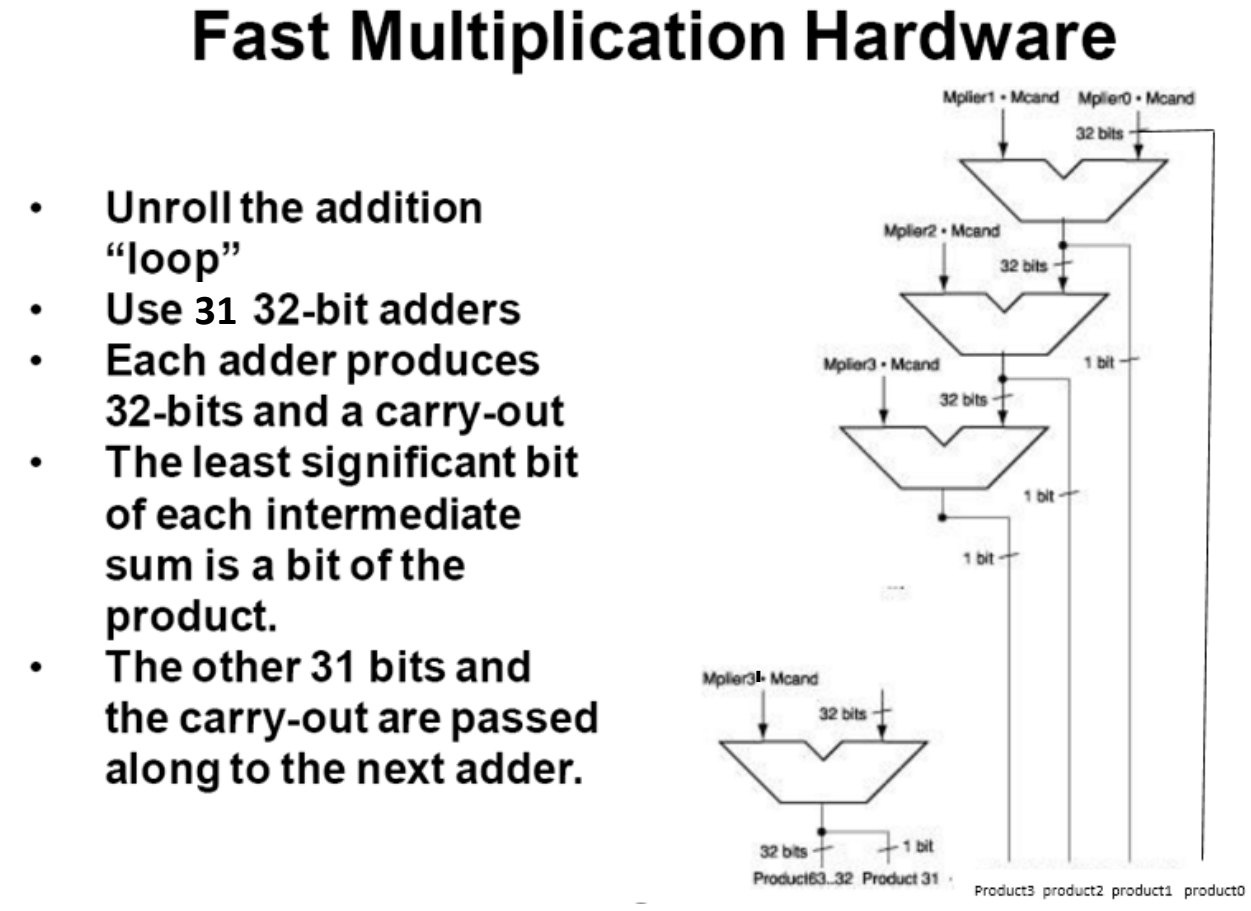

Figure 3