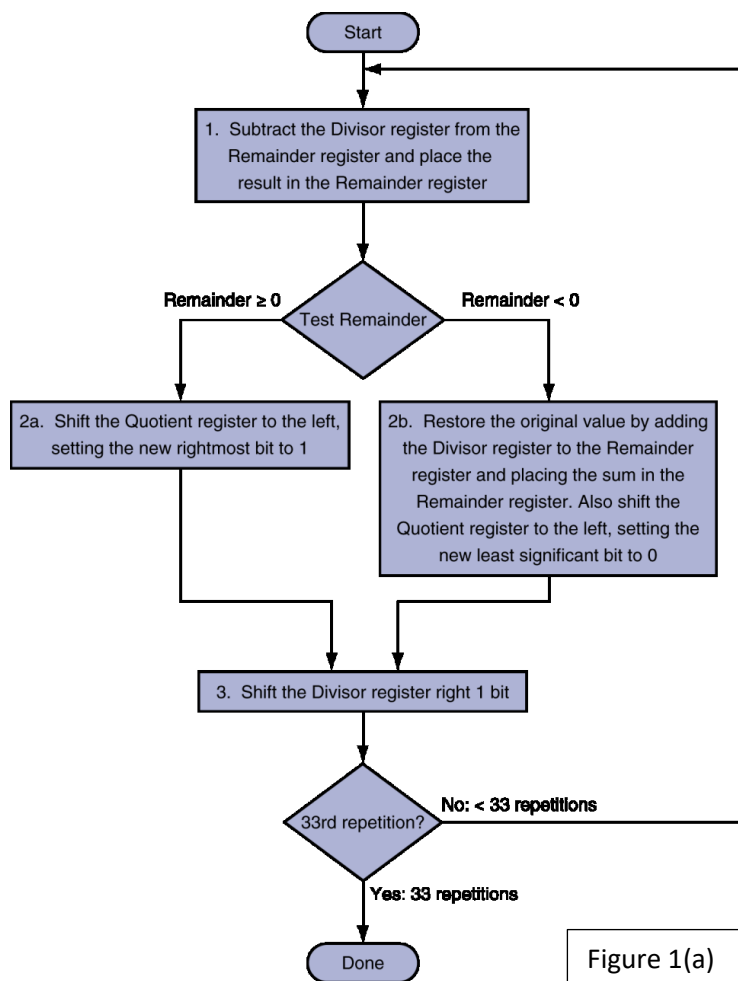
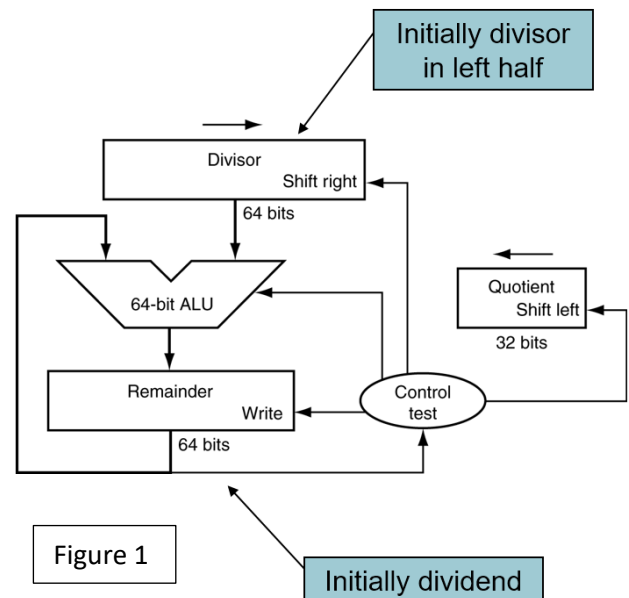


**Q1.** The Circuit as shown in Figure 1 performs the division of two 32-bit unsigned binary numbers and produces the Quotient and Remainder in the respective registers. Figure 1(a) shows the three steps division algorithm that the circuit performs to produce the result. Suppose, you are assigned to design a 5-bit division circuit that will perform the division of the two 5-bit unsigned numbers  $A=(11011)_2$  and  $B=(00101)_2$  and produce the Quotient and Remainder of the division. Draw the necessary hardware and show the results produced in each iteration of your algorithm. Hints: see figure 3.10 (page 192) of our text book.



**Q2.** The optimized version of the divider hardware and its corresponding algorithm is shown in figure 2. Note that the right half of the remainder register is now initialized with the dividend.

Suppose, you are assigned to design a 5-bit division circuit that will perform the division of the two 5-bit unsigned numbers  $A=(11011)_2$  and  $B=(00101)_2$  and produce the Quotient and Remainder of the division. Draw the necessary hardware and show the results produced in each iteration of your algorithm. Hints: see optimized divider class note (ppt) posted on the Blackboard.

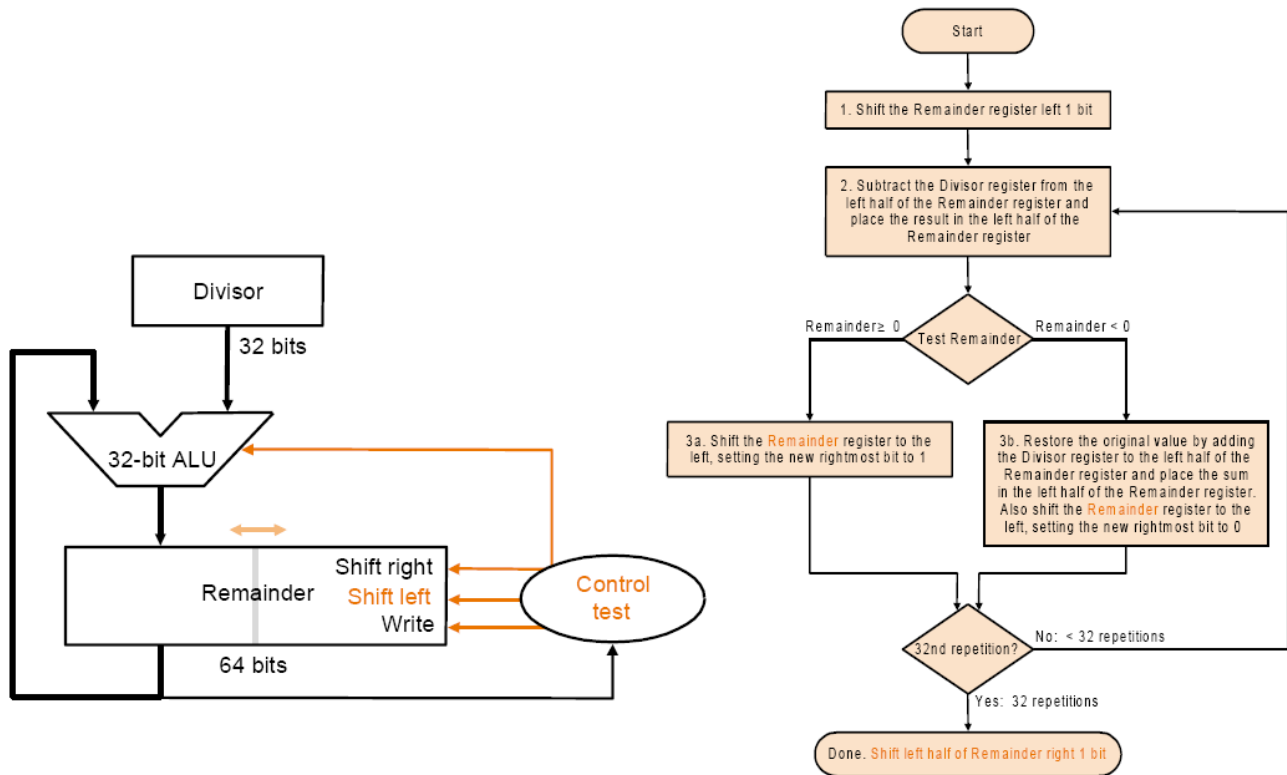


Figure 1

**Q3.** IEEE 754 binary representation of floating point numbers is widely used in today's computer systems. Consider the following decimal numbers and represent them in their corresponding single precision IEEE 754 format. Show all the steps of your calculation. Write down the single precision numbers in Hex format and use MARS to verify that your calculation is correct.

- (a)  $(6.725)_{10}$
- (b)  $(-0.3125)_{10}$