dependent on a result still in the pipeline must still work properly with this optimization. For example, to implement branch results. Moving the branch test to the ID stage implies additional forwarding and hazard detection hardware, since a branch + Moving the branch decision up requires two actions to occur earlier: computing the branch target address and evaluating value and the immediate feld in the IF/ID pipeline register, so we just move the branch adder from the EX stage to the ID + The harder part is the branch decision itself. For branch equal, we would compare the two registers read during the ID stage; of course, the branch target address calculation will be performed for all instructions, but only used when needed. stage to see if they are equal. Equality can be tested by frst exclusive ORing their respective bits and then ORing all the the branch decision. The easy part of this change is to move up the branch address calculation. We already have the PC on equal (and its inverse), we will need to forward results to the equality test logic that operates during ID