HW#1 (CSC390-Spring 2018)

SOLUTION

Q1. Computer A has an overall CPI of 1.3 and can be run at a clock rate of 600MHz. Computer B has a CPI of 2.5 and can be run at a clock rate of 750 Mhz. We have a particular program we wish to run. When compiled for computer A, this program has exactly 100,000 instructions. How many instructions would the program need to have when compiled for Computer B, in order for the two computers to have exactly the same execution time for this program?

Sol:

$$(\text{CPUTime})_A = (\text{Instruction count})_A * (\text{CPI})_A * (\text{Clock cycle Time})_A$$
$$= (100{,}000)*(1.3)/(600*10^6) \text{ ns}$$
$$(\text{CPUTime})_B = (\text{Instruction count})_B * (\text{CPI})_B * (\text{Clock cycle Time})_B$$
$$= (I)_B*(2.5)/(750*10^6) \text{ ns}$$

Since $(\text{CPUTime})_A = (\text{CPUTime})_B$,

we have to solve for $(I)_B$ and get 65000

1.6 [20] <§1.6> Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

a. What is the global CPI for each implementation?

b. Find the clock cycles required in both cases.

Solution:

1.6

a. Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.

Time = No. instr. × CPI/clock rate

Total time P1 = $(10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3)/(2.5 \times 10^9) = 10.4 \times 10^{-4}$ s

Total time P2 = $(10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)/(3 \times 10^9) = 6.66 \times 10^{-4}$ s

CPI(P1) = $10.4 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 2.6$

CPI(P2) = $6.66 \times 10^{-4} \times 3 \times 10^9/10^6 = 2.0$

b. clock cycles(P1) = $10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3 = 26 \times 10^5$

clock cycles(P2) = $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

1.8 The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

1.8.1 [5] <§1.7> For each processor find the average capacitive loads.

1.8.2 [5] <§1.7> Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

1.8.3 [15] <§1.7> If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

1.8.1 $C = 2 \times DP/(V^{2*}F)$

Pentium 4: C = 3.2E–8F

Core i5 Ivy Bridge: C = 2.9E–8F

1.8.2 Pentium 4: 10/100 = 10%

Core i5 Ivy Bridge: 30/70 = 42.9%

1.8.3

(SP_new +DP_new)/(SP_old + DP_old) = 0.90

DP_new = ½ x C x V_new^2 x F
SP_old = V_old x I
SP_new = V_new x I

Therefor,
$V\_new = [2 \times DP\_new / (CxF)]^{1/2}$

DP_new = 0.9 x (S_old +D_old) – S_new
SP_new = V_new x (SP_old/V_old)

For Pentium 4:
SP_new = V_new x (10/1.25) = V_new x 8
DP_new = 0.90x100 – V_newx8 = 90 – V_new X 8
$V\_new = [2x(90-V\_new \text{ X } 8)/(3.2E\text{-}08 \text{ X } 3.6E9)]^{1/2}$
V_new = 1.182 Volts

For Core i5:
SP_new = V_new x (30/0.9) = V_new x 33.3
DP_new = 0.90 x 70 – V_new x 33.3 = 63 – V_new x 33.3
V_new = $[2x(63\text{-}V\_new \text{ X } 33.3)/(2.9E\text{-}08 \text{ X } 3.4E9)]^{1/2}$
V_new = 0.84Volts

1.9 Assume for arithmetic, load/store, and branch instructions, a processor has CPIs of 1, 12, and 5, respectively. Also assume that on a single processor a program requires the execution of 2.56E9 arithmetic instructions, 1.28E9 load/store instructions, and 256 million branch instructions. Assume that each processor has a 2 GHz clock frequency.

Assume that, as the program is parallelized to run over multiple cores, the number of arithmetic and load/store instructions per processor is divided by 0.7 x p (where p is the number of processors) but the number of branch instructions per processor remains the same.

1.9.1 [5] <§1.7> Find the total execution time for this program on 1, 2, 4, and 8 processors, and show the relative speedup of the 2, 4, and 8 processor result relative to the single processor result.

1.9.2 [10] <§§1.6, 1.8> If the CPI of the arithmetic instructions was doubled, what would the impact be on the execution time of the program on 1, 2, 4, or 8 processors?

1.9.3 [10] <§§1.6, 1.8> To what should the CPI of load/store instructions be reduced in order for a single processor to match the performance of four processors using the original CPI values?

Sol:

1.9.1

Given, Processor frequency, f=2GHz. Formula, Execution time = CPIxInstruction/f

Processor nos.	Arithmetic Instruction	CPI-Arith	Load/Store Instruction	CPI-L/S	Brunch Instruction	CPI-Branch	Total Cycles	Execution Time	Speed-Up
1	2.56E+09	1	1.29E+09	12	2.56E+08	5	1.93E+10	9.66E+00	1.00E+00
2	1828571429	1	921428571	12	2.56E+08	5	1.42E+10	7.08E+00	1.36E+00
4	914285714	1	460714286	12	2.56E+08	5	7.72E+09	3.86E+00	2.50E+00
8	457142857	1	230357143	12	2.56E+08	5	4.50E+09	2.25E+00	4.29E+00

1.9.2

Processor nos.	Arithmetic Instruction	CPI-Arith	Load/Store Instruction	CPI-L/S	Brunch Instruction	CPI-Branch	Total Cycles	Execution Time	Speed-Up
1	2.56E+09	2	1.29E+09	12	2.56E+08	5	2.19E+10	10.94	1.00E+00
2	1828571429	2	921428571	12	2.56E+08	5	1.60E+10	7.997143	1.37E+00
4	914285714	2	460714286	12	2.56E+08	5	8.64E+09	4.318571	2.53E+00
8	457142857	2	230357143	12	2.56E+08	5	4.96E+09	2.479286	4.41E+00

1.9.3

(2.56E9*1+1.29E9*(Desired_CPI_LS)+2.56E8*5)/f=3.86

So, the Desired CPI_LS = 3.00996678