Processors	No. of Instruction Per Processors			CPI		
	Arithmetic	Load/Store	Branch	Arithmetic	Load/store	Branch
1	2.56E+09	460714286	2.56E+08	2	10	6
4	914285714	230357143	6.40E+07	2	10	6
8	457142857	115178571	3.20E+07	2	10	6

(a)

Processors	No. of Instruction Per Processors			Total Instruction	Aggregate
	Arithmetic	Load/Store	Branch		
1	2.56E+09	460714286	2.56E+08	3.28E+09	**3.28E+09**
4	914285714	230357143	6.40E+07	1.21E+09	**3.28E+09**
8	457142857	115178571	3.20E+07	6.04E+08	**3.28E+09**

Since the purpose of the parallel processors is to distribute (share) the work load among them,
Theaggregrate number of Instructions excuted by parallel processors remain same as the total number of i

(b) Execution time = total_cycles/frequency

Processor nos.	Arithmetic Instruction	CPI-Arith	Load/Store Instruction	CPI-L/S	Brunch Instruction	CPI-Branch	Total Cycles
1	2.56E+09	2	460714286	10	2.56E+08	6	1.13E+10
4	914285714	2	230357143	10	6.40E+07	6	4.52E+09
8	457142857	2	115178571	10	3.20E+07	6	2.26E+09

(C) (914285714*2+230357143*(Desired_CPI of Load/Store)+6.40E+07*6)/3GHz = 7.53E-01
So the Desired_CPI of Load/Store = 0.20155

nstruction

Execution Time	Speed-Up
3.75E+00	1.00E+00
1.51E+00	2.49E+00
7.53E-01	4.98E+00