Q1. One way to improve branch performance is to reduce the cost of the taken branch. Thus far, we have assumed the next PC for a branch is selected in the MEM stage, but if we move the branch execution earlier in the pipeline, then fewer instructions need be flushed and thereby pipelining would become more efficient. The designers observed that many branches rely only on simple tests (equality or sign, for example) and that such tests do not require a full ALU operation but can be done with at most a few gates. Equality can be tested by first exclusive ORing their respective bits and then ORing all the results. Figure 1 shows the datapath and control signals of such a MIPS processor. (Pages 316-320 of your text)

Show what happens when the branch is taken in the following instruction sequence, assuming the pipeline is optimized for branches that are not taken and the branch execution is moved to the ID stage:

10 add $10, $4, $6

14 beq $1, $7, 8

18 or $13, $2, $6

22 and $12, $2, $5

24 add $14, $4, $2

………..

50 sw $4, 50($7)

Use figure 1 to show what happen when a branch is taken. Specifically, use Figure 4.62 as a reference and indicate the input/output values of the PC, adders, pipeline register data and control signals.





