Lecture 17 In-Class Worksheet

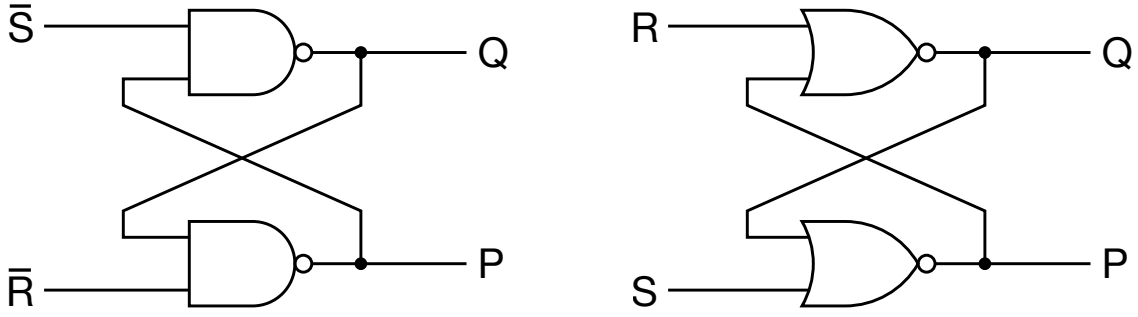
1 Learning Objectives

This worksheet is based on Lumetta course notes section 2.6. After completing this lesson, you will know how to:

- [S17-1] Construct $\bar{R}$-$\bar{S}$, R-S, and D latches and demonstrate their behavior using a timing diagram.
- [S17-2] Construct a positive edge-triggered D flip-flop and demonstrate its behavior using a timing diagram.

2 RS Latches

An $\bar{R}$-$\bar{S}$ latch (also called an $\bar{S}$-$\bar{R}$ latch) is a device capable of storing a bit of information. An implementation using **NAND** gates is shown below on the left. An R-S latch (also called an S-R latch) implemented using **NOR** gates is shown on the right. Note the *active high* inputs and their position: R input opposite the Q (non-inverted) output.



The behavior of these latches can be described using a truth table where the feedback variables Q and P appear as both inputs and outputs. To avoid confusion, we will use Q^+ to denote the output Q and P^+ to denote the output P. The truth tables for the $\bar{R}$-$\bar{S}$ is shown below on the left:

$\bar{R}$	$\bar{S}$	Q	P	Q^+	P^+
0	0	–	–	*Illegal*	
0	1	–	–	0	1
1	0	–	–	1	0
1	1	0	1	0	1
1	1	1	0	1	0

R	S	Q	P	Q^+	P^+
0	0	0	1		
0	0	1	0		
0	1	–	–		
1	0	–	–		
1	1	–	–	*Illegal*	

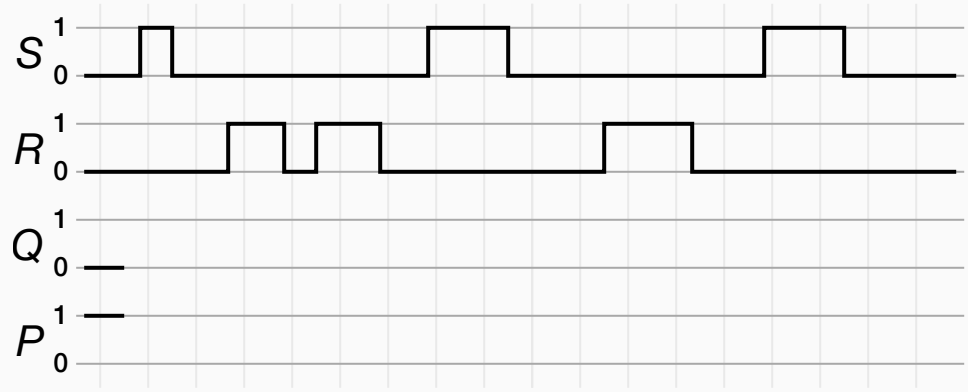
Q1. Complete the R-S latch table above, right.

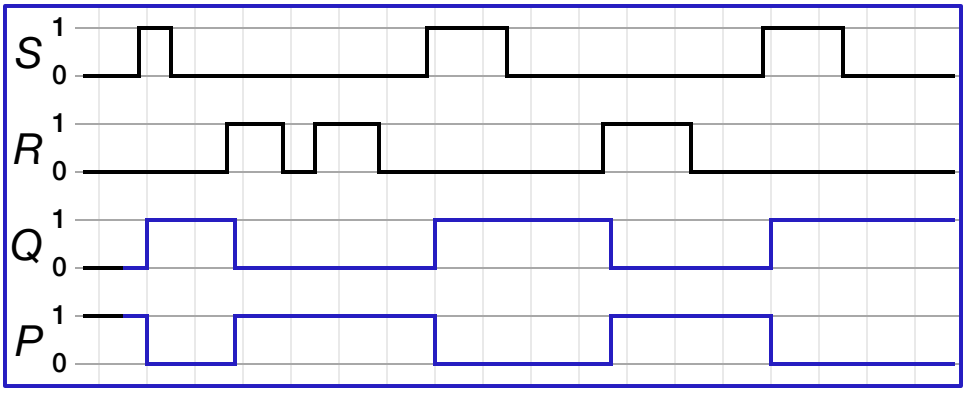
R	S	Q	P	Q^+	P^+
0	0	0	1	0	1
0	0	1	0	1	0
0	1	–	–	1	0
1	0	–	–	0	1
1	1	–	–	*Illegal*	

3 Timing Diagrams

Timing diagrams show the value of one or more signals as a function of time. Time runs left to right, and the signals are arranged vertically.

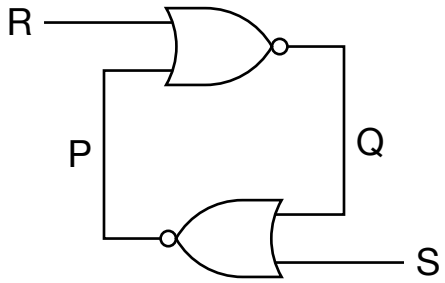
Q2. Complete the timing diagram below for an R-S latch.





4 Undesirable Behavior

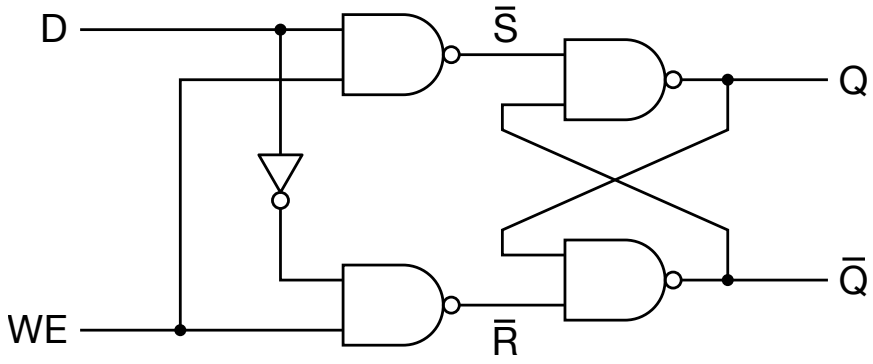
In the truth tables describing the behavior of the $\bar{R}$-$\bar{S}$ and R-S latches, we marked some inputs *Illegal*. Let's see what happens when both the *set* and *reset* signals are asserted (made active). We'll work with the R-S latch. To make things easier to see, we've redrawn it in a different way.



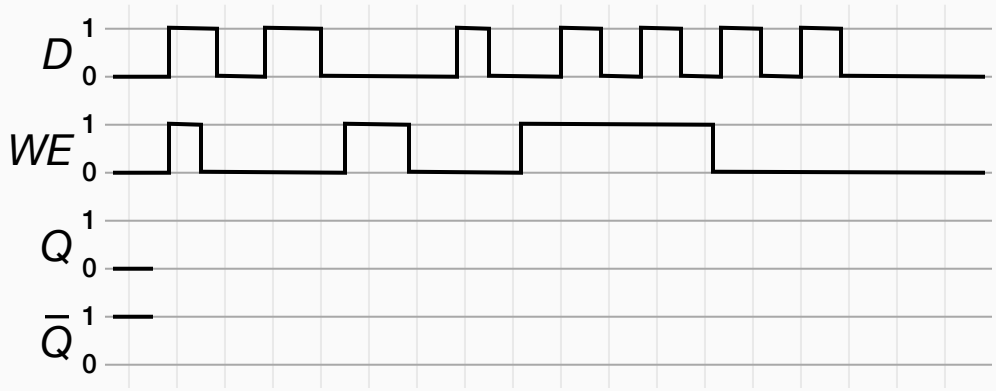
Starting with $R = S = 1$, we have $Q = 0$ and $P = 0$. What happens when we simultaneously set $R = S = 0$? The output of both NOR gates changes to 1, and we have $Q = 1$ and $P = 1$. But this causes the output of the NOR gates to change to 0, giving $Q = 0$ and $P = 0$. But this changes the output of the NOR gates to 1, and so on. In an idealized circuit, this oscillation will continue indefinitely. In practice, one of the gates will be slightly slower, and the output will settle to $Q = 0, P = 1$ or $Q = 1, P = 0$. Such unpredictable behavior is not desirable, so we avoid these inputs.

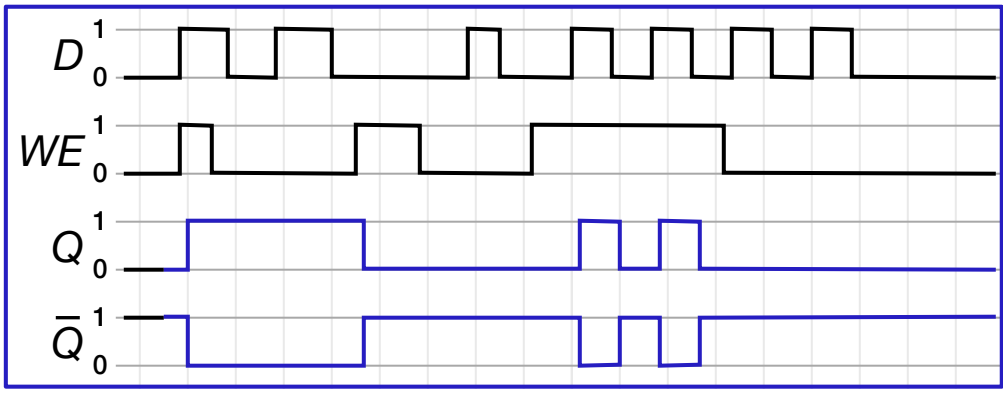
5 D Latch

The D latch avoids the undesirable behavior described above by preventing the illegal input combination. Instead, one input, D, gives the value to be stored, and the other, WE (write enable, sometimes just E), controls when the value is stored. When $WE = 1$, Q takes on value of D. When $WE = 0$, Q retains its previous value. Since P is now always the opposite of Q, we've replaced it with $\bar{Q}$.



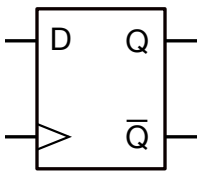
Q3. Complete the timing diagram below for a D latch.

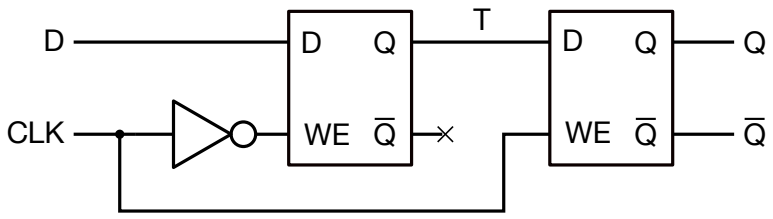




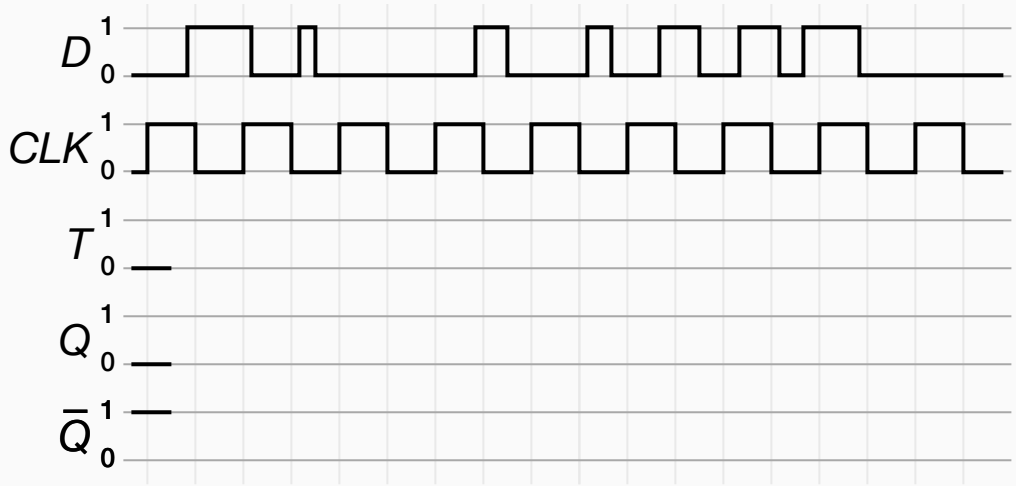
6 Positive Edge-Triggered D Flip-Flop

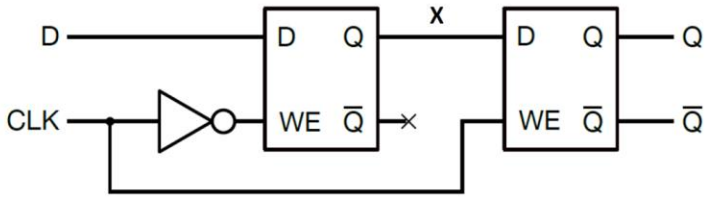
A positive edge-triggered D flip-flop can be constructed from two D latches, as shown below. *The stored value Q only changes on the rising edge of the clock CLK. At all other times, the the output does not change.* The standard symbol for a positive edge-triggered D flip-flop is shown on the right. (The input with the triangle symbol is the clock.)





Q4. Complete the timing diagram below for a positive edge-triggered D flip-flop.





Complete the timing diagram below for a positive edge-triggered D flip-flop.

Note: Just look at the rising edge of the clock- D gets stored in Q at the rising edge of the clock and remains same until the next rising edge of the clock

Complete the timing diagram below for a positive edge-triggered D flip-flop.