University of Illinois at Urbana-Champaign
Dept. of Electrical and Computer Engineering

ECE 120: Introduction to Computing

Finite State Machines (FSMs)

A Finite State Machine (FSM) Models a System

A model of a system
- system moves among a finite set of states
- motion based on external inputs
- produces external outputs

Examples include:
- coin/bill-operated machines,
- many vehicle control systems, and
- computers executing programs.

An FSM Consists of Five Parts

1. a finite set of states **(bits)**
2. a set of possible inputs **(bits)**
3. a set of possible outputs **(bits)**
4. a set of transition rules **(Boolean expressions)**
5. methods for calculating outputs **(Bool. expr's)**

When implemented as a digital system, all parts of an FSM must be mapped to … **bits!**

A Digital FSM Must be Complete

We implement FSMs as clocked synchronous sequential circuits. (So state ID bits are stored in flip-flops.)

Given **any state** and **any combination of inputs**, a **transition rule** from the given state to a next state **must be defined**.

Self-loops–transitions from a state to itself–are acceptable.

Use Keyless Entry as a Motivating Example

meaning	state	driver's door	other doors	alarm on?
vehicle locked	LOCKED	locked	locked	no
driver door unlocked	DRIVER	unlocked	locked	no
all doors unlocked	UNLOCKED	unlocked	unlocked	no
alarm sounding	ALARM	locked	locked	yes

Table is a **list of abstract states**.

A List of Abstract States Need Only List States

In a list of abstract states,

- we can just list the states.
- Adding human meanings is optional (good to have if state names are generic).

Including outputs

- is also optional,
- and implies that **outputs depend only on state**.*

*An extra assumption that we will always make in our class.

An Abstract Next-State Table Captures Expected Behavior

To specify transitions, we use **a next-state table**, which maps combinations of states and inputs into next states.

This is an **abstract next-state table**.

state	action/input	next state
LOCKED	push “unlock”	DRIVER
DRIVER	push “unlock”	UNLOCKED
(any)	push “lock”	LOCKED
(any)	push “panic”	ALARM

Abstract Next-State Table Does Not Answer All Questions

We wrote transitions for typical use cases, but **the table can be incomplete, ambiguous, and even inconsistent**.

For example, what happens if the user pushes "lock" and "unlock" at the same time?

state	action/input	next state
LOCKED	push "unlock"	DRIVER
DRIVER	push "unlock"	UNLOCKED
(any)	push "lock"	LOCKED
(any)	push "panic"	ALARM

Many Design Decisions are Usually Needed

All such **design decision questions should eventually be considered, and preferably answered.**

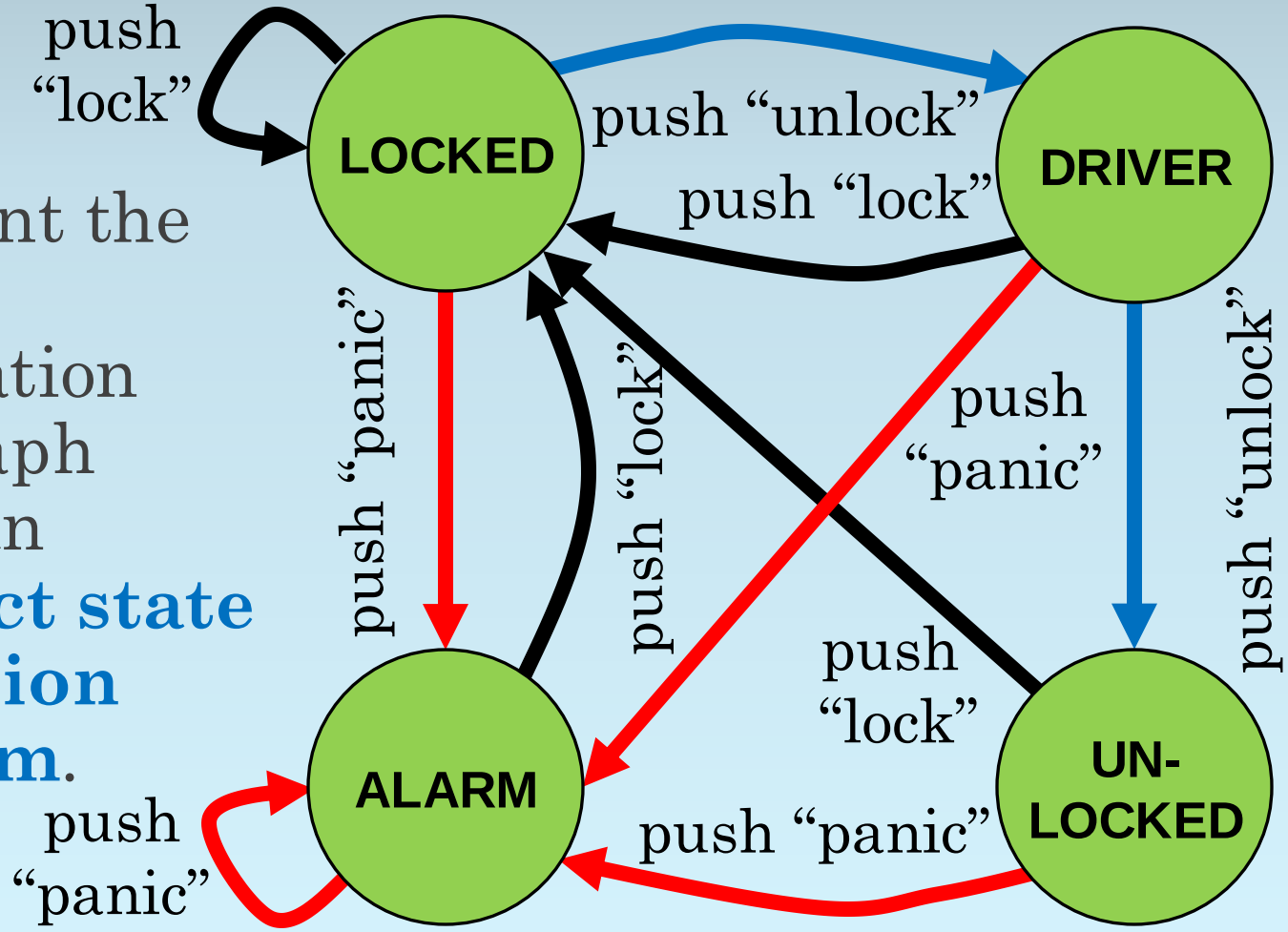
Be aware: **any digital logic implementation will define answers**.

Only when any possible answer is acceptable should you make use of "don't cares."

Typically, you should **review the final implementation** to determine how any questions left open are answered.

Abstract State Transition Diagram: the Same Information

We can represent the same information as a graph called an **abstract state transition diagram**.



It's Time to Make Our Design Complete and Concrete

The abstract next-state table and the abstract state transition diagram (can) **contain exactly the same information**.

They answer the same questions.

And **neither is complete**.

So. It's time for … **bits!**

Let's Start with the State Identifiers

How many bits do we need to identify a state?

There are 4 states.

$\lceil \log_2(4) \rceil = 2$ **bits.**

Call them S_1S_0.

"S" is for "S(tate)."

All Outputs and Inputs Must Also Use Bits

What about outputs?

D driver door; 1 means unlocked

R remaining doors; 1 means unlocked

A alarm; 1 means alarm is sounding

And inputs?

U unlock button; 1 means it's been pressed

L lock button; 1 means it's been pressed

P panic button; 1 means it's been pressed

We Next Choose a Representation for States

Now we can choose a representation for states and rewrite our list of states.

The order of states in the list doesn't matter.

meaning	state	S_1S_0	D	R	A
vehicle locked	LOCKED	00	0	0	0
driver door unlocked	DRIVER	10	1	0	0
all doors unlocked	UNLOCKED	11	1	1	0
alarm sounding	ALARM	01	0	0	1

Choice of Representation Affects Amount of Logic Needed

As you may realize

- from your experience with bit-sliced designs,
- **the representation does matter**
  (for the amount of logic needed).

We will talk more later about ways to choose.

Use $S_1^+ S_0^+$ to Denote the Next State (in Next Clock Cycle)

The +'s in $S_1^+ S_0^+$ indicate that these are values **in the next clock cycle**.

Let's rewrite the next-state table with bits.

- The table gives us $S_1^+ S_0^+$ as a function of current state $S_1 S_0$ and inputs **ULP**.
- Such tables typically use binary order for states (vertical) and inputs (horizontal).
- We use Grey code order on both axes for convenience (in copying to K-maps).

How to Fill in the Next-State Table

Where should we start?

current state S_1S_0	ULP							
	000	001	011	010	110	111	101	100
00								
01								
11								
10								

What about multiple buttons?

Let's make some design decisions first…

Completing the Design Requires Decisions

To fill in the next-state table
- starting with only the abstract design,
- we **need to make many design decisions**,
- including some that we haven't even recognized yet.

For example,
- What happens when the user presses more than one button?
- What happens when the user presses "unlock" in the **UNLOCKED** state?

Make Design Decisions Early When Possible

Let's try to **make decisions first**.

Design decisions can shape the design, and **may conflict with one another**.

Making decisions early and writing them down ensures that

- any **issues are raised early**, and that
- **known decisions are not overlooked**
- (in which case the final design answers them implicitly, with no human guidance).

Start by Deciding How to Handle Multiple Buttons

We're going to start by **prioritizing the buttons**.

Our rules:

- Panic has priority!
- Lock has second priority.
- Unlock only matters when neither of the others is pressed.

Start with the Panic Button (Highest Priority)

The next-state table gives us $S_1^+ S_0^+$.

current state S_1S_0	ULP							
	000	001	011	010	110	111	101	100
00		01	01			01	01	
01		01	01			01	01	
11		01	01			01	01	
10		01	01			01	01	

panic button pushed

Continue with the Lock Button (Second Priority)

The next-state table gives us $S_1^+ S_0^+$.

current state S_1S_0	ULP							
	000	001	011	010	110	111	101	100
00		01	01	00	00	01	01	
01		01	01	00	00	01	01	
11		01	01	00	00	01	01	
10		01	01	00	00	01	01	

lock button pushed

No Buttons? No Change. All Self-Loops

What if the user pushes nothing?

current state S_1S_0	ULP							
	000	001	011	010	110	111	101	100
00	00	01	01	00	00	01	01	
01	01	01	01	00	00	01	01	
11	11	01	01	00	00	01	01	
10	10	01	01	00	00	01	01	

no buttons pushed

Finally, Unlock … But are We Done?

Two transitions were defined for Unlock.

current state S_1S_0	ULP 000	001	011	010	110	111	101	100
00	00	01	01	00	00	01	01	10
01	01	01	01	00	00			
11	11	01	01	00	00			
10	10	01	01	00	00	01	01	11

from LOCKED

What about these?

from DRIVER

We Have More Design Decisions to Make!

What should happen if we press "unlock" when the car is already fully unlocked (in the **UNLOCKED** state)?

Maybe just stay **UNLOCKED**.

What should happen if we press "unlock" while the alarm is sounding?

- Continue to lock out an attacker / thief?
- Or open the doors so that the owner can climb inside quickly?

Let's Implement Our Decisions

Ignore Unlock in both other cases.

current state S_1S_0	ULP 000	001	011	010	110	111	101	100
00	00	01	01	00	00	01	01	10
01	01	01	01	00	00	01	01	01
11	11	01	01	00	00	01	01	11
10	10	01	01	00	00	01	01	11

from ALARM

from UNLOCKED

The Rest You Know How to Do

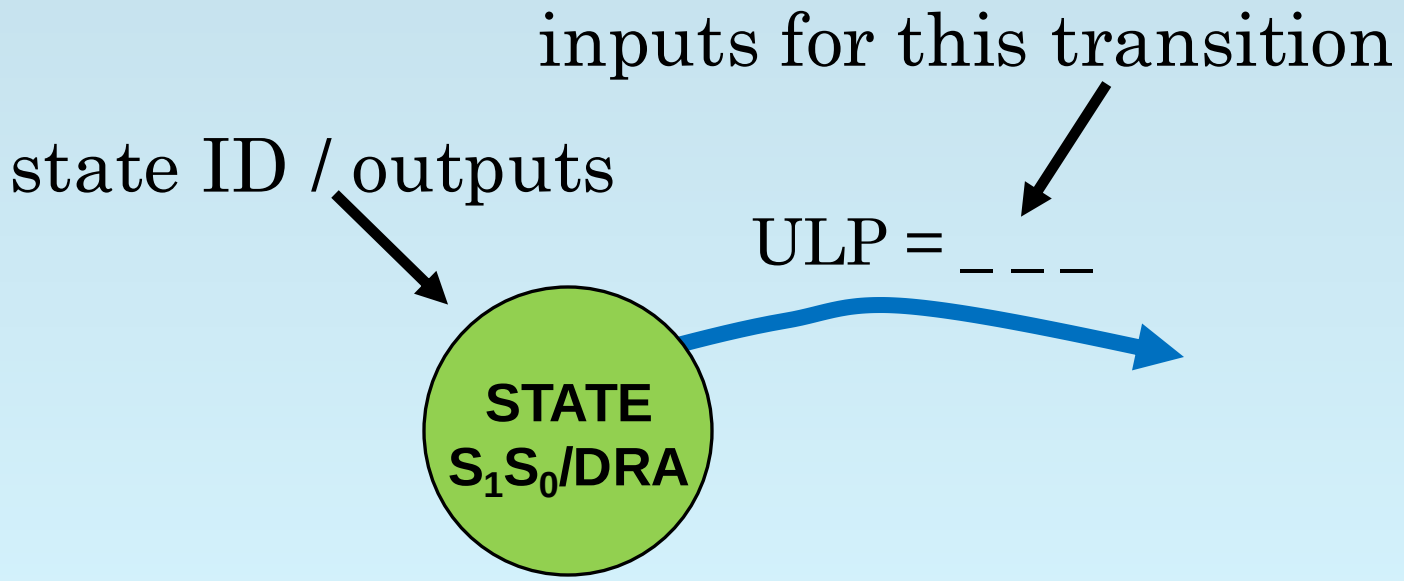
The rest is K-maps, expressions, and logic.

1. Express $\mathbf{S_1^+}$ and $\mathbf{S_0^+}$ in terms of $\mathbf{S_1}$, $\mathbf{S_0}$, **U**, **L**, and **P**.
2. Express **D**, **R**, and **A** in terms of $\mathbf{S_1}$, $\mathbf{S_0}$.
3. Build the combinational logic.
4. Put the next state expressions $\mathbf{S_1^+}$ and $\mathbf{S_0^+}$ into the **D** inputs of two flip-flops.

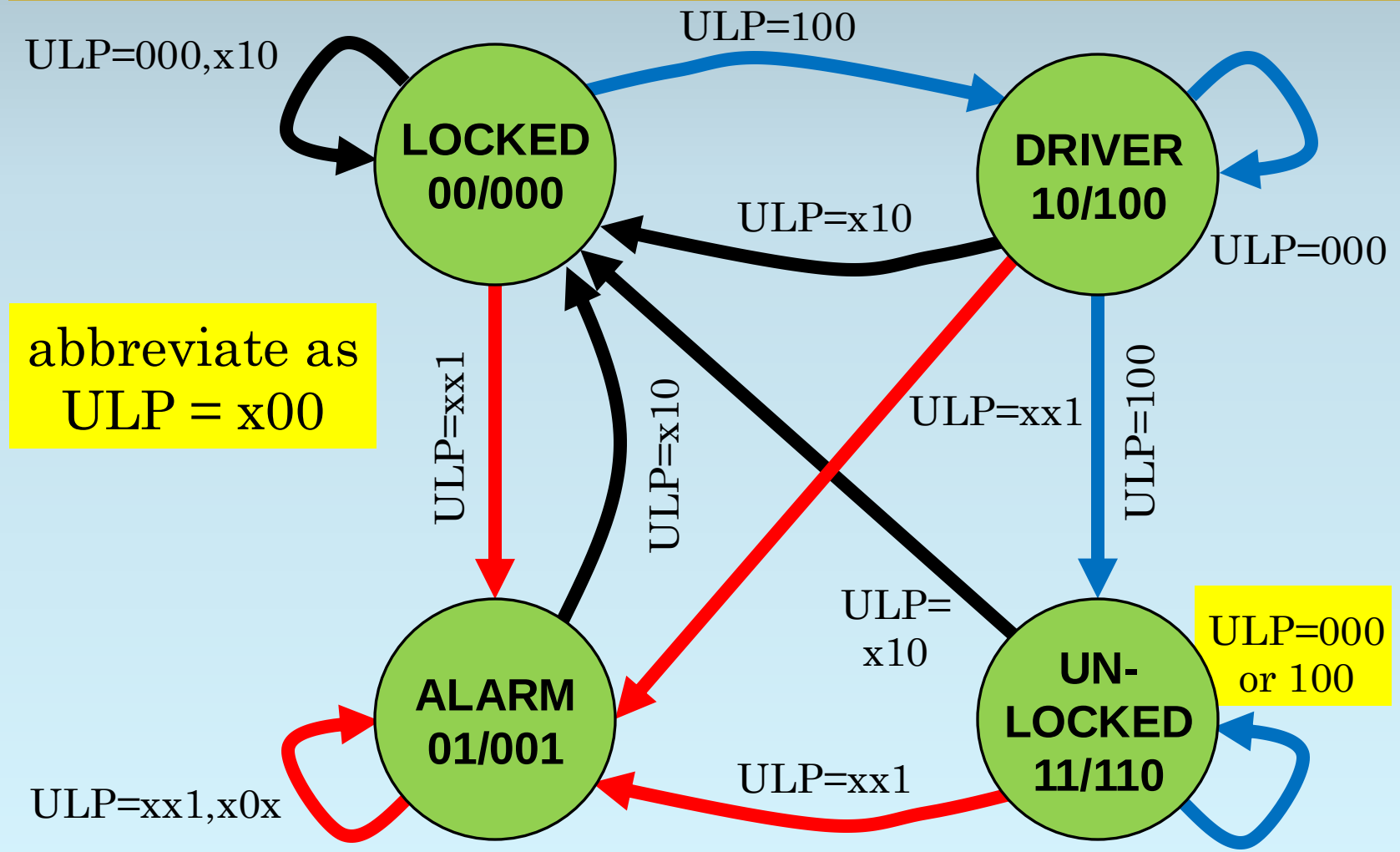
You should do it as an exercise. Break up the truth tables or use 5-variable K-maps.

One Last Tool: the Complete State Transition Diagram

The complete **state transition diagram** contains the information in both the state list and the next-state table.



Complete State Transition Diagram



Be Careful with Input Abbreviations

Input abbreviations can render a state transition diagram

- incomplete (if labels fail to cover all input combinations), or
- inconsistent (if labels indicate multiple next states).

For example,

- self-loop from **ALARM** labeled **ULP=xx1,x0x**:
- the patterns **x01** match both labels!
- In this case, these two combinations go to the same next state, so it's ok.

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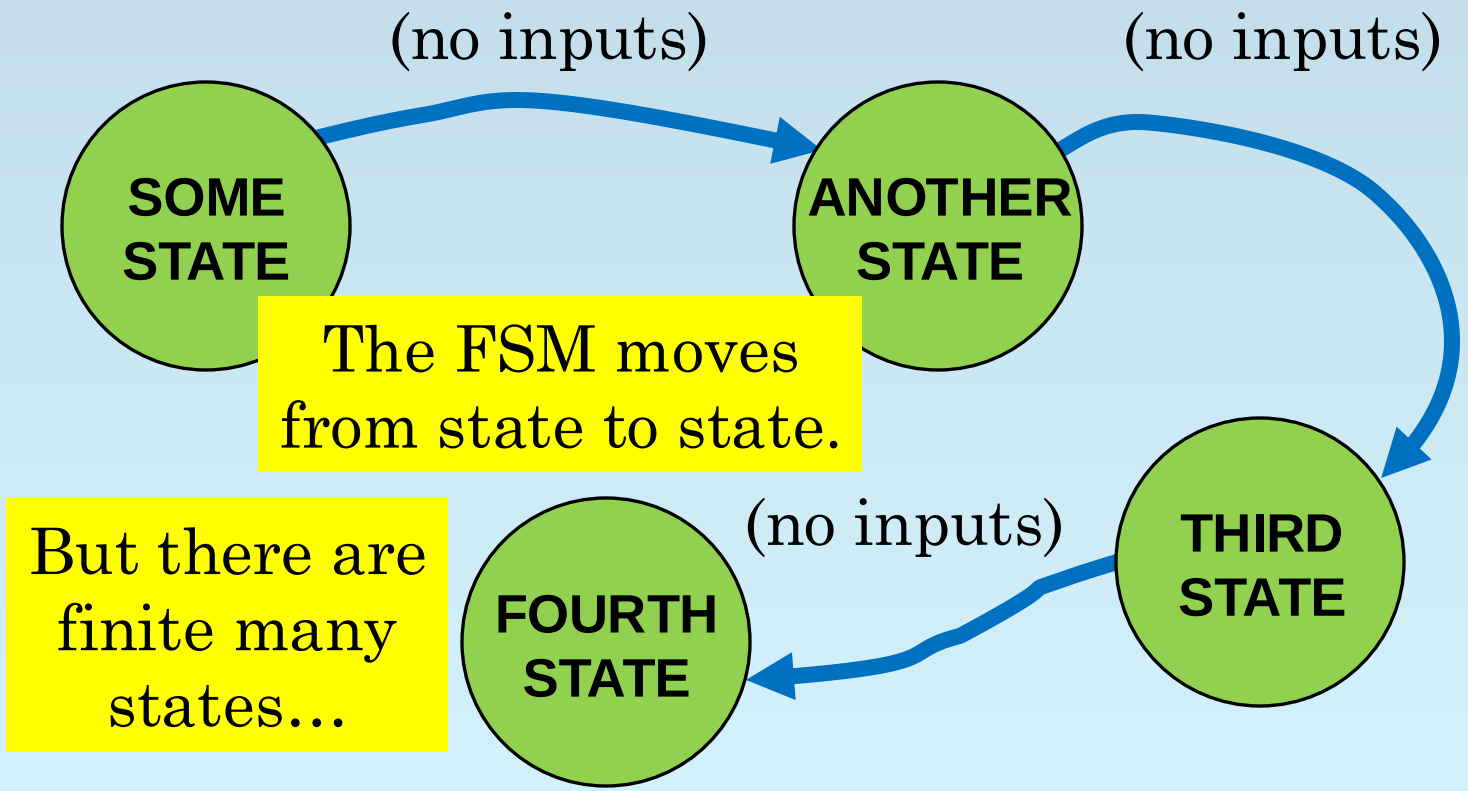
ECE 120: Introduction to Computing

Binary Counters

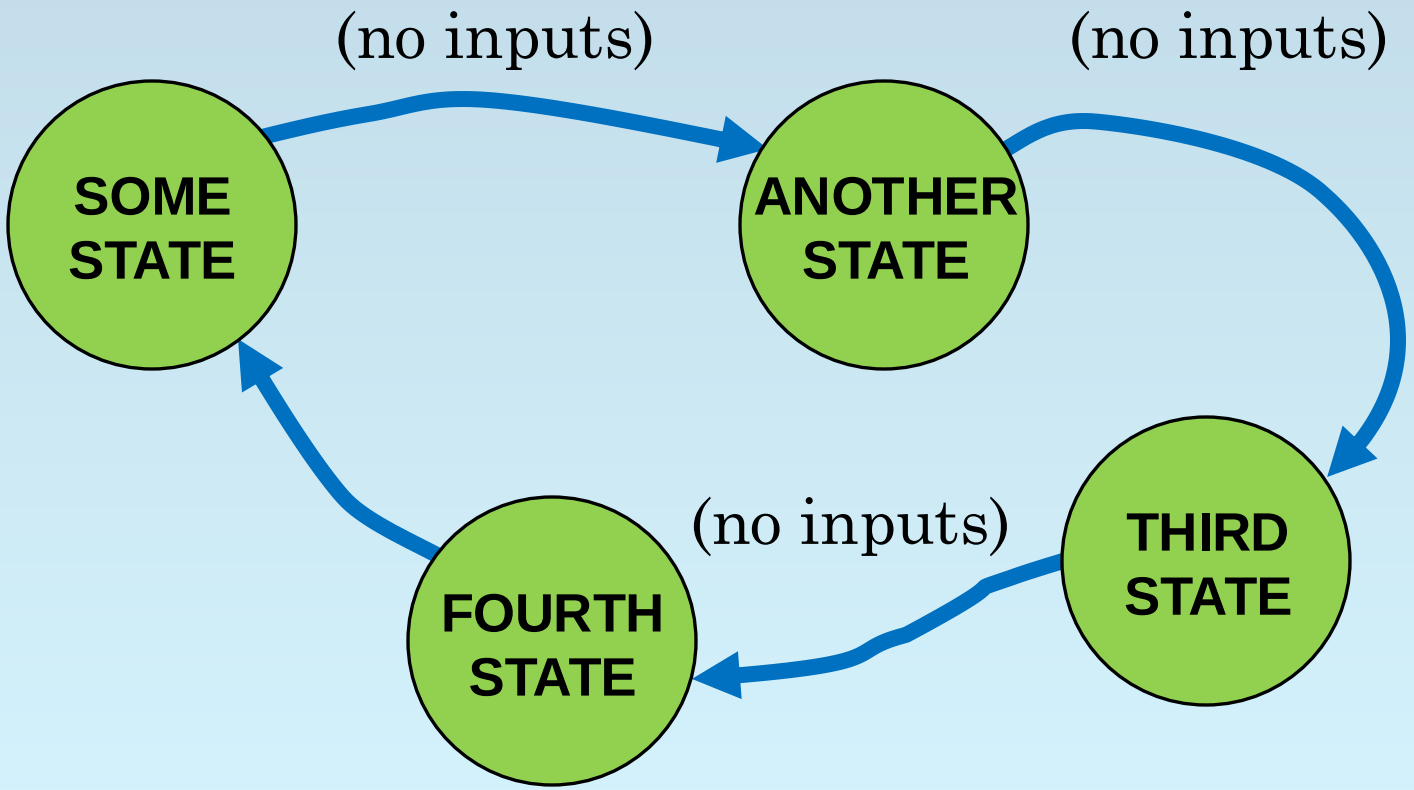
An FSM with No Inputs Moves from State to State

What happens if an FSM has no inputs?



Eventually, the States Form a Loop

So the FSM eventually returns to some state.



A Counter Repeats a Loop of States (Forever)

An FSM without inputs is called a **counter**.

A counter may sometimes have inputs

- to start/stop the counter
- to reset the counter to a known state
- and sometimes to make the counter count in different ways (for example, up or down).

But the basic idea is the same: **the normal operation of a counter is a loop of states**.

We Consider Both Synchronous and Ripple Counters

We focus mainly on

- **synchronous counters**, for which the flip-flops use a common clock signal.
- In other words, they are **clocked synchronous sequential circuits**, and allow us to pretend that time is discrete.

We will also look briefly at

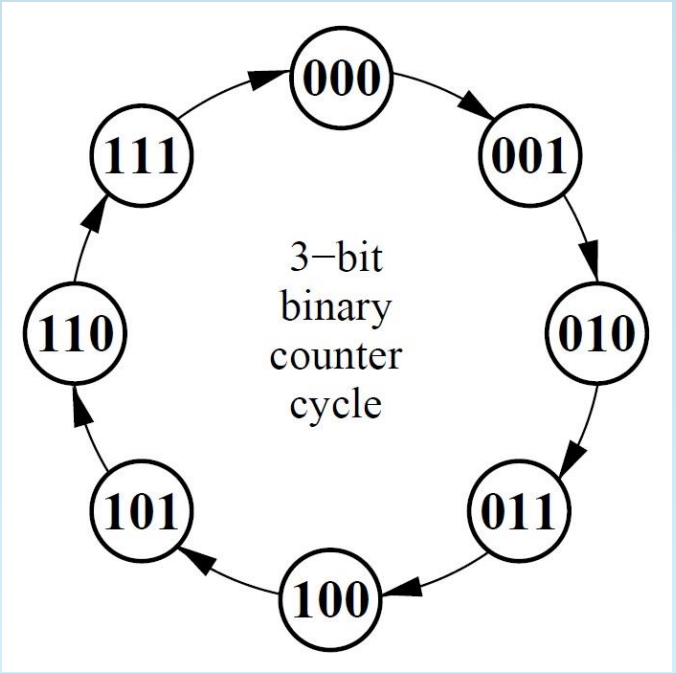
- **ripple counters**, in which flip-flop outputs are used to clock other flip-flops.
- Such designs can save significant power.

Example: 3-Bit Binary Counter

Let's do an example.

The state transition diagram to the right defines a 3-bit binary counter.

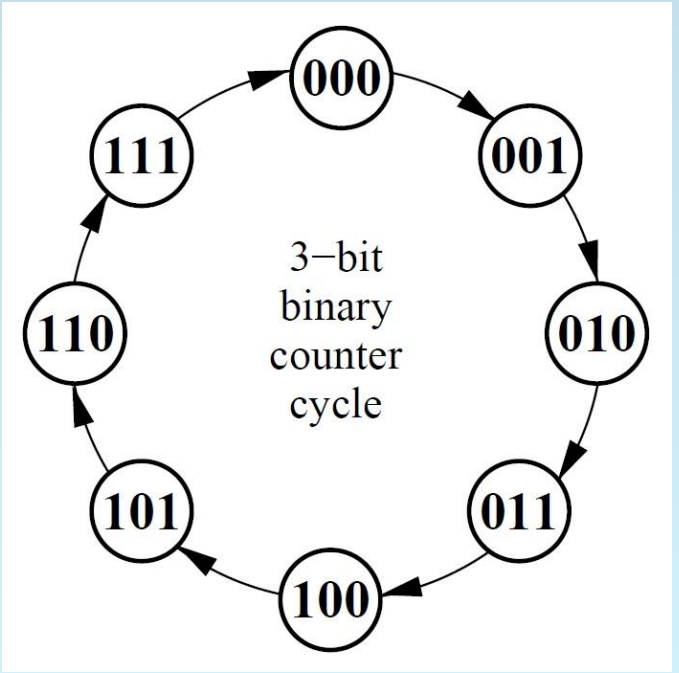
The states correspond to unsigned numbers 0 to 7, after which the counter returns to the 000 state.



Write a Next-State Table

S_2	S_1	S_0	S_2^+	S_1^+	S_0^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Start by writing a next-state table.



Now Use K-Maps to Express the Next-State Values

S_2	S_1	S_0	S_2^+	S_1^+	S_0^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Now copy into K-maps.

$$S_0^+ = S_0' = S_0 \oplus 1$$

S_0^+

S_2 \ S_1S_0	00	01	11	10
0	1	0	0	1
1	1	0	0	1

Now Use K-Maps to Express the Next-State Values

S_2	S_1	S_0	S_2^+	S_1^+	S_0^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Now copy into K-maps.

$$S_1^+ = S_1S_0' + S_1'S_0$$
$$= S_1 \oplus S_0$$

S_1^+

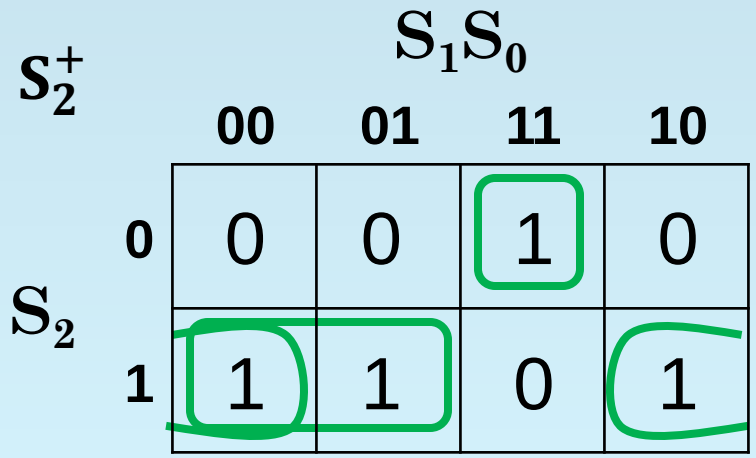
S_2 \ S_1S_0	00	01	11	10
0	0	1	0	1
1	0	1	0	1

Now Use K-Maps to Express the Next-State Values

S_2	S_1	S_0	S_2^+	S_1^+	S_0^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Now copy into K-maps.

$$S_2^+ = S_2'S_1S_0 + S_2S_1' + S_2S_0'$$



When Do Place Values Change in Decimal Counting?

When you count in decimal,
when does a place value change?

For example, when does the
number of thousands change?

0999 → 1000 1999 → 2000 2999 → 3000

What about the number of ten thousands?

09999 → 10000
19999 → 20000
29999 → 30000

Only **when the lower digits are all 9**.

Can We Use Counting to Generalize the Counter Design?

So **what about in binary**?

Only when the lower digits are all 1.

We have …

$S_0^+ = S_0' = S_0 \oplus 1$

$S_1^+ = S_1S_0' + S_1'S_0 = S_1 \oplus S_0$

$S_2^+ = S_2'S_1S_0 + S_2S_1' + S_2S_0'$

Can you simplify the last equation?

How about $S_2^+ = S_2 \oplus (S_1S_0)$?

Use our General Formula to Build Bigger Counters

If you needed a 4-bit binary counter,

- do you need to draw a K-map?
- Or can you write S_3^+ from our generalization?

$$S_3^+ = S_3 \oplus (S_2 S_1 S_0)$$

What about S_4^+?

$$S_4^+ = S_4 \oplus (S_3 S_2 S_1 S_0)$$

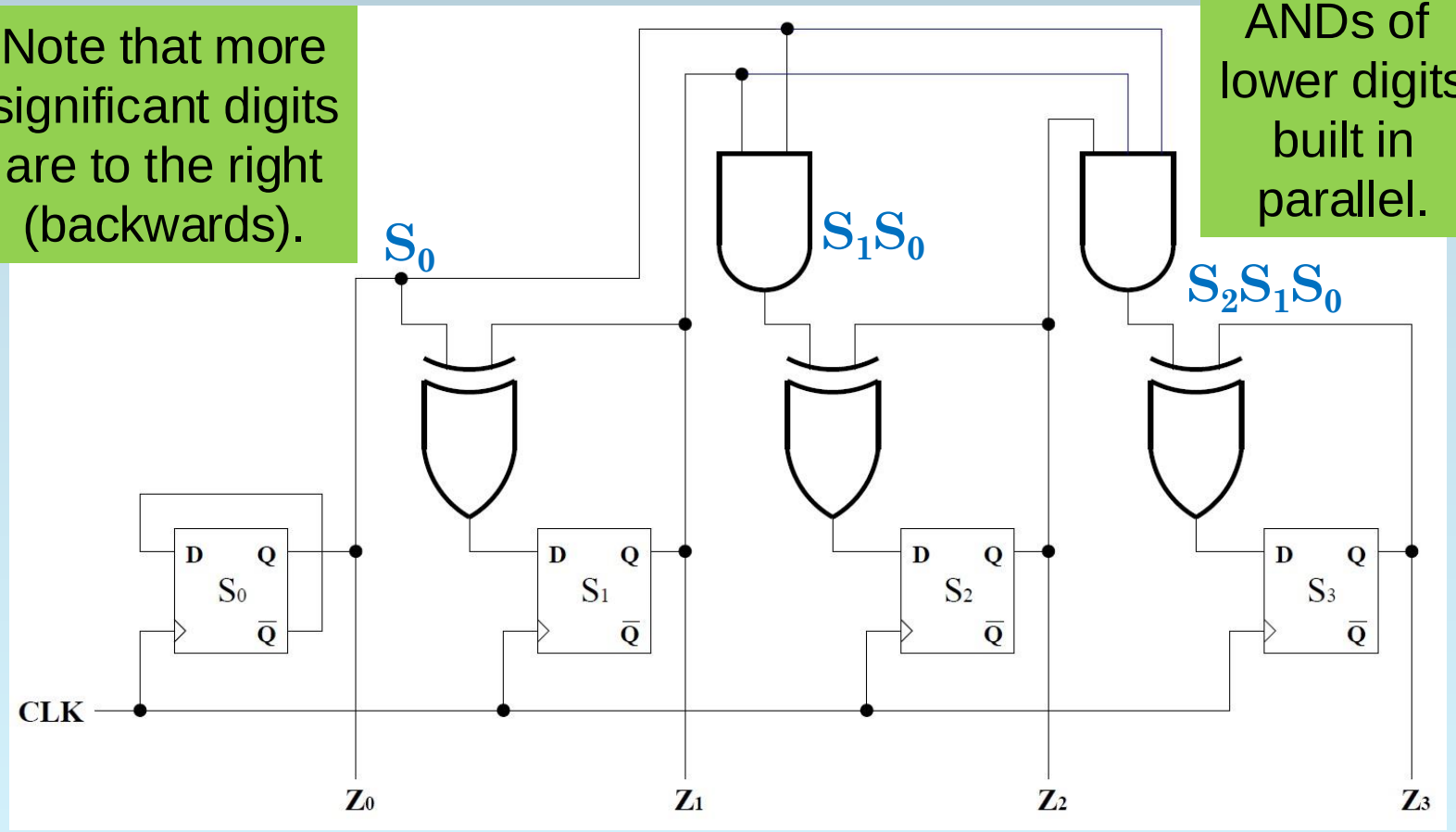
And S_5^+?

$$S_5^+ = S_5 \oplus (S_4 S_3 S_2 S_1 S_0)$$

Binary Counter with Parallel Gating

Note that more significant digits are to the right (backwards).

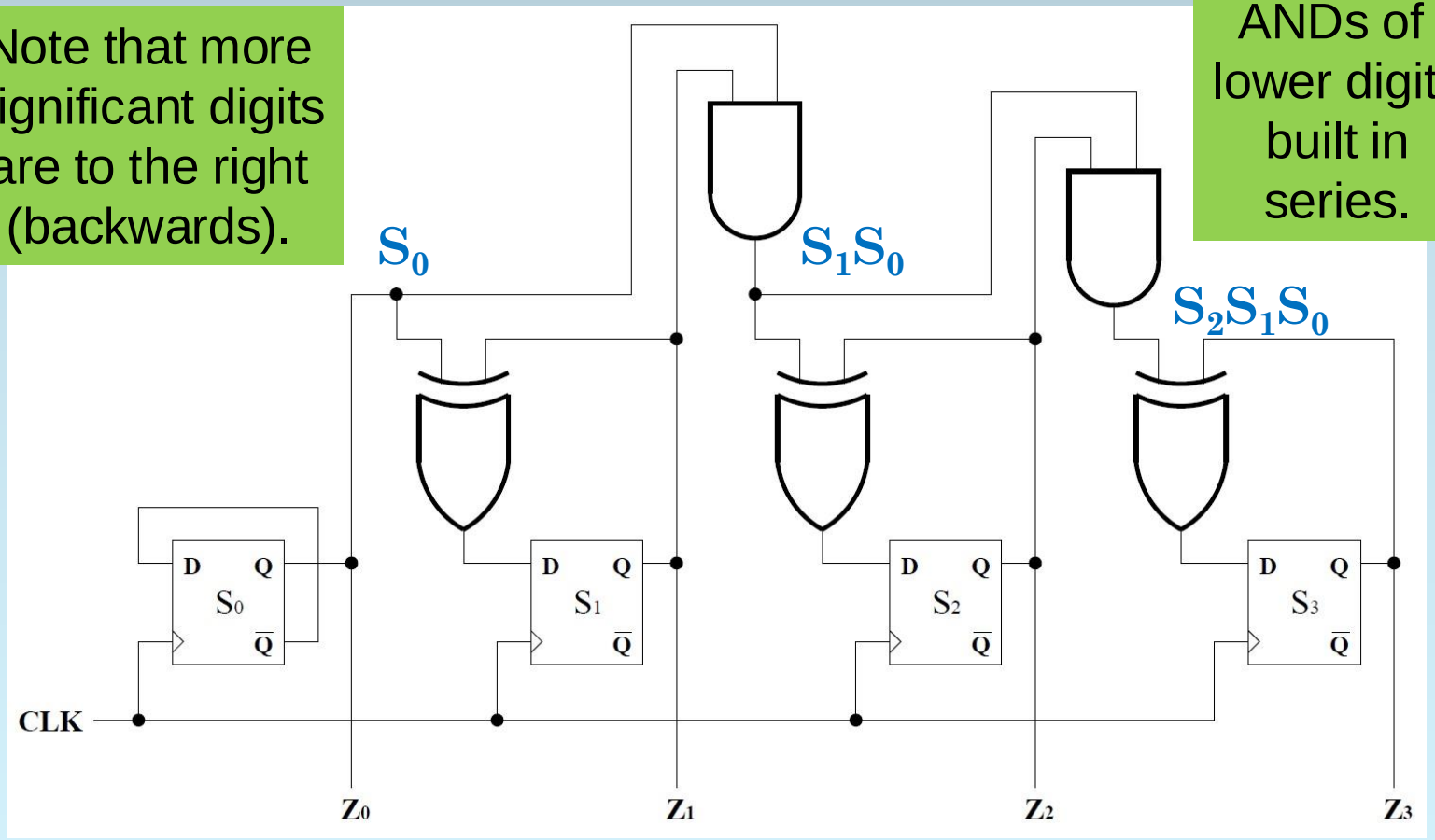
ANDs of lower digits built in parallel.



Binary Counter with Serial Gating

Note that more significant digits are to the right (backwards).

ANDs of lower digits built in series.



Comparing Serial and Parallel Gating

Parallel gating gives
- bigger gates (more area) and
- less delay.

Serial gating gives
- smaller gates (less area) but
- more delay.

In practice,
- gate sizes are limited, so
- counters use a combination of the two approaches.

Flip-Flops in a Ripple Counter Do Not Share a Clock

We just designed a

synchronous binary counter

- synchronous: flip-flops use a common clock
- binary: outputs are binary (unsigned) numbers
- counter: one loop of states

Now, let's take a look at a **binary ripple counter**, in which the clock is not shared.

Ripple Counters Require Less Power

In a ripple counter,

- **outputs from some flip-flops**
- are **used to clock other flip-flops** (used as the clock signal input).

Why?

- Recall that changing gate output values implies electric current, which implies power consumption.
- **Clocking flip-flops more slowly reduces energy consumption.**

Ripple Counters are Slower

What's the tradeoff?

Changes to internal state

- ripple through the counter from bit to bit, so
- they are **slower than synchronous counters**.

What about clock skew?

In general, it may be an issue, but

- we will only **consider one simple design**, and
- more complex ripple counters can usually be designed in isolation from other logic.

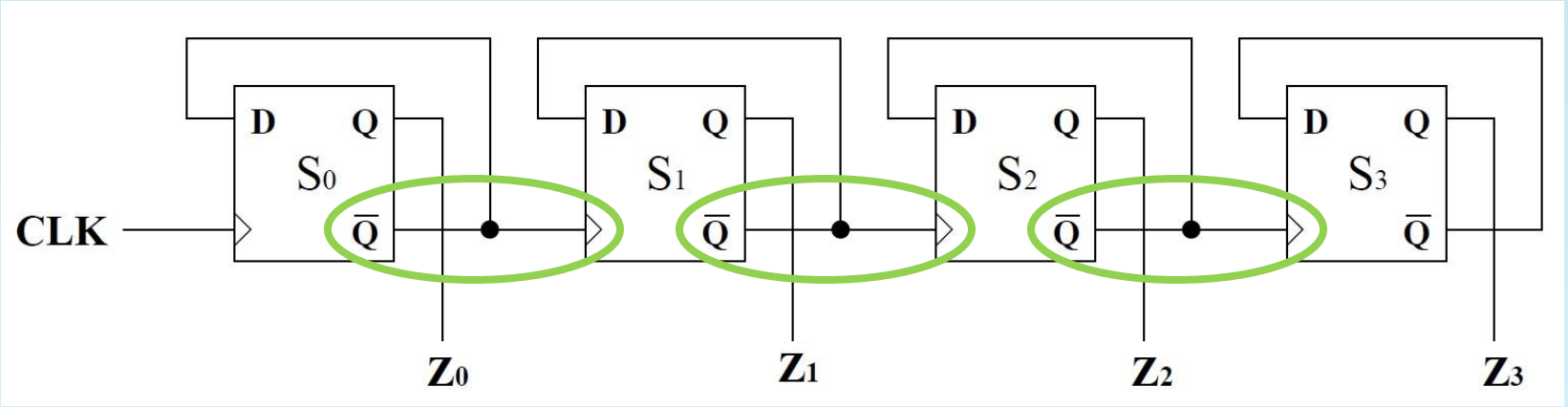
Binary Ripple Counters are Built from Bit Slices

The figure below shows a 4-bit binary ripple counter.

As you can see, the design uses a simple bit slice.

S_i' is the clock input for S_{i+1}.

S_i' is also the D input for S_i.



A Timing Diagram Illustrates Counting