Hammerhead-PC/104-*Plus*

Dual ADSP-21160 32-bit/33 MHz PC/104-*Plus* Board

User's Guide

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Hammerhead-PC/104-Plus Reference Manual

Hardware Revision 0

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Chapter 1
Introduction

The Hammerhead-PC/104-*Plus* is a PC/104-*Plus* format board featuring two ADSP-21160 SHARC® DSPs from Analog Devices, each of which provide 600 MFLOPS peak processing power. Since it is a PC/104-*Plus* format board, it features a 32-bit, 33 MHz PC/104-*Plus* interface instead of the ISA interface that the PC/104 format supports. The Hammerhead-PC/104-*Plus* supports up to 512 MB of SDRAM and 2MB of Flash memory, and the PCI interface features BittWare's Sharc®FIN™ ASIC. The SharcFIN flexibly interfaces the ADSP-21160s to the 32-bit, 33 MHz PCI interface, the SDRAM, the Flash memory, and a general-purpose expansion bus. The Hammerhead-PC/104-*Plus* can function as a standalone processor with the on-board boot Flash, or it can boot from the host computer via the PC/104-*Plus* interface, or over the external link port.

This chapter covers the following topics:

- overviews the architecture of the Hammerhead-PC/104-*Plus* system and its software
- overviews each chapter in this user's guide
- lists documents that provide more information about the Hammerhead-PC/104-*Plus*'s components and software

1.1 Overview of the Hammerhead-PC/104-*Plus* System

This section gives a brief overview of the Hammerhead-PC/104-*Plus* board and describes the software necessary to communicate with the board.

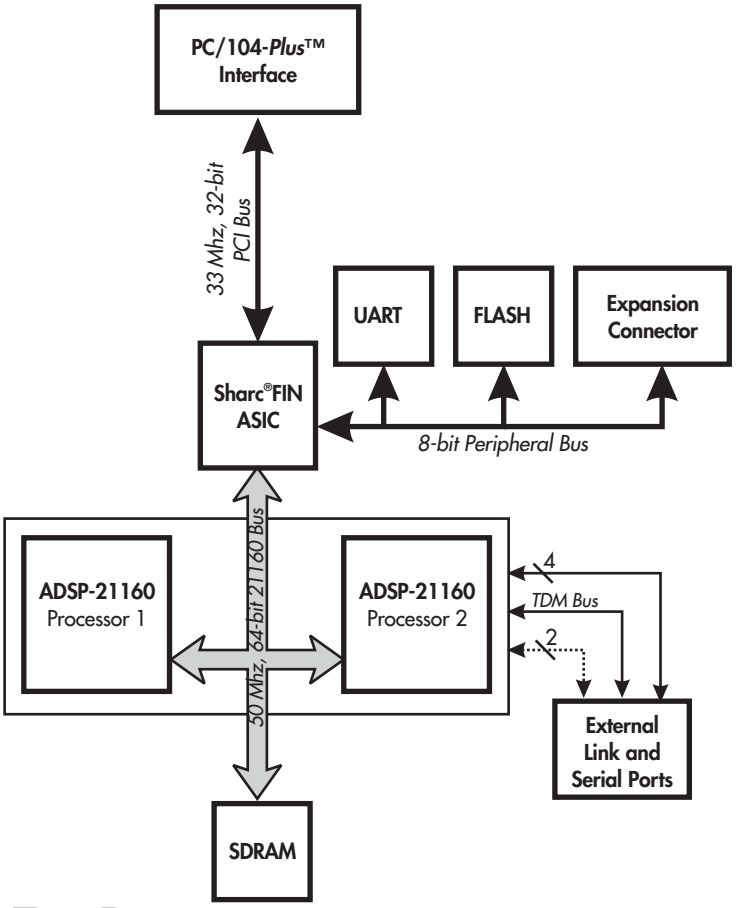
1.1.1 Hammerhead-PC/104-*Plus* Features

- one or two ADSP-21160 SHARC® processors (600 MFLOPS each)
- up to 512 MB SDRAM
- 2 MB of Flash memory with optional boot loading
- four external link ports at 100 MB/s each
- two 50 Mb/s external serial ports
- one 50 Mb/s external serial TDM bus
- BittWare's SharcFIN ASIC
- 8-bit, 25 MHz peripheral bus
- RS-232 UART
- PC/104-*Plus* interface or standalone operation

1.1.2 Hammerhead-PC/104-*Plus* System Architecture

This section gives a basic overview of the Hammerhead-PC/104-*Plus* system, and describes how all of its features work together. Figure 1–1 is a detailed block diagram of the Hammerhead-PC/104-*Plus* board and its features.

Figure 1–1 *Block Diagram of the Hammerhead-PC/104-Plus System*



BittWare's Hammerhead-PC/104-*Plus* board features two Analog Devices ADSP-21160 processors, 64-512 MB of SDRAM, 2 MB of Flash memory, four external link ports, two external serial ports, and a serial TDM bus. The board's SharcFIN ASIC interfaces between the processor bus, the PCI bus and the 8-bit peripheral bus.

ADSP-21160 SHARC DSPs

The Hammerhead-PC/104-*Plus* board is configured with two 100 MHz ADSP-21160 processors. The two ADSP-21160 processors share a common 50 MHz, 64-bit cluster bus, which gives them access to the board's SDRAM, the PCI bus interface, and the other SHARC DSP. For additional I/O, each

processor also has four flags, three interrupts, six link ports, and two serial ports.

Note

Your Hammerhead-PC/104-Plus board may be populated with 80 MHz ADSP-21160 processors because the 100 MHz DSPs may not yet be available. If your board is populated with the 80 MHz chips, the ADSP-21160 cluster bus is 40 MHz, the serial ports are 40 Mbits/s, and the link ports are 80 MBytes/s. For continuity, this user manual will assume the 100 MHz processor option, 50 MHz bus rate, 50 Mbit/s serial ports and 100 MBytes/s link ports.

SharcFIN™ ASIC for SHARC DSPs

The Hammerhead-PC/104-*Plus* incorporates BittWare's SharcFIN ASIC for SHARC DSPs. The SharcFIN flexibly interfaces the ADSP-21160 DSPs to the 32-bit, 33 MHz PCI bus, the SDRAM, the Flash memory, and a peripheral bus. It also provides a feature-rich set of DMA functions and interrupt options to support very high-speed, real-time data flow with minimum processor overhead.

I/O Support

The Hammerhead-PC/104-*Plus* offers a variety of user I/O options in addition to its 32-bit, 33 MHz PC/104-*Plus* interface: external serial port connections, external link port connections, and an RS-232 interface.

One serial port on each SHARC processor is dedicated as an external serial port on the board. The remaining serial port on each SHARC DSP connects to a TDM serial bus.

The Hammerhead-PC/104-*Plus* features four 100 MB/s external link ports. Two link ports on each DSP connect to the external connectors and four links per DSP are dedicated for interprocessor communication.

The board's dual UART allows the ADSP-21160 processors to communicate with external serial devices via an RS-232 port, facilitating remote debugging, command, and control.

1.1.3 Hammerhead-PC/104-*Plus* Software Architecture

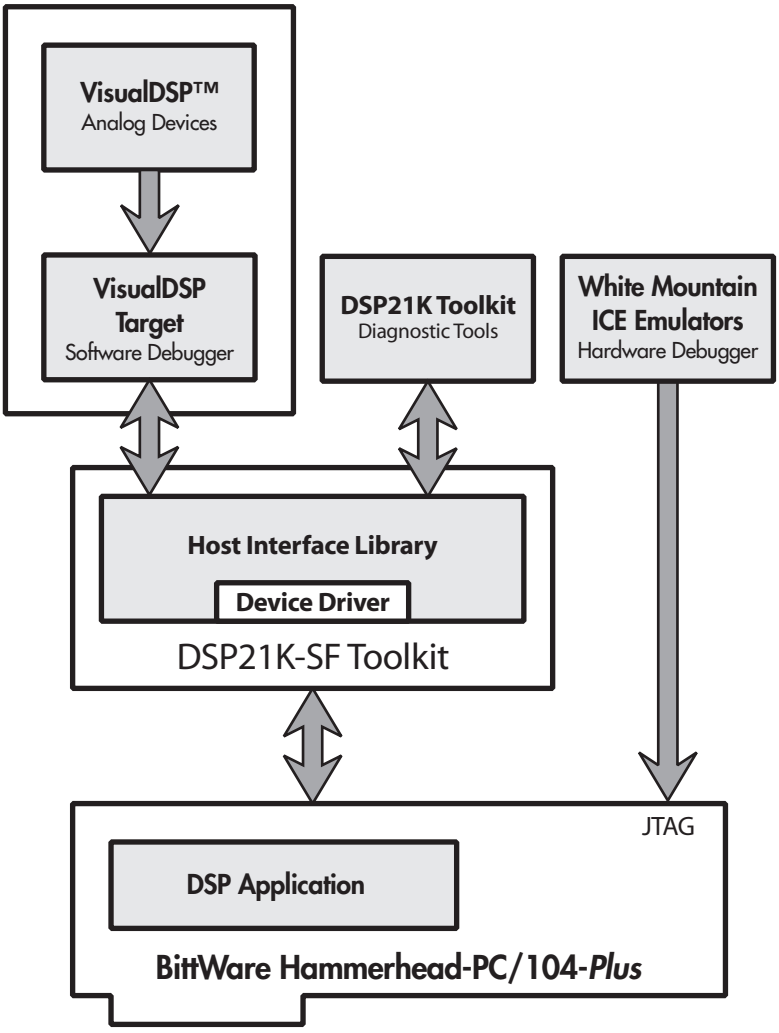
You will need three types of software development tools for the Hammerhead-PC/104-*Plus*: code development tools, debugging tools, and host interface tools. Figure 1–2 is a general block diagram of how the software development tools work together with the Hammerhead-PC/104-*Plus*.

To begin developing code for the Hammerhead-PC/104-*Plus*, use Analog Devices' VisualDSP® Integrated Development Environment (IDE). VisualDSP is an easy-to-use project management environment comprised of an integrated development environment (IDE) and software debugger.

BittWare's DSP21k-SF Toolkit provides your host interface tools. The DSP21k-SF Toolkit allows you to easily develop application code and integrate the Hammerhead-PC/104-*Plus* into your system. The software tools include a comprehensive host interface library (HIL), a standard I/O library, and diagnostic utilities.

Once you have developed your code, you can debug it using BittWare's VisualDSP Target, which is a software plug-in for VisualDSP that allows the VisualDSP debugger to communicate directly with your BittWare board. You can also use a hardware in-circuit emulator, such as the ICE emulators from White Mountain DSP, to debug your code.

Figure 1–2 *Software Model for the Hammerhead-PC/104-Plus*



1.2 About this User's Guide

This section provides an overview of each chapter's content, and it describes certain variations in text and naming conventions we have used throughout the manual.

1.2.1 Purpose of this User's Guide

This user's guide covers hardware revision 0 of the Hammerhead-PC/104-*Plus* board, which supports two ADSP-21160 SHARC processors operating at 100 MHz. The purpose of this document is to provide details about the Hammerhead-PC/104-*Plus*'s major hardware components, to describe how to install and properly operate the Hammerhead-PC/104-*Plus*, and to discuss important issues that relate to programming the board.

We assume that you are already familiar with the ADSP-21160 architecture, operation, and programming as described in the *ADSP-21160 User's Manual* from Analog Devices, Inc.

1.2.2 Conventions Used Throughout this User's Guide

We have used the following conventions throughout this user's guide.

- Since the Hammerhead-PC/104-*Plus* has two processors, we refer to them as 21160-1 and 21160-2.
- All signal names appear in small capitals (RESET).
- Active low signals appear in small capitals with an overline ($\overline{\text{RESET}}$).
- A "0x" prefix designates a number as a hexadecimal number (0x01).
- Commands that the user enters (for programs such as Diag21k or DspBad in the DSP21k-SF Toolkit) appear in the **`Courier bold`** font.
- Filenames and directories appear in the `Courier` font.

1.2.3 Chapter Overviews

Chapter 2: Getting Your Hammerhead-PC/104-Plus Ready for Operation

This chapter describes the tasks that you must perform to prepare your board for installation, install the software for the board, install the board, and test the installation.

Chapter 3: Overview of the Hardware Components

This chapter shows the location of the Hammerhead-PC/104-*Plus*'s major components and connectors and briefly discusses their function.

Chapter 4: Hammerhead-PC/104-Plus Board Architecture

This chapter discusses the board's architecture and its serial ports, link ports, flags and interrupts, and bus interfaces.

Chapter 5: Programming Details for the SharcFIN ASIC

This chapter provides programming details for the SharcFIN ASIC.

Appendix A: Debugging Your DSP Programs

This appendix gives information on debugging DSP programs with a hardware or software emulator.

Appendix B: Setting Up for Standalone Operation

This appendix describes how to set up the board and run it in standalone mode. It explains the steps involved in writing a boot program, loading the boot program into Flash memory, supplying power to the board, and booting it in Flash boot mode.

Appendix C: Troubleshooting Tips

This appendix discusses common operating problems and how to contact technical support at BittWare.

1.3 Other Helpful Documents and Tools

This section describes where to look for more information that applies to the Hammerhead-PC/104-*Plus* or its components. It also lists several third party software development tools that you may find useful.

1.3.1 Documents for Further Reference

ADSP-21160 SHARC Data Sheet – Analog Devices, Inc.

ADSP-21160 SHARC User's Guide – Analog Devices, Inc.

DSP21k-SF Toolkit Installation and Reference Guides – BittWare, Inc.

QL5064 Data Sheet (Chapters 2 and 3) – Quick Logic Corporation

SharcFIN ASIC User's Guide – Bittware, Inc.[1]

1.3.2 Software DevelopmentTools

VisualDSP and BittWare VisualDSP Target

The Hammerhead-PC/104-*Plus* is compatible with the VisualDSP software development tools from Analog Devices. VisualDSP is an easy-to-use project management environment comprised of an integrated development environment (IDE) and software debugger. The IDE provides access to Analog Devices' SHARC C compiler, C runtime library, assembler, linker, loader, simulator, and splitter. The debugger works together with a software target, an emulator, or a simulator and has an easy-to-use interface and many features that reduce debugging time by enabling you to set breakpoints, single step through code, and perform many other debugging operations.

BittWare offers the VisualDSP Target, a plug-in to the VisualDSP IDE that allows the VisualDSP debugger to communicate directly with BittWare's DSP boards. The VisualDSP Target lets you debug your DSP application without a hardware emulator, allowing you to set breakpoints, single-step through your code, view memory, and run code on multiple processors.

1. Available soon.

White Mountain In-Circuit Emulators

White Mountain DSP's ICE in-circuit emulators provide real-time hardware emulation and debugging. With the ICE emulators, you can load programs, start and stop program execution, observe and alter registers and memory, and perform other debugging operations. If you plan to use an ICE emulator with the Hammerhead-PC/104-*Plus*, refer to the documentation that comes with the emulator and to the information in Appendix A of this manual.

BittWare Host Interface Support

BittWare supplies host interface support for the Hammerhead-PC/104-*Plus* with the DSP21k-SF Toolkit. Using the Toolkit's C-callable library of routines for DOS, Windows, and Linux programs, you can download and start programs, read from and write to the Hammerhead-PC/104-*Plus's* memory, and control other board functions. Another library gives your DSP programs standard I/O routines such as screen display, keyboard input, and disk file access. The *DSP21k-SF Toolkit User's Guide* from BittWare, Inc. contains complete information about the DSP21k-SF Toolkit.

SpeedDSP Optimized Libraries for SHARC DSPs

SpeedDSP is a collection of highly optimized routines for the ADSP-21xxx family of SHARC DSP chips that includes SIMD operations for the ADSP-2116x family of DSPs. The functions are written in ADSP-21xxx assembly language and are callable from high-level languages such as C. SpeedDSP includes functions for manipulating large arrays of floating-point numbers and for performing Fast Fourier Transforms (FFTs), windowing, statistics, sorting, histogramming, trigonometry, and timing. Since the functions in the library are coded in ADSP-21xxx assembly language and take full advantage of the ADSP-21xxx architecture, they are much faster than high-level language implementations, delivering optimum speed and performance. SpeedDSP integrates easily with the Analog Devices C compiler and is completely compatible with the program/data memory specifiers and the complex data type.

BittWare's SharcLAB MATLAB Interface

SharcLAB, developed exclusively for BittWare by SDL, works with The Mathworks MATLAB, Simulink, Stateflow, and Real-Time Workshop to allow you to prototype and test DSP applications on your BittWare SHARC DSP boards. SharcLAB integrates seamlessly with the standard MATLAB environment, allowing a nearly automatic transition from MATLAB-based algorithm development to executable DSP code.

You can develop your applications in the Simulink graphical flow-chart-based simulation environment and use SharcLAB to automatically compile, download, and run the algorithms on your BittWare SHARC DSP hardware in real-time. SharcLAB allows you to change application parameters interactively and view data streams in real time in the native Simulink environment for debugging and verification without interrupting the DSP application.

Chapter 2
Getting Your Hammerhead-PC/104-*Plus* Ready for Operation

This chapter describes how to prepare your board for installation, install the software for the board, install the board, and run diagnostic tests on the board to make sure it is working properly. This chapter does not provide comprehensive instructions for all of the tasks; instead, it provides a sequence of steps for you to follow. In addition to the information in this chapter, you will also need to refer to the documentation for Analog Devices' VisualDSP, the BittWare DSP21k-SF Toolkit, and the host PC.

To prepare your Hammerhead-PC/104-Plus board for operation,

1. Unpack the Hammerhead-PC/104-*Plus* (section 2.1).
2. Set the board's configuration jumpers (section 2.2.1).
3. Configure the external serial ports (section 2.2.2).
4. Configure the board according to its location in the PC/104 stack (section 2.2.3).
5. Connect any desired external cables to the board (section 2.3).
6. Install the Analog Devices software tools (section 2.4.1).
7. Install BittWare's DSP21k-SF Toolkit (section 2.4.2).
8. Mount the board on a PC/104-*Plus* stack (section 2.4.3).
9. Run diagnostic tests on the board to ensure it is operating properly (section 2.5.1).
10. Run the example software included with the Hammerhead-PC/104-*Plus* (section 2.5.2).

2.1 Unpacking the Hammerhead-PC/104-*Plus*

Warning!

The Hammerhead-PC/104-Plus contains electro-static discharge (ESD) sensitive devices. Be sure to follow the standard handling procedures for ESD sensitive devices, taking proper precautions to ground yourself and the work area before removing the board from its anti-static bag. If you fail to follow proper handling procedures, you could damage the board.

To unpack the Hammerhead-PC/104-Plus board,

1. Carefully remove the board from the shipping box. (Save the box and packing materials in case you need to reship the board.)
2. Remove the module from the plastic bag, observing all precautions described in the warning above to prevent damage from electro-static discharge (ESD).
3. Carefully examine the board, checking for damage. If the board is damaged, ***do not*** install it. Call BittWare technical support.

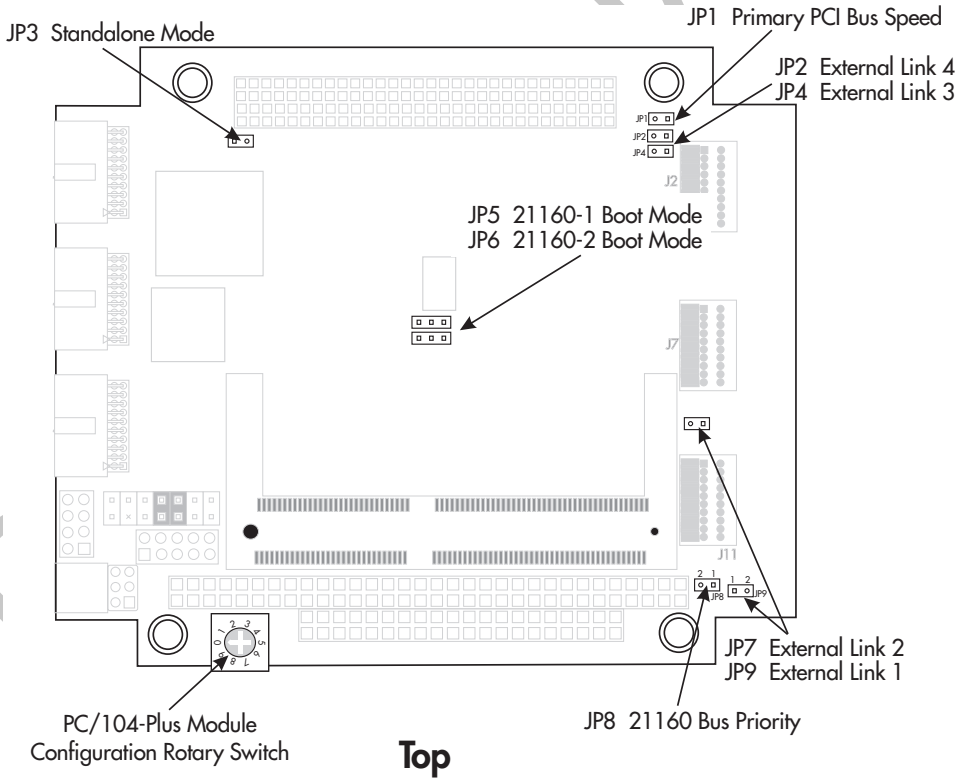
2.2 Configuring the Hammerhead-PC/104-*Plus*

This section explains how to set up the physical features of the board to get it ready for installation. It includes instructions for setting configuration jumpers, configuring the board's serial ports, and configuring the board according to its location in the PC/104-*Plus* stack.

2.2.1 Setting the Hammerhead-PC/104-*Plus* Configuration Jumpers

The Hammerhead-PC/104-*Plus* has nine configuration jumpers that allow you to control and enable several of the board's features. Before mounting the board on a PC/104-*Plus* stack, make sure you have properly set all of the configuration jumpers. Figure 2–1 below shows where each of the jumpers is located.

Figure 2–1 *Layout of the Hammerhead-PC/104-Plus Configuration Jumpers (Top)*



Ensuring Proper Speed for the PCI Bus

A jumper placed on JP1 sets the PCI bus speed to 33 MHz, which is the default setting. If this jumper is removed, the Hammerhead-PC/104-*Plus* board will not communicate properly with the host.

Configuring the Board for Standalone Mode

Jumper JP3 configures the Hammerhead-PC/104-*Plus* for standalone mode. The jumper must be on for the board to operate properly in standalone mode.

Gating Power to the External Link Port Connectors

Jumpers placed on JP2, JP4, JP7 and JP9 gate power to the external link connectors on the Hammerhead-PC/104-*Plus*.

Selecting the Boot Mode

Use jumpers JP5 and JP6 to select the boot mode for the Hammerhead-PC/104-*Plus*'s ADSP-21160 processors. The processors can boot from the host PC via the 32-bit, 33 MHz PCI interface or the link ports, or they can operate in standalone mode by booting from the Flash memory. Table 2–1 shows the settings for the boot mode selection jumpers.

Note

If you have chosen the single-processor configuration of the Hammerhead-PC/104-Plus, jumper JP6 is not used.

Table 2–1 *Settings for the Boot Mode Selection Jumpers*

Jumper	Jumper Position	Setting	Default
JP5	Pins 1–2	21160-1 will boot from on-board Flash	
	Pins 2–3	21160-1 will boot via link booting (J11, External Link 4)	
	No Jumper	21160-1 will boot from the host computer	✔
JP6	Pins 1–2	21160-2 will boot from the on-board Flash	
	Pins 2–3	21160-2 will boot via link booting (via 21160-1)	
	No Jumper	21160-2 will boot from the host computer	✔

Setting the ADSP-21160 Bus Arbitration

JP8 configures the rotating priority bus arbitration (RPBA) mode for the 64-bit ADSP-21160 cluster bus. The ADSP-21160 bus has two RPBA modes: fixed priority scheme and rotating priority scheme. The *ADSP-21160 User's Guide* (Analog Devices) explains the RPBA modes in more detail.

The fixed priority scheme for bus arbitration gives priority to the ADSP-21160 processor with the lowest multiprocessor ID. With the fixed priority scheme, 21160-1 would always have priority.

The rotating priority scheme for bus arbitration gives priority to the ADSP-21160 processors on a rotating schedule. For example, 21160-1 would have priority, then 21160-2 would have priority, and so on.

Table 2–2 *Selecting the Rotating Priority Bus Mode for the ADSP-21160 (JP8)*

Jumper Position	Setting	Default
IN	Fixed priority scheme	
OUT	Rotating priority scheme	✔

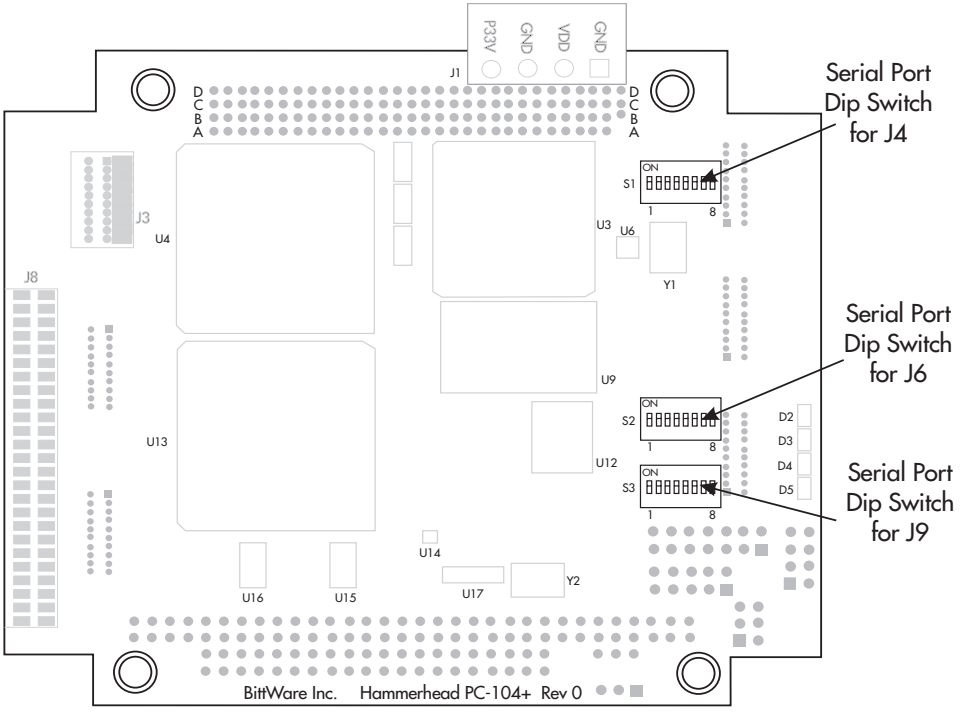
2.2.2 Configuring the External Serial Ports

The Hammerhead-PC/104-*Plus* has three 20-pin right-angle IDC external serial port connectors to provide a communication route between the ADSP-21160s and synchronous serial devices. Each connector has a corresponding dip switch that you can use to configure the connector. Table 2–3 lists the board's serial port switches and Figure 2–2 shows where the dip switches are located on the Hammerhead-PC/104-*Plus* board.

Table 2–3 *Serial Port Dip Switch Connections*

Dip Switch	Serial Port	Description
S1	J4	Connected to both ADSP-21160 processors as a TDM serial port
S2	J6	Connected to 21160-2 as a standard serial port
S3	J9	Connected to 21160-1 as a standard serial port

Figure 2–2 *Layout of the Serial Port Dip Switches (Bottom)*



Bottom

Figure 2–3 gives the standard serial port pinout, and Figure 2–4 gives the TDM serial port pinout. Table 2–4 gives the settings for the standard serial port dip switches (S2 and S3).

Figure 2–3 *Standard Serial Port Dip Switch Positions (S2 and S3)*

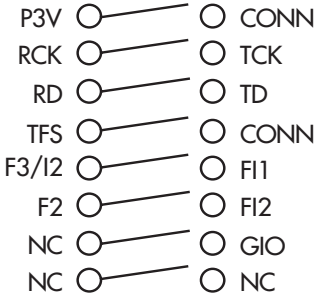


Figure 2–4 *TDM Serial Port Dip Switch Positions (S1)*

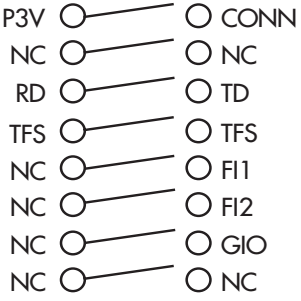


Table 2–4 *Standard Dip Switch Settings*

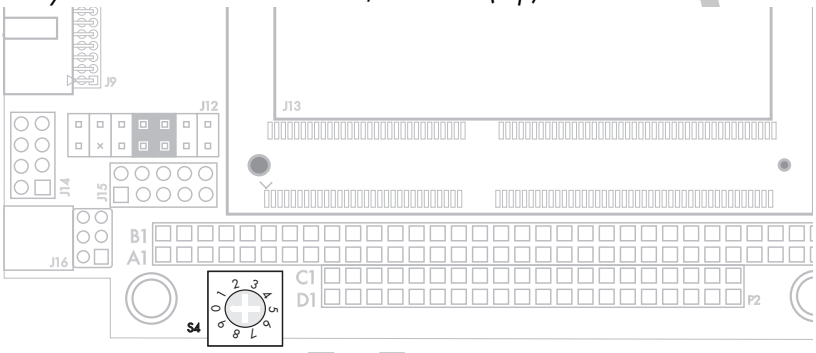
Switch	Settings
P3V	ON: If using active external adapter that needs power OFF: Otherwise
TCK/RCK	ON: TDM mode OFF: Standard mode
TD/RD	ON: TDM 1-wire OFF: TDM 2-wire, standard mode
TFS	ON: Standard with null-modem cable OFF: Otherwise
I2/FI1	ON: If SharcFIN is not driving IRQ2, FLAG3 will drive IRQ2 OFF: Otherwise
F2/FI2	ON: S2 connects ADSP-21160-2 FLAG2 to XHA2_SP1F12, S3 connects ADSP-21160-1 FLAG2 to XHA1_SP1F12 OFF: No connect
GI0	Depends on implementation

2.2.3 Configuring the Board According to Position in the PC/104-*Plus* Stack

In addition to the host CPU (carrier board), a PC/104-*Plus* stack can contain up to four PC/104-*Plus* modules. With each module added to the stack, the distance between the host CPU and the DSPs on the top module becomes greater, and clock signals can be delayed. To correct the delay in clock signals between the host CPU and the top PC/104-*Plus* modules, the Hammerhead-PC/104-*Plus* has a rotary switch that configures the board according to its position in the stack.

The rotary switch has four settings, one for each potential position in the PC/104-*Plus* stack. For example, if the board was first in the stack, you would set the rotary switch to position 0; if the board was second in the stack, you would set the switch to position 1, and so on. Table 2–6 shows the rotary switch and its settings, and Figure 2–8 shows where the switch is located on the board.

Figure 2–5 *Rotary Switch to Select Position in PC/104 Stack (Top)*



The clocks are tuned on the host CPU so that the length of CLK3 trace is 0.662" less than CLK2, CLK2 trace is 0.662" less than CLK1, and CLK1 trace is 0.662" less than CLK0. Therefore, the first module in the stack must select CLK0 (the longest trace), the second must select CLK1, and so on. These settings provide basically no clock skew between modules. Table 2–5 gives the switch settings and signals used for each module in the stack.

Table 2–5 *Rotary Switch Settings*

Switch Position	Module Slot	$\overline{\text{REQ}}$	$\overline{\text{GNT}}$	CLK	ID Address	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	$\overline{\text{INT3}}$
0 or 4	1	$\overline{\text{REQ0}}$	$\overline{\text{GNT0}}$	CLK0	AD20	$\overline{\text{INTA}}$	$\overline{\text{INTB}}$	$\overline{\text{INTC}}$	$\overline{\text{INTD}}$
1 or 5	2	$\overline{\text{REQ1}}$	$\overline{\text{GNT1}}$	CLK1	AD21	$\overline{\text{INTB}}$	$\overline{\text{INTC}}$	$\overline{\text{INTD}}$	$\overline{\text{INTA}}$
2 or 6	3	$\overline{\text{REQ2}}^*$	$\overline{\text{GNT2}}^*$	CLK2	AD22	$\overline{\text{INTC}}$	$\overline{\text{INTD}}$	$\overline{\text{INTA}}$	$\overline{\text{INTB}}$
3 or 7	4	$\overline{\text{REQ2}}^*$	$\overline{\text{GNT2}}^*$	CLK3	AD23	$\overline{\text{INTD}}$	$\overline{\text{INTA}}$	$\overline{\text{INTB}}$	$\overline{\text{INTC}}$

* Because module slots 3 and 4 share $\overline{\text{REQ2}}$ and $\overline{\text{GNT2}}$, they cannot both be bus master devices.

2.3 Connecting External Signals to the Board

This section describes how to connect external signals to the board to connect it to external devices.

2.3.1 Connecting Serial Port Cables

The Hammerhead-PC/104-*Plus* has three external serial port connectors (J4, J6, J9), which provide a communication route between the ADSP-21160 processors and other synchronous serial devices. Section 3.2.4 shows the location and pinout of the connectors. If you choose to connect the Hammerhead-PC/104-*Plus* to another serial device, the cables in Table 2–6 are available from BittWare.

Table 2–6 *Serial Port Cables Available from BittWare*

Description	BittWare Part Number
Ribbon cable for standard serial port on rear panel	CARH-N20-xx*
Ribbon cable for TDM serial port on rear panel	CARH-S20-xx

* "xx" denotes the length of the cable in inches.

2.3.2 Connecting RS-232 Cables

To connect the Hammerhead-PC/104-*Plus* to your PC via the RS-232 interface, attach a 10-pin DB9-to-AMP cable to the Hammerhead-PC/104-*Plus*'s RS-232 port (J15). The cable provides a straight-through connection from the Hammerhead-PC/104-*Plus*'s UART to the PC. Since the connector's pinout (see Table 3–12) is data communication equipment (DCE), you can connect it directly to equipment configured as data terminal equipment (DTE), such as a PC, without a null-modem cable.

BittWare offers a host serial interface cable that connects the RS-232 connectors directly to a standard PC's DB9 RS-232 Com port. To connect the Hammerhead-PC/104-*Plus* to a PC with a host serial interface cable, follow the steps below.

1. If your PC's RS-232 port is DB25, you'll need to attach a DB25-to-DB9 adapter onto the DB9 end of a DB9-to-AMP 10-pin cable (available from

BittWare, part number CARL-U10-06, or you can create one of your own).

2. Connect the end of the cable with the AMP 10-pin connector to J15 on the Hammerhead-PC/104-*Plus*. Be sure to line up the marked side with pin 1 on J15. Figure 3–14 shows where pin 1 is located.
3. Making sure that the PC's power is off, connect the serial interface cable to the PC.

2.3.3 Connecting an External Power Supply

When operating in standalone mode, the Hammerhead-PC/104-*Plus* requires a +3.3V and +5V power source. The external power connector (J1) supplies +3.3V, +5V and GND to the Hammerhead-PC/104-*Plus*. Section 3.2.2 gives the pinout of the connector and shows where it is located.

To connect an external power source to the Hammerhead-PC/104-Plus,

1. Plug a power adapter cable into the Hammerhead-PC/104-*Plus*'s external power connector (J1). Be sure to align pin 1 (GND) on the cable with the GND pin on J1.
2. Connect the remaining end of the cable to an external power source, such as a switching standalone power supply or the PC's power supply.
3. Apply power to the system.
4. Reset the Hammerhead-PC/104-*Plus* (see section 2.6).

2.3.4 Connecting an External Reset Signal to the Reset Connector

The external reset connector (J16) allows the Hammerhead-PC/104-*Plus* board to reset or be reset by other system boards. The connectors support an input reset line to allow the Hammerhead-PC/104-*Plus* to receive reset signals from other boards; it also supports an output reset line to allow the Hammerhead-PC/104-*Plus* to reset other boards. Fig is a block diagram of the external reset circuit.

To reset the Hammerhead-PC/104-Plus with the external reset connector,

1. Connect a cable (see Figure 2–6) from the external reset connector (J16) on the Hammerhead-PC/104-*Plus* board to another system board.
2. Any reset that occurs on the Hammerhead-PC/104-*Plus* reset source causes a reset on all Hammerhead-PC/104-*Plus* reset targets.

Figure 2–6 *Cable Details for the Hammerhead-PC/104-Plus' External Reset Connector (Top)*

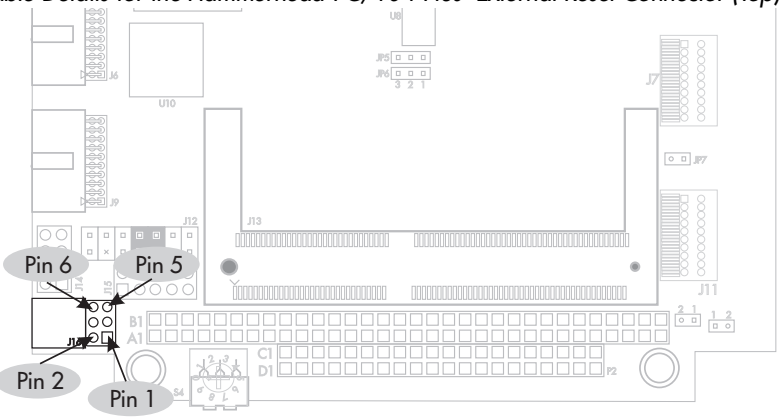
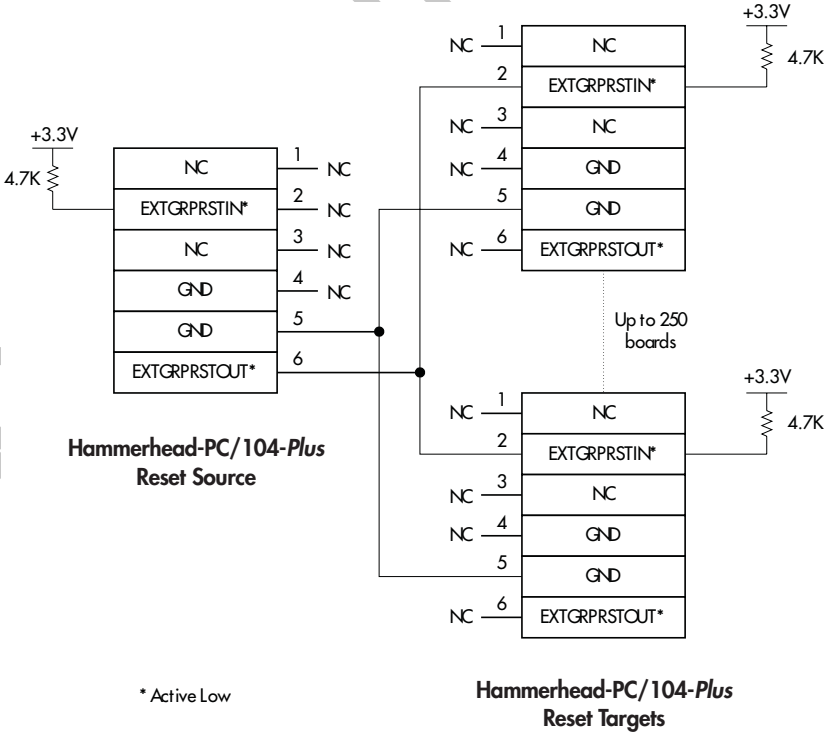


Figure 2–7 *Block Diagram of the Hammerhead-PC/104-Plus Reset Circuit*



2.4 Installing the Board and its Software

This section describes the steps necessary to install the software development tools and install the board in the PC/104-*Plus* stack.

2.4.1 Installing the Analog Devices Software Tools

The Hammerhead-PC/104-*Plus* is compatible with the VisualDSP® software development toolset from Analog Devices. VisualDSP is an easy-to-use project management environment comprised of an integrated development environment (IDE) and debugger. The VisualDSP IDE includes access to Analog Devices' 4.0 SHARC C compiler, C runtime library, assembler, linker, loader, simulator, and splitter.

BittWare's VisualDSP Target allows you to use the VisualDSP debugger with your BittWare board. It works with the VisualDSP debugger to allow direct communication with the DSPs on the Hammerhead-PC/104-*Plus*. This section describes where to find installation instructions for the VisualDSP IDE and the BittWare VisualDSP Target.

Installing the VisualDSP® IDE and Debugger

To install VisualDSP, refer to the VisualDSP user documentation.

Installing the BittWare VisualDSP Target

If you will be using the VisualDSP debugger with the Hammerhead-PC/104-*Plus*, you will need to install BittWare's VisualDSP Target after installing the VisualDSP IDE. The VisualDSP Target allows the VisualDSP debugger to communicate directly with the ADSP-21160 processors on the Hammerhead-PC/104-*Plus*. The *VisualDSP Target User's Guide* gives detailed installation instructions. You may also use the White Mountain DSP emulator in place of VisualDSP Target. Refer to Appendix A for installation instructions for the emulator.

2.4.2 Installing the BittWare DSP21k-SF Toolkit

This section gives a basic overview of installing the BittWare DSP21k-SF Toolkit; it does not give detailed instructions. For detailed installation instructions, refer to the *DSP21k-SF Toolkit Installation Guide*.

Overview of the DSP21k-SF Toolkit

BittWare's DSP21k-SF Toolkit is a set of libraries and utilities that enable you to develop DSP applications for the Hammerhead-PC/104-*Plus* more quickly and easily. It contains a host interface library of C-callable functions for PC-based programs, diagnostic utilities, demo programs, and a DSP library that provides standard I/O extensions to DSP programs.

Libraries. The primary component of the DSP21k-SF Toolkit is the ***Host Interface Library*** (HIL). The HIL is a library of C-callable functions for programs that allow you to download and start programs on the DSP, read from and write to the DSP's memory, and control other board functions.

The DSP21k-SF Toolkit also contains the ***DspHost Library,*** which gives your DSP programs standard I/O routines such as screen display, keyboard input, and disk file access. It consists of a library of standard I/O routines that you link into your DSP program and a program that runs on the PC to act as an I/O server. DspHost is an excellent tool for porting existing C applications to the DSP.

Utilities. ***Diag21k*** is a character-based diagnostic utility that lets you interactively download DSP programs, start and stop their operation, and access DSP memory.

The ***DSP Board Automated Diagnostic*** (DspBad) is a command-line operated utility that verifies the ability to communicate with the DSP from the host, tests the memory of the board, and confirms the DSP's ability to load and run a program.

Installing the DSP21k-SF Toolkit Libraries and Utilities

To install the DSP21k-SF libraries and utilities, run the DSP21k-SF Toolkit install program. The *DSP21k-SF Toolkit User's Guide* explains the procedure in more detail.

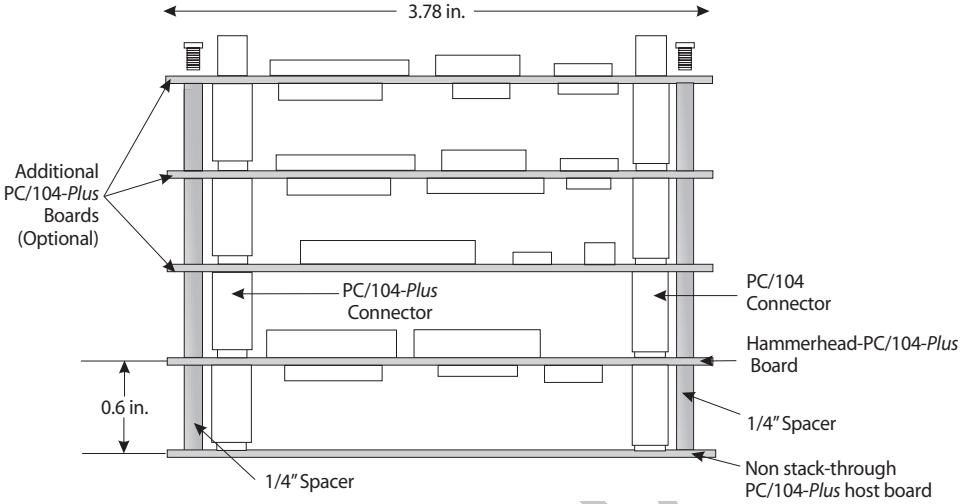
2.4.3 Mounting the Board on a PC/104-*Plus* Stack

The Hammerhead-PC/104-*Plus* plugs onto a PC/104-*Plus* stack with the ADSP-21160 processors facing the bottom of the stack.

Note

PC/104-Plus is the PCI bus, PC/104 is the ISA bus. The Hammerhead-PC/104-Plus uses the PC/104-Plus bus and passes through the PC/104 bus.

Figure 2–8 *PC/104-Plus Stack with Hammerhead-PC/104-Plus*



2.5 Testing the Board to Make Sure it is Operating Properly

This section discusses running diagnostic tests on the board after you install it to make sure it is operating properly. It runs through examples of two DSP21k-SF Toolkit diagnostic utilities and discusses the contents of the example files included with the Hammerhead-PC/104-*Plus*.

2.5.1 Testing the Board with the DSP21k-SF Toolkit Diagnostic Utilities

The DSP21k-SF Toolkit contains two diagnostic utilities for testing a DSP board to make sure it is operating properly: the DSP Board Automated Diagnostic (DspBad) and Diag21k.

- ***DspBad*** is a command-line operated utility that verifies the ability to communicate with the DSP board from the PC, tests the memory of the board, and confirms the DSP's ability to load and run a program.
- ***Diag21k*** is a character-based diagnostic utility that you start from the MS-DOS command prompt. It lets you interactively download DSP programs, start and stop their operation, and access DSP memory.

Testing the Board with DspBad

To test a processor with DspBad, enter the following command at a command prompt:

```
C:>dspbad -b<N> <enter>

or

C:>dspbad -d<N> -i<N> <enter>
```

The **<N>** in **-b<N>** represents the processor number[1]. The **<N>** in **-d<N>** represents the device number. The **<N>** in **-i<N>** represents the processor ID number of the processor you want to open on the specified device. The *DSP21k-SF Toolkit Installation Guide* explains DspBad commands in more detail.

1. The processor number is the *device number * 10 + id number*. See the *DSP21k-SF User's Manual* for further explanation.

Testing the Board with Diag21k

The example below shows you basic Diag21k commands to test the Hammerhead-PC/104-*Plus*'s memory and load and run a DSP program. Be sure to follow the example steps below in the order in which they appear. The *DSP21k-SF Toolkit User's Manual* describes the Diag21k commands in more detail.

Step 1: Start Diag21k

1. The Diag21k program is located in the `dsp21ksf\bin` directory. Start the program from the DOS prompt. The **`-b`** switch tells Diag21k which processor you will access. If you do not specify a processor number with **`-b`** (or both **`-d`** and **`-i`**), Diag21k will use all processors that are installed in your PC.

   ```
   C:\DSP21KSF\BIN>diag21k -b1

   C:\DSP21KSF\BIN>diag21k -d0 -i1
   ```

   Both of the command line options above tell Diag21k to open the first processor on device 0.

2. Diag21k will start and display a copyright banner. The command prompt shows the active board number in square brackets.

   ```
   DSP21K Interactive Diagnostic Utility
   32-bit version for SharcFIN boards under Windows 95/98 and
   Windows NT/2000. Release 6.12 [ DSP21K-SF, Dec 21 2000
   15:54:36 ], Version 3.93 Copyright (c) 1992-2000 BittWare,
   Inc. All rights reserved.

   Type "?" for a list of commands.

            Available DSP numbers: 1 2

   Opened 2 DSPs.

   Current DSP:         #1, processor 1 on Hammerhead (device 0)
   ```

Step 2: Display Board Information

3. Use the board information command to display information about the Hammerhead-PC/104-*Plus*'s processors.

   ```
   diag21k[1]>bi
   ```

```
Board/Processor Information for DSP #1  (Not Started)
Board Type: (38) Hammerhead                          DSP Type: (7) ADSP-21160
Multi-proc ID: 1                                  Interrupt Number: 11
BAR0:  0x0c800000    Size:  0x00000200      BAR3:  0x0c800200   Size:  0x00000100
BAR1:  0x0c400000    Size:  0x00400000      BAR4:  0x0a000000   Size:  0x01000000
BAR2:  0x08000000   Size:  0x02000000     BAR5:               Size:  0x0
Int. Mem: 4 Mbit           IMDW0: 32-bit data                IMDW1:  32-bit data
  MMS WS: 0       Ext Bank Size:  32768 KW  (MSIZE = 12)  DRAM PgSz:   256 W
Bank 0:  Start = 0x00800000  Width = 32 bits   Depth = 32768 KW  WS/WM = 1/2
Bank 1:  Start = 0x02800000  Width =  8 bits   Depth =  2048 KW  WS/WM = 7/0
Bank 2:  Start = 0x04800000  WS/WM = 1 / 2
Bank 3:  Start = 0x06800000  WS/WM = 7 / 0
Unbnkd:  Start = 0x08800000  WS/WM = 7 / 0
  Program loaded:  (none)
  Labels:  *not defined*
```

Step 3: Test the Hammerhead-PC/104-Plus's Memory

Notice the memory size information for the external memory banks 0 and 1. The memory test command (**mt**) uses these values when it performs various tests on different regions of the ADSP-21160's memory.

Now that you have found the memory bank settings, you can test all of the Hammerhead-PC/104-*Plus*'s memory with the following commands.

4. To ensure that neither of the processors is executing programs that might change memory while you are testing it, reset the board.

```
diag21k[1]>br
        Board reset
```

5. Next, configure the processor you selected to access external memory (MSIZE and WAIT settings):

```
diag21k[1]>pc
        processor configured
```

6. Now use the following command to test all memory banks:

```
diag21k[1]>mt aa

Program Memory Test at 0x040000, Size: 0xa000 48-bit Words
        Self-Address.............. ok
        Self-Address Complement... ok
        Checkerboard A............ ok
        Checkerboard 5............ ok
        All Bits Clear............ ok
        All Bits Set.............. ok
        Random Numbers............ ok
Data Memory Test at 0x050000, Size: 0x10000 32-bit Words
        Self-Address.............. ok
        Self-Address Complement... ok
        Checkerboard A............ ok
        Checkerboard 5............ ok
        All Bits Clear............ ok
        All Bits Set.............. ok
        Random Numbers............ ok
External Bank 0 Test at 0x800000, Size: 0x2000000 32-bit
Words
        Self-Address.............. ok
        Self-Address Complement... ok
        Checkerboard A............ ok
        Checkerboard 5............ ok
        All Bits Clear............ ok
        All Bits Set.............. ok
        Random Numbers............ ok
```

Step 4: Load and Execute a Program

Now that you have tested the memory, you know that Diag21k can successfully communicate with the Hammerhead-PC/104-*Plus* board, and you are ready to load a program and execute it.

7. The `dsp21ksf\etc` directory contains an example program that calculates the first twenty prime numbers. The source code is in the `examples\21160\prime160` directory. Load the pre-compiled executable file with the file load (**`fl`**) command.

```
diag21k[1]>fl\dsp21ksf\etc\prm21160

        "\dsp21ksf\etc\prm21160.dxe" loaded
```

8. Now that Diag21k has downloaded the executable file into the ADSP-21160's memory and holds the processor in reset, start the processor with the processor start command:

```
diag21k[1]>ps

        processor running
```

9. To see the results of the primes program, examine the variable that contains the calculated prime numbers. The C program `primes.c` defines a global array called primes, which is stored in data memory. The memory read command can use global labels to locate variables and functions. Notice that the C compiler adds an underscore to global labels.

```
diag21k[0]>mr li _primes 20

        DATA_SRAM [00050040] =       2
        DATA_SRAM [00050041] =       3
        DATA_SRAM [00050042] =       5
        DATA_SRAM [00050043] =       7
        DATA_SRAM [00050044] =      11
        DATA_SRAM [00050045] =      13
        DATA_SRAM [00050046] =      17
        DATA_SRAM [00050047] =      19
        DATA_SRAM [00050048] =      23
        DATA_SRAM [00050049] =      29
        DATA_SRAM [0005004A] =      31
        DATA_SRAM [0005004B] =      37
        DATA_SRAM [0005004C] =      41
        DATA_SRAM [0005004D] =      43
        DATA_SRAM [0005004E] =      47
        DATA_SRAM [0005004F] =      53
        DATA_SRAM [00050050] =      59
        DATA_SRAM [00050051] =      61
        DATA_SRAM [00050052] =      67
        DATA_SRAM [00050053] =      71
```

Step 5: Test the Remaining Processor

10. To test the second ADSP-21160 processor, select it with the DSP select command.

```
diag21k[1]>ds 2

      Current DSP:   #2, processor 2 on Hammerhead (device 0)
```

11. With this processor selected, you can use the same commands as before to load a program and start the processor.

```
diag21k[2]>fl ..\etc\prm21160

      "..\etc\prm21160.dxe" loaded


diag21k[2]>ps

      processor running


diag21k[2]>mr li _primes 20
```

```
DATA_SRAM [00050040] =       2
DATA_SRAM [00050041] =       3
DATA_SRAM [00050042] =       5
DATA_SRAM [00050043] =       7
DATA_SRAM [00050044] =      11
DATA_SRAM [00050045] =      13
DATA_SRAM [00050046] =      17
DATA_SRAM [00050047] =      19
DATA_SRAM [00050048] =      23
DATA_SRAM [00050049] =      29
DATA_SRAM [0005004A] =      31
DATA_SRAM [0005004B] =      37
DATA_SRAM [0005004C] =      41
DATA_SRAM [0005004D] =      43
DATA_SRAM [0005004E] =      47
DATA_SRAM [0005004F] =      53
DATA_SRAM [00050050] =      59
DATA_SRAM [00050051] =      61
DATA_SRAM [00050052] =      67
DATA_SRAM [00050053] =      71
```

Step 6: Exit Diag21k

To exit Diag21k and reset the processor you have selected, use the quit command.

```
diag21k[1]>q

        exiting...resetting processor(s)

        C:\DSP21KSF\BIN>
```

2.5.2 Testing the Board with the Hammerhead-PC/104-*Plus* Example Files

The example software provided with the Hammerhead-PC/104-*Plus* contains examples that demonstrate how to use the various features of your board and software. The examples are located in the `examples` directory of the Hammerhead-PC/104-*Plus* CD-ROM.

2.6 Resetting the Hammerhead-PC/104-*Plus*

You can use the following three methods to reset the Hammerhead-PC/104-*Plus*:

- Enable the watchdog timer
- Attach an external reset switch to the board
- Send a reset signal via the PCI interface

2.6.1 Resetting the Board with the Watchdog Timer

The watchdog timer helps to ensure that the Hammerhead-PC/104-*Plus* is operating properly. It is also useful for standalone applications that need to restart when certain errors occur or a program crashes.

The Watchdog Configuration Register, which is located in the SharcFIN ASIC, enables and disables the watchdog timer. The register is located at offset 0x0000 0043 from the base of the ADSP-21160s' memory select line MS2 (see Table 5–1 and section 5.2.4).

Disabling the Watchdog Timer

The watchdog is disabled after the board is reset. When the watchdog is disabled, the SharcFIN constantly strobes the timer to keep it from elapsing. Since it is constantly being strobed, the watchdog timer will not time out regardless of whether the program fails. Section 5.2.4 explains how to disable the watchdog timer.

Enabling the Watchdog Timer

When enabled, the watchdog timer must be reset before it expires to prevent a board reset from occurring. The watchdog timer is reset every time FLAGX from a configured processor toggles from 0 to 1 or from 1 to 0. The FLAGX signals are flags that are under program control and can strobe the watchdog timer to prevent it from elapsing.

Six bits in the Watchdog Configuration register control the watchdog timer. The first two bits enable it and select its timeout time, and the next four bits determine which flag the watchdog will respond to (see Table 5–11 and Table 5–12 in section 5.2.4). The Watchdog configuration register is a write once register; therefore, once the watchdog is enabled, it cannot be disabled except by a board reset.

If the watchdog timer is enabled, the DSP program must toggle the chosen FLAGX signal within the given time frame. The Watchdog Configuration

Register allows you to select the watchdog's timeout time (see "Enabling the Watchdog and Setting its Time-out" on page 86). If the watchdog timer elapses, it will generate a system reset and the normal boot process will begin.

2.6.2 Resetting the Board via the External Reset Connector

The external reset connector (J16) allows the Hammerhead-PC/104-*Plus* board to reset or be reset by other system boards. The connector supports an input reset line to allow the Hammerhead-PC/104-*Plus* to receive reset signals from other boards; it also supports an output reset line to allow the Hammerhead-PC/104-*Plus* to reset other boards.

To reset the Hammerhead-PC/104-Plus with the external reset connector,

1. Connect a cable from the external reset connector (J16) on the Hammerhead-PC/104-*Plus* board to another system board. Refer to Figure 2–6 for cable details.
2. Any reset that occurs on the Hammerhead-PC/104-*Plus* reset source causes a reset on all Hammerhead-PC/104-*Plus* reset targets.

2.6.3 Resetting the Board via the PCI Interface

A register bit in the SharcFIN ASIC allows the board to reset from the host PC. When the register is written, all components on the board will be reset. Refer to procedure 3B on page 3-185 of the *QL5064 User Manual* for host side reset.

Chapter 3
Overview of the Hardware Components

This chapter gives a brief description of each of the Hammerhead-PC/104-*Plus*'s major hardware components, connectors, and jumpers. Section 3.1 describes the layout and function of the major components, section 3.2 describes the layout and function of the external connectors, and section 3.3 describes the layout and function of the configuration jumpers and switches.

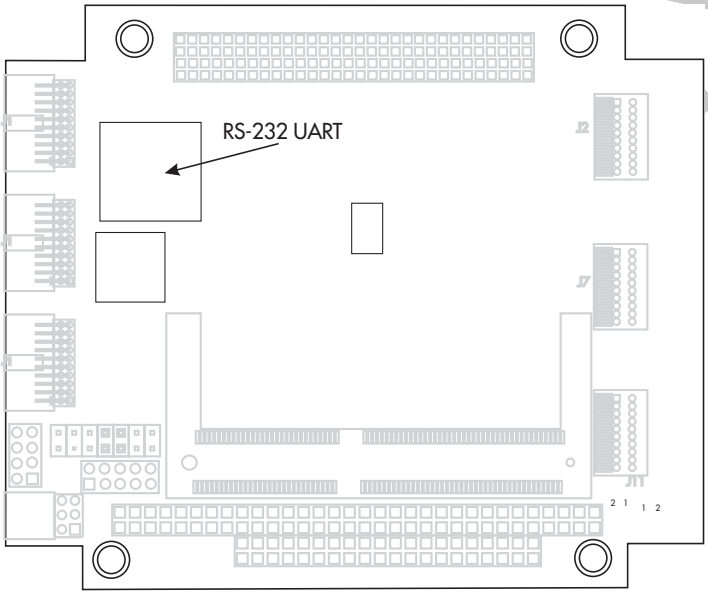
This chapter covers the following components and connectors:

- ADSP-21160 SHARC processors
- Flash memory
- SDRAM
- SharcFIN ASIC
- On-board oscillators
- UART
- User LEDs
- Watchdog timer
- PC/104-*Plus* module configuration rotary switch
- PC/104-*Plus* connector
- JTAG connector
- External serial ports
- External link ports
- Expansion connector
- Buffered inverted flag outputs
- External power connector
- External reset connector
- RS-232 connector
- Configuration jumpers
- Serial port configuration switches

3.1 Function and Location of the Major Components

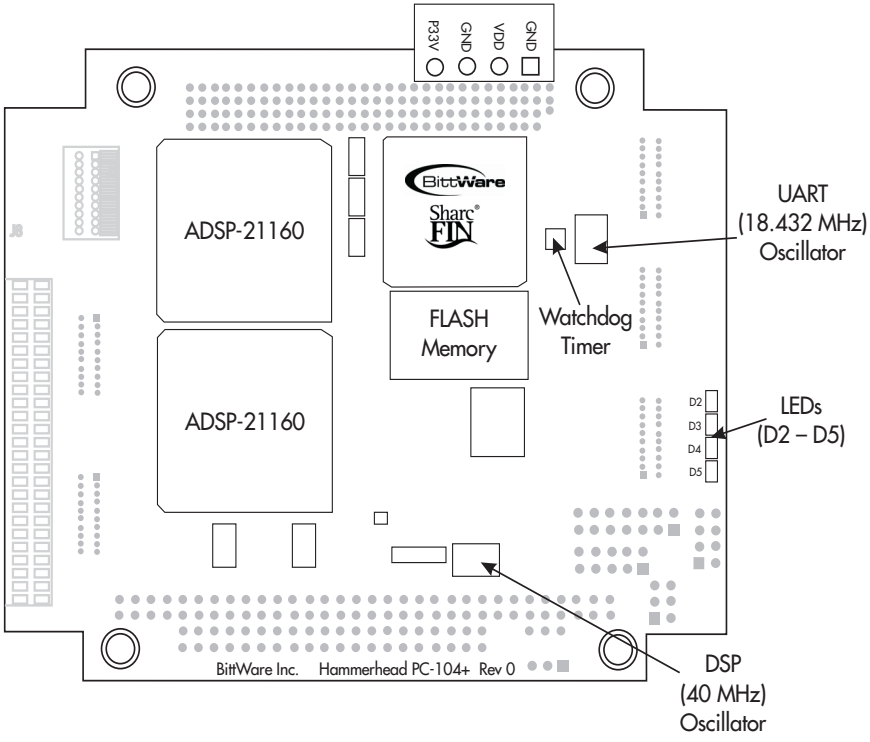
Figure 3–1 highlights the major components on the top side of the Hammerhead-PC/104-*Plus*, and Figure 3–2 highlights the components on the bottom. The sections that follow describe the features labeled in the diagrams.

Figure 3–1 *Layout of the Hammerhead-PC/104-Plus's Major Components (Top)*



Top

Figure 3–2 *Layout of the Hammerhead-PC/104-Plus's Major Components (Bottom)*



Bottom

3.1.1 ADSP-21160 SHARC Processors

The Hammerhead-PC/104-*Plus* features two ADSP-21160 SHARC digital signal processors from Analog Devices. The DSPs feature 600 MFLOPS of processing power and operate at 100 MHz. Each processor supports two I^2S serial ports, 14 DMA channels, four flags, three interrupts, six link ports, and 4 Mbits of dual-ported on-chip SRAM.

The two processors share a common processor bus, which gives them direct access to the SDRAM and the SharcFIN. The SharcFIN provides access to the PCI interface, the Flash, and the UART.

3.1.2 External Memory Banks

Flash Memory

The board's 2 MB (2M × 8) bank of Flash memory has two uses. It stores programs that boot the ADSP-21160 processors, allowing the Hammerhead-PC/104-*Plus* to boot without a host computer (see Appendix B). It also functions as non-volatile storage space, allowing the ADSP-21160s to read, write, and erase its contents.

SDRAM

The Hammerhead-PC/104-*Plus* has a standard 144-pin SODIMM for adding a 64, 128, 256 or 512 MB SDRAM module to the board for banked external memory. The ADSP-21160s can access the SDRAM at rates up to 50 MHz (see section 4.2).

3.1.3 SharcFIN ASIC

BittWare's SharcFIN ASIC flexibly interfaces the ADSP-21160 DSPs to a wide range of the Hammerhead-PC/104-*Plus*'s interfaces, including the 32/33 MHz PCI bus (Rev. 2.2 compliant), SDRAM, UART, I^2C serial ports, Flash, and a general purpose expansion bus. The SharcFIN also provides a feature-rich set of DMA functions and interrupt options to support very high-speed, real-time data flow with a minimum of processor overhead. The following is a list of the SharcFIN's features:

- 32-bit, 33 MHz PCI Rev. 2.2 compliant interface (528 MB/s burst, 400 MB/s sustained)
- Connected to the 32-bit, 50 MHz ADSP-21160 processor bus
- Connected to the peripheral bus
  - 8 bits wide @ 25 MHz
  - Accessible from the ADSP-21160 cluster bus and the PCI bus
  - Flash interface for SHARC boot and non-volatile data storage
- Four independent DMA controllers with support for fly-by and chaining (two transmit, two receive)
- Six independent FIFOs (2.4 KB total)
  - Four DMA buffers, 64×64 each (two transmit, two receive)
  - Two target buffers, 32×64 write, 16×64 read
- Direct, single PCI access from the ADSP-21160 processor bus
- 16-byte configurable PCI mailbox registers

- I_2O™ V1.5 compliant
- Programmable interrupt multiplexer: 10 inputs, 7 outputs (1 of each dedicated to PCI)
- Standard UART and I^2C

3.1.4 On-Board Oscillators

DSP Clock

A 50 MHz system oscillator chip provides the clock for the ADSP-21160 processors. Figure 3–2 shows where it is located. Please note that a 40 MHz oscillator will take the place of the 50 MHz oscillator if the DSPs on your board are 80 MHz.

UART Clock

An 18.432 MHz oscillator chip provides the clock for the UART. Figure 3–2 shows where it is located.

3.1.5 Dual RS-232 UART

The dual RS-232 UART allows the ADSP-21160 processors to communicate with external devices, such as the host computer, via the Hammerhead-PC/104-*Plus*'s RS-232 ports. The UART is accessible via the 8-bit, 25 MHz peripheral bus.

3.1.6 User LEDs

You can use the four LEDs on the Hammerhead-PC/104-*Plus* board to indicate certain conditions in the software or to provide feedback. Each LED has a corresponding flag pin that controls it on one of the ADSP-21160 processors. Section 4.2.5 shows which LED is connected to which flag.

3.1.7 Watchdog Timer

The watchdog timer helps to ensure that the Hammerhead-PC/104-*Plus* is operating properly. It is useful for standalone applications that need to restart when certain errors occur or a program crashes. Section 5.2.4 explains how to enable and disable the watchdog timer.

3.2 Layout and Function of the External Connectors

Figure 3–3 highlights the external connectors on the top side of the Hammerhead-PC/104-*Plus*, and Figure 3–4 highlights the external connectors on the bottom. Table 3–1 gives a brief description of each connector.

Figure 3–3 *Layout of the Hammerhead-PC/104-Plus's External Connectors (Top)*

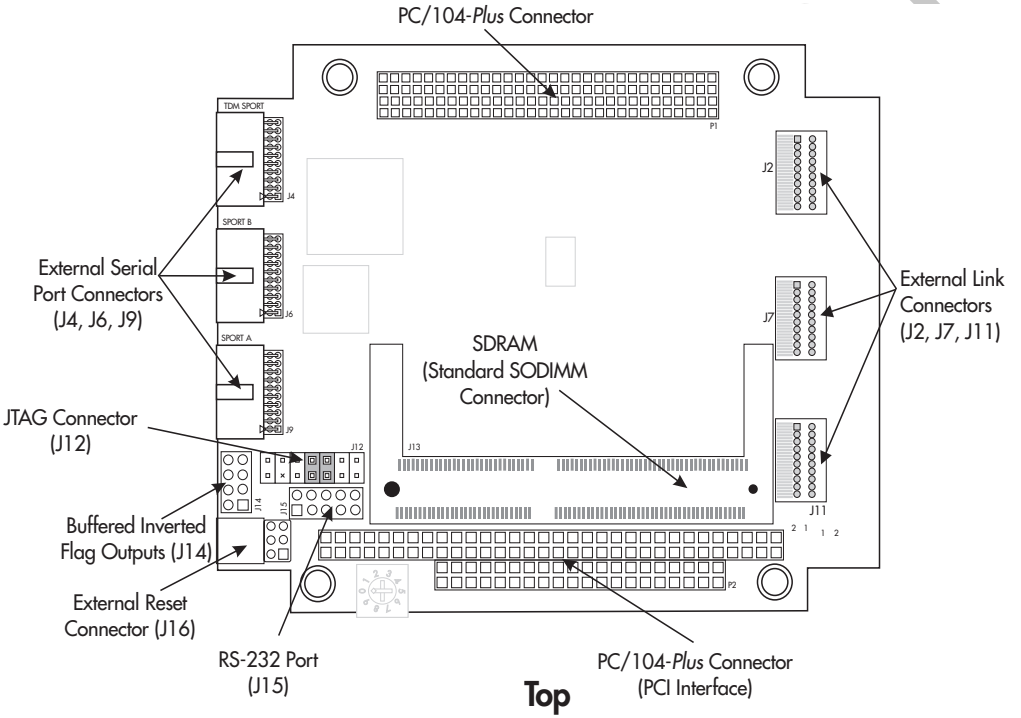
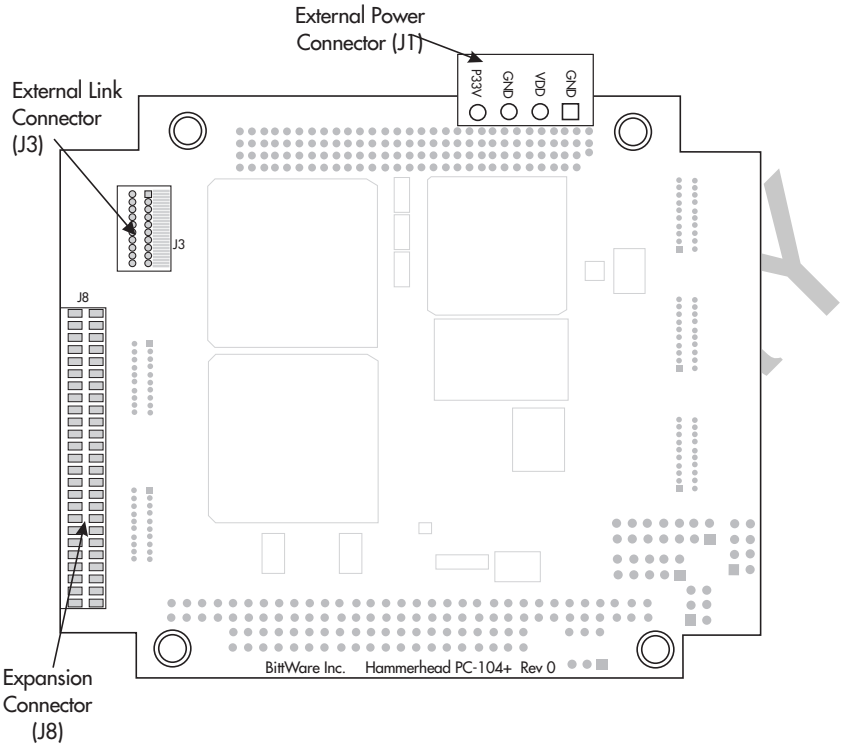


Figure 3–4 *Layout of the Hammerhead-PC/104-Plus's External Connectors (Bottom)*



Bottom

Table 3–1 *Overview of the External Connectors*

Connector	Number	Type	Description
PC/104	P1	PC/104	PC/104 stack-through connector with PCI bus interface
PC/104-*Plus*	P2	PC/104-*Plus*	PC/104-*Plus* stack-through connector
External Power	J1	4-pin	Connection for 3.3V and +5V external power supply
External Link Ports	J2, J3, J7, J11	26-pin	100 MB/s communication route between external devices and ADSP-21160s
External Serial Ports	J4, J6, J9	20-pin IDC	Communication route between ADSP-21160s and synchronous serial devices
Expansion Connector	J8	50-pin	Connection for custom peripheral on 8-bit, 25 MHz expansion bus
JTAG	J12	14-pin	Connection for ICE in-circuit emulator
SDRAM (SODIMM)	J13	144-pin	Connection for standard 144-pin SODIMM SDRAM modules
Buffered Inverted Flag Outputs	J14	16-pin	Access to FLAG2 and FLAG3 on each processor
RS-232	J15	10-pin	External serial interface to UART
External Reset	J16	6-pin	Connection for external reset signals

3.2.1 PC/104-*Plus* Connectors

The PC/104-*Plus* interface consists of two connectors: a 120-pin (4×30) connector that provides the PCI bus interface, and a standard 104-pin PC/104 connector that provides the PC/104 bus interface. The connectors are stack-through, allowing multiple PC/104-*Plus* modules in a stack. Figure 3–5 below gives the location of the PC/104-*Plus* connector pins, and Table 3–2 gives the connector pinouts. Table 3–3 gives the pinouts for the standard PC/104 connector.

Figure 3–5 *Location of the PC/104-Plus Connector Pins*

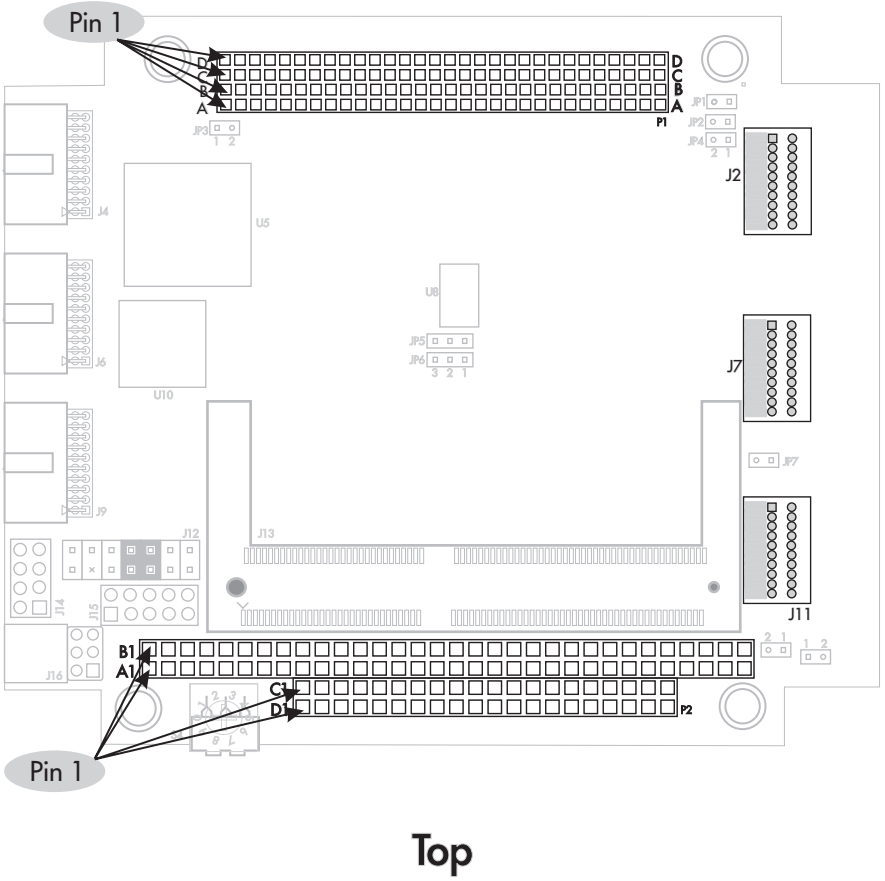


Table 3–2 *PC/104 Connector Pinout*

P1:A		P1:B		P1:C		P1:D	
A1	GND	B1	Reserved	C1	+5V	D1	AD00
A2	VI/O	B2	AD02	C2	AD01	D2	+5V
A3	AD05	B3	GND	C3	AD04	D3	AD03
A4	$\overline{\text{CBE0}}$	B4	AD07	C4	GND	D4	AD06
A5	GND	B5	AD09	C5	AD08	D5	GND
A6	AD11	B6	VI/O	C6	AD10	D6	M66EN
A7	AD14	B7	AD13	C7	GND	D7	AD12
A8	+3.3V	B8	$\overline{\text{CBE1}}$	C8	AD15	D8	+3.3V
A9	$\overline{\text{SERR}}$	B9	GND	C9	$\overline{\text{SB0}}$	D9	PAR
A10	GND	B10	$\overline{\text{PERR}}$	C10	+3.3V	D10	SDONE
A11	$\overline{\text{STOP}}$	B11	+3.3V	C11	$\overline{\text{LOCK}}$	D11	GND
A12	+3.3V	B12	$\overline{\text{TRDY}}$	C12	GND	D12	$\overline{\text{DEVSEL}}$
A13	$\overline{\text{FRAME}}$	B13	GND	C13	$\overline{\text{IRDY}}$	D13	+3.3V
A14	GND	B14	AD16	C14	+3.3V	D14	$\overline{\text{CBE2}}$
A15	AD18	B15	+3.3V	C15	AD17	D15	GND
A16	AD21	B16	AD20	C16	GND	D16	AD19
A17	+3.3V	B17	AD23	C17	AD22	D17	+3.3V
A18	IDSEL0	B18	GND	C18	IDSEL1	D18	IDSEL2
A19	AD24	B19	$\overline{\text{CBE3}}$	C19	VI/O	D19	IDSEL3
A20	GND	B20	AD26	C20	AD25	D20	GND
A21	AD29	B21	+5V	C21	AD28	D21	AD27
A22	+5V	B22	AD30	C22	GND	D22	AD31
A23	$\overline{\text{REQ0}}$	B23	GND	C23	$\overline{\text{REQ1}}$	D23	VI/O
A24	GND	B24	$\overline{\text{REQ2}}$	C24	+5V	D24	$\overline{\text{GNT0}}$
A25	$\overline{\text{GNT1}}$	B25	VI/O	C25	$\overline{\text{GNT2}}$	D25	GND
A26	+5V	B26	CLK0	C26	GND	D26	CLK1
A27	CLK2	B27	+5V	C27	CLK3	D27	GND
A28	GND	B28	$\overline{\text{INTD}}$	C28	+5V	D28	$\overline{\text{RST}}$
A29	+12V	B29	$\overline{\text{INTA}}$	C29	$\overline{\text{INTB}}$	D29	$\overline{\text{INTC}}$
A30	-12V	B30	Reserved	C30	Reserved	D30	3.3VKEY

Table 3–3 *PC/104-Plus Connector Pinout -* ***PCI Interface***

P2:A		P2:B		P2:C		P2:D	
A1	IOCHCHK	B1	GND	C0	GND	D0	GND
A2	SD7	B2	RESET	C1	SBHE	D1	$\overline{\text{MEMCS16}}$
A3	SD6	B3	VDD	C2	LA23	D2	$\overline{\text{IOCS16}}$
A4	SD5	B4	IRQ9	C3	LA22	D3	IRQ10
A5	SD4	B5	N5V	C4	LA21	D4	IRQ11
A6	SD3	B6	DRQ2	C5	LA20	D5	IRQ12
A7	SD2	B7	N12V	C6	LA19	D6	IRQ15
A8	SD1	B8	ENDXFR	C7	LA18	D7	IRQ14
A9	SD0	B9	P12V	C8	LA17	D8	$\overline{\text{DACK0}}$
A10	IOCHRDY	B10	(KEY)	C9	$\overline{\text{MEMR}}$	D9	$\overline{\text{DRQ0}}$
A11	AEN	B11	$\overline{\text{SMEMW}}$	C10	$\overline{\text{MEMW}}$	D10	$\overline{\text{DACK5}}$
A12	SA19	B12	$\overline{\text{SMEMR}}$	C11	SD8	D11	DRQ5
A13	SA18	B13	$\overline{\text{IOW}}$	C12	SD9	D12	$\overline{\text{DACK6}}$
A14	SA17	B14	$\overline{\text{IOR}}$	C13	SD10	D13	DRQ6
A15	SA16	B15	$\overline{\text{DACK3}}$	C14	SD11	D14	$\overline{\text{DACK7}}$
A16	SA15	B16	$\overline{\text{DRQ3}}$	C15	SD12	D15	DRQ7
A17	SA14	B17	$\overline{\text{DACK1}}$	C16	SD13	D16	VDD
A18	SA13	B18	$\overline{\text{DRQ1}}$	C17	SD14	D17	$\overline{\text{MASTER}}$
A19	SA12	B19	$\overline{\text{REFRESH}}$	C18	SD15	D18	GND
A20	SA11	B20	SYSCLK	C19	KEY	D19	GND
A21	SA10	B21	IRQ7				
A22	SA9	B22	IRQ6				
A23	SA8	B23	IRQ5				
A24	SA7	B24	IRQ4				
A25	SA6	B25	IRQ3				
A26	SA5	B26	DACK2				
A27	SA4	B27	TC				
A28	SA3	B28	BALE				
A29	SA2	B29	VDD				
A30	SA1	B30	OSC				
A31	SA0	B31	GND				
A32	GND	B32	GND				

3.2.2 External Power Connector

When operating in standalone mode, the Hammerhead-PC/104-*Plus* can receive power from an external power supply via the 4-pin external power and reset connector. The external power connector (J1) supplies +3.3V, +5 VDD, and GND to the board. Figure 3–6 below shows the location of the external power connector pins, and Table 3–4 gives the pinout.

Figure 3–6 *Location of the External Power Connector Pins (Bottom)*

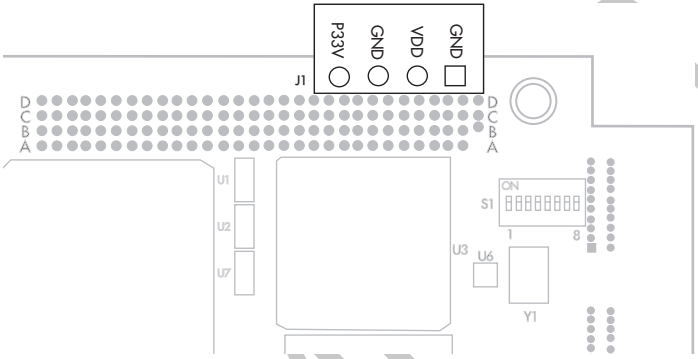


Table 3–4 *External Power Connector Pinout (J1)*

Pin	Signal
1	GND
2	VDD
3	GND
4	3.3V

3.2.3 External Link Ports

The Hammerhead-PC/104-*Plus* has four 26-pin external link port connectors: J2, J3, J7, and J11. The external link ports allow you to connect the Hammerhead-PC/104-*Plus* directly to other boards.Table 3–5 gives the connector pinout; Figure 3–7 shows the location of the link pins on the top side of the board, and Figure 3–8 shows the link pins on the bottom.

Table 3–5 *Link Port Connector Pinout (J2, J3, J7, and J11)*

J2		J3		J7		J11	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	NC	1	NC	1	NC	1	NC
2	EA_L4CLK	2	EA_L3CLK	2	EA_L2CLK	2	EA_L1CLK
3	EA_L4ACK	3	EA_L3ACK	3	EA_L2ACK	3	EA_L1ACK
4	EA_L4DAT0	4	EA_L3DAT0	4	EA_L2DAT0	4	EA_L1DAT0
5	EA_L4DAT1	5	EA_L3DAT1	5	EA_L2DAT1	5	EA_L1DAT1
6	EA_L4DAT2	6	EA_L3DAT2	6	EA_L2DAT2	6	EA_L1DAT2
7	EA_L4DAT3	7	EA_L3DAT3	7	EA_L2DAT3	7	EA_L1DAT3
8	EA_L4DAT4	8	EA_L3DAT4	8	EA_L2DAT4	8	EA_L1DAT4
9	EA_L4DAT5	9	EA_L3DAT5	9	EA_L2DAT5	9	EA_L1DAT5
10	EA_L4DAT6	10	EA_L3DAT6	10	EA_L2DAT6	10	EA_L1DAT6
11	EA_L4DAT7	11	EA_L3DAT7	11	EA_L2DAT7	11	EA_L1DAT7
12	NC	12	NC	12	NC	12	NC
13	NC	13	NC	13	NC	13	NC
14	GND	14	GND	14	GND	14	GND
15	GND	15	GND	15	GND	15	GND
16	GND	16	GND	16	GND	16	GND
17	GND	17	GND	17	GND	17	GND
18	GND	18	GND	18	GND	18	GND
19	GND	19	GND	19	GND	19	GND
20	GND	20	GND	20	GND	20	GND
21	GND	21	GND	21	GND	21	GND
22	GND	22	GND	22	GND	22	GND
23	GND	23	GND	23	GND	23	GND
24	GND	24	GND	24	GND	24	GND
25	GND	25	GND	25	GND	25	GND
26	JP2	26	JP4	26	JP7	26	JP9

Figure 3–7 *Location of External Link Connectors J2, J7, and J11 (Top)*

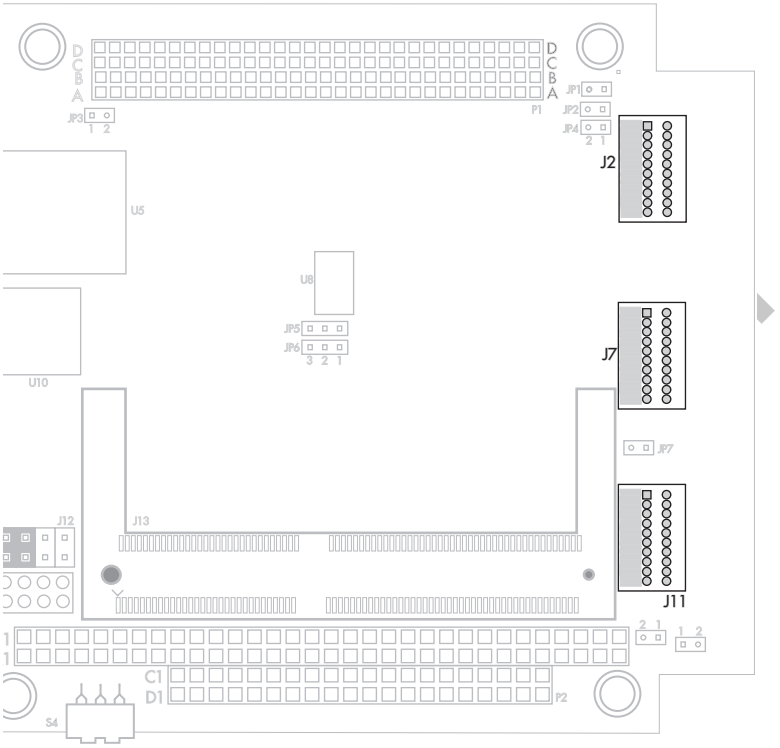
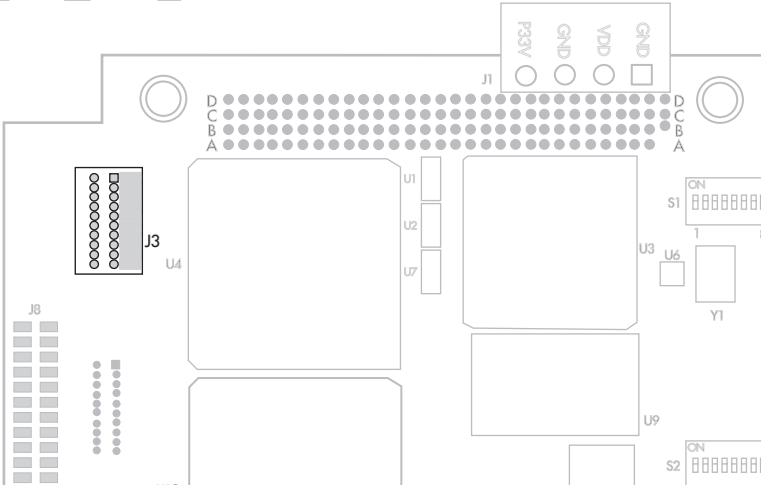


Figure 3–8 *Location of External Link Connector J3 (Bottom)*



3.2.4 External Serial Ports

Three 20-pin, 50mm right-angle IDC external serial port connectors (J4, J6, J9) provide a communication route between the ADSP-21160s and synchronous serial devices at rates up to 50 Mbits/s. The serial ports on the Hammerhead-PC/104-*Plus* conform to BittWare's "*Universal Serial Port Specification*" (available from BittWare upon request).

External Serial Port Connections and Usage

Each serial port has a corresponding dip switch that allows you to configure its signal connections.Table 3–6 below lists the connections for each serial port and the dip switches that correspond to each serial port.

Table 3–6 *External Serial Port Connections and Usage*

Serial Port	Dip Switch	Description
J4	S1	Connected to both ADSP-21160 processors as a TDM serial port
J6	S2	Connected to 21160-2 as a standard serial port
J9	S3	Connected to 21160-1 as a standard serial port

Available Serial Port Cable Components

If you choose to create a cable to connect the Hammerhead-PC/104-*Plus* to another serial device, the components in Table 3–7 are available from BittWare.

Table 3–7 *Serial Port Cables Available from BittWare*

Location	Type	Manufacturer	Part Number
Hammerhead-PC/104-*Plus* (J4, J6, J9)	Coax Ribbon, TDM or Standard	BittWare	HH-SP-TDM-04 HH-SP-STD-04

Serial Port Connector Pinout

Figure 3–9 shows where the pins are located on the serial port connectors, and Table 3–8 gives their pinouts. The signals in the pinout tables come directly from the ADSP-21160 pins they are associated with, and they exhibit the same timing characteristics described in the *ADSP-21160 User's Manual* (Analog Devices, Inc.). The signals are series terminated with 82Ω.

Figure 3–9 *Location of the External Serial Port Connector Pins (Top)*

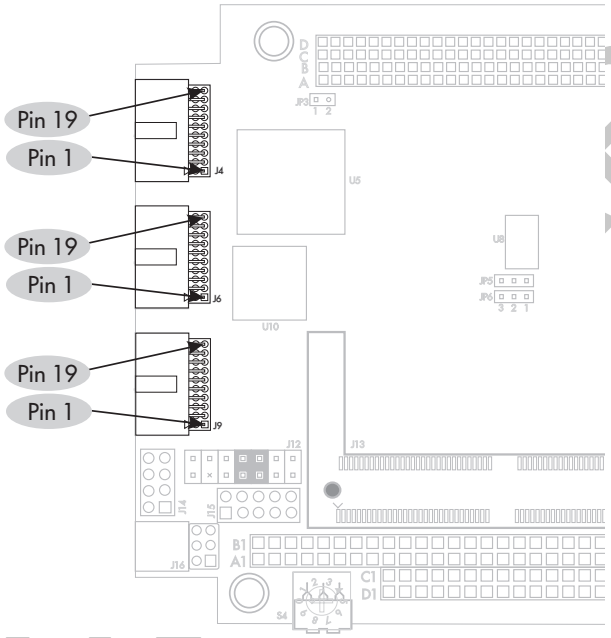


Table 3–8 *External Serial Port Connector Pinout (J4, J6, J9)*

Pin	Signal	Pin	Signal
1	P33V	2	GND
3	RCK	4	GND
5	RFS	6	GND
7	RD	8	GND
9	RD2/FI1	10	GND
11	GND	12	TD2/FI2
13	GND	14	TD
15	GND	16	TFS
17	GND	18	TCK
19	GND	20	GIO

3.2.5 Expansion Connector

The HHP4 features an expansion connector that provides access to the board's 8-bit, 25 MHz peripheral bus. Table 3–10 shows the location of the pins, and Table 3–9 gives the pinout for the connector.

Figure 3–10 *Location of the Expansion Bus Connector Pins (Bottom)*

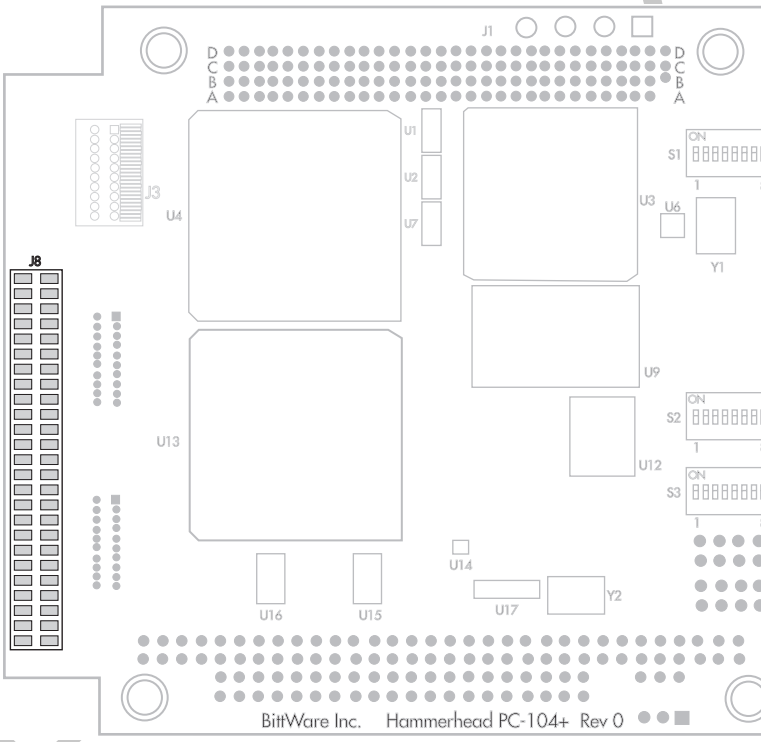


Table 3–9 *Peripheral Bus Connector Pinout*

Pin	Description	Pin	Description
1	$\overline{\text{PRA\_INT}}$	2	GND
3	$\overline{\text{PRA\_RST}}$	4	GND
5	$\overline{\text{PRA\_WR}}$	6	GND
7	$\overline{\text{PRA\_RD}}$	8	GND
9	$\overline{\text{PRA\_ACK}}$	10	GND
11	PRA_D00	12	GND
13	PRA_D01	14	GND
15	PRA_D02	16	GND
17	PRA_D03	18	GND
19	PRA_D04	20	GND
21	PRA_D05	22	GND
23	PRA_D06	24	GND
25	PRA_D07	26	GND
27	$\overline{\text{PRA\_UBSEL}}$	28	GND
29	PRA_A00	30	GND
31	PRA_A01	32	GND
33	PRA_A02	34	GND
35	PRA_A03	36	GND
37	PRA_A04	38	GND
39	PRA_A05	40	GND
41	PRA_A06	42	GND
43	PRA_A07	44	GND
45	PRA_A08	46	GND
47	PRA_A09	48	GND
49	PRA_A10	50	GND

3.2.6 JTAG Connector

The JTAG connector (J12) is a 14-pin connector that allows you to attach an optional White Mountain DSP ICE emulator for program debugging. Appendix A overviews installing and using in-circuit emulators with the Hammerhead-PC/104-*Plus*. Refer to Figure 3–11 below for the location of the JTAG connector pins and to Table 3–10 for the connector pinout.

Figure 3–11 *Location of the JTAG Connector Pins (Top)*

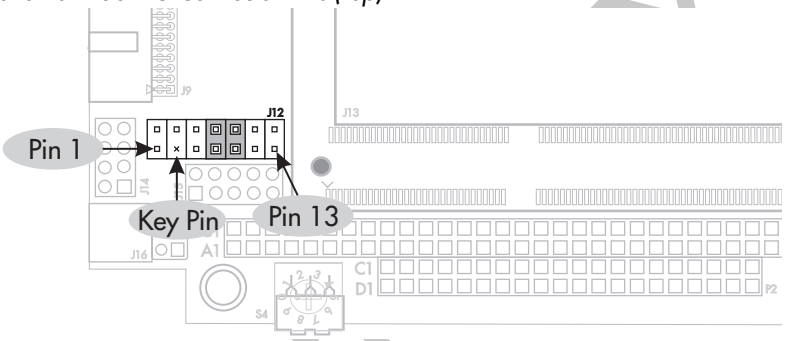


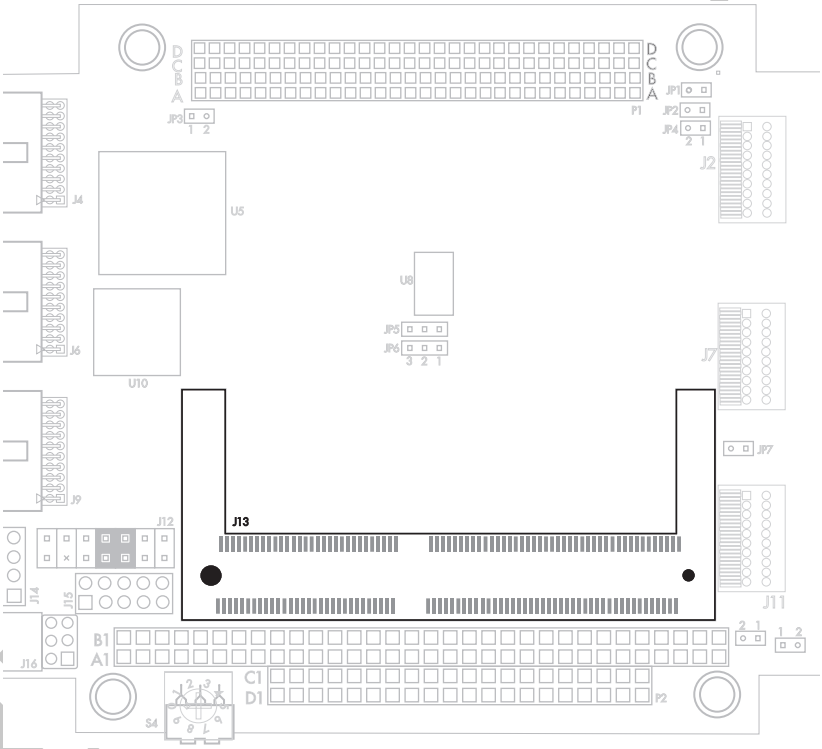
Table 3–10 *JTAG Connector Pinout (J12)*

Pin	Signal	Pin	Signal
1	GND	2	$\overline{\text{EMU}}$
3	KEY	4	CLK
5	BTMS	6	TMS
7	BTCK	8	TCK
9	$\overline{\text{BTRST}}$	10	$\overline{\text{TRST}}$
11	BTDI	12	TDI
13	GND	14	TDO

3.2.7 SDRAM (SODIMM)

The Hammerhead-PC/104-*Plus* has an industry-standard 144-pin connection for a standard SODIMM module. The SODIMM modules are available in 64, 128, 256, and 512 MB modules. Figure 3–12 shows where the connector pins are located on the board.

Figure 3–12 *Location of the SODIMM Connector Pins (Top)*



3.2.8 Buffered Inverted Flag Outputs

The buffered inverted flag output connector (J14) allows access to the FLAG2 and FLAG3 signals on each ADSP-21160 DSP. The ADSP-21160s' flag signals are routed through an inverting buffer and are outputs only. Figure 3–13 shows where pin 1 is located on the connector, and Table 3–11 gives the connector pinout.

Figure 3–13 *Location of the Buffered Inverted Flag Output Connector Pins (Top)*

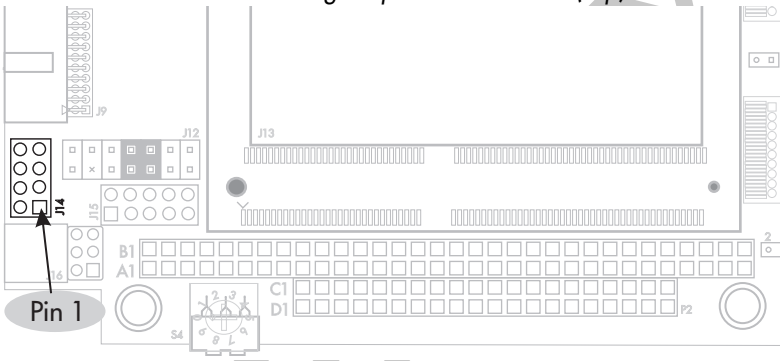


Table 3–11 *Buffered Inverted Flag Output Pinout*

Pin	Signal	Pin	Signal
1	HA1_F2	2	GND
3	HA1_F3	4	GND
5	HA2_F2	6	GND
7	HA2_F3	8	GND

3.2.9 RS-232 Connector

The Hammerhead-PC/104-*Plus* is configured with a 10-pin RS-232 connector (J15). The connector transports serial data between the host and the UART, which interfaces the data to the ADSP-21160 processors. Figure 3–14 shows the location of the RS-232 connector pins, and Table 3–12 gives the connector pinout. An RS-232 cable is available from BittWare, part number CARL-U10-06, or you may provide your own.

Figure 3–14 *Location of the RS-232 Connector Pins (Top)*

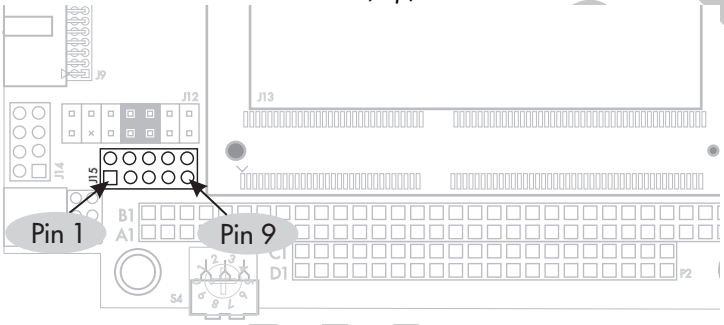


Table 3–12 *RS-232 Connector Pinout (J15)*

Pin*	Signal	Pin	Signal
1		2	
3	TXD	4	$\overline{\text{CTS}}$
5	RXD	6	$\overline{\text{RTS}}$
7		8	NC
9	GND	10	NC

* Pins 1, 2, and 7 are connected together on the board.

3.2.10 External Reset Connector

The external reset connector (J16) allows the Hammerhead-PC/104-*Plus* board to reset or be reset by other system boards. The connector supports an input reset line to allow the Hammerhead-PC/104-*Plus* to receive reset signals from other boards; it also supports an output reset line to allow the Hammerhead-PC/104-*Plus* to reset other boards. Figure 3–15 shows the location of the external reset connector pins.

Figure 3–15 *External Reset Connector Pins (Top)*

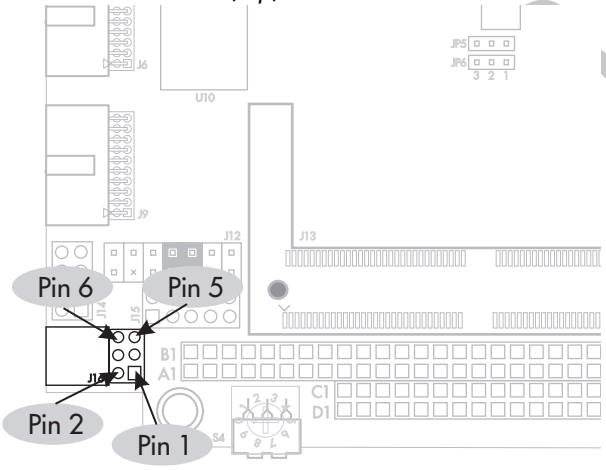


Table 3–13 *External Reset Connector Pinout (J16)*

Pin	Signal	Pin	Signal
1	NC	2	HA_EXTGRPRSTIN
3	NC	4	GND
5	GND	6	HA_EXTGRPRSTOUT

3.3 Function and Location of the Configuration Jumpers and Switches

The Hammerhead-PC/104-*Plus* has nine configuration jumpers and four dip switches that allow you to control and enable certain features on the board. Before installing and operating the Hammerhead-PC/104-*Plus*, make sure to properly set all of the configuration jumpers. Table 3–14 below gives an overview of the jumpers, Table 3–15 gives an overview of the dip switches, and section 2.2 describes their settings in detail. Figure 3–16 and Figure 3–17 show the locations of the configuration jumpers and switches.

Table 3–14 *Hammerhead-PC/104-Plus Configuration Jumpers*

Jumper	Name	Type	Description
JP1	Primary PCI bus speed	2-pin	Sets the speed of the primary PCI bus to either 33 MHz or 66 MHz
JP2, JP4, JP7, JP9	External link port power	2-pin	Gates power to the external link port connectors*
JP3	Standalone mode	2-pin	Jumper must be on to operate board in standalone mode
JP5	21160-1 boot mode jumper	3-pin	Sets 21160-1 to boot from host computer, on-board FLASH, or remote processor via link port
JP6	21160-2 boot mode jumper	3-pin	Sets 21160-2 to boot from host computer, on-board FLASH, or remote processor via link port
JP8	21160 bus priority	2-pin	Sets bus priority as either fixed or rotating

* These jumpers are for custom use only. Contact BittWare for more information prior to setting JP2, JP4, JP7 or JP9.

Table 3–15 *Hammerhead-PC/104-Plus Serial Port Dip Switches*

Dip Switch	Name	Type	Description
S1	Serial port dip switch for J4	8-pos dip	Configures serial port J4 as a TDM serial connection to both ADSP-21160 DSPs
S2	Serial port dip switch for J6	8-pos dip	Configures serial port J6 as a standard serial connection to 21160-2 (SPORT B)
S3	Serial port dip switch for J9	8-pos dip	Configures serial port J9 as a standard serial connection to 21160-1 (SPORT A)
S4	PC/104-*Plus* module configuration rotary switch	10-pos rotary	Configures the board according to its position in the PC/104-*Plus* stack

Figure 3–16 *Location of the Configuration Jumpers and Switches (Top)*

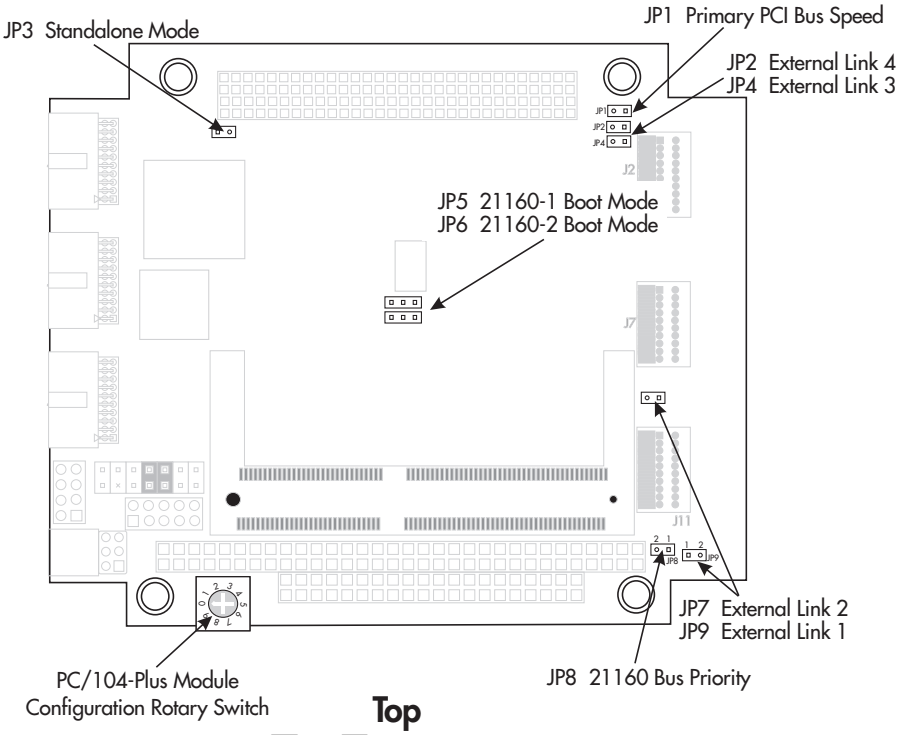
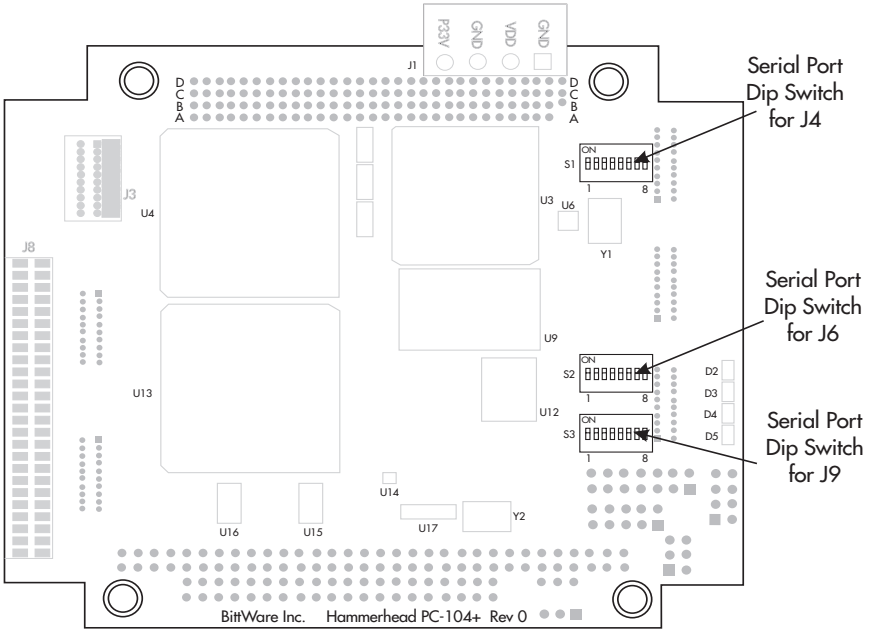


Figure 3–17 *Location of the Configuration Jumpers and Switches (Bottom)*



Bottom

Chapter 4
Hammerhead-PC/104-*Plus* Board Architecture

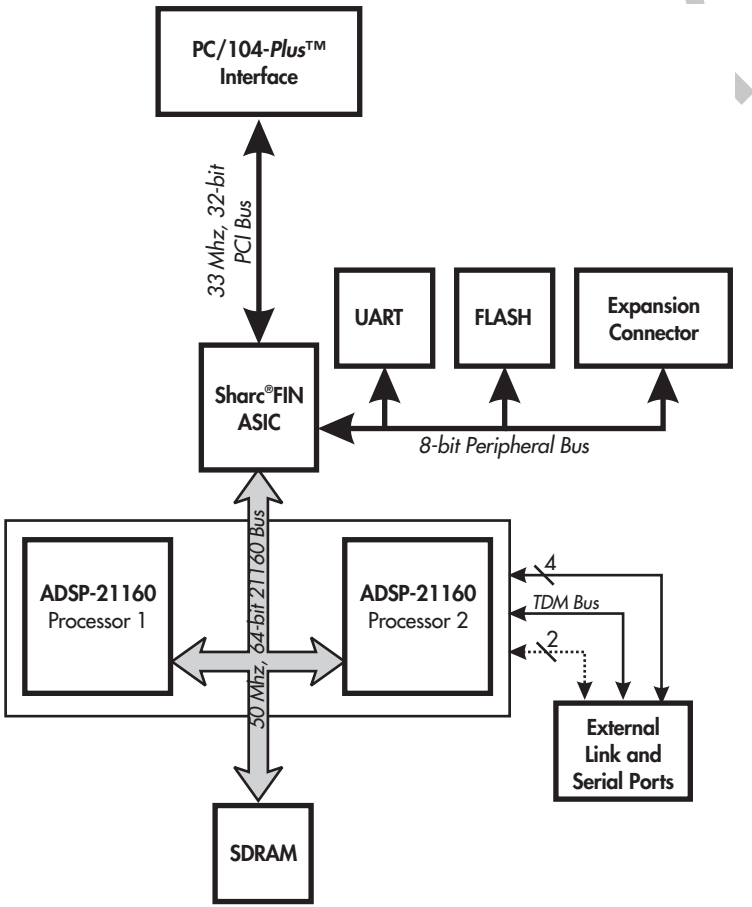
This chapter discusses the architecture of the board, describing how the ADSP-21160 DSPs communicate with other DSPs, with the host, and with other I/O peripherals. This chapter covers the following topics:

- how the DSPs access internal and external memory
- the connections of the DSPs' serial ports
- the connections of the DSPs' link ports
- the connections of the DSPs' flags and interrupts
- the connections to the DSPs' 32-bit cluster bus
- the structure of the PCI interface (including the SharcFIN ASIC, PCI bus, and peripheral bus)

4.1 Overview of the Board Architecture

This section briefly describes how data flows through the Hammerhead-PC/104-*Plus* board. The sections that follow discuss the board's architecture in more detail.

Figure 4–1 *Block Diagram of the Hammerhead-PC/104-Plus System*



The Hammerhead-PC/104-*Plus* features two ADSP-21160 DSPs operating at 100 MHz. The processors communicate via the 64-bit, 50 MHz processor bus, and have access to a bank of up to 512 MB SDRAM, the SharcFIN ASIC, 2 MB bank Flash RAM, a UART, and an expansion connector.

There are three buses on the Hammerhead-PC/104-*Plus*: the processor bus, the PCI bus, and the peripheral bus. The 64-bit, 50 MHz processor bus connects the ADSP-21160 DSPs and provides access to the bank of SDRAM. The processor bus also connects to the SharcFIN ASIC, which provides a bridge between the DSPs and the 32-bit, 33 MHz PCI bus. A peripheral bus extends off the SharcFIN, providing access to the UART, Flash RAM and the expansion connector.

For I/O options, the board features three serial port connectors, four link connectors, an RS-232 port, and an expansion connector. Two of the serial connectors are standard serial ports, the third is a serial TDM port. The RS-232 port connects to the UART to allow serial communication with the ADSP-21160 DSPs, and the expansion connector provides access to the 8-bit, 25 MHz peripheral bus.

4.2 ADSP-21160 Architecture

This section gives a short description of the architecture of the ADSP-21160 DSPs. For additional information, refer to the *ADSP-21160 User's Manual* (Analog Devices, Inc.).

4.2.1 Resources Available to the ADSP-21160s

This section discusses the resources available to each processor: memory banks, flags and interrupts, serial ports, and link ports. The following tables summarize how the DSPs' resources are used on the Hammerhead-PC/104-*Plus*. The row labeled "MS" refers to the DSPs' external memory select lines (MS0–MS3).

Table 4–1 *Resources for 21160-1*

	MS	Serial Port	Interrupt	Flag	Link Port
0	SDRAM	TDM Bus	SharcFIN*	SharcFIN	21160-2 L0
1	Flash	External	SharcFIN	SharcFIN	External J2
2	SharcFIN		21160-2 F2 21160-2 F3	SharcFIN SPORT A J9 LED D3	21160-2 L4 External J7
3	UART			SharcFIN LED D5	21160-2 L5 External J3
4					External J11
5					21160-2 L2

* IRQ0, IRQ1, FLAG0, FLAG1, FLAG2, and FLAG3 on each processor connect to the SharcFIN ASIC interrupt multiplexer. From the SharcFIN, you can route them to different locations on the board.

Table 4–2 *Resources for 21160-2*

	MS	Serial Port	Interrupt	Flag	Link Port
0	SDRAM	TDM Bus	SharcFIN	SharcFIN	21160-1 L0
1	Flash	External	SharcFIN	SharcFIN	External J7
2	SharcFIN		21160-1 F2 21160-1 F3	SharcFIN SPORT B J6 LED D4	21160-1 L5
3	UART			SharcFIN LED D2	External J3
4					21160-1 L2
5					21160-1 L3

4.2.2 ADSP-21160 Memory Structure

This section describes the memory structure of the ADSP-21160 DSPs. The processors can access their own internal memory, the internal memory of other processors in the same cluster, and external memory devices. The sections below describe each type of memory.

Internal Memory

Internal memory addresses an ADSP-21160 DSP's on-chip, dual-ported SRAM. Each ADSP-21160 DSP has 4 Mbits of on-chip SRAM. The *ADSP-21160 SHARC User's Manual* gives details about the on-chip SRAM's limitations and how to configure it.

Multiprocessor Memory

Multiprocessor memory space (MMS) is the on-chip SRAM of the other ADSP-21160 DSPs in the same cluster. A cluster is up to six ADSP-21160 DSPs that share a common processor bus, and any DSP that is connected to the processor bus shares the MMS. The Hammerhead-PC/104-*Plus* has two DSPs on board that share a common bus (the ADSP-21160 cluster bus); each processor can view the other DSP's on-chip SRAM.

External Memory

External memory space consists of other devices that share the ADSP-21160's 64-bit cluster bus. The external memory space is divided into four banked sections of memory. Each ADSP-21160 DSP has four memory select lines,

MS0–MS3, which allow it to access the external memory banks located on the 64-bit ADSP-21160 cluster bus and on the 8-bit peripheral bus.

Setting the Size of the External Memory Banks. The MSIZE bits of the ADSP-21160's SYSCON register define the size of the four banked sections of memory, which are numbered 0 to 3. All four memory banks are the same size (refer to the *ADSP-21160 SHARC User's Manual* for more details). Bank 0 starts at 0x0800 0000, and its MSIZE determines the starting address of each of the other banks.

Use the BittWare Configuration Manager utility included with the DSP21k-SF Toolkit to set the MSIZE (see Section 2.4.2). The default setting for MSIZE should be equal to the size of the largest external memory device, which is the SDRAM. Table 4–3 lists the recommended settings for MSIZE and shows how MSIZE affects the bank addresses. Note that programming the MSIZE bits may affect where other resources available to the ADSP-21160 processor are located.

Table 4–3 *Recommended MSIZE Settings for the Hammerhead-PC/104-Plus*
TBD

Accessing the SDRAM. The Hammerhead-PC/104-*Plus* supports a bank of up to 512 MB of SDRAM, which is located on the 64-bit ADSP-21160 cluster bus. The SDRAM is accessible via MS0.

Accessing the Flash Memory. The Hammerhead-PC/104-*Plus* supports a 2 MB bank of Flash memory, which is located on the 8-bit peripheral bus. The Flash memory is accessible via MS1.

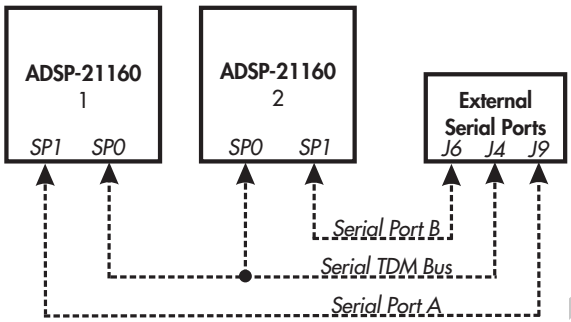
Accessing the SharcFIN ASIC. The DSPs access the SharcFIN ASIC via MS2. The SharcFIN's user-configurable registers begin at offset 0x40 from the base address of MS2.

Accessing the Dual UART. The Hammerhead-PC/104-*Plus*'s UART is located on the 8-bit peripheral bus. The DSPs access the UART via MS3.

4.2.3 Serial Port Connections

Each ADSP-21160 DSP has two 50 Mbit/sec serial ports. One serial port from each processor is connected to a TDM serial bus, which connects the processors to an external TDM serial port connector. The remaining serial port on each processor is connected to an external serial port. Figure 4–2 below shows the serial port connections on the Hammerhead-PC/104-*Plus* board.

Figure 4–2 *Block Diagram of Serial Port Connections*



Serial Port Connections to the Serial TDM Bus

SP0 on both ADSP-21160 processors is connected to external connector J4 as a TDM serial port. Dip switch S1 configures the signals on the external connector. Section 2.2.2 explains how to set the dip switch (see Figure 2–4 and Table 2–4).

Serial Port Connections to the External Serial Ports

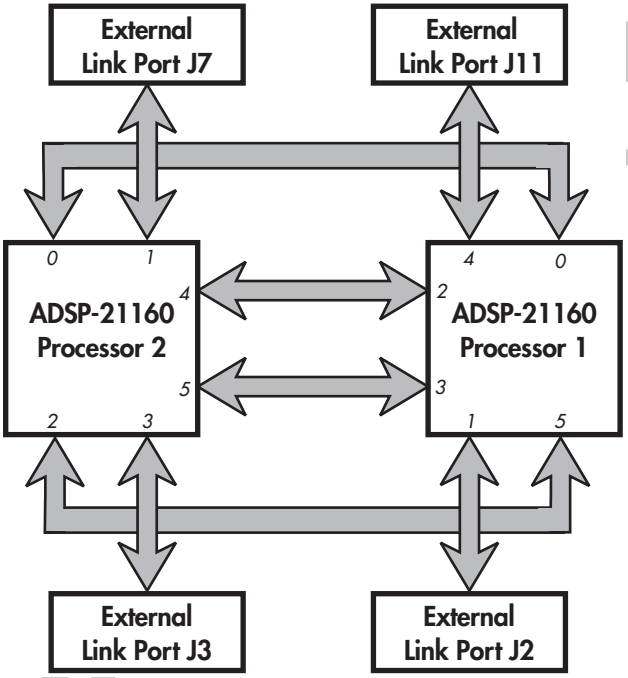
Serial port 1 on 21160-1 is connected to external connector J9 as a standard serial port. Dip switch S3 configures the external connector. Section 2.2.2 explains how to set the dip switch (see Figure 2–3 and Table 2–4).

Serial port 1 on 21160-2 is connected to external connector J6 as a standard serial port. Dip switch S2 configures this serial port. Section 2.2.2 explains how to set the dip switch (see Figure 2–3 andTable 2–4).

4.2.4 Link Port Connections

Each ADSP-21160 DSP has six 100 Mbyte/sec link ports, which allow it to communicate with the other DSP on the Hammerhead-PC/104-*Plus* board and with DSPs on other boards. Each processor has two external link ports that allow you to interface directly with other boards. Figure 4–3 below shows how the link ports on the two DSPs are connected.

Figure 4–3 *Block Diagram of Link Port Connections*

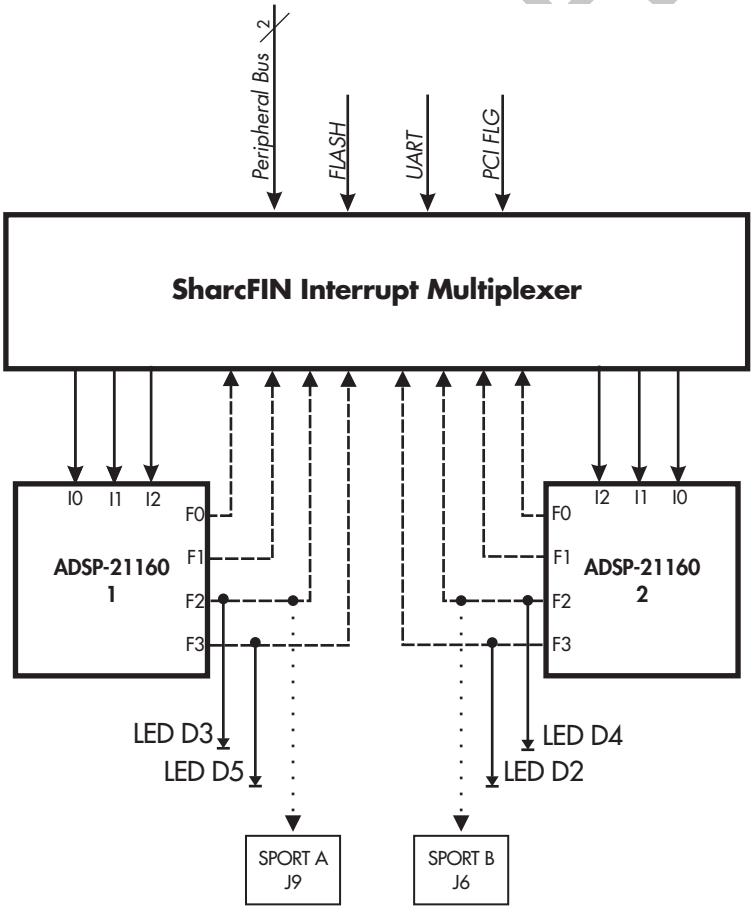


4.2.5 Flag and Interrupt Connections

Each ADSP-21160 DSP has four flags and three interrupts. This section covers the DSPs' flag and interrupt inter-processor connections and connections to the SharcFIN ASIC and LEDs.

All of the flags and interrupts from each DSP connect to the SharcFIN ASIC. Using registers in the SharcFIN, you can change the routing of those flags and interrupts (see Section 5.2.7). Figure 4–4 below illustrates the connections.

Figure 4–4 *Block Diagram of Flag and Interrupt Connections*



Flag Connections

Figure 4–4 and Table 4–4 illustrate the flag connections on the Hammerhead-PC/104-*Plus*. Each ADSP-21160 DSP has four flag signals. All four flags from each DSP connect to the SharcFIN ASIC, where you can configure their routing.Two flags from each DSP also connect to LEDs, and one flag additionally connects to an external serial port.

Table 4–4 *ADSP-21160 Flag Connections*

	21160-1	**21160-2**
FLAG0	SharcFIN*	SharcFIN
FLAG1	SharcFIN	SharcFIN
FLAG2	SharcFIN SPORT A J9 LED D3	SharcFIN SPORT B J6 LED D4
FLAG3	SharcFIN LED D5	SharcFIN LED D2

* FLAG0 – FLAG3 on each DSP connect to the SharcFIN ASIC interrupt multiplexer. From the SharcFIN, you can route them to different locations on the board.

Interrupt Connections

Figure 4–4 and Table 4–5 illustrate the interrupt connections on the Hammerhead-PC/104-*Plus.* Each ADSP-21160 DSP has three interrupts. One interrupt from each DSP is dedicated for interprocessor communication. Two interrupts from each DSP go to the SharcFIN, where you can configure their routing in the SharcFIN's configuration space. You can program the DSPs and host interface to generate and receive interrupts from the following sources:

- Flags from other ADSP-21160 DSPs
- Local interrupt from the SharcFIN ASIC, which is also programmable and has many sources (for example, the DMA channels)
- SharcFIN Mailbox registers
- Peripheral bus
- RS-232 port

Table 4–5 *ADSP-21160 Interrupt Connections*

	21160-1	21160-2
IRQ0	SharcFIN*	SharcFIN
IRQ1	SharcFIN	SharcFIN
IRQ2	SharcFIN	SharcFIN

* IRQ0 – IRQ2 on each DSP connect to the SharcFIN ASIC interrupt multiplexer. From the SharcFIN, you can route them to different locations on the board.

SharcFIN Interrupts. The SharcFIN ASIC can generate interrupts to and from the flag registers, interrupt registers, UART, peripheral bus and PCI bus. The routing of any input interrupt is user-configurable to any output.

DSP-to-Host and Host-to-DSP Interrupts. Registers in the SharcFIN's configuration space allow the host and the ADSP-21160 DSPs to generate and receive interrupts from several sources. Depending on how you configure the interrupts in the SharcFIN, each ADSP-21160 DSP will be able to receive up to three interrupts from the host, and the host will be able to receive one interrupt from the DSPs. Three flags on each DSP are available to generate interrupts to the host.

4.2.6 ADSP-21160 Cluster Bus

The Hammerhead-PC/104-*Plus* has a 64-bit, 50 MHz ADSP-21160 cluster bus that connects the two ADSP-21160 processors and a bank of up to 512 MB SDRAM. It connects to the PCI interface through the SharcFIN ASIC. The ADSP-21160 cluster bus is a 64-bit data, 32-bit address bus and uses 3.3 volt signaling. It allows transactions between the ADSP-21160s, the SDRAM, and the SharcFIN bridge.

The ADSP-21160 cluster bus has access to the secondary PCI bus via a single PCI access channel capable of reading or writing single words from the PCI bus. The reads or writes may be memory mapped, I/O mapped, or configuration operations.

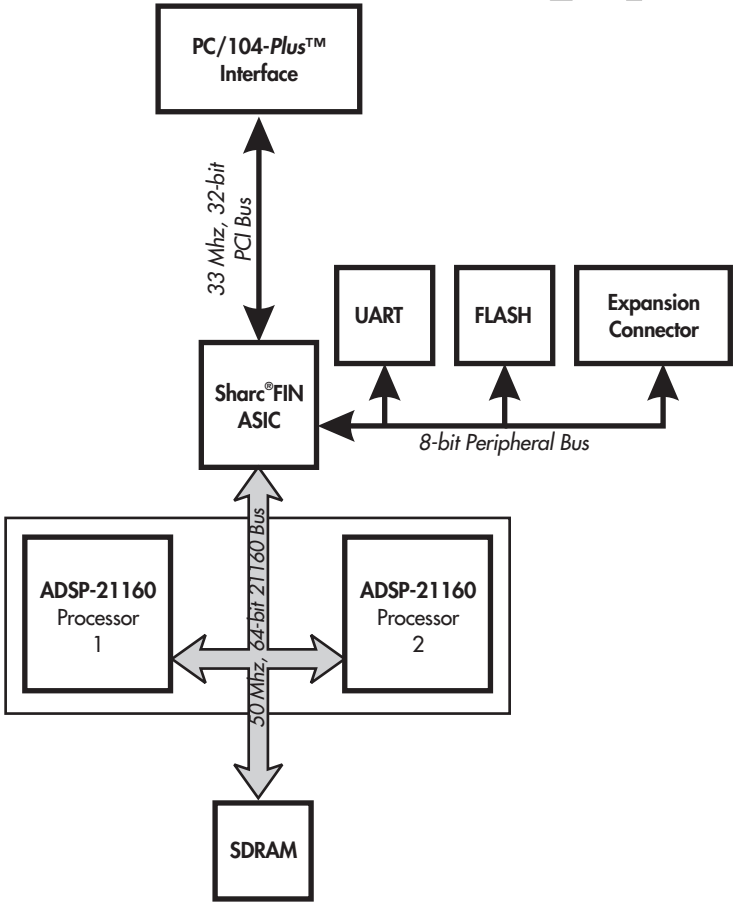
The ADSP-21160 cluster bus has access to the peripheral bus via

- BMS
- MS1
- MS3
- Unbanked memory

4.3 PCI Interface Architecture

The Hammerhead-PC/104-*Plus*'s PCI interface consists of the PCI bus, the SharcFIN ASIC, and the peripheral bus. The SharcFIN ASIC connects the 33 MHz, 32-bit PCI bus with the 50 MHz, 64-bit ADSP-21160 bus. An 8-bit peripheral bus is also connected to the SharcFIN, providing access to the Flash memory, the UART, and the expansion connector. Figure 4–5 is a diagram of the PCI interface.

Figure 4–5 *Block Diagram of the PCI Interface*



4.3.1 SharcFIN Architecture

The Hammerhead-PC/104-*Plus* features a BittWare SharcFIN ASIC. The SharcFIN interfaces the ADSP-21160 DSPs to the PCI bus, SDRAM, and devices on the peripheral bus. It also provides an interrupt multiplexer to allow you to configure the interrupt connections on the board. This section provides an overview of the SharcFIN architecture. Figure 4–6 below is a simplified block diagram of the SharcFIN architecture as it is implemented on the Hammerhead-PC/104-*Plus* board.

Figure 4–6 *Simplified Block Diagram of the SharcFIN Architecture*

Interface to ADSP-21160 Cluster Bus

The first function of the SharcFIN is to interface to the ADSP-21160 cluster bus. The SharcFIN provides a 64-bit interface to the ADSP-21160 cluster bus; it also integrates a full-featured SDRAM controller, which allows the ADSP-21160s to access SDRAM using burst mode access at sustained data rates of 400MB/sec.

Interface to PCI

The second function of the SharcFIN is to interface to PCI. The SharcFIN implements a full 32-bit/33MHz master PCI interface. The PCI interface is PCI rev 2.2 compliant and provides 16 Bytes of configurable PCI mailbox registers.

Interface to Peripheral Bus

A third bus interface is provided by the SharcFIN's peripheral bus. The peripheral bus is a general-purpose utility bus that allows easy interface to standard microprocessor peripherals such as UARTs and Flash memory. It provides a simple, glueless way to add additional functionality to the Hammerhead-PC/104-*Plus*. The SharcFIN's I^2C/serial controller integrates some of the most common peripheral requirements right into the SharcFIN. Uses include UART control, data communications, SharcFIN interconnection, as well as hardware configuration and identification.

Interrupt Multiplexer

The SharcFIN integrates an extensive interrupt and flag multiplexer to facilitate system-level control and coordination of multiprocessors. This programmable resource allows each ADSP-21160 to select the sources of its hardware interrupts; sources include other processors, PCI, peripherals, and the internal DMA engines.

4.3.2 PCI Bus Interface

The 32-bit, 33 MHz PCI bus interface connects the host to the SharcFIN ASIC, which acts as a bridge between the PCI interface and the ADSP-21160 processors.

4.3.3 Peripheral Bus Interface

The 25 MHz, 8-bit peripheral bus connects to low-speed peripherals such as the Flash RAM, the UART, and the expansion connector. The purpose of the peripheral bus is to allow additional components to communicate with the ADSP-21160s without affecting the signal quality of the ADSP-21160 bus. It connects to the SharcFIN, which interfaces it to the ADSP-21160 DSPs and the PCI interface. The peripheral bus operates at either 3.3 volts or 5 volts.

Chapter 5
Programming Details for the SharcFIN ASIC

This chapter provides programming details for the SharcFIN ASIC. It provides the information you will need when you are writing programs that allow the DSPs and the host to communicate. This section is not comprehensive. Instead, it provides only programming information that is specific to the Hammerhead-PC/104-*Plus* board. You will also need to refer to the documentation for the DSP21k-SF Toolkit, the ADSP-21160 SHARC processors, the Analog Devices development tools, and the SharcFIN ASIC.

5.1 Programming the SharcFIN PCI Interface

BittWare's SharcFIN ASIC flexibly interfaces Analog Devices' SHARC DSPs to a wide range of the Hammerhead-PC/104-*Plus*'s interfaces, including: 32/33 MHz PC/104-*Plus* bus, SDRAM, UART, I^2C serial ports, Flash, and a general-purpose expansion bus (the 8-bit peripheral bus).

The SharcFIN consists of two main sections: the first section acts as the bridge between the PC/104-*Plus* interface and the ADSP-21160 DSPs and covers the address space from 0x00 to 0x3F. The second section contains the logic for the board and several user-configurable registers, which cover the address space from 0x40 to 0x5F.

5.2 Setting the SharcFIN User-Configurable Registers

This section describes the memory locations and settings for the SharcFIN's user-configurable registers. The registers are located in the address space from 0x40 to 0x5F of the SharcFIN. All addresses described in this section are offsets from the base address of MS2 and are accessible from the ADSP-21160 DSPs and from the PC/104-*Plus* interface. Table 5–1 below gives the memory mapping for the user-configurable registers in the SharcFIN.

Note

Most of the user configurable registers are already set and do not require you to program them. You will only need to set them if you are writing your own host interface programs.

Table 5–1 *Memory Map for the SharcFIN User-Configurable Registers*

Address	Register	Read/ Write	Description
0x40	Address Override Register*	W	Allows addressing of IOP registers when Hammerhead is using a host packing mode
0x41	Status Register	R	Indicates the number of processors, ADSP-21160 cluster bus status, and last reset source
0x42	Peripheral Bus Configuration Register	R/W	Configures and shows status of wait cycles of the 8-bit peripheral bus
0x43	Watchdog Config Register	WORM†	Enables and disables the watchdog timer
0x44–45	Unused		
0x46	Onboard I^2C Control Register	R/W	Controls the I^2C™ interface
0x47	Unused		
0x48	SD Size Config Register*	W	Resets and reinitializes the SDRAM controller
0x49	SD Config Word Register*	W	Configures the SDRAM
0x4A	SD Window Register*	W	Selects which 16 MB of SDRAM the ADSP-21160 DSPs will view
0x4B	UART Interface Register	R/W	Allows communication with on-board UART
0x4C–4F	Unused		
0x50–54	H1I0, H1I1, H2I0, H2I1, H1I2	R/W	Configure ADSP-21160 DSPs' interrupts; show status of interrupts
0x55	Unused		
0x56	H212	R/W	Configure ADSP-21160 DSPs' interrupts; show status of interrupts
0x57	Unused		
0x58	PCInt	R/W	Configures PCI interrupts
0x59	Unused		
0x5A–5D	Unused		
0x5E	Flags	R	Shows state of all flags
0x5F	IRQ	R	Shows state of all interrupts

* Use with caution.
† Write Once Read Many

5.2.1 Setting the Address Override Register

The Address Override Register configures how the ADSP-21160 DSPs access the least significant 32 bits on the ADSP-21160 cluster bus. It allows access to the DSPs' IOP space before the SYSCON register has been configured.

Note

Only use this register if you are writing your own host interface programs.

Table 5–2 *Contents of the Address Override Register*

Bit	Name	Description
B0	A0 Override En	Address override enable for booting across the PCI bus
B1	Overridden A0	Overridden address
B2	Bus Lock Request	Requests that SharcFIN acquire the ADSP-21160 cluster bus and not give it up
B3	Destructive FIFO Read Enable	When B3=1, a read to the DMA FIFOs causes the FIFOs to advance. When B3=0, a read to the DMA FIFOs does not cause the FIFOs to advance.

Setting the Address Override Bits

The Address Override bits B0 and B1 should not be used under normal setup conditions. If the Hammerhead-PC/104-*Plus* is being run in standalone mode and you are booting across the PCI bus, then the bits can be changed. However, extreme caution should be exercised as data loss or corruption will occur if the bits are improperly set.

Setting the Bus Lock Request Bit

The Bus Lock Request bit allows the SharcFIN to acquire the ADSP-21160 bus and locks access to the bus so that only the SharcFIN can access it. Table 5–3 shows the settings for B2, the Bus Lock Request bit.

Table 5–3 *Bit Settings for the Bus Lock Request Bit (B2)*

B2 Setting	Description
0	Disabled
1	Requests that the SharcFIN acquire the ADSP-21160 bus and not give it up

5.2.2 Reading the Status Register

The Status Register is a 16-bit read only register that gives information about various features on the board.

Table 5–4 *Contents of the Status Register*

Bit	Name	Description
B0	HHPres0	Combined settings of B0 and B1 indicate how many processors are installed on the board
B1	HHPres1	
B2	Bus Locked	Indicates whether the SharcFIN has locked and acquired the ADSP-21160 bus
B3	Last Reset Source	Indicates whether the PC/104-*Plus* interface or the watchdog was the source of the last board reset
B4	SPCI Done	Refer to QL5064 documentation for details
B5	RCV0_FIFO_EF	Receive FIFO 0 Empty Flag; refer to QL5064 documentation for details
B6	RCV1_FIFO_EF	Receive FIFO 1 Empty Flag; refer to QL5064 documentation for details

Determining How Many Processors are Installed on the Board

B0 and B1 of the Status Register show how many processors are on the Hammerhead-PC/104-*Plus* board. Table 5–5 shows their combined settings.

Table 5–5 Settings for the Processor Bits

B0	B1	Description
0	0	1 processor
1	0	2 processors
0	1	Reserved
1	1	Reserved

Determining Whether the ADSP-21160 Bus is Locked

B2, the Bus Locked bit, shows whether the processors on the board have granted ownership of the ADSP-21160 cluster bus to the SharcFIN. Table 5–6 below shows the settings for the Bus Locked bit.

Table 5–6 Bit Settings for the Bus Locked Bit

B2 Setting	Description
0	ADSP-21160 bus is not locked
1	ADSP-21160 bus is locked

Determining the Last Reset Source

B3, the Last Reset Source bit, shows whether the PC/104-*Plus* interface or the watchdog timer was the source of the last board reset. Table 5–7 below shows the settings for the Last Reset Source bit.

Table 5–7 Bit Settings for the Last Reset Source Bit

B3 Setting	Description
0	PC/104-*Plus* reset
1	Watchdog reset

5.2.3 Setting the Peripheral Bus Configuration Register

The Peripheral Bus Configuration Register allows you to configure the wait cycles of the Hammerhead-PC/104-*Plus*'s 8-bit peripheral bus.

Table 5–8 *Contents of the Peripheral Bus Configuration Register*

Bit	Name	Description
B0–B3	PC/104-*Plus* to Pbus Wait	Select the number of wait cycles the SharcFIN will wait before completing a transaction on the peripheral bus
B4	Pbus Ack Enable	Selects whether the SharcFIN will monitor the peripheral bus Ack line after the peripheral bus wait time has expired
B5	Pbus Reset	Resets the peripheral bus reset line, the Flash, and the UART

Selecting the Number of Wait Cycles

B0 – B3 set the number of wait cycles the SharcFIN must wait before completing a transaction on the peripheral bus. The actual value of wait cycles is one greater than the value in the register (for example, if the register value = 0, the number of wait cycles = 1). Table 5–9 shows the settings for the bits.

Table 5–9 *Default Setting for Selecting the Number of Wait Cycles*

B0	B1	B2	B3	Description
1	0	1	0	6 wait cycles

Enabling the Peripheral Bus Ack Line

The setting of the Pbus Ack Enable bit (B4) determines whether the SharcFIN will wait five wait cycles and then monitor the peripheral bus Ack line or whether it will wait five wait cycles and then consider the transaction complete. Table 5–10 gives the settings for the Pbus Ack Enable bit.

Note

Five wait cycles is the minimum amount of wait cycles required to talk to the Flash memory.

Table 5–10 *Settings for the Pbus Ack Enable Bit*

B4	Description
0	SharcFIN will wait the selected number of wait cycles and consider the transaction complete
1	SharcFIN will wait the selected number of wait cycles and then monitor the Ack line

Setting the Peripheral Bus Reset Bit

When set to 1, B5, the Peripheral Bus Reset bit, resets the Flash, the UART, and all devices on the peripheral bus. The reset stays active until cleared by another write to the register. You can also reset the Flash, the UART, and all devices on the peripheral bus via a board reset.

5.2.4 Setting the Watchdog Configuration Register

The Watchdog Configuration Register is a WORM (Write Once Read Many) register that allows you to enable or disable the watchdog timer, set its time-out time, and select which processor will reset its timer. Once the watchdog is enabled, it can not be disabled except by a board reset, which can be from the PCI interface, the watchdog, or an external source.

Table 5–11 *Contents of the Watchdog Configuration Register*

Bit	Name	Description
B0	WatchdogEn0	Enable the watchdog timer and select its time-out time
B1	WatchdogEn1	
B2–B3	Unused	
B4–B5	H1F0 En, H2F0 En	Select which processor will strobe the watchdog timer

Enabling the Watchdog and Setting its Time-out

B0 and B1 enable and disable the watchdog and set its time-out time.Table 5–12 below shows their settings.

Table 5–12 *Settings for the Watchdog Enable Bits*

B0	B1	Description
0	0	Disabled
0	1	Enabled; short time-out (200 ms)
1	0	Enabled; medium time-out (600 ms)
1	1	Enabled; long time-out (1.2 s)

Selecting the Processor to Run the Watchdog

B4–B7 select the processor that will run the watchdog.You can select more than one processor, but it is not recommended. Table 5–13 shows the settings for B4–B7.

Table 5–13 *Settings for the Processor Selection Bits*

B4	B5	B6	B7	Description
1	0	0	0	21160-1 FLAG0 will strobe the watchdog timer
0	1	0	0	21160-2 FLAG0 will strobe the watchdog timer
0	0	1	0	Reserved
0	0	0	1	Reserved

5.2.5 Setting the Onboard I²C Control Register

The Onboard I²C Control Register controls the I²C interface. The I²C interface is a two-wire bus; one wire is a clock signal and the other is a data signal. Both the clock and the data lines are pulled up. Table 5–14 below shows the contents of the register.

As per standard I²C, both the clock and data lines are pulled high. Devices on the I²C bus either do not drive the bus or they drive it low. Any device on the I²C bus can drive either the clock or data line low when required. You can also read the actual status of the lines.

Table 5–14 *Contents of Onboard I²C Control Register*

Bit	Name	Description
B0	Clock	Read/Write; on write, drives the clock line. On read, shows the state of the clock line
B1	Data	Read/Write; on write, drives the data line. On read, shows the state of the data line

When you write a 1 to either the clock or data line in this register, the SharcFIN does not drive the corresponding line. When you write a 0 to either the clock or the data line, the SharcFIN drives the corresponding line to 0. When you read either line, you read the actual state of the line rather than what you have written to it. If you are not driving the line, it will be 0 if another device is driving it and 1 if nothing is driving it. Table 5–15 below shows the effect of the values written to the Clock and Data bits.

Table 5–15 *Settings for Writing the Clock and Data Bits*

Value Written	Description
0	Drives the line low; when read back, shows 0
1	When read back, shows the actual state of the I²C line

5.2.6 Configuring the SDRAM

The SharcFIN contains three registers that configure the SDRAM:

- the SDRAM Size Configuration Register
- the SDRAM Configuration Word Register
- the SDRAM Window Register

Setting the SDRAM Size Configuration Register

The SDRAM Size Configuration Register sets the size of the SDRAM. The settings for this register depend on the type of SODIMM modules used on the board. Table 5–16 below shows the contents of the register.

Table 5–16 *Contents of the SDRAM Size Configuration Register*

Bit	Name	Description
B0	SD Bank Size 0	Sets the size of SDRAM bank 0
B1	SD Bank Size 1	Sets the size of SDRAM bank 1
B2	SD RF Size	
B3	SD Reset*	Resets the SDRAM controller and reinitializes the SDRAM

* Do not change this bit.

Setting the SDRAM Configuration Word Register

The SDRAM Configuration Word Register configures the SDRAM. This register is already set with appropriate settings. User modification should not be required.

Warning!

Do not change the value of this register. BittWare's Host Interface Library sets the value of these bits upon reset. Modifying this register will cause the SDRAM not to function properly.

Setting the SDRAM Window Register

The SDRAM Window Register lets you select which 16 MB section of memory in the SDRAM to view from the host over the PC/104-*Plus* interface. However, you will not need to configure this register since the Diag21k utility, which is included with the DSP21k-SF Toolkit, will take care of setting these bits. Table 5–17 lists the bits included in this register.

Table 5–17 *Contents of the SDRAM Window Register*

Bit	Name	Description
B0	Window A0	Selects window A0 of the SDRAM
B1	Window A1	Selects window A1 of the SDRAM
B2	Window A2	Selects window A2 of the SDRAM
B3	Window A3	Selects window A3 of the SDRAM
B4	Window A4	Selects window A4 of the SDRAM

5.2.7 Configuring the ADSP-21160 and PCI Interrupts

The registers from offset 0x50 to 0x5B configure the direction of the ADSP-21160 and PCI interrupts and show their status. Each register is identical except that each one corresponds to a different interrupt on the PCI interface or ADSP-21160 processors. Table 5–18 shows which register corresponds to which interrupt.

Table 5–18 *ADSP-21160 Interrupt Configuration Registers*

Address	Register	Description
0x50	H1I0	Configures the direction of 21160-1 IRQ0
0x51	H1I1	Configures the direction of 21160-1 IRQ1
0x52	H2I0	Configures the direction of 21160-2 IRQ0
0x53	H2I1	Configures the direction of 21160-2 IRQ1
0x54	H1I2	Configures the direction of 21160-1 IRQ2
0x55	Unused	
0x56	H2I2	Configures the direction of 21160-2 IRQ2
0x57	Unused	
0x58	PCInt	Configures the direction of the PCI interrupt
0x59	Unused	
0x5A–5B	Unused	

The registers are 32-bit registers. The first 16 bits (0–15) are read/write and select the source that will generate an interrupt to the processor. The second 16 bits (16–31) are read only and show which of the enabled interrupts are generating an interrupt. Bits 16–31 are masked interrupt lines and are masked by 21160-1 IRQ0's interrupt mask. Table 5–19 shows the bits included in each register.

Table 5–19 *Settings for the Interrupt Configuration Registers*

Bit	Name	Description*
B0	H1F0	The interrupt will respond to 21160-1 FLAG0
B1	H1F1	The interrupt will respond to 21160-1 FLAG1
B2	H2F0	The interrupt will respond to 21160-2 FLAG0
B3	H2F1	The interrupt will respond to 21160-2 FLAG1
B4–B7	Unused	
B8	PCFlg	The interrupt will respond to a flag from the PCI interface
B9–B10	Unused	
B11	PRFlg	The interrupt will respond to a flag from the peripheral bus
B12	UART0	The interrupt will respond to UART0
B13	UART1	The interrupt will respond to UART1
B14–15	Unused	
B16	H1F0	21160-1 FLAG0
B17	H1F1	21160-1 FLAG1
B18	H2F0	21160-2 FLAG0
B19	H2F1	21160-2 FLAG1
B20–B23	Unused	
B24	PCFlg	PCI flag
B25–B26	Unused	
B27	PRFlg	Peripheral bus flag
B28	UART0	UART0 flag
B29	UART1	UART1 flag
B30–31	Unused	

* All descriptions in this column apply when bits are set to 1.

5.2.8 Reading the Status of All Flags and Interrupts

The registers at offsets 0x5E and 0x5F are 16-bit unmasked registers that show the status of all flags and interrupts. The register at 0x5E shows the status of the flags, and 0x5F shows the status of the interrupts. Table 5–20 and Table 5–21 describe the bits in the registers.

Table 5–20 *Reading the Status of the Flags*

Bit	Name	Description*
B0	H1F0	Status of 21160-1 FLAG0
B1	H1F1	Status of 21160-1 FLAG1
B2	H2F0	Status of 21160-2 FLAG0
B3	H2F1	Status of 21160-2 FLAG1
B4–B7	Unused	
B8	PCFlg	Status of PCI flag
B9–B10	Unused	
B11	PRFlg	Status of peripheral bus flag
B12	UART0	Status of UART0 flag
B13	UART1	Status of UART1
B14–15	Unused	

* All descriptions in this column apply when bits are set to 1.

Table 5–21 *Reading the Status of the Interrupts*

Bit	Name	Description*
B0	H1I0	Status of 21160-1 IRQ0
B1	H1I1	Status of 21160-1 IRQ1
B2	H2I0	Status of 21160-2 IRQ0
B3	H2I1	Status of 21160-2 IRQ1
B4–B7	Unused	
B8	PCInt	Status of PCI interrupt
B9–B10	Unused	
B11–15	Unused	

* All descriptions in this column apply when bits are set to 1.

Appendix A
Debugging Your DSP Programs

This appendix provides information on debugging DSP programs with either a hardware or a software emulator.

A.1 Debugging with a Hardware (In-Circuit) Emulator

This section discusses attaching an in-circuit emulator (ICE) from White Mountain DSP to the Hammerhead-PC/104-*Plus* board. To attach an ICE to the Hammerhead-PC/104-*Plus*, follow the steps below:

1. Connect the probe on the ICE card to the Hammerhead-PC/104-*Plus*'s JTAG connector.
2. Depending on the type of ICE you are using, either install it in or connect it to your PC.
3. Set up the Hammerhead-PC/104-*Plus* for operation.
4. Apply power to the Hammerhead-PC/104-*Plus*.
5. Start the emulator software on the PC.

A.1.1 Overview of the ICE Emulator

The Hammerhead-PC/104-*Plus* is compatible with White Mountain DSP's ICE emulators, which are separate ISA bus, PCI bus, Ethernet, or USB cards that connect to the Hammerhead-PC/104-*Plus*'s JTAG connector and connect to your PC. The emulator provides a controlled environment for observing, debugging, and testing real-time activities in a target hardware environment by connecting directly to the target processor through its JTAG interface.

When the ICE is attached to the Hammerhead-PC/104-*Plus*, the Hammerhead-PC/104-*Plus* becomes the target system for the emulator, allowing you to operate it completely from the emulator's user interface. A powerful tool for debugging

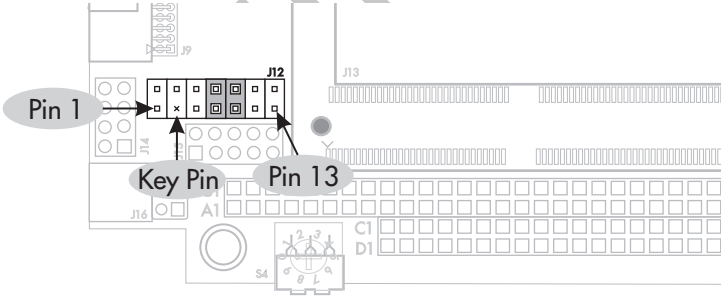
programs running on the ADSP-21160 processors, the emulator monitors system behavior while running at full speed, and you can use it to download programs, start and stop program execution, set breakpoints, and observe and change the contents of the registers and memory.

A.1.2 Attaching the ICE to the Hammerhead-PC/104-*Plus*

To attach the ICE to the Hammerhead-PC/104-Plus, follow the instructions below.

1. Locate the JTAG connector (J12) on the Hammerhead-PC/104-*Plus* (see Figure 3–3).
2. A cable extends from the ICE card to a probe that connects to the JTAG connector on the Hammerhead-PC/104-*Plus*. Connect the ICE probe to the JTAG connector. Figure A–1 shows the location of the pins on the connector.

Figure A–1 *JTAG Connector*



Pin 3 on the JTAG connector is missing (see Figure A–1) to prevent you from installing the emulator incorrectly. One of the sockets in the ICE probe has a plug inserted in place of the pin. Table 3–10 in Chapter 3 shows the connector pinout.

A.1.3 Installing the ICE and Hammerhead-PC/104-*Plus* In a PC

Once you have connected the ICE to the Hammerhead-PC/104-*Plus*, install the emulator in your host computer. The install procedure for the emulator depends on the platform you are using: ISA, PCI, Ethernet, or USB. Refer to the *Emulator Hardware and Software Installation Guide* from Analog Devices for instructions on installing the emulator.

A.1.4 Operating the ICE

To start operating the ICE with the Hammerhead-PC/104-Plus,

1. Apply power to the Hammerhead-PC/104-*Plus*.

Note

As long as the emulator software is not running, you can safely attach and remove the ICE probe while the Hammerhead-PC/104-Plus is running.

2. Start the emulator software on your PC. To download and run programs, follow the instructions in the ICE documentation.

A.2 Debugging with a Software Emulator

BittWare's VisualDSP Target is a fully functional software emulator, which allows you to debug your DSP projects right on your BittWare board without installing a hardware (in-circuit) emulator.

A.2.1 About the VisualDSP Target

If you have installed Analog Devices' VisualDSP integrated development environment (IDE), you can use BittWare's VisualDSP Target to debug your DSP programs. BittWare's VisualDSP Target is a plug-in to ADI's VisualDSP that allows the VisualDSP debugger to communicate directly with your BittWare DSP board.

Since the BittWare VisualDSP Target is integrated right into the VisualDSP debugger, you can compile and link your code in the VisualDSP integrated development environment and immediately debug your code directly on the BittWare board. A full-featured software debugger, the VisualDSP Target allows you to set breakpoints, single-step through your code, view memory, and run code on multiple processors.

A.2.2 Installing the VisualDSP Target

To install the VisualDSP Target, insert the VisualDSP Target CD-ROM into your computer's CD-ROM drive, and follow the installation instructions on the screen. Once you have installed the Target, follow the instructions in the *VisualDSP Target User's Guide* to prepare your DSP program for debugging.

Appendix B
Setting Up for Standalone Operation

The Hammerhead-PC/104-*Plus* can boot from a boot program stored in its Flash memory, which allows it to operate in standalone mode, free from a host computer. This section lists the steps necessary to prepare your Hammerhead-PC/104-*Plus* board to operate in standalone mode.

To prepare the Hammerhead-PC/104-Plus to operate in standalone mode,

1. While in development mode, develop a boot loader and a standalone operating program for the DSPs (see B.1.1).
2. Program the Flash with the boot loader and standalone operating program (see B.1.2).
3. Place a jumper on Standalone Mode JP3 to operate the board in standalone mode (see B.1.4.).
4. Power down and set the Hammerhead-PC/104-*Plus*'s boot mode to "Flash boot" (see B.1.5).
5. Mount standoffs on the board (see B.2).
6. Apply an external power source to the board (see B.3).
7. Boot the board in Flash boot mode.

B.1 Booting the Hammerhead-PC/104-*Plus* in Standalone Mode

When operating in stanadalone mode, the Hammerhead-PC/104-*Plus* boots from a boot program stored in its Flash memory

B.1.1 Developing the Boot Program

Use the Analog Devices software development tools and BittWare's host interface tools (DSP21k-SF Toolkit) to develop a boot program for the ADSP-21160 processors. The example software included with the Hammerhead-PC/104-*Plus* includes example programs that demonstrate how to create a DSP program in the proper form and then load it into Flash memory so that it automatically boots and begins executing after the board is powered on or the DSPs are reset.

B.1.2 Loading a Boot Program into the Flash Memory

Use programs provided with the Hammerhead-PC/104-*Plus* to load the Flash memory with a boot program.

B.1.3 Testing the Boot Program

The `flash` directory contains utilities and a test program that uses the utilities. These programs provide easy access to the Flash memory on the Hammerhead-PC/104-*Plus* board.

B.1.4 Setting the Standalone Mode Jumper

To operate the board in standalone mode, the standalone mode jumper JP3 must be installed. Place the jumper across the two pins of JP3. See Figure 2–1 on page 13 for the location of the pins.

B.1.5 Setting the Boot Mode to Flash Boot

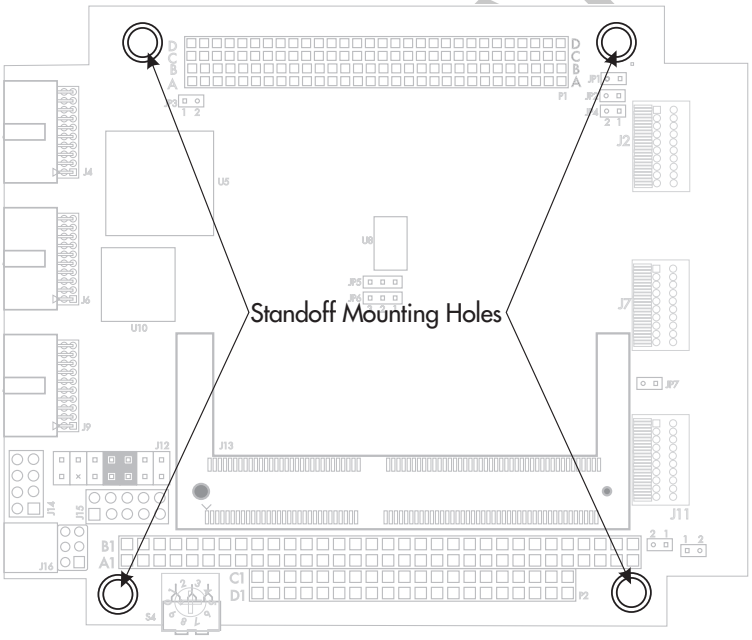
To operate in standalone mode, the Hammerhead-PC/104-*Plus* must be set to boot from a boot program stored in the on-board Flash memory. Configuration jumpers JP5 and JP6 allow you to select the Hammerhead-PC/104-*Plus*'s boot mode (see section "Setting the Hammerhead-PC/104-Plus Configuration Jumpers" on page 13 for instructions).

B.2 Mounting Standoffs on the Board

If you are not mounting the Hammerhead-PC/104-*Plus* on a PC/104-*Plus* carrier board (see section 2.4), mount standoffs on the board to provide proper support and adequate clearance between the bench and the Hammerhead-PC/104-*Plus*'s components.

1. Place a ¼" standoff in each of the four standoff mounting holes on the Hammerhead-PC/104-*Plus*. Figure B–1 shows where the holes are located.
2. Secure each standoff with a ¼" screw.

Figure B–1 *Location of the Standoff Mounting Holes*



B.3 Connecting an External Power Supply

When operating in standalone mode, the Hammerhead-PC/104-*Plus* requires a +5V power source. The external power connector (J1) supplies +3.3V, +5V and GND to the Hammerhead-PC/104-*Plus*. Section 3.2.2 gives the pinout of the connector and shows where it is located.

To connect an external power source to the Hammerhead-PC/104-*Plus*,

1. Plug a power adapter cable into the Hammerhead-PC/104-*Plus*'s external power connector (J1). Be sure to align pin 1 (+5V) on the cable with the +5V pin on J1.
2. Connect the remaining end of the cable to an external power source, such as a switching standalone power supply or the PC's power supply.
3. Apply power to the system.
4. Reset the Hammerhead-PC/104-*Plus* (see section 2.6).

Appendix C
Troubleshooting Tips

This section lists the information you will need to have ready before calling technical support at BittWare. It also provides the telephone number and email address for BittWare technical support.

C.1 Before You Call Technical Support

To allow us to serve you better, please perform the following checks and record any significant results before contacting BittWare for assistance.

- Run DspBad on the board and note the results.
- Run Diag21k on the board; enter **`br`** at the first prompt, **`pc`** at the next, and then initiate memory tests by entering **`mt aa`**.
- Try re-installing the tools and checking your path if you are getting "file not found" or similar errors.
- Try changing the hardware to see if the problem tracks with the board or the PC:
  - If you have access to a different board, please try it.
  - Try the board in a different PC.
  - Try a different operating system.
- Finally, when contacting BittWare, please have the results of these tests and the following information ready:
  - Information identifying the hardware and software you purchased (see the BittWare packing list)
  - Which operating system you are using: DOS, Windows 3.1, Windows 95/98, Windows 95B (OSR2), Windows NT Version 3.51, Windows NT Version 4.0, Windows 2000, or Linux

- The release number of your DSP21k Toolkit (enter **`diag21k -v`** at a DOS prompt)

- If you could be at the PC with problems when making the call, we would better be able to start investigating the problem.

C.2 Contacting Technical Support

You can reach technical support at BittWare, Inc. using one of the following methods:

- Phone (8:30am – 5:30pm ET): (603) 226-0404
- FAX: (603) 226-6667
- E-mail: support@bittware.com

Bittware also maintains the following internet sites:

http://www.bittware.com	Contains product information, technical notes, support files available for download, and answers to frequently asked questions (FAQ).
ftp://ftp.bittware.com	Contains technical notes and support files. Login as "anonymous" and use your email address for the password.