Channel Coding

FPGA based DVB-T transmitter

| Revision | Date | Description | Author |
| --- | --- | --- | --- |
| 0.1 | 06/2010 | Initial Draft | Juan Gago |
| 0.2 | 07/2010 | Functional RTL simulations | Juan Gago |
| 1.0 | 09/2010 | Gate Level simulations | Juan Gago |
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Table 1 Revision history

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# 1. Introduction

* mux adaptation and energy dispersion
* outer encoder (Reed Solomon)
  + outer\_rdy = inner\_rfd
* outer interleaver
* inner coder = f (FEC)
* resampler = f (QAM)
  + Only implemented for the non-hierarchical case.
  + Not included in the channel coder
  + fft\_rfd: used as ready input at the output fifo of that resampler (***source\_rdy***)

sourcebit

Coding   
FEC: = 34

sinkbyte

s

valid

valid

sop,eop

sop,eop

ready

FIFO

wr

rd

**Resampler**

sourcebit

valid

fft\_rdy

x0 → b0,0x1 → b2,0x2 → b4,0x3 → b1,0x4 → b3,0x5 → b5,0

# 2. RTL Design

#### **Multiplex Adaptation + Randomization for Energy Dispersion**

Multiplex Adapter

sinkbyte

sourcebyte

valid

valid

ready

ready

Implementation

* A FSM loads the initial sequence of the PRBS generator at the beginning of each eight TS packets.

PRBS\_INIT\_SEQUENCE (14 downto 0) := B"0000\_0001\_0101\_001"

* Additionally to the FSM, other resources are included

Table 2 Multiplex adapter resources

|  |  |
| --- | --- |
| **Counters-based FSM:** | **Input / Output Interface:** |
| TS – packet counter (1:8) Byte counter (1:188) Bit counter (1:1504) | Byte Serializer: parallel byte to 8 serial bits Bit Parallelizer: 8 serial bits to parallel byte FIFO to interface the RS encoder (***sink\_rdy***) |

Byte Serializer

mux\_adapter.vhd

FIFO

wr

rd

Byte Pa-rallelizer

Output Generator

FSM

**PRBS Generation**

#### **Outer Encoder (Reed Solomon)**

Outer Encoder

sinkbyte

sourcebyte

valid

valid

sop,eop

sop,eop

ready

ready

Implementation

* Startofpacket, Endofpacket (sink and source) exported to the top design
* 204 -188 = 16 bytes
* Based on the altera megafunction (auk\_rs\_enc\_top\_atl)

#### **Outer Interleaver**

Outer Interleaver

sinkbyte

sourcebyte

valid

valid

Implementation

* Forney + Rasmsey approximation with I = 12.
* Other parameters of the approximation:

N = 204 bytes (periodicity);  
M = N/I = 17 registers;

FIFO (j) = j × M bytes where j = 0:11

* There is a memory inside which length is estimated in 2048 bytes:

outer\_memo = 17×0 + 17×1 +... + 17×11 = 1122 bytes > 1024 bytes

* Back pressure is not used in this component (bypass)

outer memo

2

outer\_interleaver.vhd

#### **Inner Coder = f (FEC)**

Inner Encoder  
generic FEC : natural := 34

sinkbyte

sourcebit

valid

valid

ready

ready

Implementation

* “Convolutional Encoder” LogiCore used in the Xilinx version of the core.
* RTL design in the Altera version. Patterns:

|  |  |
| --- | --- |
| Pattern X = "0000001" when FEC = 23;  Pattern Y = "0000011" when FEC = 23; | Irate = FEC rem 10; -- input rate  Orate = FEC mod 10; -- output rate |

Table 3 Generator

|  |  |  |
| --- | --- | --- |
| **Output** | **Generator (Octal)** | **Generator (Binary)** |
| **X** | G1 = 171 | G1 = 1111001 |
| **Y** | G2 = 133 | G2 = 1011011 |

inner\_coder.vhd

FIFO

wr

rd

**Convolutional  
Encoder**

rfd