DVB-T core

User guide

| Revision | Date | Description | Author |
| --- | --- | --- | --- |
| 0.1 | 06/2010 | Initial Draft | Juan Gago |
| 0.2 | 07/2010 | Functional RTL simulations | Juan Gago |
| 1.0 | 09/2010 | Gate Level simulations | Juan Gago |
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# Introduction

This document details the DVBT IP core testbench. The testbench currently covers the following core features:

#### Entrada

* SPI (es el MPEG-TS más sencillo) 27.99 Mbps

#### Parámetros de Codificación

* Ancho de banda de canal 8 MHz
* Modo de transmisión OFDM 2K
* Relación de codificación FEC 3/4
* Numero de portadoras 1512
* Constelación QAM 64-QAM uniforme (α = 1)
* Período Elemental (T) 7/64 useg
* Período de Símbolo Útil (Tu) 2048\*T
* Espaciado entre portadoras 1/Tu
* Espaciado entre la 1ª y la última portadora 7.61 MHz
* Intervalo de guarda (Δ) 0
* Ts = Tu + Δ 2048\*T

#### Salida

* IQ Modulator 9.143 MHz
* Up - Sampling 64 MHz
* Frecuencia Intermedia 16 MHz
* Automatic Control Gain 18 bits
* Complex DAC 18 bits

La norma ETSI EN300744 sólo habla de modulación del flujo TS de entrada en banda base con los siguientes valores:

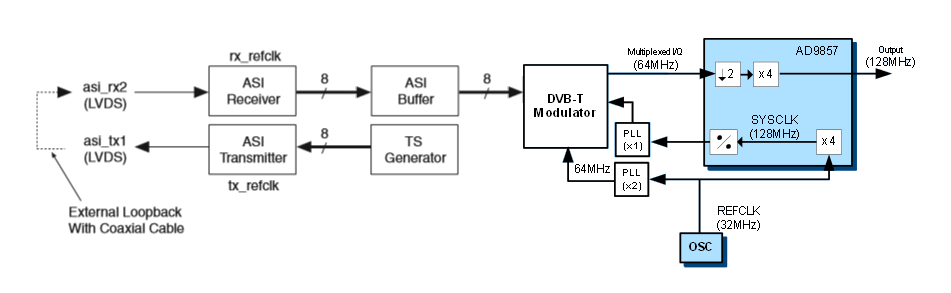
* Frecuencia de Reloj (F\_CLOCK) 64 MHz
* Período Elemental (T) 7/64 useg
* Frecuencia de Símbolo (F\_SYMBOL) 64/7 MHz

# Testbench

The testbench consists in a DVBT IP Core connected to some external cores. There is a source of MPEG packets feeding the DVBT IP core.

* MPEG packet
  + mpeg\_rdy = outer\_rfd
* channel coding = f(FEC)
  + outer\_rdy = inner\_rfd
  + fft\_rfd: used as source\_rdy of the resampler
* data carriers gen = f(QAM,OFDM)
  + fft\_rfd: used as chip-enable
* baseband = f(OFDM, GI)
  + baseband\_rdy = interpolator\_rfd and 9143 KHz divider
* interpolator (I, Q)
  + interpolator\_rdy = ‘1’

The testbench is shown in the figure.

****

**Figure 1 DVBT Testbench**

This testbench is located at the /sim folder. The associated files are

* dvbt\_core\_tb.vhd: testbench with the instantiation of cores and generators.
* pipeline\_2k.vho:
* filter\_64M.vho:
* contador7x.vhd: divider to generate a 9,143 kHz clock-enable
* up\_package.vhd:

# External MegaCore Functions

## **ASI Receiver**

## **Baseband**

Baseband

init

xk\_re (16)

xn\_re(16)

xk\_im (16)

xn\_im (16)

valid

valid

sop,eop

sop,eop

ready

ready

#### 

#### Implementation

* Chosen parameters
  + length ≤ 8192 points
  + 16 bit input data width (signed)
  + output: scaled, convergent rounding, cpv

baseband.vhd

FIFO

wr

rd

**Fast Fourier  
Transform**

rfd

## **Interpolator**

Interpolator

data\_out(16)

data\_in (16)

ready

valid

valid

#### 

#### Implementation

* FIR Filters:

    49 taps (7 x 7)   
    fc = 4.4 MHz  
    16 bit input data width (signed)  
    33 bit output data width (full precision)  
 nd, rfd protocol (input interface)

* FIR Coefficients  
    
      fichero.coe con 4 decimales (signed)  
      16 bit width (max dynamic range quantization)

**Fir  
64 MHz**

rfd

9143 KHz  
Divider

interpolator.vhd

## **Quadrature Upconverter**

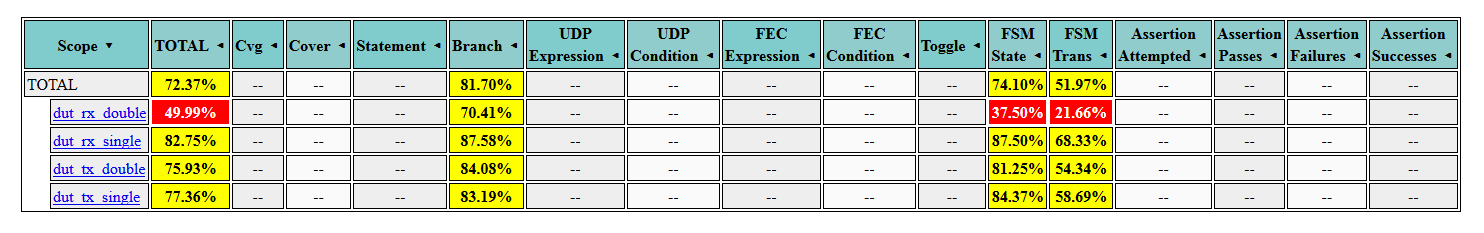
# Simulation

## **Standard Procedure**

* Open the file **sim.mpf** at the /sim folder
* Create the working design library. Type at the modelsim> prompt
  + vlib work; vmap work work
* In the Project window select Compile > Compile All from the pop-up menu
* Click on **dvbt\_core** to load the design
* Add all signals to the Wave window. Type at the vsim> prompt
  + add wave -r sim:/dvbt\_core\_tb/\*; run -all
* Verify the transmitted

## **Code Coverage Report**

* Open the project and compile the sources. Type at the modelsim> prompt
  + do dvbt\_exclusions.do
* Click on **dvbt\_sim\_coverage** to load the design
* Run the simulation
* Select Tools > Coverage Report > HTML from the Main window menu bar



# References

[AN344] ASI Demonstration Application Note

[UG\_RSII] Reed-Solomon II MegaCore Function

[UG\_FFT] FFT MegaCore Function

[UG\_FIR] FIR Compiler

[AD9857] Quadrature Digital Upconverter