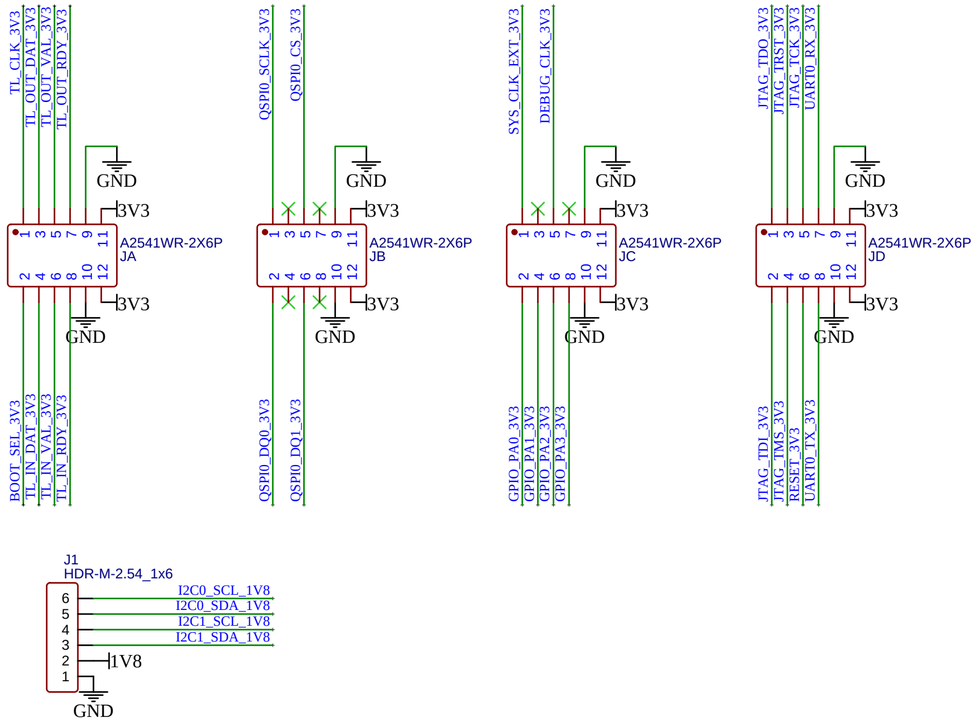
Arty PMOD Connectors

JA and JD are standard IO connectors

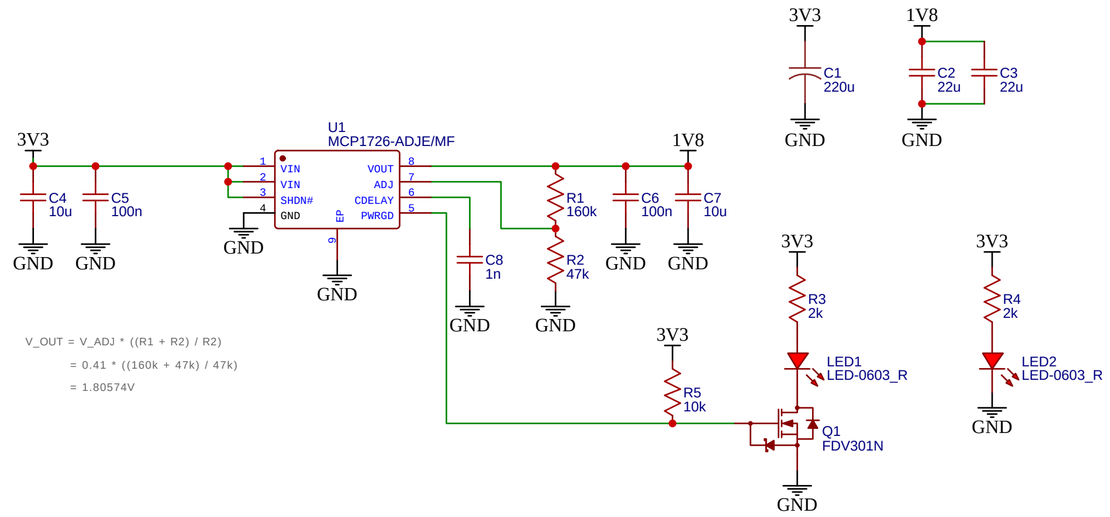
JB and JC are high speed IO connectors. We are running single ended signal here, so the negative side is left unconnected.

GPIOs are relativly low speed and more robust to crosstalk, so we are running it all through JC. Worst case, we just pull PA1 and PA3 to GND.

Reference: https://digilent.com/reference/programmable-logic/arty-a7/reference-manual#usb-uart_bridge_serial_port

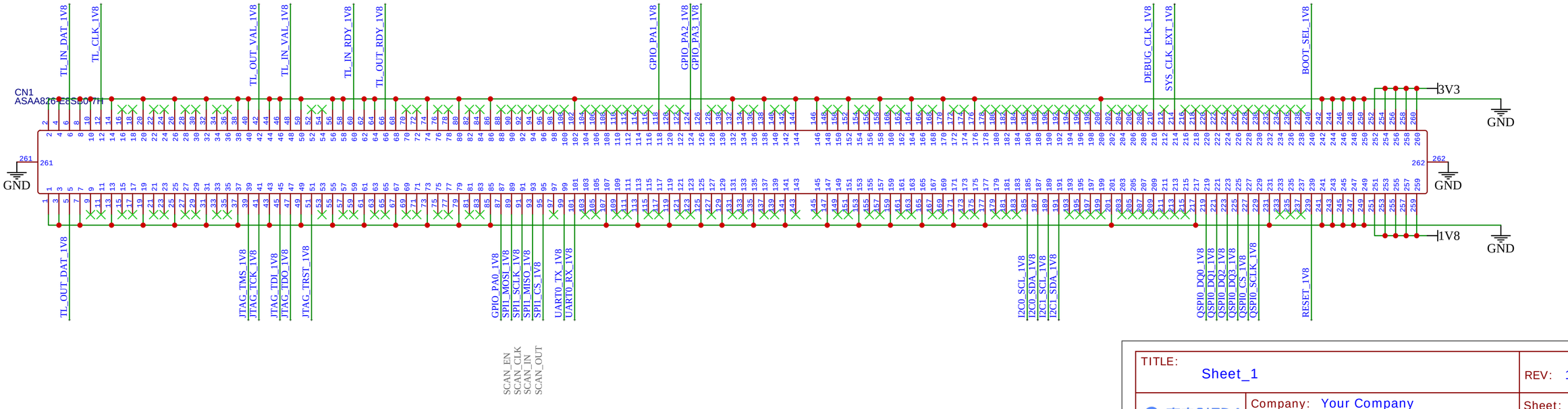


LDO



SODIMM Connection

SODIMM Layout: https://atta.szlcsc.com//upload/public/pdf/source/20180612/C225725_24F8E3125FAF536DE50EBBF33D1AD3EA.pdf



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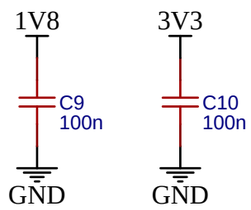
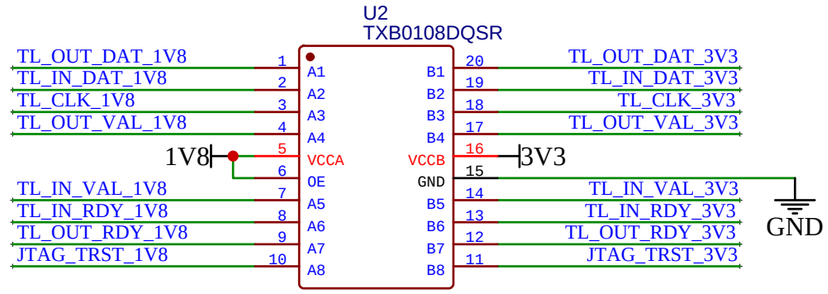
Level Shifts

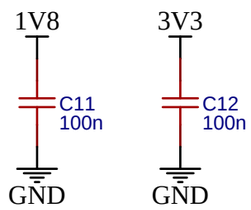
If pullup or pulldown resistors are needed, the resistor value must be over 50 kΩ.

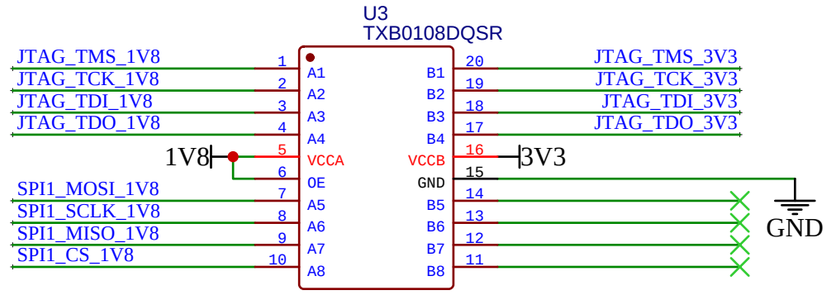
When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. The TXB0108 is designed so that the OE input circuit is supplied by VCCA.

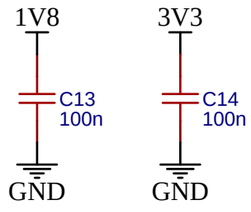
The TXS0108E device has smart internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary.

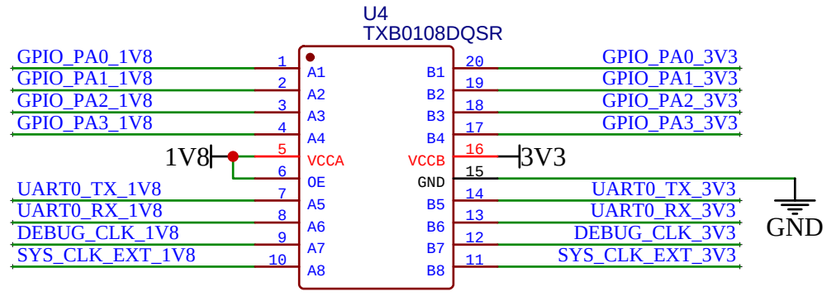


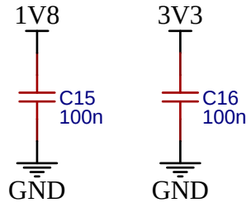


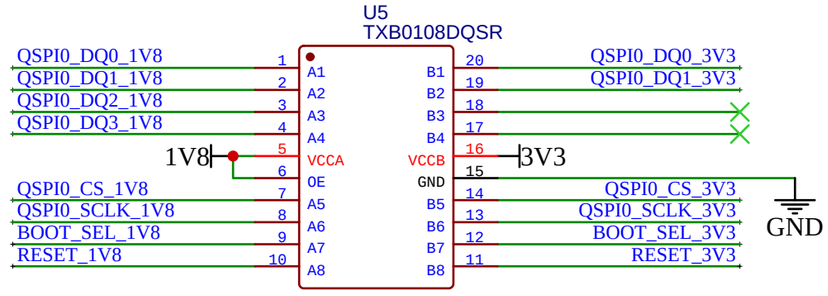












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