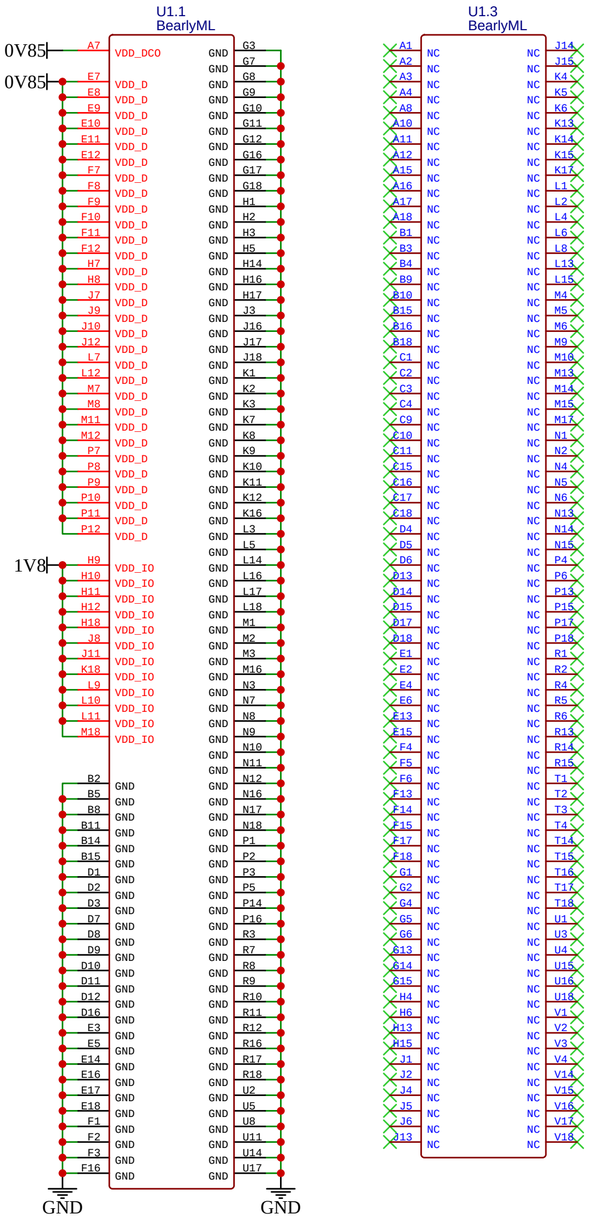
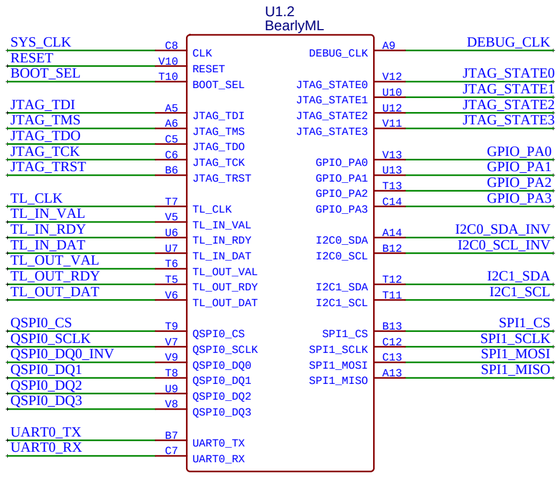
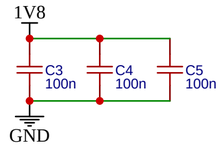
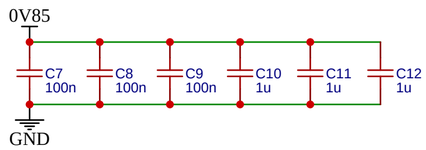
SoC

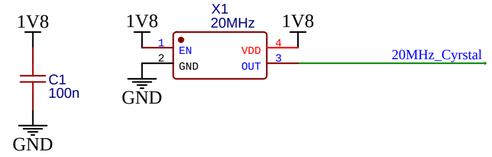






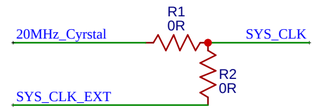


Crystal



Clock Selection

default use crystal (R1 jumped)



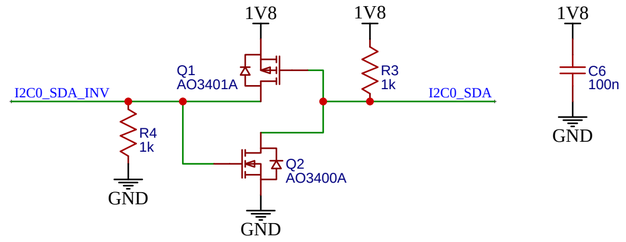
R2 not added to BOM

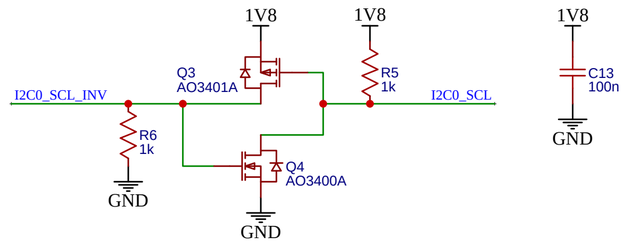
Signal Patch

NOT gate fixing MOSI polarity

MOSFET magic fixing SDA and SCL polarity

SDA and SCL requires bidirectional flip from open-collector to open-drain



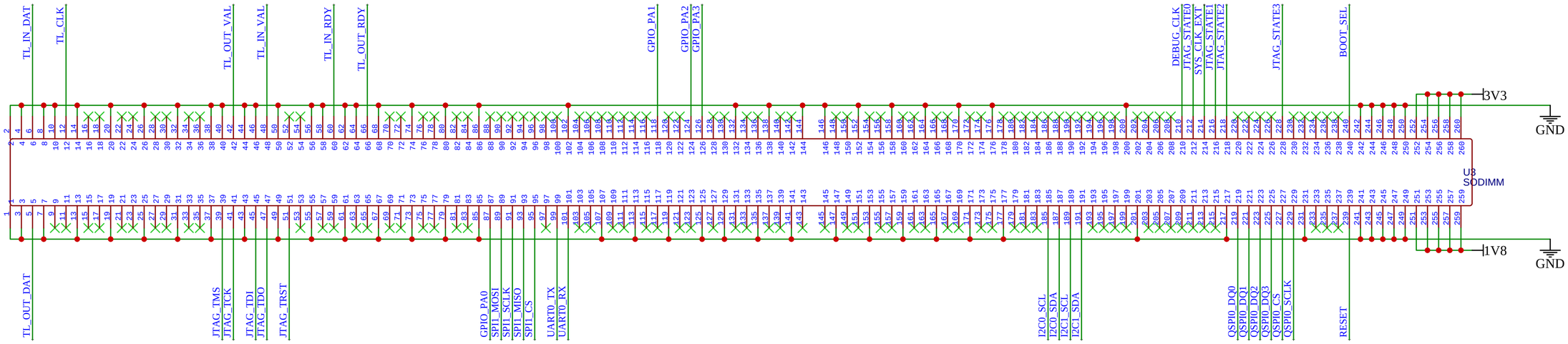


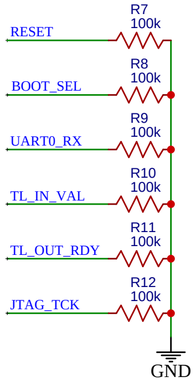
TITLE: Sheet_1		REV: 1.0
嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2022-12-16 Drawn By: T-K-233	

SODIMM Connection

SODIMM Layout: https://atta.szlcsc.com//upload/public/pdf/source/20180612/C225725_24F8E3125FAF536DE50EBBF33D1AD3EA.pdf

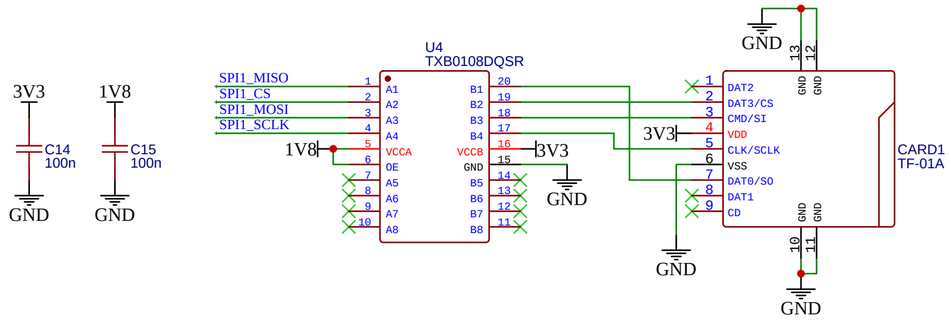
JTAG Signal Pull Rules: https://www.intel.com/content/www/us/en/docs/programmable/683546/current/pull-up-and-pull-down-of-jtag-pins-during.html





pulling the necessary signals with very weak pull-down to ensure correct operation in minimal setup

TF Card Slot



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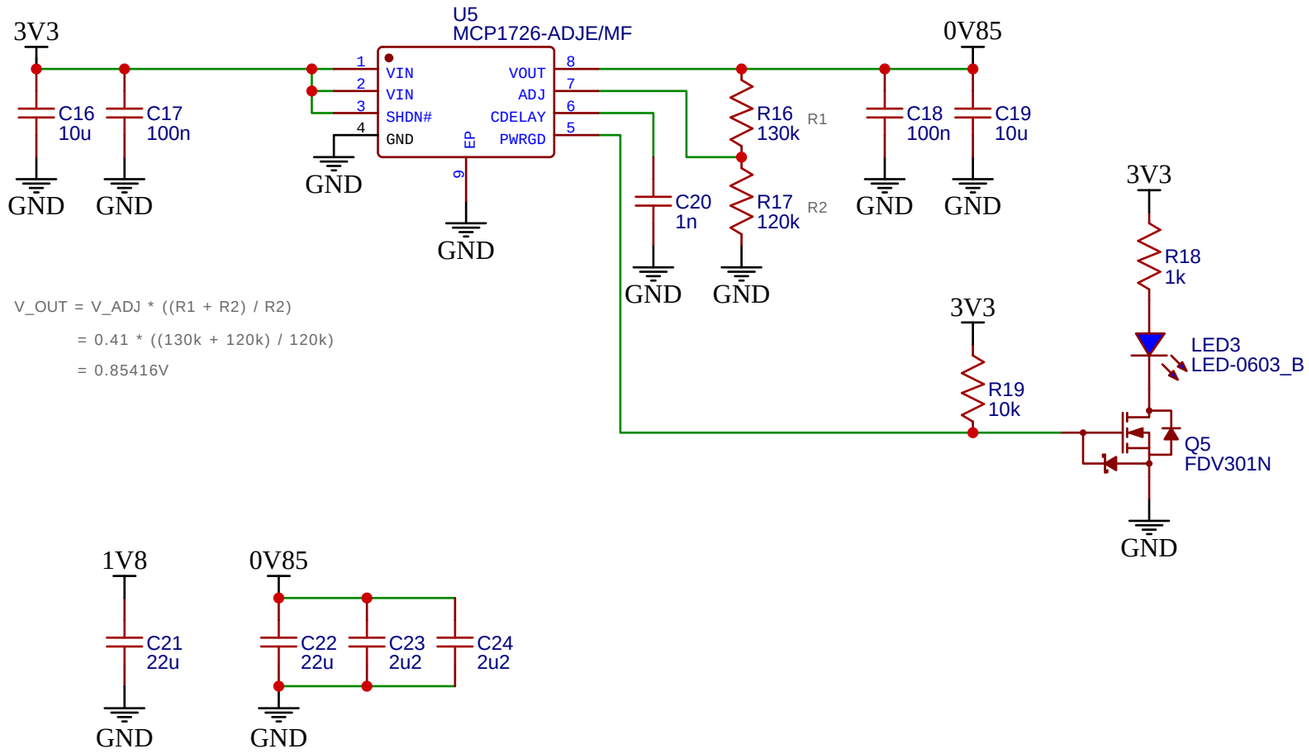
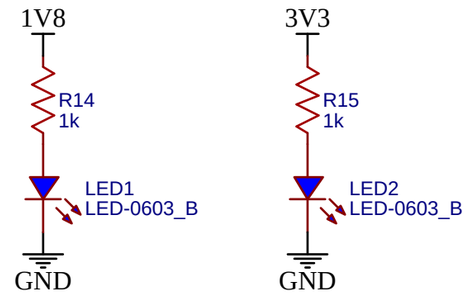
嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2022-12-16 Drawn By: T-K-233	

LDO



Power Indicator LEDs



TITLE: Sheet_3		REV: 1.0
嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2022-12-16 Drawn By: T-K-233	