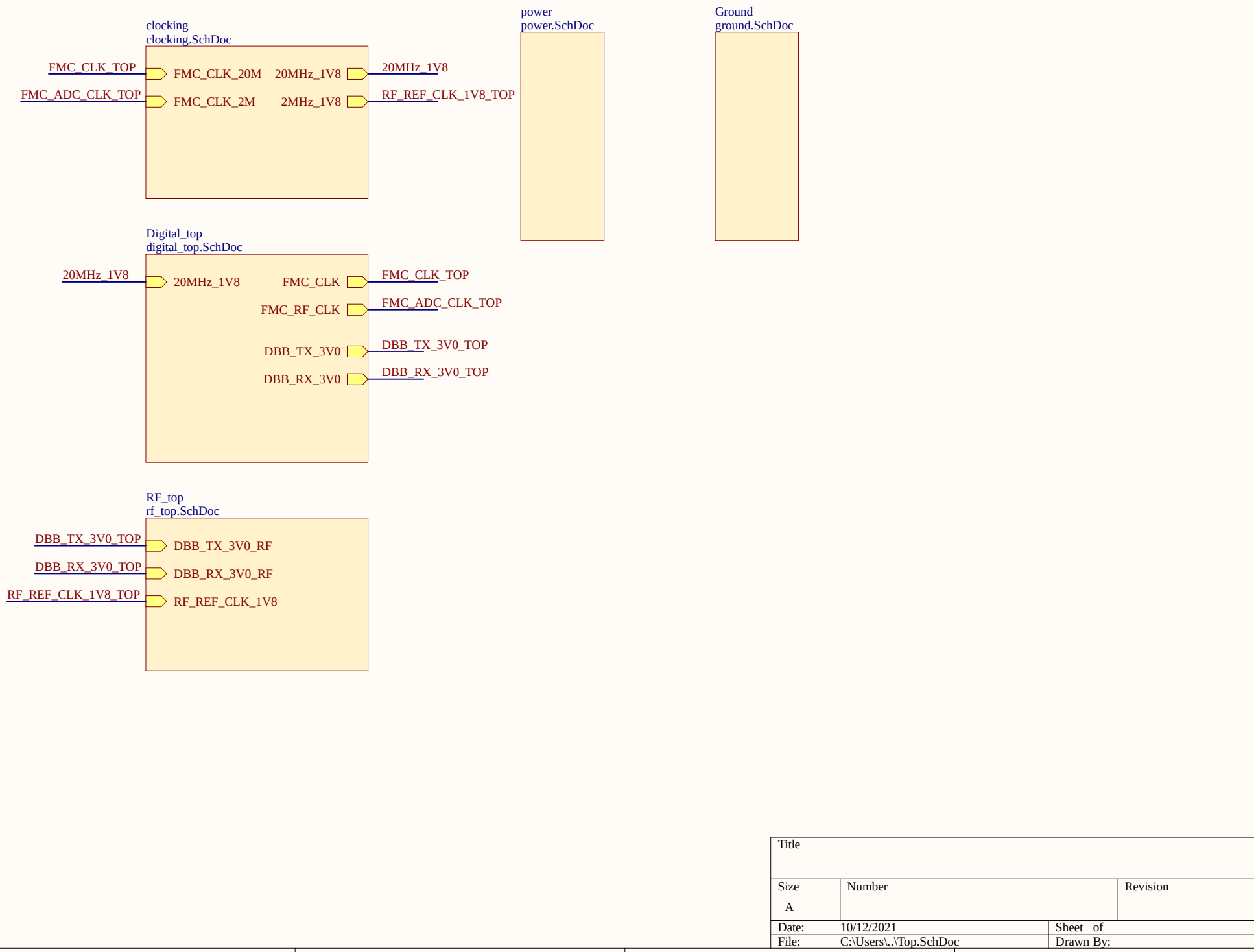
clocking
clocking.SchDoc
FMC_CLK_TOP
FMC_ADC_CLK_TOP
FMC_CLK_20M
FMC_CLK_2M
20MHz_1V8
2MHz_1V8
20MHz_1V8
RF_REF_CLK_1V8_TOP
power
power.SchDoc
Ground
ground.SchDoc
Digital_top
digital_top.SchDoc
20MHz_1V8
20MHz_1V8
FMC_CLK
FMC_RF_CLK
DBB_TX_3V0
DBB_RX_3V0
FMC_CLK_TOP
FMC_ADC_CLK_TOP
DBB_TX_3V0_TOP
DBB_RX_3V0_TOP
RF_top
rf_top.SchDoc
DBB_TX_3V0_TOP
DBB_RX_3V0_TOP
RF_REF_CLK_1V8_TOP
DBB_TX_3V0_RF
DBB_RX_3V0_RF
RF_REF_CLK_1V8
Title
Size
A
Number
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File:
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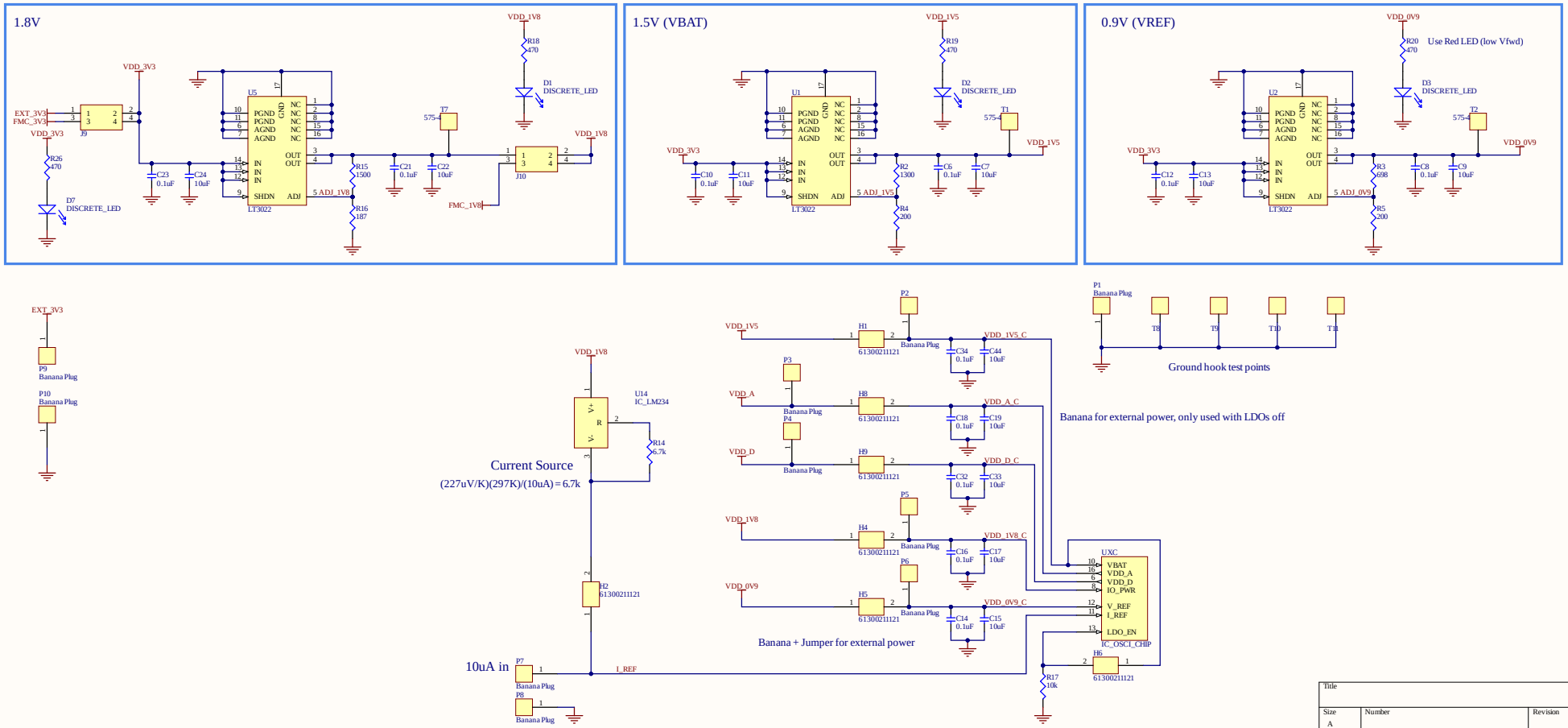
1.8V
VDD_1V8
R18
470
D1
DISCRETE_LED
VDD_3V3
EXT_3V3
FMC_3V3
J9
U5
LT3022
R26
470
D7
DISCRETE_LED
C23
0.1uF
C24
10uF
R15
1500
R16
187
C21
0.1uF
C22
10uF
T7
575-
FMC_1V8
J10
VDD_1V8
5 ADJ_1V8
1.5V (VBAT)
VDD_1V5
R19
470
D2
DISCRETE_LED
U1
LT3022
T1
575-
VDD_1V5
C10
0.1uF
C11
10uF
R2
1300
R4
200
C6
0.1uF
C7
10uF
5 ADJ_1V5
0.9V (VREF)
VDD_0V9
R20
470
Use Red LED (low Vfwd)
D3
DISCRETE_LED
U2
LT3022
T2
575-
VDD_0V9
C12
0.1uF
C13
10uF
R3
698
R5
200
C8
0.1uF
C9
10uF
5 ADJ_0V9
EXT_3V3
P9
Banana Plug
P10
Banana Plug
Current Source
(227uV/K)(297K)/(10uA) = 6.7k
VDD_1V8
U14
IC_LM234
R14
6.7k
H2
61300211121
10uA in
P7
Banana Plug
P8
Banana Plug
I_REF
P2
P3
P4
P5
P6
H1
H8
H9
H4
H5
61300211121
Banana Plug
VDD_1V5
VDD_A
VDD_D
VDD_1V8
VDD_0V9
VDD_1V5_C
VDD_A_C
VDD_D_C
VDD_1V8_C
VDD_0V9_C
C34
0.1uF
C44
10uF
C18
0.1uF
C19
10uF
C32
0.1uF
C33
10uF
C16
0.1uF
C17
10uF
C14
0.1uF
C15
10uF
Banana + Jumper for external power
Banana for external power, only used with LDOs off
UXC
VBAT
VDD_A
VDD_D
IO_PWR
V_REF
I_REF
LDO_EN
IC_OSC1_CHIP
H6
61300211121
R17
10k
P1
Banana Plug
T8
T9
T10
T11
Ground hook test points
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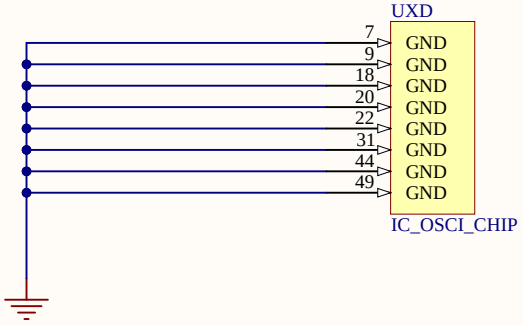

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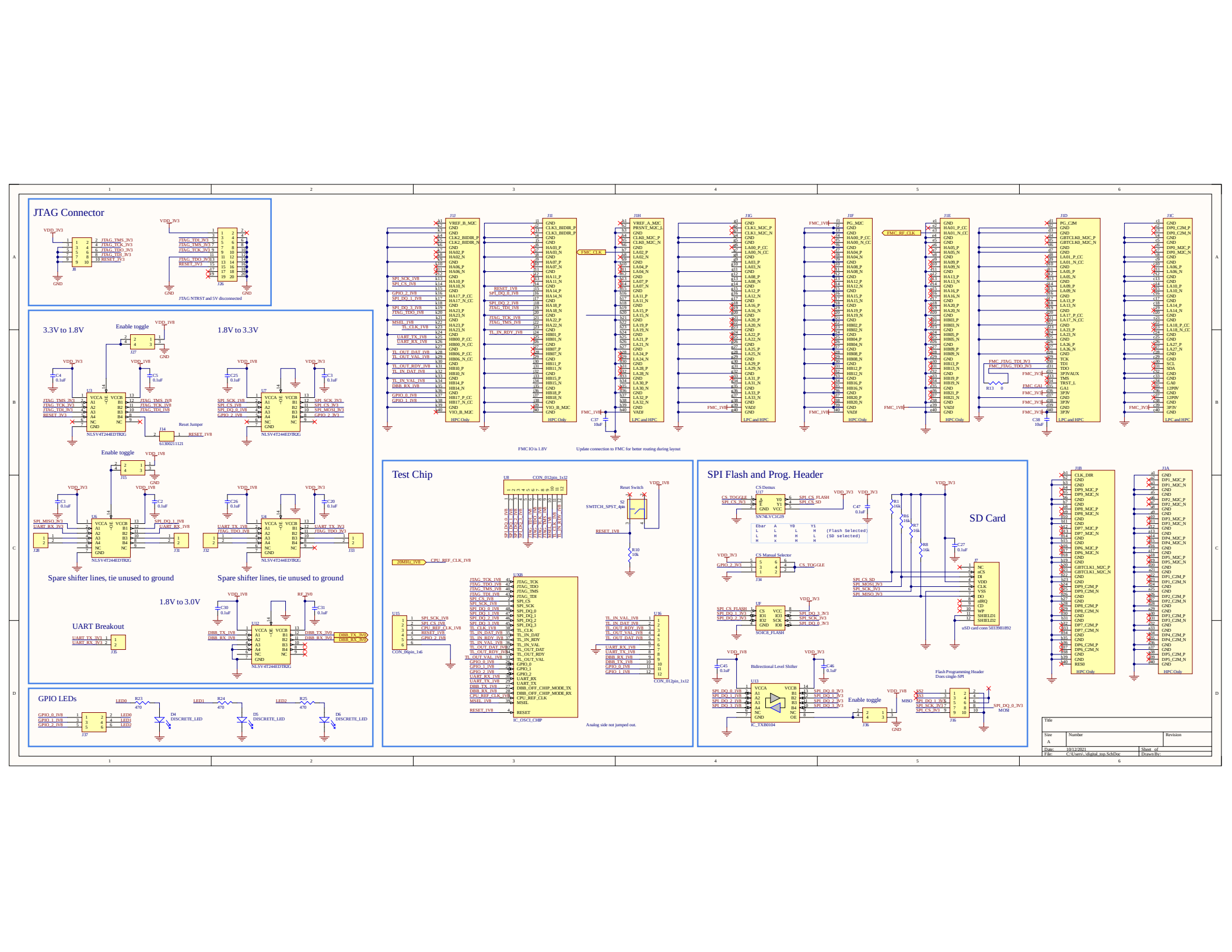
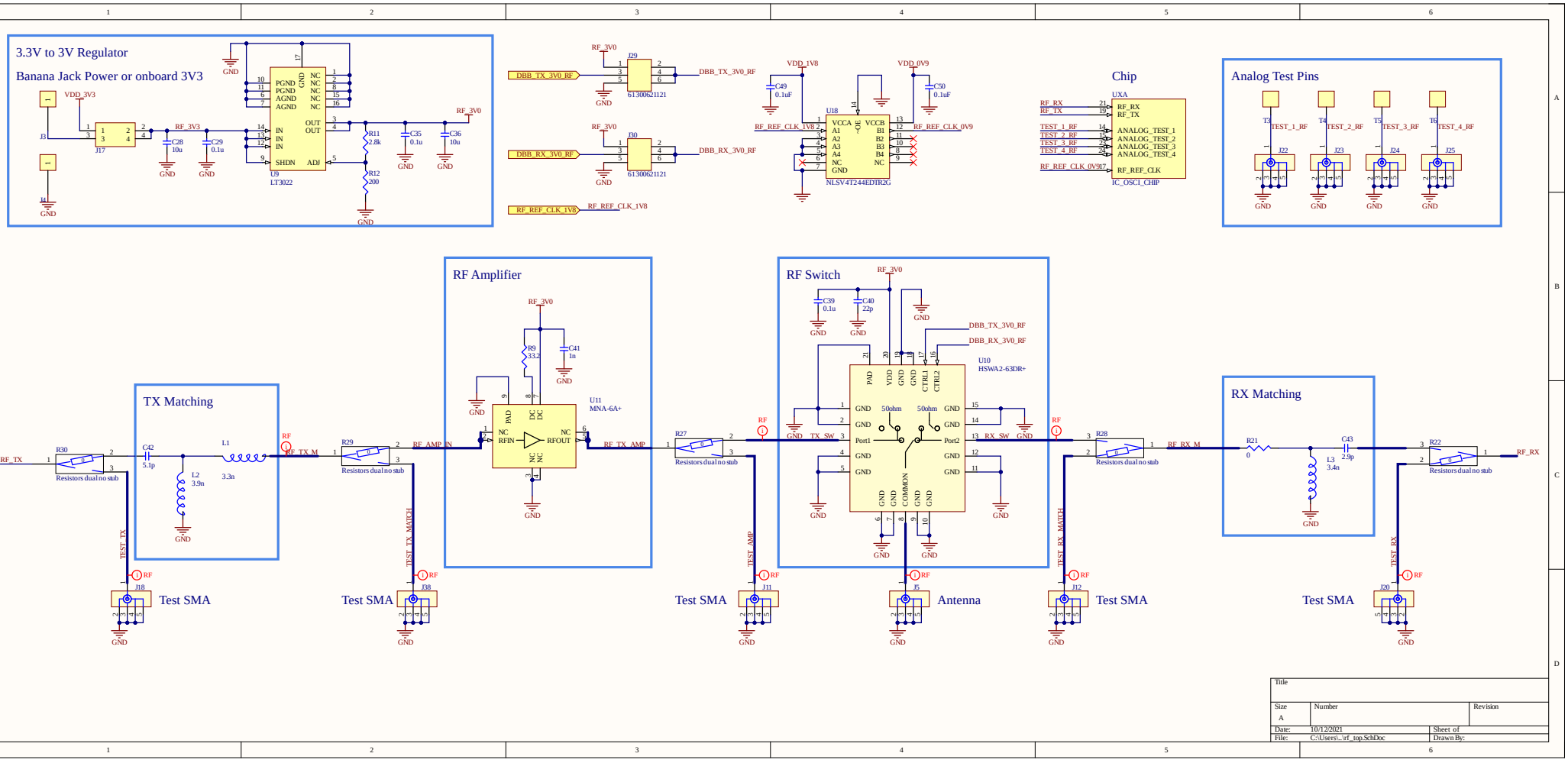

JTAG Connector
JTAG NTRST and 5V disconnected
3.3V to 1.8V
Enable toggle
1.8V to 3.3V
Reset Jumper
Spare shifter lines, tie unused to ground
Spare shifter lines, tie unused to ground
1.8V to 3.0V
UART Breakout
GPIO LEDs
FMC IO is 1.8V
Update connection to FMC for better routing during layout
Test Chip
Analog side not jumped out.
SPI Flash and Prog. Header
SD Card
Flash Programming Header
Does single-SPI
Enable toggle


3.3V to 3V Regulator
Banana Jack Power or onboard 3V3
VDD_3V3
RF_3V3
RF_3V0
LT3022
C28 10u
C29 0.1u
C35 0.1u
C36 10u
R11 2.8k
R12 200
DBB_TX_3V0_RF
DBB_RX_3V0_RF
RF_REF_CLK_1V8
RF_REF_CLK_0V9
VDD_1V8
VDD_0V9
C49 0.1uF
C50 0.1uF
NLSV4T244EDTR2G
Chip
IC_OSCI_CHIP
Analog Test Pins
TEST_1_RF
TEST_2_RF
TEST_3_RF
TEST_4_RF
RF Amplifier
U11
MNA-6A+
R9 53.2
C41 1n
RF Switch
U10
HSWA2-63DR+
C39 0.1u
C40 22p
TX Matching
RF_TX
RF_TX_M
RF_AMP_IN
RF_TX_AMP
RF_RX_M
RF_RX
R30
R29
R27
R28
R22
C42 5.1p
L1 3.3n
L2 3.9n
RX Matching
R21 0
C43 2.0p
L3 3.4n
Resistors dual no stub
TEST_TX
TEST_TX_MATCH
TEST_AMP
TEST_RX_MATCH
TEST_RX
Test SMA
Antenna
Title
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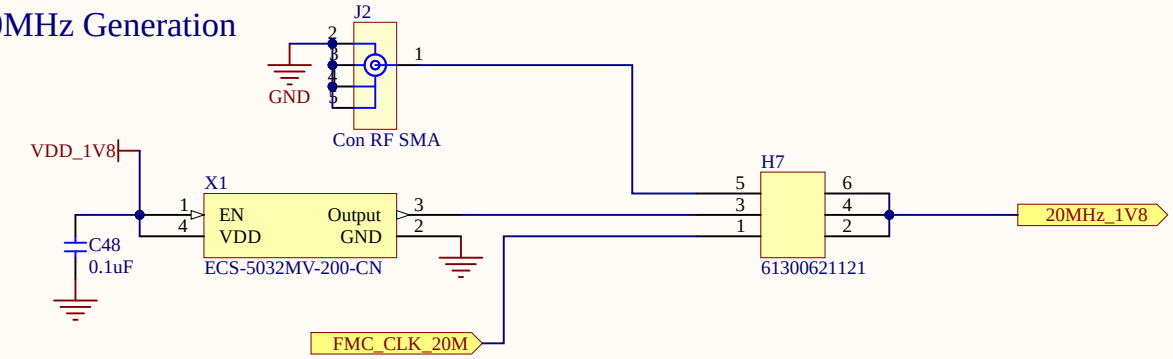
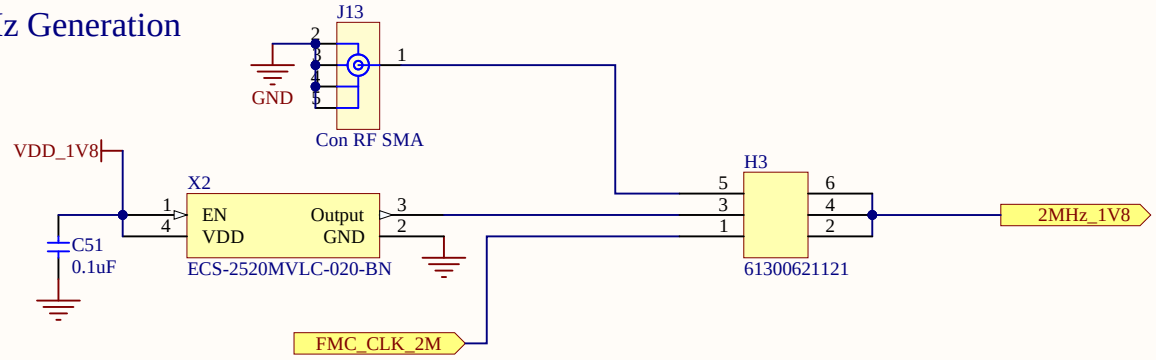
20MHz Generation



2MHz Generation



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Size: A	Number	Revision
Date: 10/12/2021		Sheet of
File: C:\Users\..\clocking.SchDoc		Drawn By: